PCB EMC Design Guidelines: A Brief Annotated List

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Abstract

Some of the worst printed circuit board design choices are made by engineers who are trying to comply with a list of EMC design guidelines Nevertheless, a short list of design guidelines can be helpful at times. This paper reviews some of the more general EMC design guidelines for printed circuit board layout.

INTRODUCTION

As much as we hate to admit it, EMC engineers and printed circuit board (PCB) designers rely heavily on design guidelines when designing or evaluating PCBs or diagnosing EMC problems. Of course, a good engineer does not rely solely on guidelines. If a particular design feature violates a guideline, a more thorough analysis is normally called for to determine whether or not the violation is likely to present a problem. Ideally PCB EMI design guidelines serve as a starting point. They help the designer to make layout choices without stopping to analyze every decision. Design guidelines play a role in making design trade-offs and they help to identify potential problem areas.

Unfortunately, there are nearly as many design guidelines as there are design engineers. Some guidelines are based on circuit or radiation models, some are based on experience and others have no known origin. A few guidelines are very important and can nearly always be applied. Others apply only to specific situations and are not appropriate in general.

The guidelines presented here were selected from a much longer list that was compiled over the past year. The longer list contains guidelines contributed by some of the companies that we work with here at the university. It also includes guidelines published in books, magazines and on the web. In the longer list, guidelines often conflict with one another and many of them are out of date or applicable only to certain very specific types of boards.

The longer list was shortened by eliminating all the guidelines that didn't make sense, were out-dated or could not be applied to a wide variety of board designs. Also eliminated, were guidelines that could easily be misinterpreted causing a designer to inadvertently make things worse. The remaining guidelines were grouped into four categories: component placement, trace routing, board decoupling and the top four.

THE TOP FOUR

While any ranking of EMC design guidelines is subjective, there are four guidelines that, in the opinion of the author, deserve special attention. A significant percentage of EMC problems are the direct result of board designs that violate one of these four guidelines. Sometimes designers are aware of these guidelines, but violate them in an effort to comply with less important guidelines.

1. Minimize signal current loop areas

Although digital designers don't always realize this, all electrical signals have current as well as voltage. Signal currents always return to their source (i.e. they flow in loops). Minimizing signal current loop areas is perhaps the single most important thing you can do to prevent energy in the signal from coupling to other circuits or radiating. Printed circuit board designers should always keep track of where the signal currents are flowing and ensure that a low impedance path is provided to return every signal current to its source.

2. Don't locate circuitry between connectors

I/O connectors generally represent the best possible way for energy to be coupled onto or off from the board. High-speed circuitry between two connectors with attached cables will easily drive one cable relative to the other with enough voltage to exceed radiated emissions specifications [1]. This will be true even if the cables are well shielded and the circuitry is located above a solid signal return plane. Transients and RF currents induced by external sources are very likely to flow onto a board on one cable and off of the board on another. Circuitry located between two cable connections is more difficult to protect.

3. Control transition times in digital signals

It is not uncommon to see products fail to meet emissions requirements at frequencies that are 10 – 100 times the fundamental clock frequency. However, by controlling the rise- and fall-times of the signal, it is possible to attenuate these upper harmonics significantly without degrading the signal quality or bit error rate. Signal transition times are readily controlled by choosing logic families that are appropriate to the task or (for capacitive loads) by putting a resistance in series with the source.

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4. Provide a solid (not gapped) signal return plane

This rule is essentially a corollary to the first rule, but it deserves special mention. Radiated EMI problems often result when well meaning designers cut a gap in a signal return plane forcing high-frequency currents to find their way back to the source by high-impedance paths. Often the gap is created in an attempt to avoid a perceived susceptibility problem. Although there are a few circumstances where a gap in the plane is called for, this is a decision that should be part of a well thought-out plan. Solid return planes should never be gapped just to comply with a guideline or an application note.

GUIDELINES FOR COMPONENT PLACEMENT

- Connectors should be located on one edge or on one corner of a board.

The purpose of this guideline is to make is easier to comply with Guideline #2 above.

- A device on the board that communicates with a device off the board through a connector should be located as close as possible to that connector.

- Components not connected to an I/O net should be located at least 2 cm away from I/O nets and connectors.

I/O lines represent one of the easiest ways to couple unwanted energy on or off the board.

- All off-board communication from a single device should be routed through the same connector.

This is to prevent radiated emission and susceptibility problems as described under Guideline #2 above.

- Clock drivers should be located adjacent to clock oscillators.

This is consistent with the idea of minimizing loop areas (see Guideline #1 above).

GUIDELINES FOR TRACE ROUTING

- All power planes and traces should be routed on the same layer.

This helps prevent unwanted noise coupling between power buses. It usually results in an efficient layout, since no two devices require the same power at the same point and devices using the same power bus are generally grouped.

- Critical signal traces should be buried between power/ground planes.

Signals on traces between solid planes are less likely to interact with external sources or antennas.

- No trace unrelated to I/O should be located between an I/O connector and the device(s) sending and receiving signals using that connector.

- Signals with high-frequency content should not be routed beneath components used for board I/O.

I/O lines represent one of the easiest ways to couple unwanted energy on or off the board.

- Critical nets between planes should be routed at least 2 mm away from the board edge.

Signals on traces very close to the board edge are more easily coupled onto and off from the board.

- On a board with power and ground planes, no traces should be used to connect to power or ground. Connections should be made using a via adjacent to the power or ground pad of the component.

Traces take up space on the board and increase the inductance of the connection.

- On boards with multiple signal return planes, all vias connected to one signal return plane should also connect to the others.

Attempts to control the flow of signal return currents by connecting to different planes usually create more problems than they solve. It is generally desirable to have all return planes in a PCB at the same potential. They should be shorted together at every opportunity.

GUIDELINES FOR BOARD-LEVEL DECOUPLING

1.1 Boards with closely spaced planes

- On boards with closely spaced (i.e. less than 0.25 mm) power and ground planes, the location of decoupling capacitors is not nearly as important as the inductance associated with their connection to the planes [2].

- Decoupling capacitors should be connected directly to power/ground planes using vias in or adjacent to the pads.

- It is unnecessary and ineffective to use capacitors with a nominal value that is less than the board's interplane capacitance. At low frequencies, higher values of capacitance are desirable. At high frequencies, connection inductance is much more important than the nominal value of the capacitor.

- Power supply leads from active devices and decoupling capacitors should be connected directly to the power and ground planes. No attempt should be made to connect chip leads directly to a decoupling capacitor.

1.2 Boards with widely spaced planes

- On boards with widely spaced (i.e. greater than 0.5 mm) power and ground planes, a local decoupling capacitor should be located near each active device. If the active device is mounted on the side of the board nearest the ground plane, the decoupling capacitor should be located near the power pin. If the active device is mounted on the side of the board nearest the power plane, the decoupling capacitor should be located near the ground pin {3,4}.
- Decoupling capacitors should be connected directly to power/ground planes using vias in or adjacent to the pads. Decoupling capacitors can share a power or ground via with the active device if this can be accomplished without traces (or with a traces length less than the power/ground plane spacing).
- It is unnecessary and ineffective to use capacitors with a nominal value that is less than the board's interplane capacitance. At low frequencies, higher values of capacitance are desirable. At high frequencies, connection inductance is much more important than the nominal value of the capacitor.

1.3 Boards with no power plane

- On boards with no power plane, a local decoupling capacitor should be located near each active device. The inductance of the decoupling capacitor connection between power and ground should be minimized. Two local decoupling capacitors with a few centimeters of space between them, can be used to provide more effective decoupling than a single capacitor [5].

SUMMARY

A brief annotated list of EMC design guidelines has been presented. Although this represents a small subset of the guidelines the average EMC engineer is likely to have available, these guidelines can be applied to a wide variety of PCB designs.

REFERENCES

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