Fatigue Strength of Through Hole in Printed Circuit Board

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***Abstract*— Through holes which were for electric signal communication were formed in printed circuit board. The surface of through hole was plated by thin metal and the irregularities were shaped on the free surface or on the interface due to hole-drilling process for making through holes in circuit board. Fracture of through hole was occurred by stress concentration due to its irregularity. In this study, inelastic thermal stress simulation was performed by using a large scale simulator ADVENTURECluster which was based on FEM to discuss fatigue strength around through hole of a printed circuit board.**

Keywords—FEM(Finite Element Method), Through hole, Fatigue strength, Printed circuit board, TCT(Thermal Cycle Test)

I. Introduction

Currently, high performance and downsizing are required for electronic devices. A printed circuit board on the electronic devices has been required to have high density integration. Multilayer build-up wiring board have been used a printed circuit board. Conductive layers and insulating layers are alternately stacked in multilayer build-up wiring board. A cross sectional photograph of the printed circuit board with through hole was shown in Fig.1 [1]. The through hole is a cylindrical hole extending through the printed circuit board. The through hole connects each layer and conducts electric signals to the layers. High reliability of electrical conductivity is particularly required of through hole around core layer [2-3]. The temperature of printed circuit board was changed under the conditions of reliability evaluation test and reflow process. A printed circuit board is heated up to 260 deg. C in reflow process. A printed circuit board is heated up to 125 deg. C and is cooled to -65 deg. C in the reliability evaluation test. It has been reported that the crack was occurred in through hole in the reliability evaluation test and reflow process due to that the stress concentration was occurred on the interface of materials. It is necessary to consider about mechanical strength and area of stress concentration to reveal the number of cycle to failure [4]. In this study, irregular shape of interface was reproduced by cross section data of through holes and inelastic thermal stress simulation was performed with the irregular shape model under thermal condition of MIL standard.

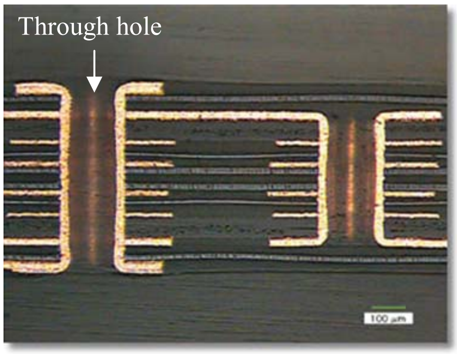

Fig.1 Cross section of stacked structure of a printed circuit board

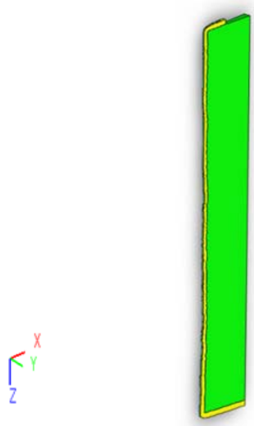

Fig.2 5 degrees sector model of the circuit board

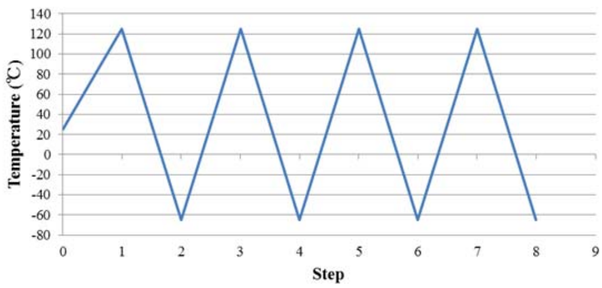

Fig.3 History of thermal cycle

II. SIMULATION METHOD

SIMULATION MODEL

A printed circuit board that have stacked structure of resins and wiring boards was extensively used for electronic devices. In this study, it is assumed that the simulation model have a symmetry as central axis and the simulation model was created by rotating cross sectional shape data of through hole for 5 degrees in the central axis. This simulation model is called 5 degree sector model in this study. The 5 degree sector model was shown in Fig.2. The model was generated by Cu through holes and FR-4 printed circuit board. The irregular shape was modeled on the interface of through hole and printed circuit board. The thickness of printed circuit board is about 3.2mm. Diameter of through hole is about 0.28mm. Through hole thickness is about 0.03mm-0.045mm.

THERMAL STRESS SIMULATION

Thermal stress simulation is performed at a cyclic thermal condition of MIL standards. Reference temperature is 25 deg. C. Maximum temperature is 125 deg. C and minimum temperature is -65 deg. C. History of thermal cyclic load was shown in Fig.3. In this study, axisymmetric conditions were used as boundary conditions. The displacements along normal direction of symmetry planes were constrained. The displacement along thickness direction at the lowest node of the model was also constrained. Scheme of boundary condition was shown in Fig.4.

COMPUTING SYSTEM

Specification of the work station is as follows. CPU is Intel Xeon X5560 3.47GHz 12cores. Memory is 96GB RAM. Graphics board is NVIDIA Quadro FX 4800. Simulation code is ADVENTURECluster Solver (ver.4.6.0). The code is a large scale simulator ADVENTURECluster [5] which was based on FEM, and it can be operated computer with multiprocessor and be ran a parallel processing.

FEM MODEL

Uniformly coarse elements were adopted in the simulation model and elastic thermal stress simulation was performed to find evaluation area. We decided the evaluation points in where the maximum three equivalent stresses were occurred. Higher stresses were occurred at notch shaped interface of copper and FR-4 as printed circuit board. After then, fine elements were adopted at three evaluation points that we have obtained. At a range of 6μm from evaluation point, fine elements size of 0.4μm were used. At a range up to 12μm from evaluation point, element size of 1μm was used. At a range up to 20μm from evaluation point, elements size of 2μm was used. The simulation model, which was far from evaluation points, was divided with coarse elements. FEM model and enlarged areas of evaluation points was shown in Fig.5. Mesh used in this study was generated by using Hyper Mesh [6] and element type is quadratic hexahedron. The number of elements is 93,788. Degree of freedom is1,433,259. The material properties of copper and FR-4 of the model were shown in Table.1. The copper was elastic-plastic material [7] and FR-4 was anisotropic materials of CTE [8].

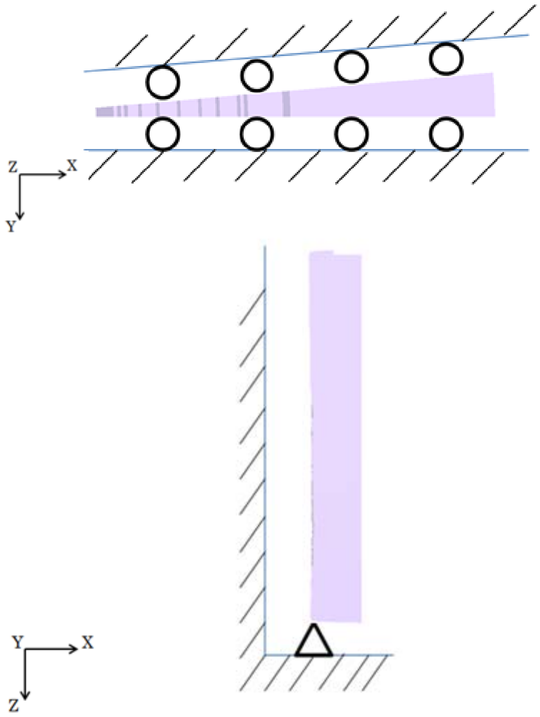

Fig.4 Scheme of boundary conditions

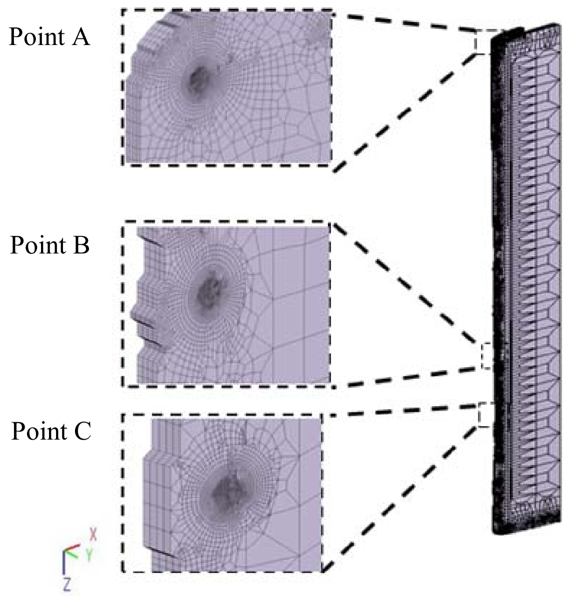

Fig.5 FEM model and enlarged areas of evaluation points.

III. RESULT

The irregular shape was occurred on printed circuit board when the through hole was created by drilling process. The stress concentration was occurred in the point of irregular shape. The points of stress concentration and the points of strain concentration were specified by our simulation. It has been reported that the crack was occurred at the center part of through hole in the actual reliability evaluation test. But the stress concentration was not occurred at the center part of through hole in the study. Distribution of nodal equivalent plastic strain and close up point of maximum plastic strain were shown in Fig. 6. The distribution was the plastic strain at step 8 (-65 deg. C.). The level of point C showed the most highest in the model. The relation between equivalent plastic strain and distance of maximum plastic strain point along -45 degrees in point C were shown in Fig.7. The data of the plastic strain of step 7 and step 8 were used to obtain plastic strain range. The relation between plastic strain range and distance of maximum plastic strain point were shown in Fig.8. Coffin-Manson law is an empirical formula that the product of the plastic strain range and the exponential of the fatigue life are a constant value when the load level was evaluated by the plastic strain range in the low cycle fatigue. Coffin-Manson law was represented by the following formula,

$$N_f = \left(\frac{C}{\Delta\varepsilon_{in}}\right)^{\frac{1}{m}}$$

where, m shows the fatigue ductility index and C showed the fatigue ductility coefficient. A numerical value of fatigue ductility index was 0.568. A numerical value of fatigue ductility coefficient was 0.487 in this study. The relationship between plastic strain range and the distance from the origin along -45 degrees of the through hole were obtained. The fatigue strength was expected by the relationship between the plastic strain range and the distance. The equivalent plastic strain range and the number of cycle to failure were summarized in this simulation was shown in Table.2.

IV. CONCLUSIONS

In this study, inelastic thermal stress simulation was performed with a large scale simulator ADVENTURECluster which was based on FEM to estimate fatigue strength of through hole of a printed circuit board.

Inelastic thermal stress simulation was performed by using the irregular shape model. The point of plastic strain concentration and the stress concentration were identified in this simulation model.

The area of strain concentration obtained in the simulation was not consisted with region of crack where was observed in experiment. It suggested that stacked structure of insulating layer and conducting layer should be modeled as printed circuit board.

Table.1 Material property

	Young's modulus [GPa]	Poisson's ratio	CTE [ppm/K]	Work hardening coefficient [GPa]	Yield stress [MPa]
Cu	123	0.35	16.5	1.7	210
FR-4	21	0.3	17(in plane) 58(out plane)	-	-

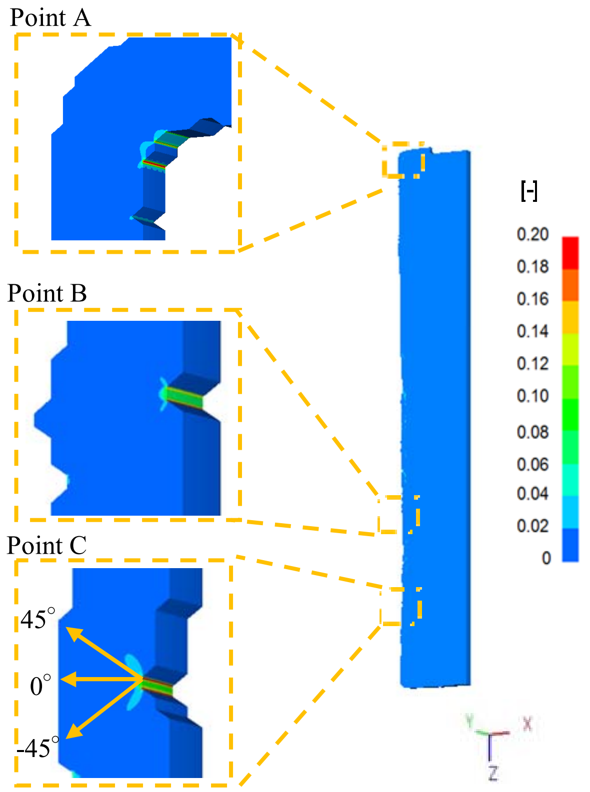

Fig.6 Distribution of nodal equivalent plastic strain step8

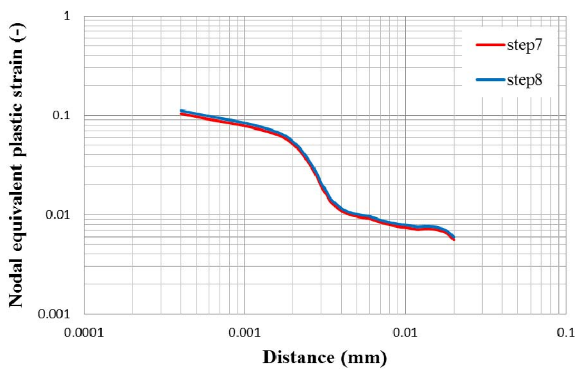

Fig.7 Relationship between equivalent plastic strain and distance along -45degrees from origin at point C

The relationship between plastic strain range and the distance from origin along the thickness direction of through hole were obtained and fatigue life cycles were shown by Coffin-Manson law.

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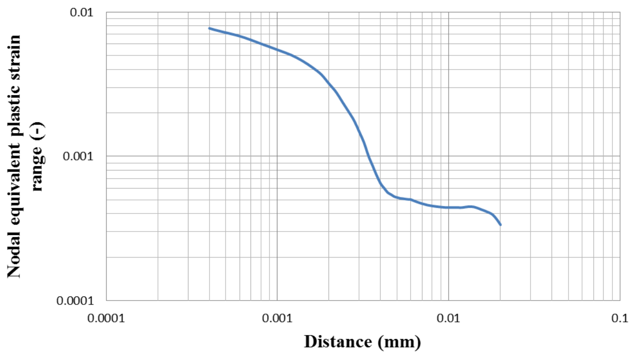

Fig.8 Relationship between equivalent plastic strain range and distance along -45degrees from origin in point C

Table.2 Relationship between distance from origin, plastic strain range and fatigue life cycle at point A, B and C

	Distance [μm]	Plastic strain range	Fatigue life cycle
Point A	0	0.0121	669
	1	0.0033	6,587
	5	0	-
	10	0	-
Point B	0	0.0131	581
	1	0.0049	3,284
	5	0.0004	270,498
	10	0.0002	916,529
Point C	0	0.0153	442
	1	0.0054	2,768
	5	0.0005	182,620
	10	0.00044	228,712