PCB Layout Design for EMI/EMC Compliance

Prakash Chand   **BN Gangopadhyay**   **Meenakshi Kumar**

Defence Electronics Applications Laboratory,
Raipur Road, Dehradun – 248001 (INDIA)

Abstract - This paper is based on the background studies and experiences in identification and implementation of the fundamental design techniques for making a PCB layout that needs a high degree of compliance for EMI/EMC. It suggests the use of techniques for considering PCBs configuration, Interplane coupling, Grounding methods, use of Bypassing and Decoupling capacitor and many other techniques required for making good PCB layout design.

I INTRODUCTION

Electromagnetic Interference (EMI) is becoming an exceptionally crucial issue in the design of modern electronic systems. Integration trends are squeezing entire systems into extraordinary high circuit densities, while frequencies are continuously increasing. On the other hand managing fast clock speeds and rapid edge rates are becoming a greater challenge. High speed switching has the capability of producing electromagnetic waves that generate resonance, power/ground bounce, simultaneous switching noise, reflections, and coupling between traces and power/ground planes. The effects of improper ground plane design can hinder the performance of high-speed clocks and synchronous busses. Most major sources of EMI problems appear related to signal parameters such as the clock or pulse repetition frequency, signal edge rate, and signal ringing due to impedance mismatches. The greater the performance characteristics of semiconductor components in a circuit design, the more electromagnetic interference that may occur. Therefore, the design of a PCB must eliminate or minimize all possible causes, which may result in radiation of electromagnetic energy. Loops of signal and the corresponding ground return lines carrying high frequency signals must be minimized. Cross talk of forward and backward behave quite differently, which should be understood and prevented. Many of the design features used for EMI/EMC hardening are inexpensive to implement (or even free) when they are considered and incorporated during early designs of the product and implemented in development process.

II PRINTED CIRCUIT BOARD – DESIGN CONSIDERATION FOR EMI/EMC

The first step in an EMI/EMC design consideration is to examine circuit board construction and layout. Key issues include component placement, the use of multiple layers, and separation of analog and digital circuits. Circuit board components need to be grouped by both function and speed. During the EMC review, designers should look for high-speed circuits (and traces) that have inadvertently been located next to low-speed circuits or input/output (I/O) circuits. It is helpful to highlight critical traces such as clocks or reset circuits on a schematic and then determine their actual locations on the circuit board. Warning signs of potential EMI problems are clock or reset traces near I/O ports and clock or reset traces running next to other traces for several inches or more.

PCBs CONFIGURATION

Determine the number of layers based on functional specifications, noise immunity, signal category, separations, number of nets to be routed, and impedance control & component density. Selection of a PCB stackup may be followed as given below.

- Two Layer PCB: Use two layer PCB for low-frequency analog designs running at less than 10 kHz. Route all power traces from the power supply to all components on the same routing layer. Route all the ground and power traces adjacent to (in parallel with) each other. Maintain the minimum length of all the traces to prevent the loop currents. Avoid tying traces of a tree to other traces to prevent ground loops from being created.

- Four-layer PCB: Route high-speed clock traces adjacent to a ground plane and not to the power plane for optimal performance. Ist layer is best for flux cancellation. For lower power impedance use small distance between 2nd & 3rd layers. 4th layer may not exhibit good flux cancellation.

- Six-layer Type-1 PCB: 1st layer is the only best routing layer for flux cancellation. 2nd & 3rd layers will offer a poor flux cancellation. 4th layer is not suitable for good noise margins on signal at layer

2nd & 3rd. 5th layer – power plane. 6th layer will offer poor noise margins on layer 2, 3 & 4 since power flux must migrate through signal to ground.

- Six-layer Type-2 PCB: 1st layer is not good for flux cancellation. 2nd layer is good for flux cancellation. 3rd layer- ground plane. 4th layer - power plane (lower power impedance between power and ground). 5th & 6th layers are not very good for flux cancellation.

- Six-layer Type-3 PCB: 1st layer is excellent routing along X-axis for flux cancellation. 2nd layer for X-Y paired ground traces. 3rd layer is excellent routing along Y-axis for flux cancellation. 4th layer power plane. 5th layer ground plane with lower power impedance. 6th layer is excellent routing for flux cancellation.

- *Eight-layer Type-1 PCB:* Use this configuration, when flux cancellation is not an important requirement. Suitable to accommodate large number of nets, high component density. 1st layer just suitable for flux cancellation. 2nd layer excellent routing layer along X-axis. 3rd layer X-Y paired ground traces. 4th layer excellent routing layer along Y-axis. 5th layer not suitable for flux cancellation. 6th layer-power plane. 7th layer not for good noise margin. 8th layer not suitable for good noise margin.

- Eight-layer Type-2 PCB: Use this configuration, when requirement for very tight flux cancellation is to be met. 1st layer is an excellent routing layer along X-axis. 2nd layer X-Y paired ground traces. 3rd layer is an excellent routing layer along Y-axis. 4th layer ground layer. 5th layer is an excellent flux cancellation layer between power and ground plane. 6th layer is an excellent routing layer along X-axis. 7th layer X-Y paired ground traces. 8th layer is an excellent flux routing layer along Y-axis.

- Ten-layer PCB: Configuration of layers may be made similar to eight layers PCB and according to the need of high density PCB or excellent flux cancellation PCBs. 4th layer is susceptible to power noise.

INTERPLANE COUPLING (FRINGING)

In case of very high speed PCBs (using high speed logic and clocks), boundary of power voltage planes must be physically smaller than the closest ground plane by 20-H (where H is the isolation separation between planes usually about 0.006 inches). Boundary of power plane may be made smaller than the closest ground plane by 100-H, in case of requirement is for 98% flux boundary.

GROUNDING METHODS

Use of ground on a PCB should not be left to chance and be designed based on the requirements of digital/ analog circuits, safety, signals, noise, quiet, single/ multipoint.

- Single-point grounding is used, when speed of components, circuits, interconnects is in the range of 1MHz or less.

- High frequency design (above 1MHz) generally requires use of multiple chassis ground connections.

- Locate high-speed logic components and oscillators as close as possible to a ground stitch connection to chassis ground.

- Calculate aspect ratio of all ground points locations and straight line distance between two ground stitches shall be not more than $\lambda/20$ to avoid RF loop, which may cause RF energy propagation.

- At digital frequencies, parallel grounding shall be done between signal traces.

- All parallel ground traces shall be terminated at single point ground.

PLACEMENT & LOCALIZED GROUND PLANE

- Clock circuits shall be located near the center on a single localised ground plane, which shall be positioned next to and connected to a ground stitch location.

- Clock trace shall be terminated directly at the connector by making point-to-point radial (by manual trace routing), unterminated clock lines acts as a monopole antenna.

- Clock oscillator shall be installed directly on the PCB and "DO NOT USE SOCKETS"

- Avoid placing any other traces "near, under, or through" this clock circuit on an adjacent signal routing layer.

- Clock trace shall be routed on component/ solder side with an image plane.

- Do not place solder mask on the localized ground plane. (Dielectric constant of solder mask will minimize desired RF coupling between source and ground).

IMAGE PLANES

- RF currents must return to their source through a mirror image plane of its original trace route, a power plane, a ground plane or chassis plane.

- RF current generated between traces and nearest plane (through capacitive/ inductive coupling) shall be minimized by ensuring 100% coupling between RF current trace and its mirror image plane.
- Use ground plane, adjacent to signal routing layer to minimize coupling of its RF energy to other signal planes.
- Signal traces should not be located in the ground/power.
- Through-holes in a power or ground plane creates "Swiss cheese syndrome" i.e. a slot in the ground/ power plane. No signal traces should travel over the slot.

BYPASSING AND DECOUPLING CAPACITOR

- Select bypass and decoupling capacitors based on calculated frequency of logic family and clock speed to be used.
- Select the capacitor based on its self resonant frequency: 2.5 MHz -1.0 μf, 5.0 MHz - 0.1 μf, 15.0 MHz - 0.01 μf, 50.0 MHz - 0.001 μf, 70.0 MHz - 500 pf , 150.0 MHz - 100 pf, 230.0 MHz - 50 pf, 500.0 MHz - 10 pf.
- Use of leaded capacitor at high frequency becomes inductive and ceases the function of RF coupling. (Minimize lead length inductance and locate as closely as possible to the component). Use SMT capacitors for high frequency circuits, as self-resonant frequency of SMT capacitors is generally higher by a factor of 10. (Lower lead length)
- In certain applications, two capacitors in parallel provide a better RF suppression. Above the self-resonant frequency of the larger value capacitor where its impedance increases with frequency (inductive). The impedance of the smaller capacitor is decreasing (capacitive). At some point, the impedance of the smaller value capacitor will be smaller than that of the larger value capacitor and will dominate, there by giving a smaller net impedance than that of the larger value capacitor alone.
- For optimal performance, parallel capacitor must differ by two order of magnitude of value (e.g. 0.1μf and 0.001μf) or 100x.
- Use combination of 0.1μf and 0.001μf capacitor for system below 50MHz.
- Use combination of 0.01μf and 100pf capacitors for 50MHz systems and higher clock frequencies.
- Decoupling capacitors must be provided for every component with edges faster than 5 ns.

- Provide the bulk capacitor (Tantalum dielectric) in addition to decoupling capacitors at the following locations:
- Power entry connector from the power supply to the PCB.
- Power terminals on I/O connectors for daughter cards peripheral devices and secondary circuits.
- Adjacent to power consuming circuits and components.
- The farthest location from the input power connectors.
- High-density component placement remote from the dc input power connector.
- Adjacent to clock generation circuits.

IMPEDANCE CONTROL

- Maintain clock line impedance at a constant value throughout the route (50Ω/75Ω+/- 10%)
- Use of large number of vias, change the impedance of a trace (1 to 3 nH of each via).

PROPAGATION DELAY

- Propagation delay is a function of capacitance per unit length of line. The capacitance is a function of the dielectric constant, the line width, and the thickness of the dielectric between the trace and image plane. PCB base material FR4 with 35μm copper thickness will have propagation delay of 0.36 ns/cm (approx.) for Embedded microstrip and 0.48 ns/cm (approx.) for Stripline.
  :
- Locate the signal/ clocks on PCB, so that traces are routed for a best straight-line path possible with minimal trace length and number of vias.
- Avoid signal/ clock trace traverse from one routing plane to another. This transition should occur at a component lead and not anywhere else.

IMPEDANCE MATCHING – REFLECTIONS

As signal edges become faster, consideration must be given to the propagation and reflection delays of the routed trace.

- Terminate the un-terminated signal in a matched load to avoid pulse ringing and match phase relationship.
- If a clock trace is electrically long and contain clock edges faster then 3ns, route this trace using transmission line techniques. It will help in

minimizing ringing & reflections and maintaining constant impedance on the trace.

ROUTING LAYERS

- Route all clock and high-threat signal traces on only one routing. (X-and Y-axis routes are in the same plane) and maintain minimum trace length.

- Use a solid ground plane adjacent to the routing layer, with no discontinuities in the route created by use of vias, where the ground plane is used as the image for the X- and Y – axis immediately above or below the plane.

- Connect resistor to the pin of the component without use of a via between the resistor and component.

- Do not route clock traces on the bottom layer of a multilayer board.

- Use the bottom half of a board (below the center power/ ground plane) for large signal buses and I/O circuitry.

- Avoid sharp turn (90° or more) on a routed trace as it changes the impedance and become source of RF radiation.

GUARD/ SHUNT TRACES - COMMON-MODE CURRENT

A PCB with a solid ground plane can produce common-mode RF currents all by itself, due to a finite inductance encountered by RF current in the ground plane material. This inductance creates a voltage gradient, commonly called ground-noise voltage.

- Use guard and shunt traces to provide additional return path for common-mode current and prevent common-mode RF coupling from high-threat signal traces (small line width) to other circuit traces.

- Make multiple connections to any ground planes by vias, along the edges of the guard trace.

CROSS-TALK

Cross-talk occurs by mutual capacitance and inductance between parallel traces. It is associated not only with clocks and periodic signals, but also with data, address, control and I/O traces.

- Use 3-W rule, the distance separation between traces must be 3 times the width of the trace as measured from centerline to centerline of the two adjacent traces.

- Differential pair traces, if not routed in parallel on the same routing plane (due to lack of space),

must be routed on adjacent plane. One trace must physically be three times the width of its corresponding trace along the entire route.

- Another technique to prevent or minimize crosstalk between parallel traces is to improve trace routing by separating traces with a minimum parallel length.

INTERCONNECTS AND I/O

One of the more sensitive parts of a PCB, in terms of RFI, ESD and other forms of radiated and conducted susceptibility, are the I/O and related interconnects.

- Use metal I/O connector RF bonded to chassis ground via a low-impedance path.

- Provide signal and/or chassis shield ground immediately at the connector entrance point without use of a pigtail for circuit operating at 1MHz and above.

- I/O drivers and receivers must be physically located as close to the I/O connector as possible to minimise the trace lengths and coupling with other signals.

- Low-frequency I/O ports may be bypassed with high frequency capacitors (usually 470pf to 1,000pf) located near the connection.

- Use filter between the driver/receiver devices and connectors for data signal.

- I/O signals may be filtered through a high impedance common-mode inductor or protector by a ferrite bead-on-lead component.

ISOLATION & PARTITIONING (MOATING)

Isolation is created by an absence of copper on ALL planes of the PCB by 50 mils minimum from one section to another. Moat serves as a "keep out " zone for signals and traces that are unrelated to the moated area or its interface.

- Use isolation transformer or optical isolators for Ethernet circuits.

- Use common-mode data line filter (toroidal) in both analog and digital applications.

- Capacitive decoupling may be required to remove digital noise from I/O power.

- No signal must pass over moat. (a plane void region).

- Locate any bypass capacitors directly at the connector entry point for both radiated emissions and radiated susceptibility.
- Position the data line filter (inductor or common-mode choke) between the controller side of the signal trace and the I/O connector with a by pass capacitor (100pf – 1000pf depending on the signal bandwidth) in between data line filter – I/O connector.
- Use bypass capacitor on the input side of the data line filter to prevent from ESD, a fast transient burst or pulse or conducted fields from adjacent products.

ELECTROSTATIC DISCHARGE PROTECTION

ESD is transient in nature, digital circuit edge rate faster than 3ns & more prone to ESD upsets than are slow analog, for that matter, low-bandwidth digital device circuits. In fact, ESD rarely upsets the functionality of analog circuits.

- Spark gaps: There are sharply pointed triangle aimed at each other, with the pointed tips separated by a maximum of 10 mils and minimum of 6mils. One triangle is part of the ground plane, and the other is situated on a signal traces. The triangles are not components but are made up of traces of copper on the PCB layout. This triangle spark gap must be placed only on the component layer of the PCB, with no solder mask.
- High-voltage capacitor: These disc-ceramic capacitors must be rated at 1500V minimum and located immediately adjacent to the I/O connector.
- Tranzorbs: These are semiconductor devices specifically designed for transient voltage suppression applications. They have the advantage of a stable and fast time constant to avalanche, and a stable clamping level after avalanche.
- LC filters: A low pass LC filter can prevent high frequency ESD energy from entering the system. Inductance presents a high-impedance source to the pulse, thus attenuating the impulse energy that enters the system. The capacitor, located on the input side of the inductor will shunt high frequency ESD spectral level components to ground.
- Keep all power and ground traces close together, if power planes are not used.
- Keep signal lines as close as possible to ground line/plane.
- Fill in both top and bottom layers of the PCB with

ground plane as possible.

- Implement moating/ isolation between ESD sensitive components & other functional areas.
- Internal ground planes should surround every PTH to minimize ground loops.

BACK PLANES AND DAUGHTER CARDS

A back-planes is essentially the free way of signal flow between interface circuits and daughter cards, hence special consideration must be taken to ensure proper impedance control and termination of signal/ lines exist. Back-planes with through-hole connector pins have large via holes, which result in drop of the impedance from 50Ω to 30Ω.

- Select proper connector pin assignment with large number of ground pins to minimize cross talk, reduce emissions and enhance signal quality.
- Use impedance-controlled connector wherever possible.
- Plan as many ground planes and pins as feasible on the back-planes. Use signal and ground traces alternately and do not bunch return grounds to a single set of multiple pins at opposite ends of the connector.
- Ensure an image-plane adjacent to each and every signal plane.
- Top layer of the back plane may be used as a ground plane, it will help in minimizing the impedance mismatch between back-plane and I/O connector & adapter cards.
- Route all traces orthogonal between layers.
- Avoid vias between planes for traces, clocks and signals. Traces must be on the same plane.
- Using short traces to prevent ringing and reflection.
- Terminate all signal and clock traces in their characteristic impedance.
- Use a signal return ground trace between parallel traces in a back-plane.

CIRCUITS

All EMI/EMC problems begin and end at a circuit, there are four types of circuits that deserve special attention: clocks, reset circuits, low-level analog circuits, and voltage regulators.

- Clocks are considered major sources of emissions due to their harmonics. Filtering may be necessary to slow down clock edges, so it is a good idea to provide pads for series ferrites or

resistors and shunt capacitors early in the design process. Emissions due to power pulses on circuit power can be handled by providing adequate high-frequency decoupling capacitors located next to the each clocked device. Clock generators, associated components and distribution lines significantly account for the RF emissions on a PCB. A 2ns edge rate circuit can be expected to radiate RF energy upto 160MHz ($f = 1/\pi t$) and spectrum of 1.6GHz (10X f_{max}).

- Reset circuits are very sensitive to spike-type interference, such as ESD and electrical fast transient (EFT) pulses. Thus, it's desirable to position high-frequency capacitors (1000 pF typical) at all inputs to these circuits.

- Low-level analog circuits and voltage regulators are vulnerable to RFI. The primary failure mode in these cases is rectification, so the best design strategy is to prevent such interference from reaching these critical circuits. The inputs and outputs should be protected by ferrite beads and shunt capacitors (100–1000 pF) that provide RF filtering.

- Ground the body case of the oscillator (above 50 MHz) through a wire, strap or spring clip.

III CONCLUSION

Auto-routing facility of the PCB design tools has certain limitations and is not a complete solution as it operates with a limited design-rule-check, but using semi-automatic routing the layout designer can easily implement the EMI/EMC aspect by routing critical tracks in manual mode and the non-critical tracks using auto-routing facility. While using these PCB design tools in manual mode, one may apply the above basic techniques in making PCB layout design. Use of above-mentioned techniques in considerations of PCBs configuration, Interplane coupling, Grounding methods, use of Bypass/ Decoupling capacitor and others have been found very effective in making a PCB compliance for EMI/EMC.

REFERENCES

[1] R Ball, W. Burdock, *Cost Effective EMC Design – Background Study.* Advanced Technology Centre, University of Warwick.

[2] Shahrooz Shahparnia and Omar M. Ramahi, *Electromagnitc Interference (EMI) Reduction from Printed Circuit Board (PCB) using Electromagnetic Bandgap structures,* IEEE Transactions on Electromagnetic Compatibility, Vol. 46, No 4. Nov 2004

[3] Jim Balistrern, *High Speed Multi-layer copper Interconnect Systems in the Datacom Market,* JAE Electronics, Inc. – ECN. 9/1/2004.

[4] eEngineer – EME, EMC, EMI: Printed Circuit Boards (PCBs) Tips#2common Printed Circuit Design Problems. Radioing.com-eEngineer

AUTHORS' BIO-DATA

Shri Prakash Chand joined Defence Electronics Research Laboratory, Hyderabad in 1972 after doing his Master Degree in Physics (Electronics) from Meerut University. He specialised in the field of Reliability Engineering & Quality Assurance and made significant contribution in products improvement for Electronics Warfare Systems and Integrated Guided Missiles Development Programs. In 1990, he joined Director under Ministry of Industries and brought the movement of Quality & Reliability in Himachal Pradesh. In 1991, at Defence Electronics Applications Laboratory, (DEAL) Dehradun, he established the Product Assurance set-up for MMW, Satellite Communication and Data link Projects. DEAL became the first ISO 9001 certified R&D Laboratory in INDIA during 1996 and winner of Golden Peacock National Quality Award- 1997. DRDO Technology Award - 1996 was given to him for his excellent contribution in the field of Quality System.

Shri BN Ganagopadhyay joined Defence Electronics Applications Laboratory, Dehradun in 1982 after doing his Bachelor Degree in Science and Engineering Diploma in Telecommunication from Calcutta University. He is specialized in the field of Computer-Aided Printed Circuit Board Layout Design, Signal Integrity and EMI/EMC simulations. He has established a set up of computerized PCB Layout Centre with laboratory wide networking. He has made significant contribution in making highly dense and complex multiplayer PCBs meeting signal integrity and EMI/EMC requirements.

Mrs.Meenakshi Kumar joined Defence Electronics Applications Laboratory, Dehradun in 1992 after doing her Engineering Diploma in Electronics from Roorkee. She is specialized in Quality assurance of Printed Circuit Board Layout design, bare and assembled PCBs. She has also prepared a guide on PCB layout design considering the requirements of vibration, shock and EMI/EMC. Presently she is working on reliability & maintainability predictions during design and development phases of the electronics products and coordinating for sustenance of Quality Management System at DEAL.