OVERVIEW ON DESIGN TECHNIQUES FOR PRINTED CIRCUIT BOARD LAYOUT USED IN HIGH TECHNOLOGY PRODUCTS

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Abstract

Computers used in Information Technology Equipment are now generating higher clock speeds than similar state-of-the-art products developed only a few years ago. Design techniques commonly used in the past have become insufficient for suppression of EMI at the printed circuit level and, perhaps, for basic functional signal quality as well. This paper presents an overview using a hands-on approach to solving radio frequency (rf) emissions on printed circuit boards.

Introduction

Recently published articles describe how rf occurs on two and four-layer printed circuit boards (pcbs). There has been limited discussions for layout of six or more layers. Clock speeds have easily exceeded 50 MHz. High speed, high technology processors (32/64 bit CISC processors, RISC processors, and similar devices) are being used in increasingly large numbers. Implementing the items presented in this paper will help reduce rf generated on the printed circuit board. Suppression of RF energy at the printed circuit board level minimizes costly containment schemes. Containment cannot always be relied upon for EMI compliance required for total product life cycle in a cost-efficient manner.

This presentation clarifies concepts and topic areas frequently overlooked during component layout. These concepts are highlighted to help 'junior level' engineers with minimal experience in the field of EMC become aware of different concepts and available tools.

PCB Configuration

Main areas of concern are: microstrip versus stripline topology, impedance control between planes, impedance control between loads, impedance control between sources and traces, voltage-ground plane imaging, and trace termination.

Microstrip topology refers to traces on a printed circuit board separated by a dielectric medium; e.g., adjacent planes. Although this topology provides for minimal suppression of rf energy on a board, faster clock and logic signals are possible. See Figure 1.

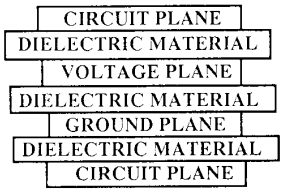

FIGURE 1
Microstrip Topology

Stripline topology refers to placement of circuit planes between image planes: either voltage, ground, or chassis. This topology provides for better noise immunity from rf emissions, but at the expense of degraded clock signals and system performance. See Figure 2.

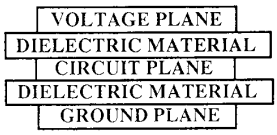

FIGURE 2
Stripline Topology

Impedance control in pcbs is based on various parameters, including dielectric height between planes, thickness of copper used, separation distance between trace layers, circuit trace plane location relative to a voltage or ground plane, and dielectric constant of the planar material. Calculations to determine exact impedance of planes is difficult due to these and many other parameters, however, exact calculations can be made by using method of moments. Approximate calculations of impedance for microstrip and stripline topology are presented in Equations 1 through 4. Although Equations 1 and 3 only approximate pcb impedance, they provide sufficient information required to determine impedance between planes. When all signal (circuit)

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planes are approximately the same impedance value, optimal signal transfer between components occurs with minimal crosstalk and rf standing waves. Control of packaging impedance also plays a factor in impedance control of pcbs.

Approximate formula for Microstrip Impedance:

$$Zo = \left(\frac{87}{\sqrt{Er + 1.414}}\right) Ln\left(\frac{5.98H}{0.8W}\right) \quad (1)$$

Propagation Delay for Microstrip Impedance:

$$Do = 1.016\sqrt{0.475Er + 0.76} \text{ nS/ft.} \quad (2)$$

Approximate formula for Stripline Impedance:

$$Zo = \left(\frac{60}{\sqrt{Er}}\right) Ln\left(\frac{4B}{0.67\pi(0.8W + T)}\right) \quad (3)$$

Propagation Delay for Stripline Impedance:

$$Do = 1.016\sqrt{Er} \text{ nS/ft.} \quad (4)$$

where

Zo = characteristic impedance
Do = propagation delay
W = width of the trace
T = thickness of the trace
H = thickness of the plane
Er = dielectric constant of the plane material

High density pcbs are generally created with computer aided design (CAD) systems and software. Most CAD application software provides for calculation of plane impedance.

The optimal plane stacking schemes for 6 and 8 layer pcbs are shown in Figures 3 and 4 where both microstrip and stripline topology is employed. For reasons of power impedance, the configuration of Figure 4 is preferred for fast edge and high trace or high signal density as compared to the power impedance of Figure 3.

Plane 1	CIRCUIT TRACE
Plane 2	VCC PLANE
Plane 3	CIRCUIT TRACE
Plane 4	CIRCUIT TRACE
Plane 5	GROUND PLANE
Plane 6	CIRCUIT TRACE

FIGURE 3
Stackup - 6 Layer PCB

Voltage and ground planes must be determined by functional application. Locating a power or ground plane adjacent to each and every circuit trace plane produces an image plane. RF energy is created by current in a trace. When this trace is located adjacent to a plane, an rf image is developed in parallel with this trace. The net result is, in simple terms, cancellation of rf energy and suppression of radiated noise. Hence, every circuit plane must be located adjacent to an image plane for maximum rf suppression. Prevention of crosstalk between planes is also minimized. [1]

Plane 1	CIRCUIT TRACE
Plane 2	GROUND PLANE
Plane 3	CIRCUIT TRACE
Plane 4	VCC PLANE
Plane 5	GROUND PLANE
Plane 6	CIRCUIT TRACE
Plane 7	GROUND PLANE
Plane 8	CIRCUIT TRACE

FIGURE 4
Stackup - 8 Layer PCB

Attention to detail must be observed when designing with picosecond transitions to avoid an effect similar to capacitive loading that occurs during normal routing of signals. When a trace makes a bend on the board, its capacitance per unit length will increase and its inductance per unit length will decrease. This is true for sharp angles of 90 degrees or more. See Figure 5.

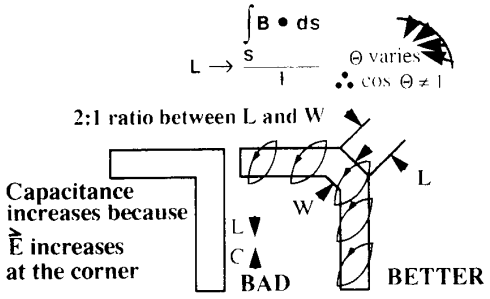


FIGURE 5
Trace Routing for Corners

Table 1 illustrates different impedance values of a pcb trace, 1/8" wide [2]. RF energy generated is also shown. With short trace lengths, higher frequencies

of rf energy occurs. Case shielding generally provides sufficient containment of high frequency rf energy if designed properly.

TABLE 1

Impedance of a PC Trace (1/8" Wide)

Frequency	Length 1"	3"	10"
1 MHz	.13 ohm	.38 ohm	1.25 ohm
10 MHz	1.25 ohm	3.75 ohm	12.5 ohm
100 MHz	12.5 ohm	37.5 ohm	125 ohm

Based on the formula $Z = 2\pi f(MHz) x20$ nh/in

Impedance of a 10" Wire As a Function of Gauge

Guage	Inductance	Impedance at 100 MHz
No. 10	450 nh	275
No. 20	520 nh	325
No. 30	600 nh	375
No. 40	650 nh	405

Impedance of a 10" x 10" Copper Metal Plane

Frequency (MHz)	Skin Depth (cm)	Impedance (Ohms/sq.)
1 MHz	6.6 x 10-3	.00026
10 MHz	2.1 x 10-3	.00082
100 MHz	6.6 x 10-4	.0026
1 GHz	2.1 x 10-4	.0082

Power and ground planes should not be the same physical dimension (width/length) when placed adjacent to each other. One plane should be physically smaller to remove rf fringing that occurs between edges of the power planes.

If necessity dictates that a multilayer design have two signal planes adjacent to each other, the traces should be orthogonal to each other. This minimizes the parallel runs that cause signal coupling.

Trace termination plays an important role in reduction of rf energy and standing waves on traces. Use of a series resistor from the clock driver circuit provides higher quality signal transfer. Clock signals are often daisy-chained between logic devices. Unless the distances are small between loads, (devices with respect to the propagation of signal rise time), reflections will result from daisy-chains. This impacts signal quality and EMI energy spectral distribution, therefore radial drive connections for fast edge signals and clocks are frequently preferred over daisy-chain. Each component should have its trace terminated, in addition to termination at the load circuit in its characteristic input impedance of the logic device. See Figure 6.

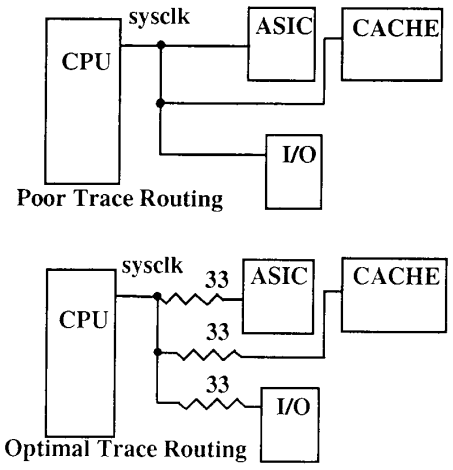


FIGURE 6
Trace Termination

Coupling of High Speed Components

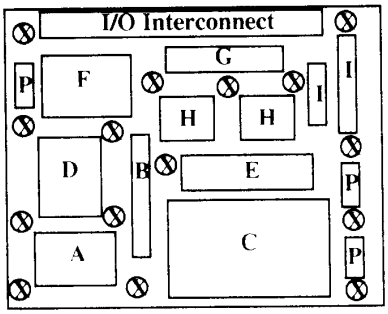
Optimal placement of oscillators and frequency-generating components provide for minimizing rf energy on pcbs. The most common layout rule is to locate high-speed devices away from I/O interconnects and control circuits. All devices using common clock signals must be placed adjacent to each other in order to minimize trace length. Placement of clock signals should be routed on the same internal plane, otherwise, routing clock traces on two different internal planes allows additional inductance in the circuit trace which may produce unwanted rf energy.

CAD systems used in high density layouts utilize auto-routing. While this feature saves time in routing traces, it incorporates worse case trace placement for clock signals. Before auto-routing, manually hand route all periodic signal traces for optimal performance (component placement) and to minimize trace length.

Proper placement of components is crucial in pcb layout. Most designs incorporate functional subsections (in logic). Grouping each functional area adjacent or between other subsections minimizes periodic signal trace lengths and rf standing waves; maintains signal quality. Functional subsections should be routed on the same circuit trace plane. Avoid use of vias (interconnects between planes) where possible. Figure 7 illustrates functional

should be routed on the same circuit trace plane. Avoid use of vias (interconnects between planes) where possible. Figure 7 illustrates functional grouping on a stand-alone cpu pcb.

Extensive use of chassis ground connections is also illustrated in Figure 7. High frequency, high technology products require new methodologies for bonding logic and power grounds to the chassis.



A = CPU, F. P., Osc. (high speed logic)
B = Memory Buffers (high speed logic)
C = Memory Array (high speed logic)
D = Gate Arrays (high speed logic)
E = DMA Controller (high speed logic)
F = I/O Logic (low speed logic)
G = User Interface Logic (low speed logic)
H = Support Logic (low speed logic)
I = Peripheral I/O (low speed logic)
P = Power for Peripherals
X = Chassis Bond Connection

FIGURE 7
Component Placement
PCB Layout

Systems with clocks above 50 MHz require frequent ground connections to minimize the effects of common-mode eddy currents present between functional areas. At least four ground points surround each of the following sections; CPU/Floating Point components, memory array, DMA, control logic and I/O. Note that a chassis bonding (ground connection via a screw or other securement method) is located on both ends of the power connectors used for peripheral devices. Noise generated on either the pcb or peripheral power subsystem is shunted to chassis ground, thus optimizing signal quality for data transfer. Many chassis bond connections are not be popular with manufacturing, but, Class B radiated performance will be assisted with this multiple chassis bonding technique.

Decoupling

Decoupling refers to preventing energy transference from one circuit to another. Three areas of concern exist: power and ground planes, components, and internal power connections.

Multilayer pcbs generally contain one or more pair of voltage and ground function planes. As shown in Figures 3 and 4, optimal placement of power planes function as one large low-inductance capacitor which removes rf energy generated from components and traces. Power planes alone are not sufficient. Multiple chassis bond connections to the ground planes prevent voltage gradients which are a major reason for common mode noise created between planes.

RF energy present on layers 3 and 4 (Figure 3) is suppressed by layers 2 and 5 (voltage and ground), with the impedance of voltage/ground increased by the distance between planes. RF energy generally will not radiate to the outside environment, so clock traces must be located in either layer 3 or 4, but not both.

The same is true for the layers shown in Figure 4. RF energy present on layer 3 is contained by layers 2 and 4 (voltage and ground) while rf energy on layer 6 is contained between layers 5 and 7 (ground and voltage/ground). It is not necessary to have an equal number of voltage and ground planes; one voltage plane and three ground planes is sometimes preferred since image plane effects are what we want to achieve. Layers 4 and 5 remove additional common mode rf energy that is present.

Ten or more layer pcbs must follow the convention of placing a circuit plane adjacent to an image plane (voltage or ground). If any traces are routed in an image plane, benefits of rf suppression by imaging are reduced and signal quality may be compromised.

Some components still require additional decoupling. Standard TTL logic is decoupled by the power planes. CMOS, ECL, and other fast logic families require additional separate decoupling capacitors as used in standard component layout. In addition, the placement of 1 nF (1000 pF) capacitors (capacitors with very high self-resonant frequencies), on one inch centers throughout the pcb provides additional protection from standing waves and rf energy generated by traces, especially if the

higher power impedance implied by Figure 3 is used (compared to the lower power impedance of Figure 4).

If a power connector is located on the pcb, rf noise may be generated between the power planes and an external device. A simple method to remove rf noise is to place two capacitors in parallel immediately adjacent to each voltage pin, as shown in Figure 8. Capacitance values must differ by a factor of 100. The total capacitance of parallel capacitors is not important, rather the parallel reactance provided (by the capacitors) and their rf filtering characteristics is what is important due to the self-resonant frequency of the capacitors.

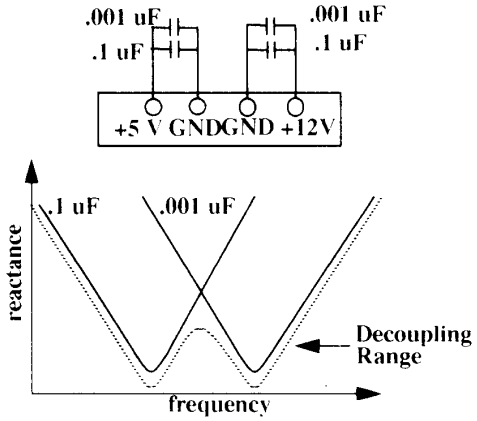


FIGURE 8
Internal Power Decoupling

I/O Interconnections

Most FCC, VDE and CISPR compliance problems deal with I/O interconnects. Simple layout techniques on the pcb minimize rf emissions in addition to increasing electrostatic discharge (esd) immunity at no additional cost. These techniques include use of fences, moats, and connector ground schemes.

A fence is simply a metal barrier strip soldered to the ground plane(s) at half inch (1/2") intervals to prevent radiated rf energy generated on the pcb from entering other functional areas. A fence is essentially a can without the top cover covering a circuit area.

Provision for fences must always be provided on the pcb, however usage may not be required as determined by testing.

Moats are used to prevent unwanted rf energy present in the logic and power planes from entering I/O interface components and connectors. A moat is the absence of copper through all layers of the pcb except for one small drawbridge large enough to pass specific circuit traces. Both ends of the drawbridge must be bonded to chassis ground with screw or equivalent means. If an isolation transformer is used (e.g. Ethernet), place the moat between the input and output terminals. Signals or power traces are not allowed to cross moats without ground bridges in order to preserve image impedance and to circumvent eddy currents. Figure 9 illustrates how a moat appears on a pcb.

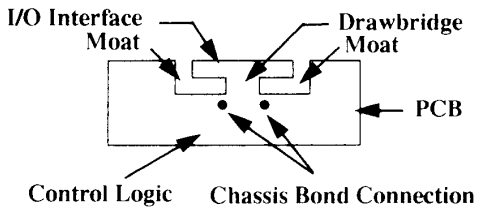


FIGURE 9
Moat Implementation

Another advantage of fences and moats is that they prevent esd from damaging critical, expensive components. The cost of replacing an RS-232 transceiver is much less than replacing LSI, VLSI, and ASIC components.

All I/O connectors must have their face plate bonded to the metal chassis to provide a low impedance ground for rf currents present on cable shields. Also, ground the metal face plate of the I/O connector to the ground plane of the pcb to provide absolute grounding for both rf noise and esd suppression should metal-to-metal contact between the connector face plate and the metal chassis be lost.

Summary

Layout of high density, high technology pcbs using high speed clocks requires different implementation schemes from products developed only a few years ago. Main areas of concern are:

- Prevention of ground loops between functional areas
- Multiple bonding of ground plane(s) to chassis
- Usage of an image plane adjacent to each circuit plane
- Extensive use of decoupling capacitors place in a grid array
- Decoupling power interconnects
- Impedance control on planes
- Usage of fences and moats

Items presented illustrate major concerns one faces during pcb layout. Only a brief list of items was presented to make one aware of ideas and methods available when designing for compliance to emi regulatory approvals.

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