An Overview of Digital Circuit Design and PCB Design Guidelines – An EMC Perspective

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ABSTRACT

There is a revolution in modern digital ICs &PCB designs and their usage triggers the need for better understanding of PCB design[apart from digital circuit design] in detail. Design of digital circuits need special cares with respect to EMC and hence the associated mounting of components besides PCB design layout. These aspects are addressed in this paper with Check list in the form of detailed design guidelines for both areas. Also the current trend and future challenges in PCB design for next generation ELECTRONICS are discussed in brief.

I. INTRODUCTION

PCB designs are undergoing dramatic changes in recent time's with respect to reduction of size and weight while making them more electrically and environmentally friendly. EMI-EMC properties are equally given importance while providing enhanced functionality and ease of manufacturing. As high speed applications are on the increase with respect to digital computers and single board computer cards in the computing and communication industries, there are more challenges in PCB design, signal integrity and its EM compatibility. The design and layout techniques require a critical relock with regard to fundamental approach in tackling RF/EMI suppression to achieve EMC. Selection of digital logics, their placement in PCB, interconnections, component protections from EMI/transient point of view and observing basic design guidelines go a long way to prove the reliability of PCBs in its associated interfaces in subsystems and systems.

Design and layout techniques for suppression of EMI within a PCB is most cost effective way to use than relying upon containment measures provided by its housing / metallic enclosures. Once the PCB design ensures the compliance requirements, containment can add to the life time protection and EMC, though they are removed or damaged by end user later. Still the intrinsic functions are ensured to the user. Noise source on a PCB relates to frequency generating circuits, long PCB trace (electrical lengths) poor impedance control, cable interconnects etc. Therefore these aspects ultimately determine the EMC compliance requirements.

II. DESIGN OF DIGITAL CIRCUITS

Before the designer start the design of digital circuits, the designer is reminded with a few fundamental issues. Firstly when dealing with emissions, one should understand the rule of thumb. That is higher the frequency, the greater is the likely hood of a radiated coupling path, the lower the frequency the greater the likely hood of a conducted coupling path. Also the major considerations for EMC analysis deals with (a) frequency (b) amplitude (c) time (d) impedance and (e) dimension. This means defining the problem in frequency spectrum to realise how strong is source energy level and how great is its potential to cause harmful interference effect etc. Also, is time a continuous problem or exist only during certain cycles of operation, impedance of source and receptor and the transfer mechanism between the two.

Physical dimensions due to trace length determine the frequencies that are likely to be observed. Simplified equation is $V_{rf} = I_{rf} Z$ ..... (1)

accounts for the EMI to be created with in the PCB. If a low impedance direct line path from load to source does not exist, RF current cannot return to the source to satisfy the circuit in an optimal manner. This path may exist as free space (377 ohm) if a solid return path is not available. But there is a finite physical distance between trace and RF current return path that makes the magnetic flux coupling and return structure partially.

This finite amount of left over RF current which is not coupled to a return structure is a primary cause of EMI within the PCB. Rise and fall time of signal restricted and maintained within 5 to 15% of pulse duration will optimise the bandwidth, without impairing normal functioning of circuits. Design of digital circuits for high speed high power logic needs careful planning particularly circuits handling parallel data. Each bit of a byte or word of parallel data needs the same wave

shapes or filtering so that all the parameters are identical.

III. EMC MEASURES & DESIGN GUIDELINES FOR HIGH SPEED DIGITAL CIRCUIT DESIGN

Digital ICs tend to be both culprits and victim of EMI. Therefore following guidelines are applicable in design of digital circuits.

(a) To prevent glitches un terminated transmission lines must be kept smaller than

1c =o.5 tr/tu metres long. (Fig 1) .....(2)

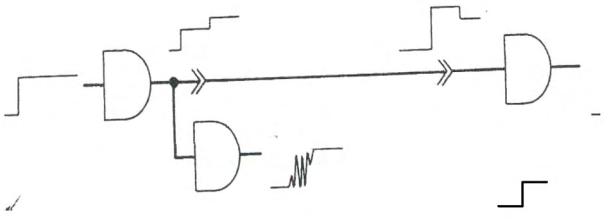


Figure 1 Glitches caused by reflections on long wires

(b) Noise on input signals must be less than the noise margin estimated

(c) To reduce noise emission from digital logics, keep signals slow with small voltage swings, limit the number of signals that at one time and use good grounding and by passing techniques.

(d) To reduce noise pick up, use slow synchronous ICs with Schmitt trigger inputs.

(e) If the system has long cables, use differential drivers and differential receivers connected by balanced transmission lines to reduce noise emission/pickups.

(f) Cables, PCB traces and wires should be terminated whenever the signal propagation time exceeds half the signal rise or fall time. Flat cables, twisted pairs and coaxial cables should be terminated in their characteristic impedance

$$Z_o = 20\Omega \; < \; Z_0 \; < \; 200\Omega \quad \ldots\ldots \quad (3)$$

(g) Design clock line routings which minimises the clock line loop size and ensure clock line return path next to clock line.

(h) Design metal housings for shielding of active components like clocks, ICs, microprocessors etc. EMI suppression sheets made of magnetic Materials/layers with intervening conducting layers act as effective Shields. This is available in various forms like cable wrap, cubic cap, Sheets for structures and also in paint form (DIP coating).

(i) Positioning the PC board is an important aspect. (i) Bypass ground plane at I/O connector (ii) group regulators/power supplies near I/O connector. (iii) place crystals/RC clocks, circuits next to ICs. Grouping of same family of electronic devices together will form a better design. (ex, analog, low, medium and high speed logics, interfaces) Auto route the PC board one partition group at a time with signal lines last Fig (2 a, b & c).

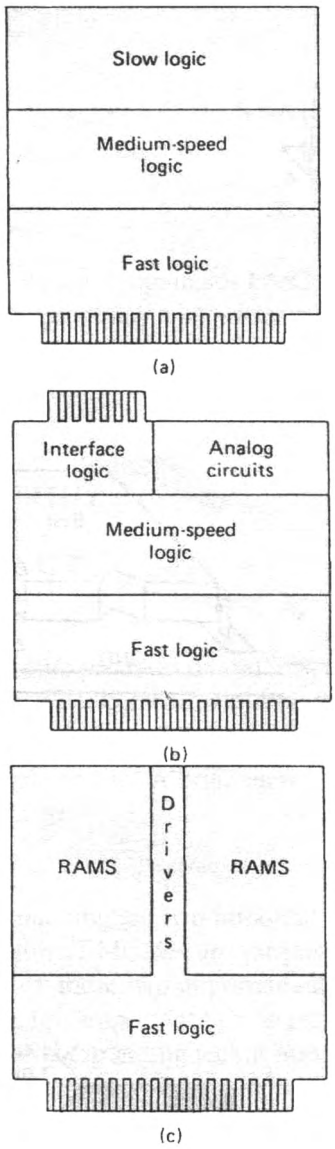


Figure 2 Partitioning digital printed circuit boards: (a) Processor board, (b) interface board (c) ram board

(j) Design the power distribution system for minimum drop, minimum noise pick up and radiation. Power

entry and return lines should be close to each other for minimum impedance and loop size.

(k) Provide bypass to all lines at i/o connections which reduces RF entry and also RF leaving the PC board at exit

(l) Decoupling of active components and power supply line is recommended which minimises instantaneous current drawn on the power bus (by placing a capacitor) from the IC power to the IC ground. Calculated capacitor value can be exact to the problem. Bulk decoupling capacitor of 10-100uf electrolytic at power entry point is recommended. Designer should not overlook the location/placement of decoupling capacitor especially in ICs (Fig 3 a, b & c). For different package the lead frame inductance varies and the lowest is to be picked. (Typically 1.8 to 9nh for various leads of ICs). The larger the decoupling capacitor value, the self resonant frequency will be lower. Too small a decoupling capacitor will not have sufficient charge storage for transient current needed by the integrated circuit. Different integrator circuit package configurations will change the IC lead frame inductance.

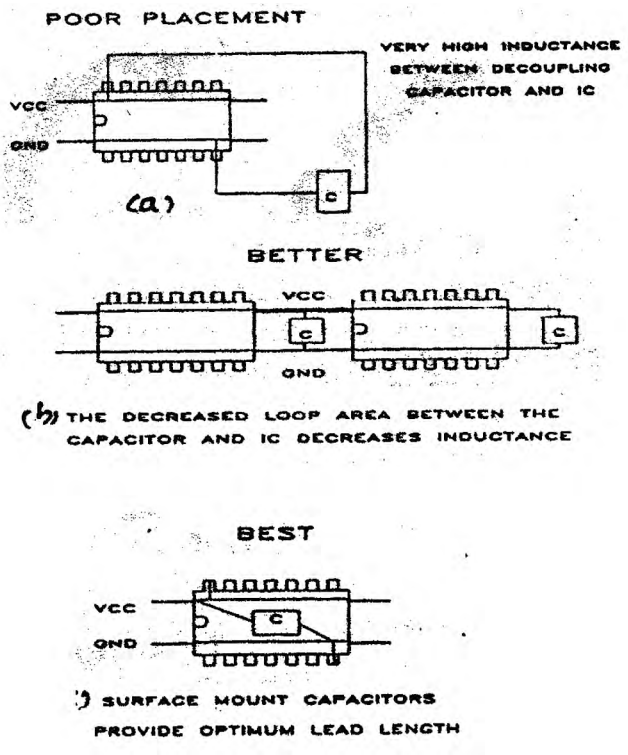
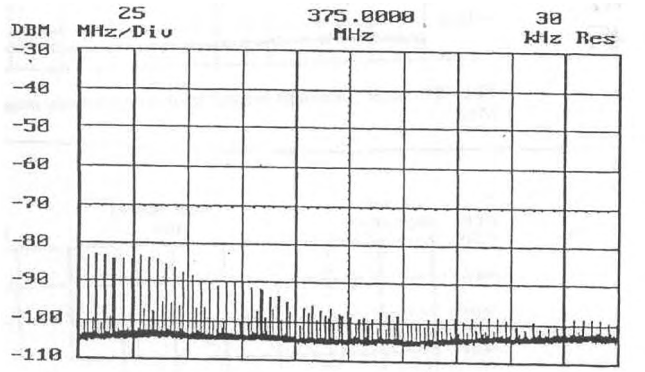


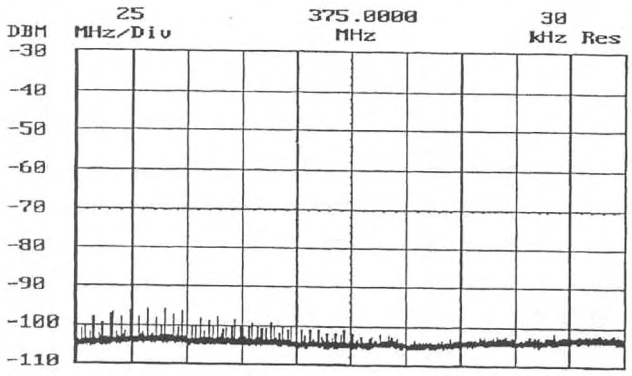
Figure 3 Placement of decoupling capacitors in ICs

(m) All unused IC input pins are to be grounded which reduce IC noise by lowering the ground impedance and eliminate unused IC pins from acting like antennas.

(n) IC process size affects EMC. Therefore selection of process size with fast rise time like 2.4ns can be of troublesome emission problem (1.5µn) Designer must make qualitative measurement for better choice.(Figures 4a & b)



(a)



(b)

Figure 4 a) Magnetic emission of 1.5-micron process from 250 to 500 MHz

b) Magnetic emission of 1.95-micron process from 250 to 500 MHz

(o) In the power/grounding scheme of PCB traces, coplanar lines work well on wire wrap boards and double sided PCBs. (Fig 5a) Laminar buses (Fig 5b) help reduce Vcc to ground noise but require special busbars. Multilayer PCBs can use solid ground planes and voltage planes (Fig 5c) or they can split voltage planes between several supply voltages. For best noise performance, the top and bottom layer board should be ground planes of voltage planes with signal planes in the middle.

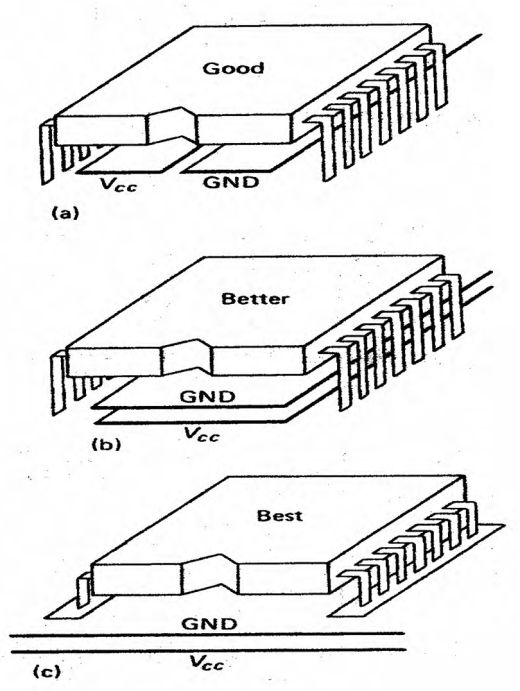


Figure 5 Power/ground bussing
(a) coplanar lines (b) laminar bus (c) ground

(p) Line impedance terminator is

$$Z_o = \left(\frac{R_1 R_2}{R_1 + R_2}\right)\left(\frac{2V_1 - 2}{V_2}\right) \text{ohms} \quad \ldots\ldots(4)$$

(q) Even harmonics of clocks can be greatly reduced by using clocks=50% of duty cycles. Number of ICs served by each clock to be limited. If clock must go to several boards, use Schmitt trigger input gates as buffers and limit the voltage swing and edge rate of the main clock signals.

(r) If clocks are to be controlled by off board switches do not route the clocks through the switches. Instead switch should operate control lines to on board gates that in turn enable/disable the clocks. Staggering the clock signals and using multiple oscillators will also help reduce clock noise.

(s) To reduce transient currents on Vcc and ground, use staggered clocks to control small group of ICs. Use synchronous ICs and input data strobes to reduce the % of time that a system is sensitive to noise.

(t) To prevent noise problem each i/p signal to a board should go to only one IC (preferably that with Schmitt trigger input). Schmitt trigger inputs increase the noise immunity and easily handle slow signals. If i/p signals must go to a regular gate, keep the rise and fall times short to prevent oscillations

$$\frac{dv}{dt} \geq \frac{0.1v}{t_1 h} \quad \ldots\ldots\ldots (5)$$

(u) The outputs of flip flops, counters and shift registers should be buffered through gates or line drivers to prevent glitches problems.

(v) Never use single point grounding in case of digital circuits. Multipoint grounding technique is a must.

IV. PRINTED CIRCUIT BOARD DESIGNS

When power supply and return traces are in close proximity they form a transmission line which significantly reduces distribution impedance and cross talk. The characteristic impedance,

$$Z_o = (120 // \varepsilon_r) \log T(\varpi + t) \text{ for } \omega >> t \quad \ldots. (6)$$

for a vertical bus the formula reduces to

$$Z_o = 377 // \varepsilon_r (h / \omega) \text{ where } w >> 3h \quad \ldots\ldots.(7)$$

h>>3t.

For parallel trace of h = 2.5m, w=2mm, t=0.035mm, εr = 1, we get Zo = 162 ohm and for vertical bus ε_r = 4.7 (for glass epoxy), t=0 1 mm of copper sheet Zo = 7 ohm. Parallel strips are good for minimising noise. Parallel strips with glass epoxy in between have low impedance. Since impedance is low, barrier layer ceramic capacitor need not be used at every DIP. Hence reliability of the configuration is high. Following guidelines shall be applicable for PCBs to reduce cross talk between adjacent traces.

a) Adding a ground trace between the generator and the victim trace could be used beneficially for reducing the cross talk between circuits

b) It is advantageous to have a bottom large copper plane to reduce cross talk.

c) Increasing the edge to edge trace separation leads to reduction of cross talk between adjacent traces.

- PCB cross talk can be reduced considerably by employing one or more of the following techniques in case of micro strip lines.;
  1. Increasing the trace separation
  2. Decreasing trace to ground height,
  3. Using ground trace between source and victim traces
- The grounded guard traces can minimize the cross talk
- To minimize the cross talk between two conductors, increasing the separation between them is better.

- Some other techniques to obtain better performance of minimizing crosstalk are;
  1. Using slower rise time.
  2. Terminating both the ends of traces.
  3. Avoiding the parallelism between traces.

V. EMC CHECK LIST FOR PCBS

Following check list can help the designer in perfecting the EMC design of PCBs for workable solutions in difficult situations.

(a) Select the slowest switching speed for electrical devices (thereby ensuring minimum bandwidth) which leads to reduced radiated emissions and susceptibility.

(b) Design PC board jumper cables to minimise loop area so that emission or susceptibility is reduced. This is achieved by having return paths for all types of signal and power lines.

(c) While organising multipin connections through ribbon cables keep the highest amplitude and lowest amplitude signals far apart in pin connections. Between adjacent pins observe the criteria of comparable signal leads. While using multilayer ribbons, in the top layer keep the higher amplitude signal pin in descending order and lower layer still lower amplitude signal pin in same order like top layer. This organised signal concept can reduce the EMI both emission and susceptibility because low impedance signals are less susceptible to EMI and high impedance signals are more susceptible to EMI. (Fig. 6) Similarly low power signal generates weak EM fields while high power signals generate strong EM field.

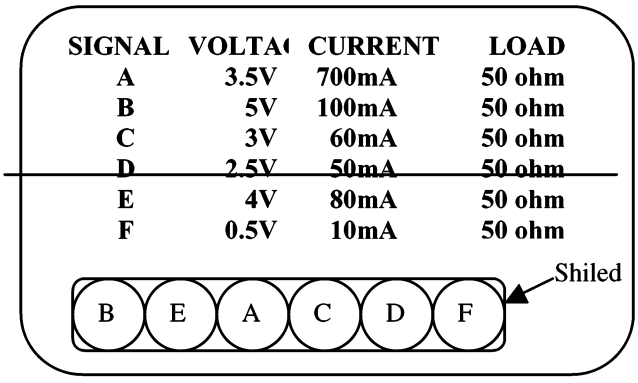


Figure 6 Organised signal concept

(d) Signal traces when laid should not have sharp bends (Fig 7a) Chopping of corners, limiting boards to 90' or using gentle curves (Fig 7 b, c & d) will ensure the trace impedance nearly constant from dc to several GHz.

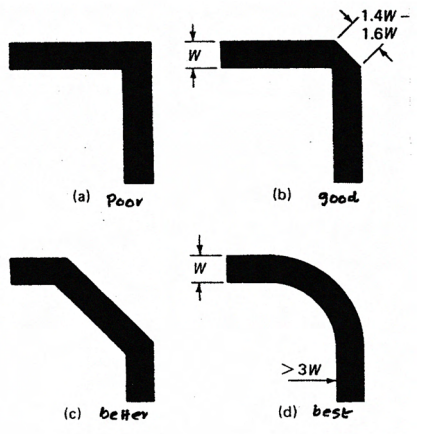


Figure 7 PCB Track bends

VI. CURRENT TRENDS IN EMI SUPPRESSION OF NEXT GENERATION PCBS

So long, a technology called multi chip module (MCM) concepts have brought dramatic changes in chip size, weight, and performance improvements. They are expensive and best suited to high end electronic subsystems of mainframes and workstations beside military and telecom switching systems. A recent innovation known as sequential build up technology (SBT) aims at low cost for high volume requirements.

SBT depends on the application of additional thin laminates or dielectric layers into the standard PCB core. Various techniques can be applied to create feed through or vias between electrical layers such as laser drilling and plasma etching. Presently FR4-PC B technology is nearing the end of its life with its track width, via diameters and spacing such that its performance (of low power dissipation and low EMI radiation) along with packaging density reaching its ultimate limit. Now SBT allows the partial replacement of discrete resistors by buried printed resistors on inner layers. Using buried resistor technology relieves broad area freed up by reducing the amount of discrete component area.

As smaller size is allowed in SBT the usage of thin film dielectric build up layers, the density of track length/unit square can be increased almost by a factor of 2 and also the reduction in cross section of the board thickness reduces the value of the board. Therefore the track topology is shortened which means shorter current loops and shorter stub length. Since EMI emissions are proportional to the area of current loops, this significantly reduces EMI emissions and also

susceptibility. Smaller size also means that high i/o package density flip chips and ball grid array components can be used which again reduces inter connects thus current loops will be reduced.

The reduction in track topology due to these improvements will also reduce Stray inductance and capacitance, which will lead to reduction of power consumption and high frequency performance improvement. This lower power consumption is beneficial for manufacture of palm top computer or portable telephones/mobiles, as reduction in the size and weight of the operating batteries will be possible. This in turn will also attract for the lighter product and also make it cheaper to manufacture.

For the next generation digital designs, the use of tightly coupled package(s) will improve signal integrity because Parasitic effects are reduced and also significantly "reduce or even eliminate EMI". SBT is a promising candidate for this in near future.

VII. CONCLUSIONS

EMC approach to digital circuit designs and PCB designs are discussed briefly. A detailed checklist on PCB making from the point of view of achieving EMC is addressed. Current trends in EMI suppression techniques of next Generation of PCBs are also briefed.

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