# PDF document

Sunday, September 13, 2020 7:26 PM



PDF document

## Solutions to FIT1047 week-6

## Week-6 topics:

- Discuss CPU, Boot, Motherboard, chipsets and Boot Process:
- Discuss the Assignment -1 progress with the students.

#### CPI

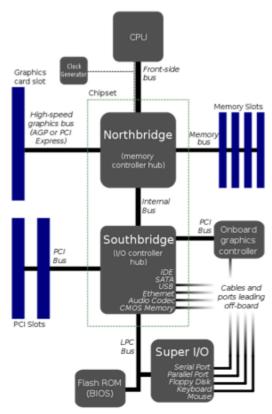
**Exercise 1:** What is the difference between the three methods used by the CPU to interact with I/O devices?

#### **Boot Process:**

**Exercise 2:** Difference between the Booting Process with UEFI and the Booting Process with BIOS

#### Exercise 3: Motherboard, chipsets and Boot Process:

a) Explain with respect to the diagram below, what a computer chipset is?



b) Explain how the communication takes place between Northbridge and Southbridge?

## PART-II

### Second hour of Lab.

Discuss the Assignment -1 progress with the students.

1

#### Ex1

1.

Polling is the system continue looping for check if the device finished or not For example, the mouse, the driver can set the report rate per second. The polling frequency is depended on the resolution required of the

The interrupt is the driver sending a command, then the system stopped and starts transfer data to memory.

Direct Memory Access (DMA), which is moving the entire block of data, the CPU is only control the start and the end(interrupt) of transferring.

2.

- 1, UEFT can boot 2.2tb or larger with the upper limit 9.4 zettabytes, but BIOS can't boot them with restricted 1M space.
- 2, BIOS runs in 16 bits mode, UEFT can run 32- or 64-bits mode which is faster.
- 3, BIOS cant initialize multiple hardware at the same time, but UEFT can.
- 4, UEFI can boot the network before OS started
- 5, UEFI only allows authentic driver load in boot time, which is safety.

3.

- A) The chipset is the control center between the CPU, Memory, Peripherals, Bus slots, and I/O devices. The chipset is directly connecting with the CPU every device has to communicate with the CPU through the chipset. Northbridge connects with the CPU, graphic card, and memory, southbridge connect with the PCI bus, graphic controller, BIOS which have a lower position.
- B) Northbridge and the southbridge communicate through the BUS. Due to the CPU is on the northbridge, the northbridge is faster than then south, but the south just connects with the PCI, I/O, and BIOS, which means it won't need so fast. The BUS is a connect between two bridge and allow the data transfer between two bridges.