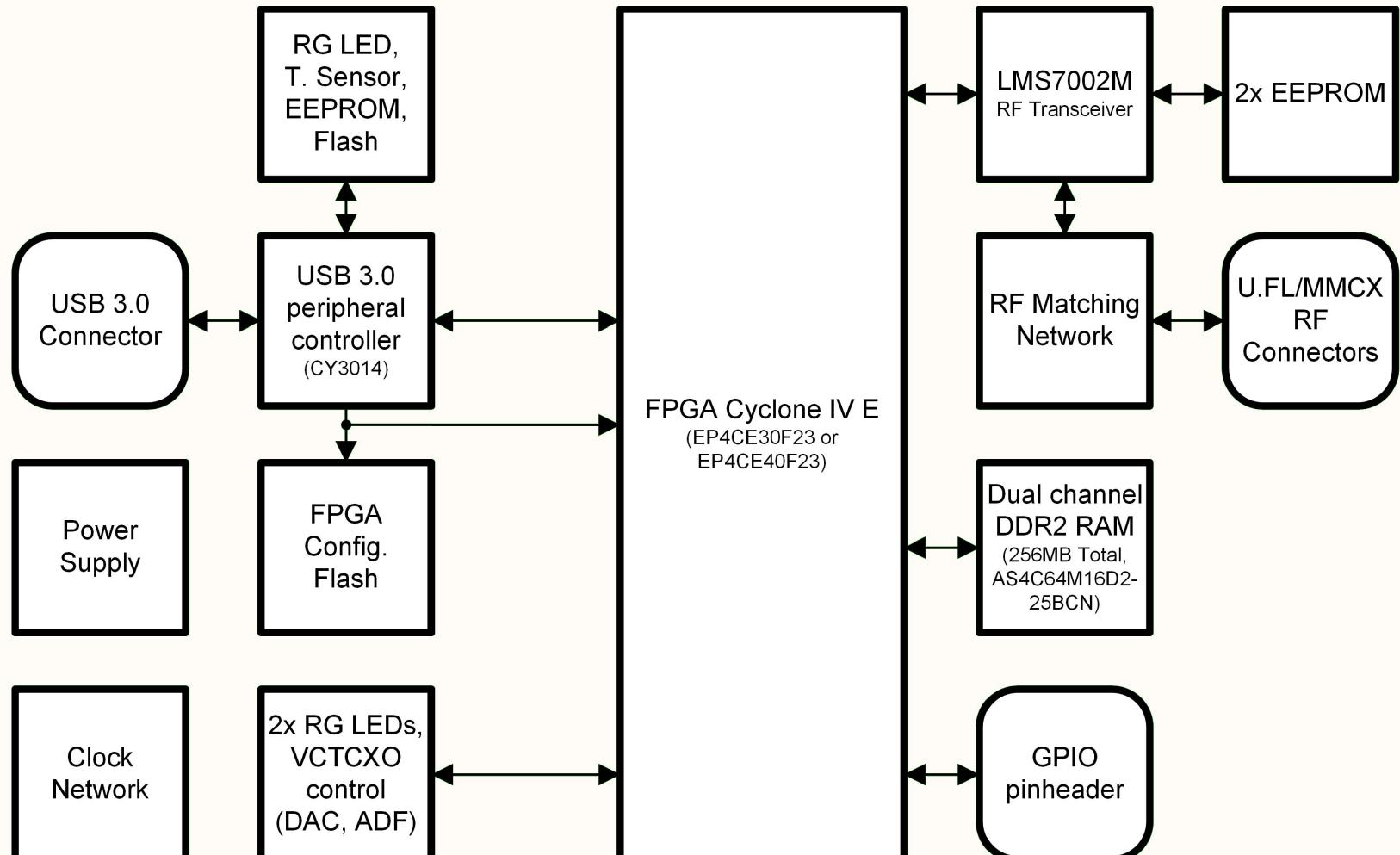


Block diagram



Project name: **LimeSDR_1v2.PrfPcb**

Title: **Block diagram**

Size: **A4** Revision: **v1.2**

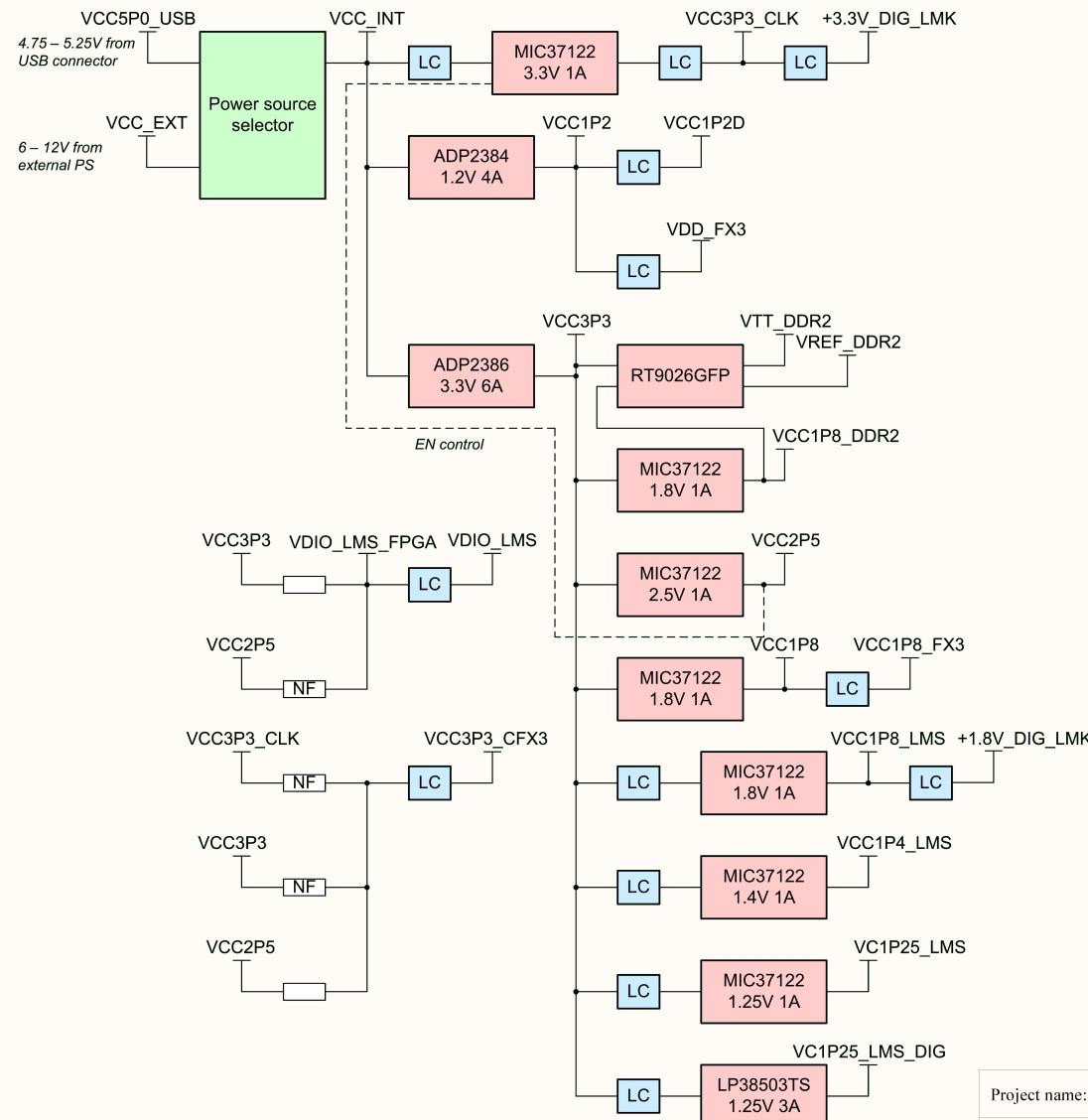
Date: **2016-04-21** Time: **10:28:44** Sheet**1** of **14**

File: **01_BlockDiagram.SchDoc**

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Surrey
United Kingdom



Power diagram



Project name: **LimeSDR_1v2.PrjPcb**

Title: *Power diagram*

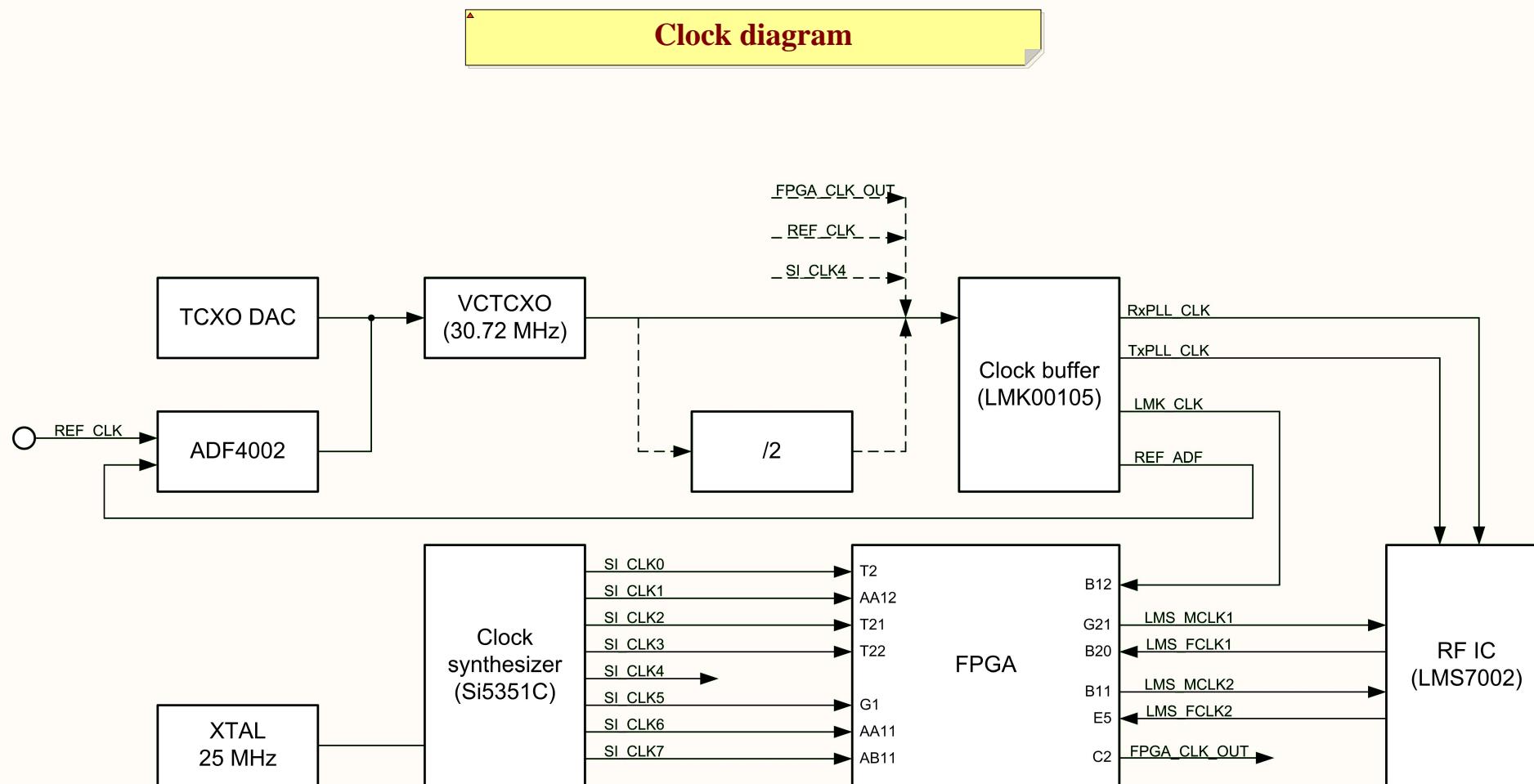
Size: A4 Revision: v1.

Date: 2016-04-21 Time: 10:28:49 Sheet 2 of 14

File: 02_PowerDiagram.SchDoc

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United Kingdom*





Project name: **LimeSDR_1v2.PrfPcb**

Title: **Clock diagram**

Size: **A4** Revision: **v1.2**

Date: **2016-04-21** Time: **10:28:59** Sheet**3** of **14**

File: **03_ClockDiagram.SchDoc**

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LMS7002M digital circuit

A

B

C

D

E

F

G

H

A

B

C

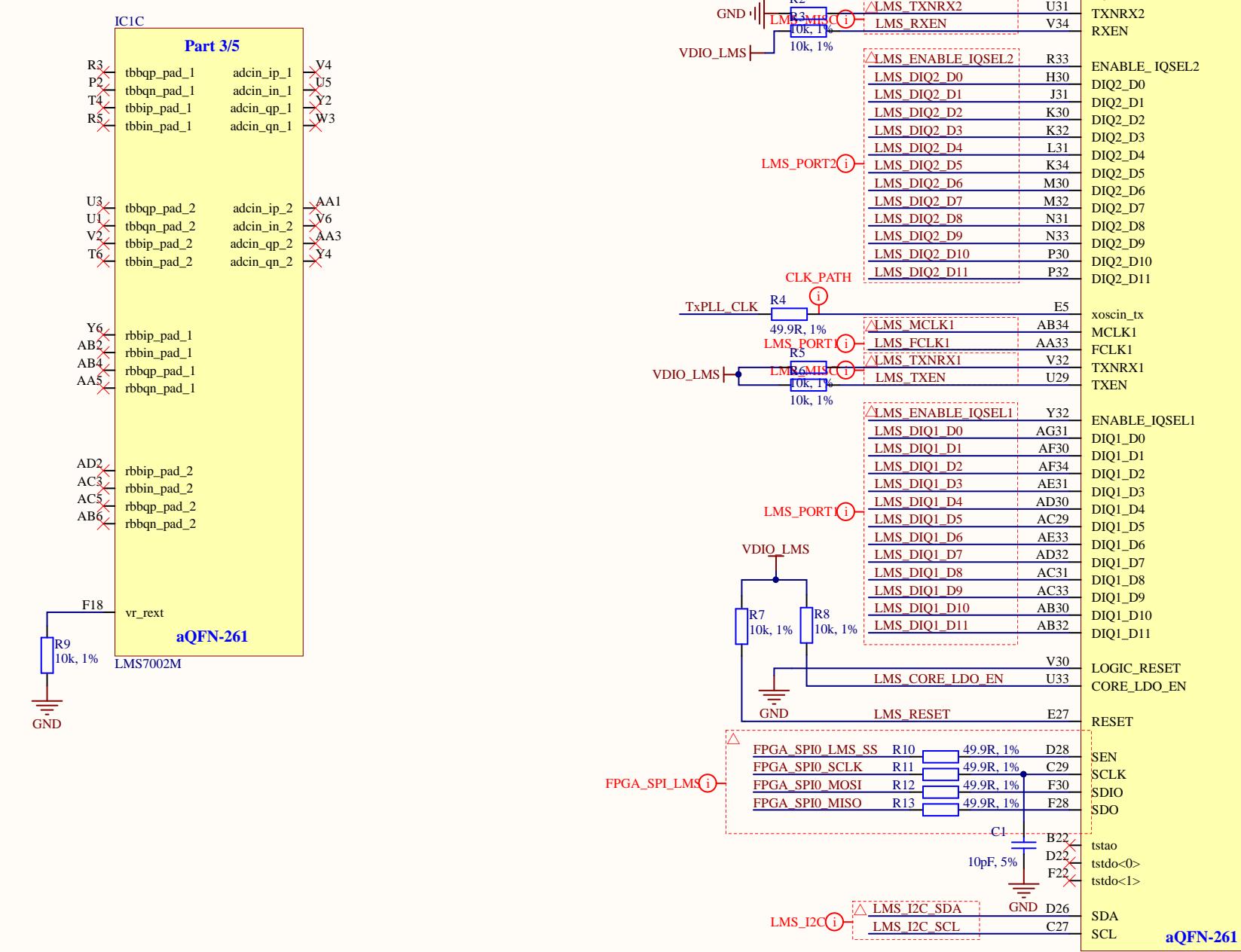
D

E

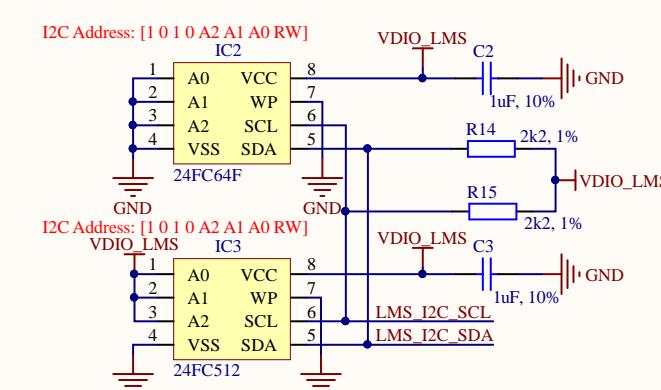
F

G

H



LMS EEPROMs



Project name: LimeSDR_1v2.PrbPcb

Title: LMS7002M digital circuit

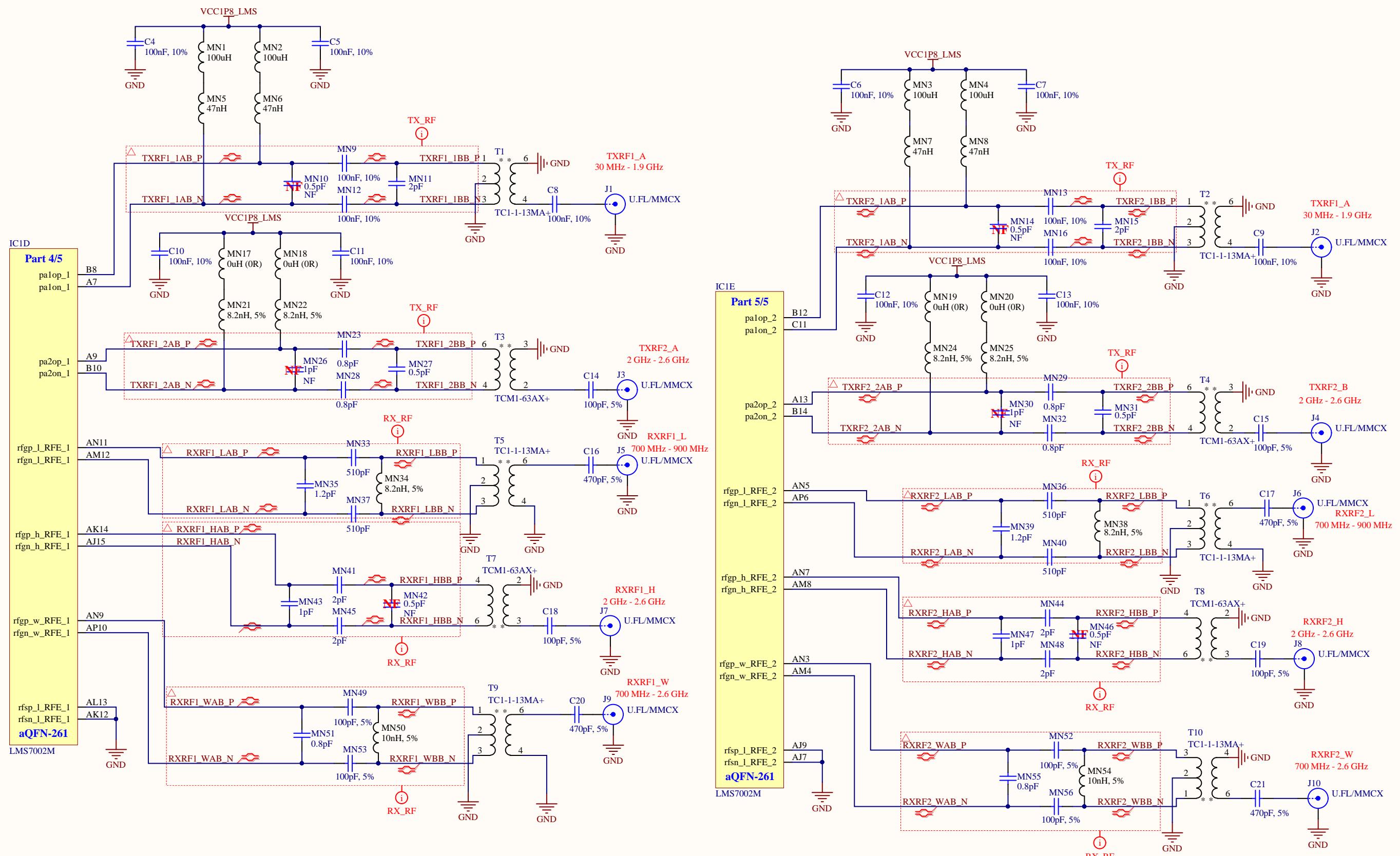
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United Kingdom



Size: A3 Revision: v1.2
Date: 2016-04-21 Time: 10:29:04 Sheet 4 of 14
File: 04_LMS7002M_Digital.SchDoc

NF elements on sheet: MN10, MN26, MN42, MN14, MN30, MN46
Number of NF elements on sheet: 6

LMS7002M RF circuits



Project name: LimeSDR_Iv2.PjPcb

Title: LMS7002M RF

Size: A3 Revision: v1.2

Date: 2016-04-21 Time: 10:29:07 Sheet 5 of 14

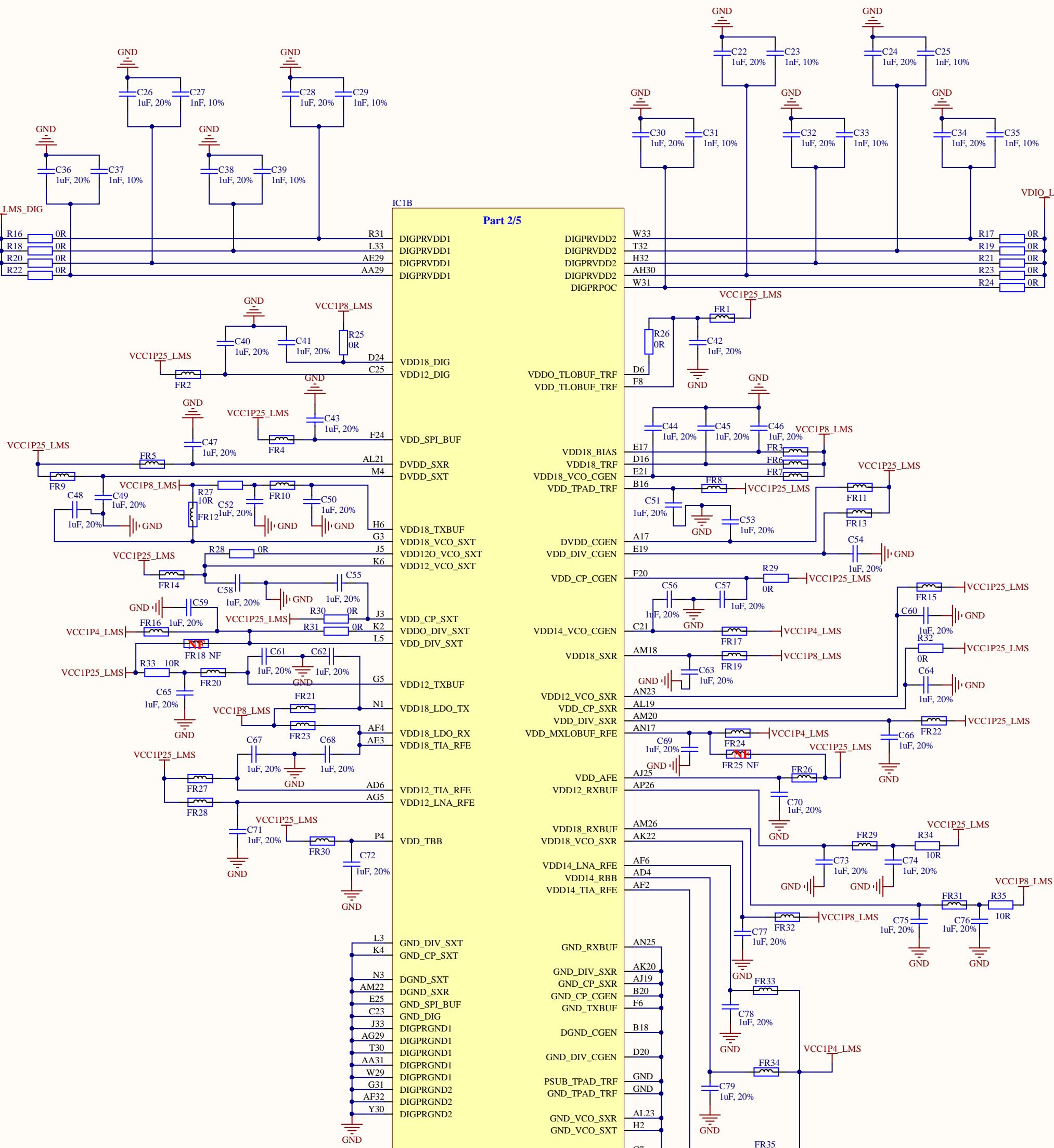
File: 05_LMS7002M.RFSchDoc

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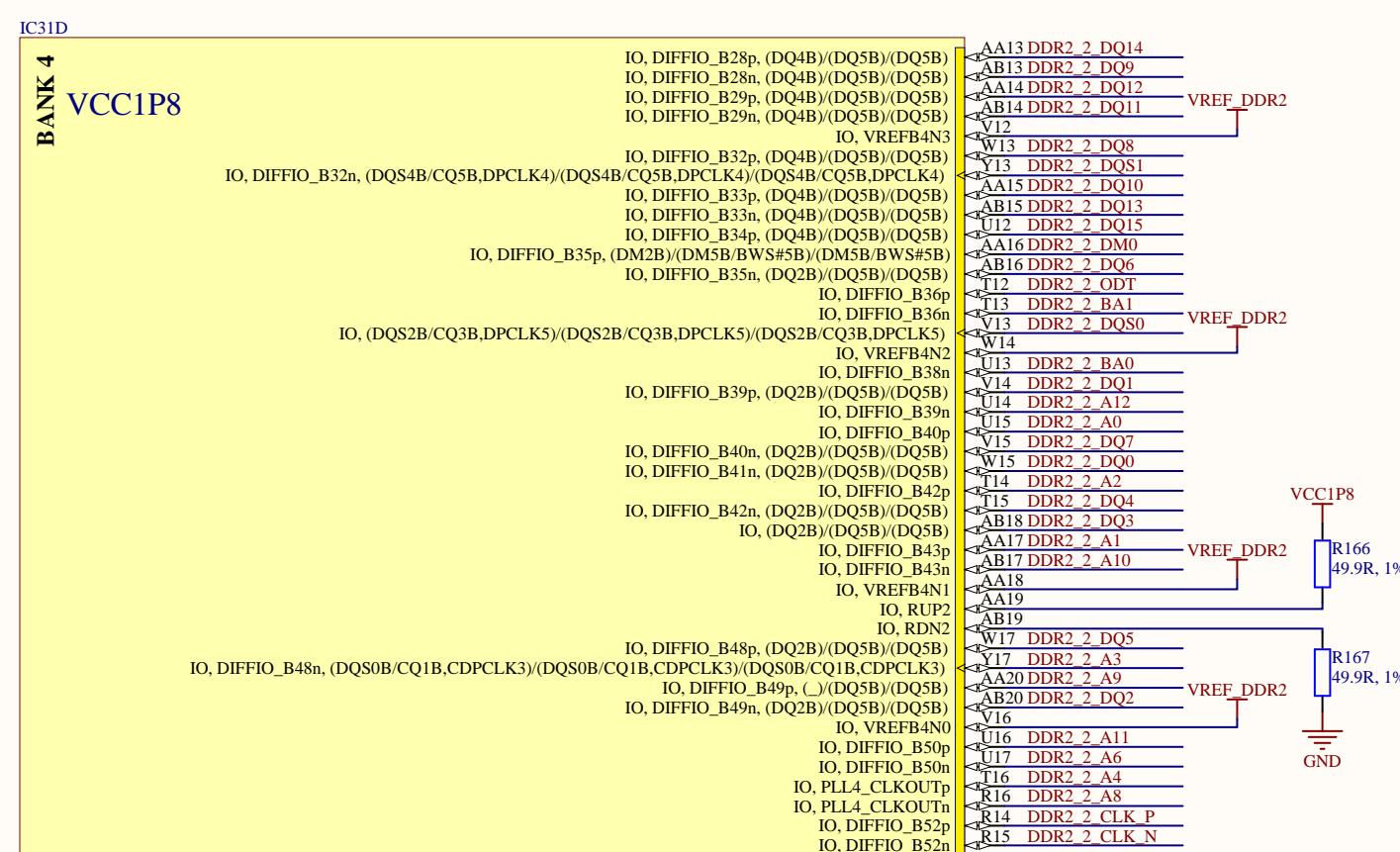
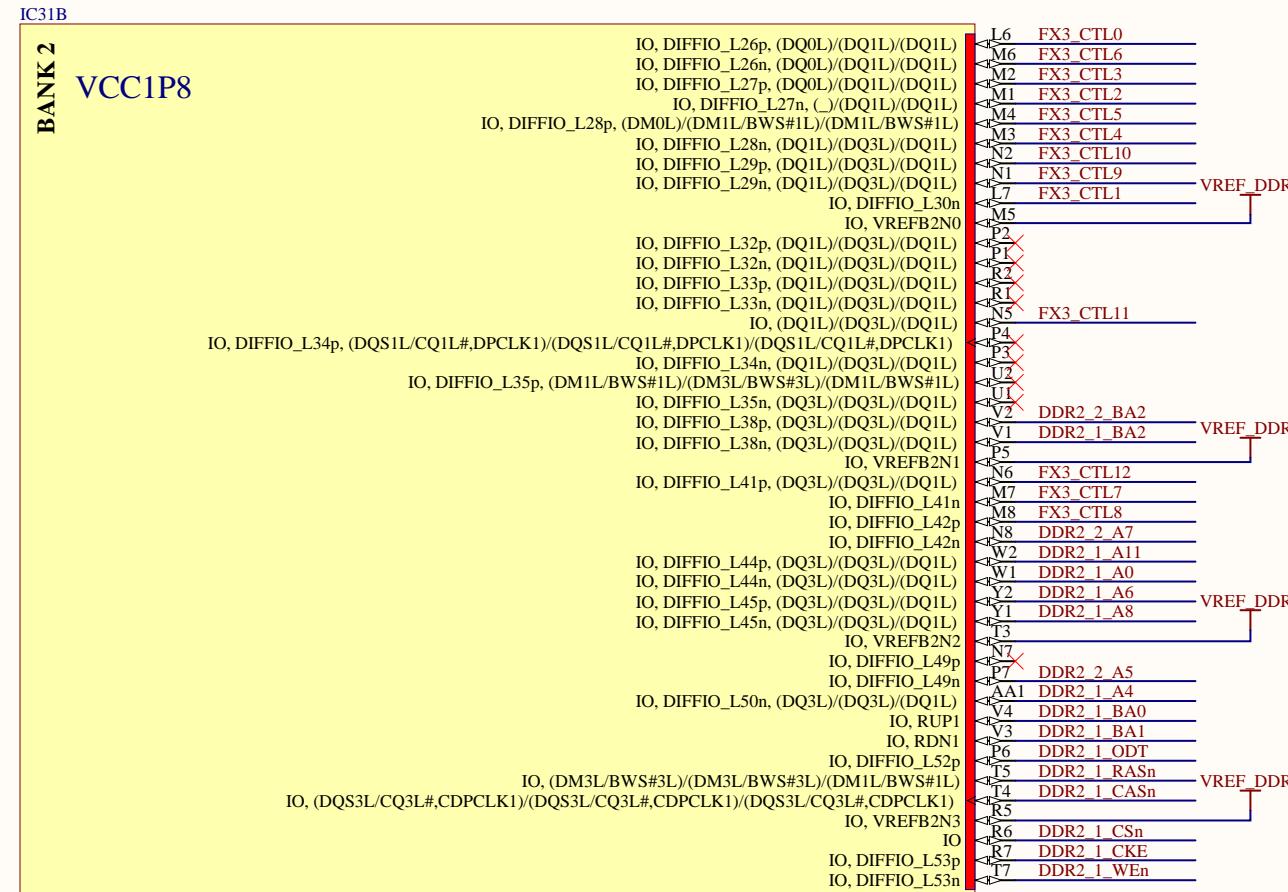
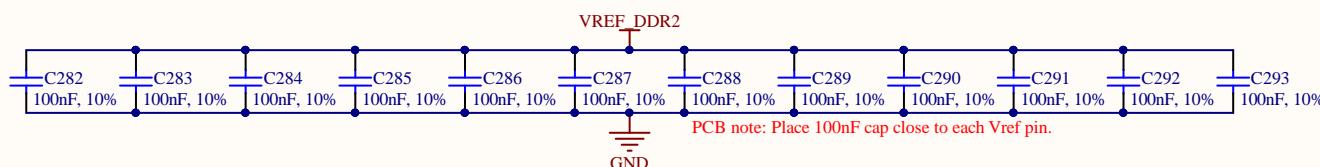
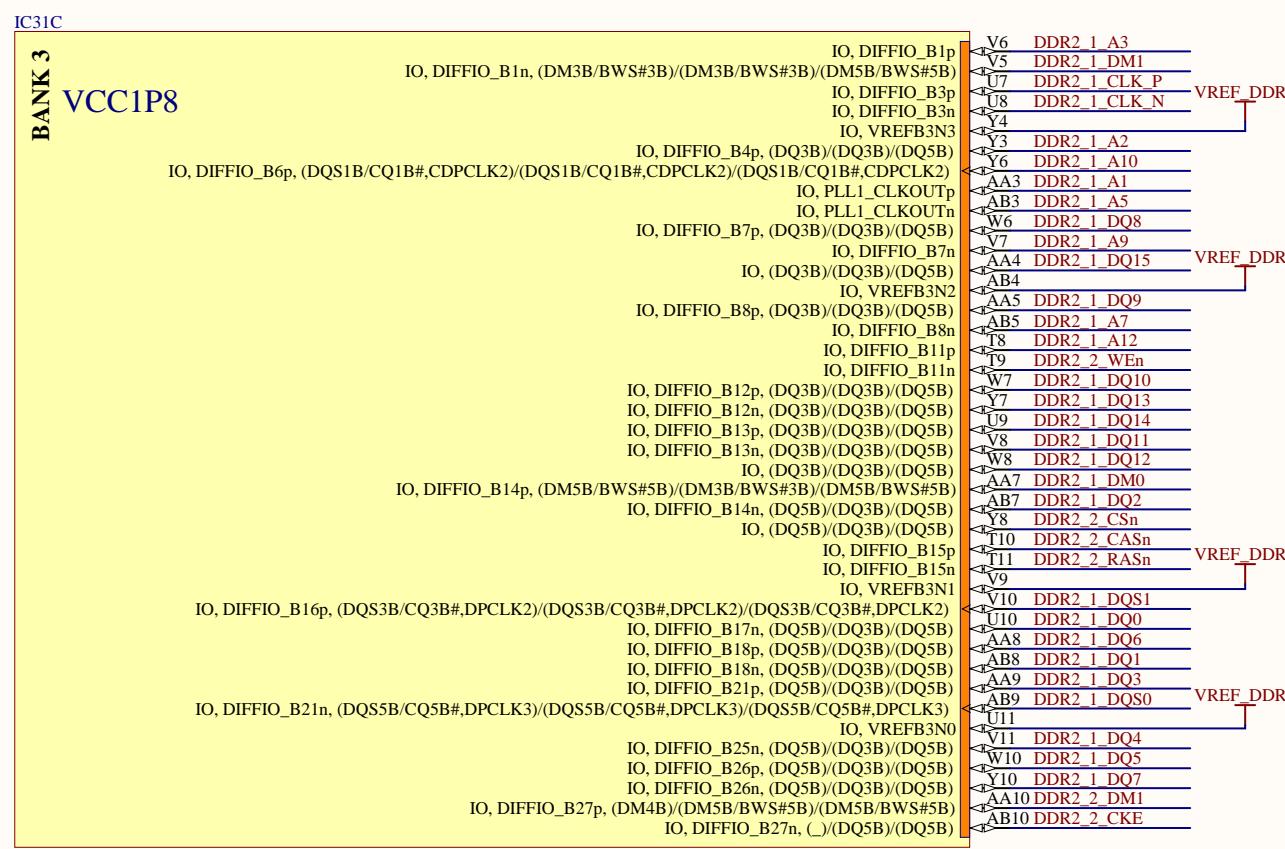
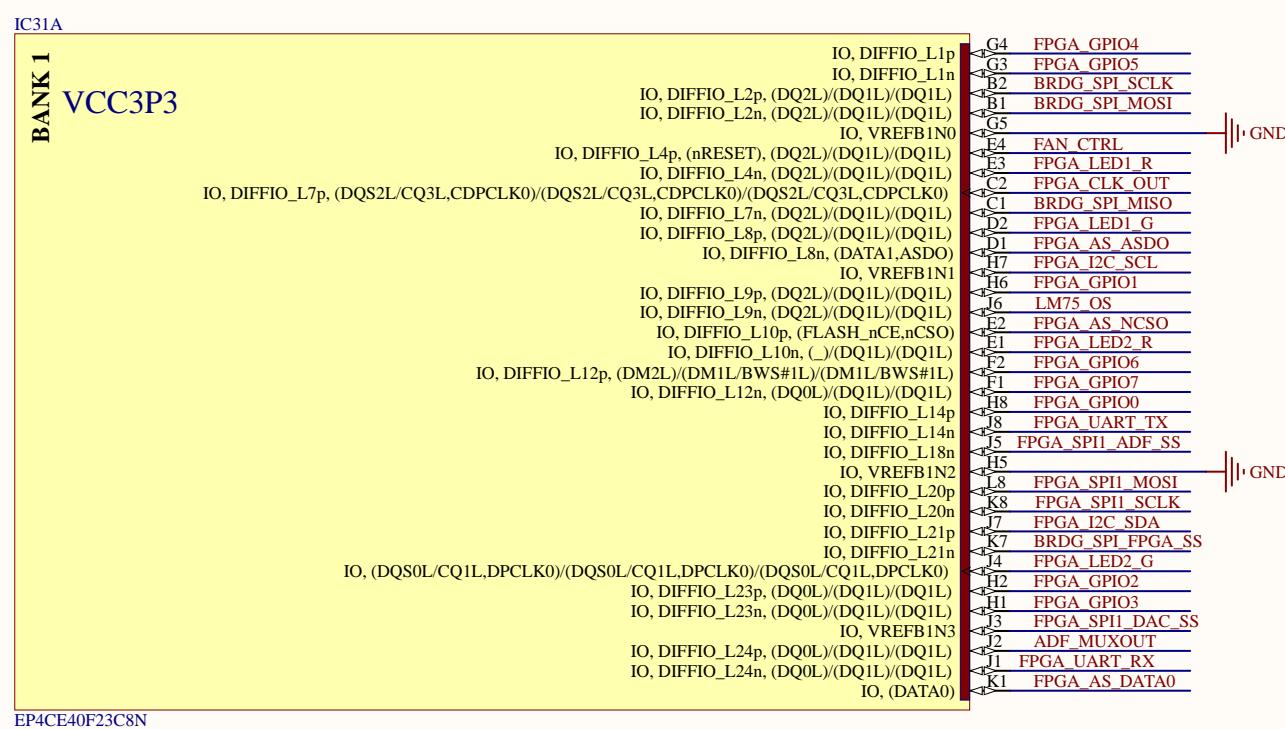
LMS7002M power supply circuit

NF elements on sheet: FR18, FR25
Number of NF elements on sheet: 2

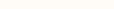


NF elements on sheet: -
Number of NF elements on sheet: 0

FPGA banks 1, 2, 3, 4

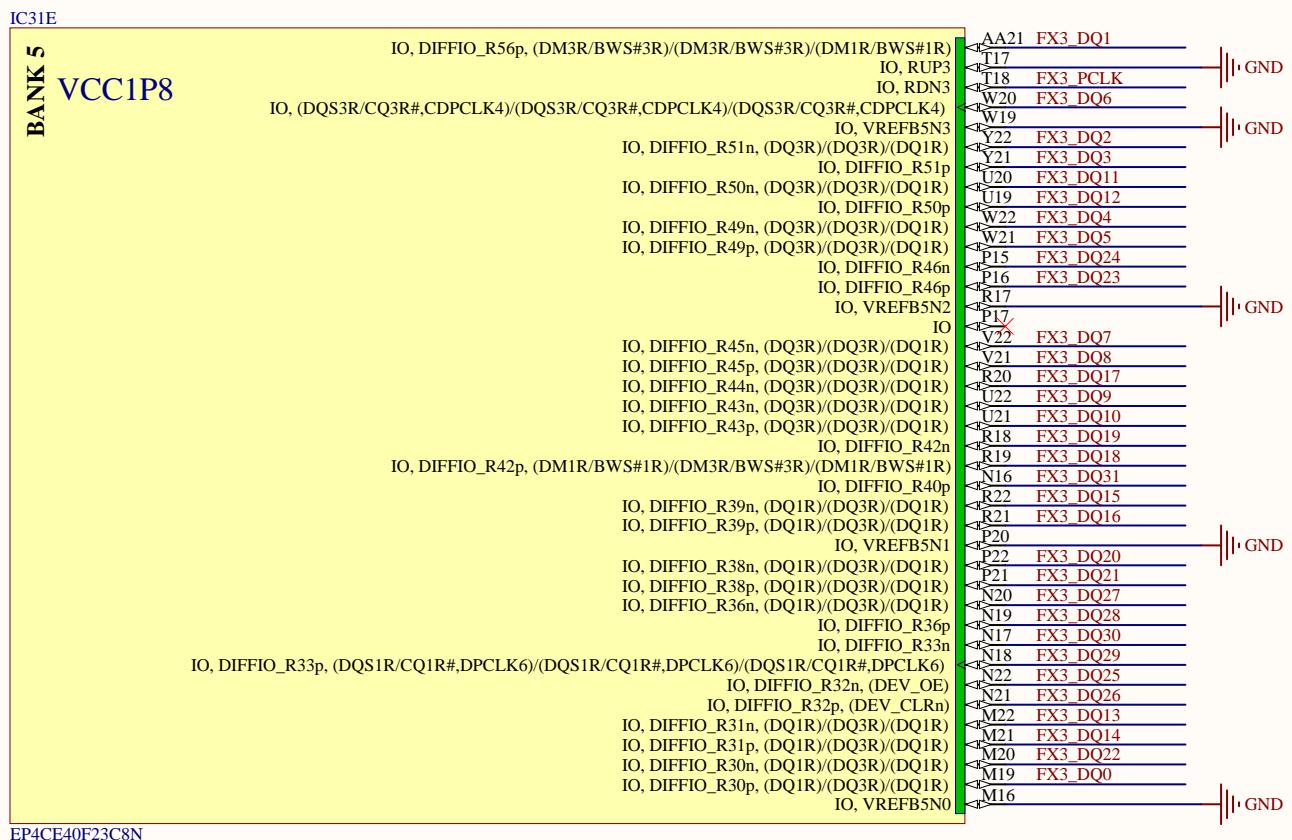


Project name: **LimeSDR_1v2.PrjPcb**
 Title: **FPGA banks 1, 2, 3, 4**
 Size: A3 Revision: v1.2
 Date: 2016-04-21 Time: 10:29:13 Sheet 7 of 14
 File: 07_FPGA_banks_1_2_3_4.SchDoc

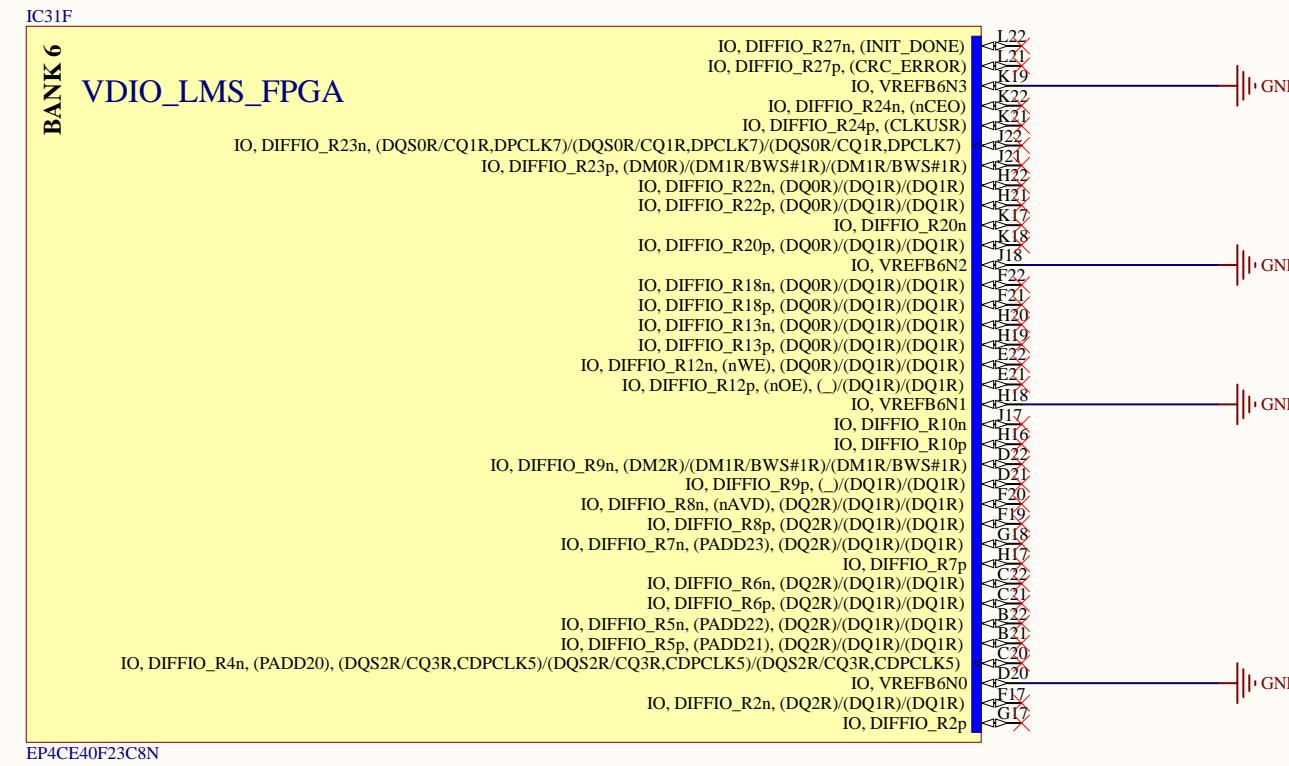
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 United Kingdom*


NF elements on sheet: -
Number of NF elements on sheet: 0

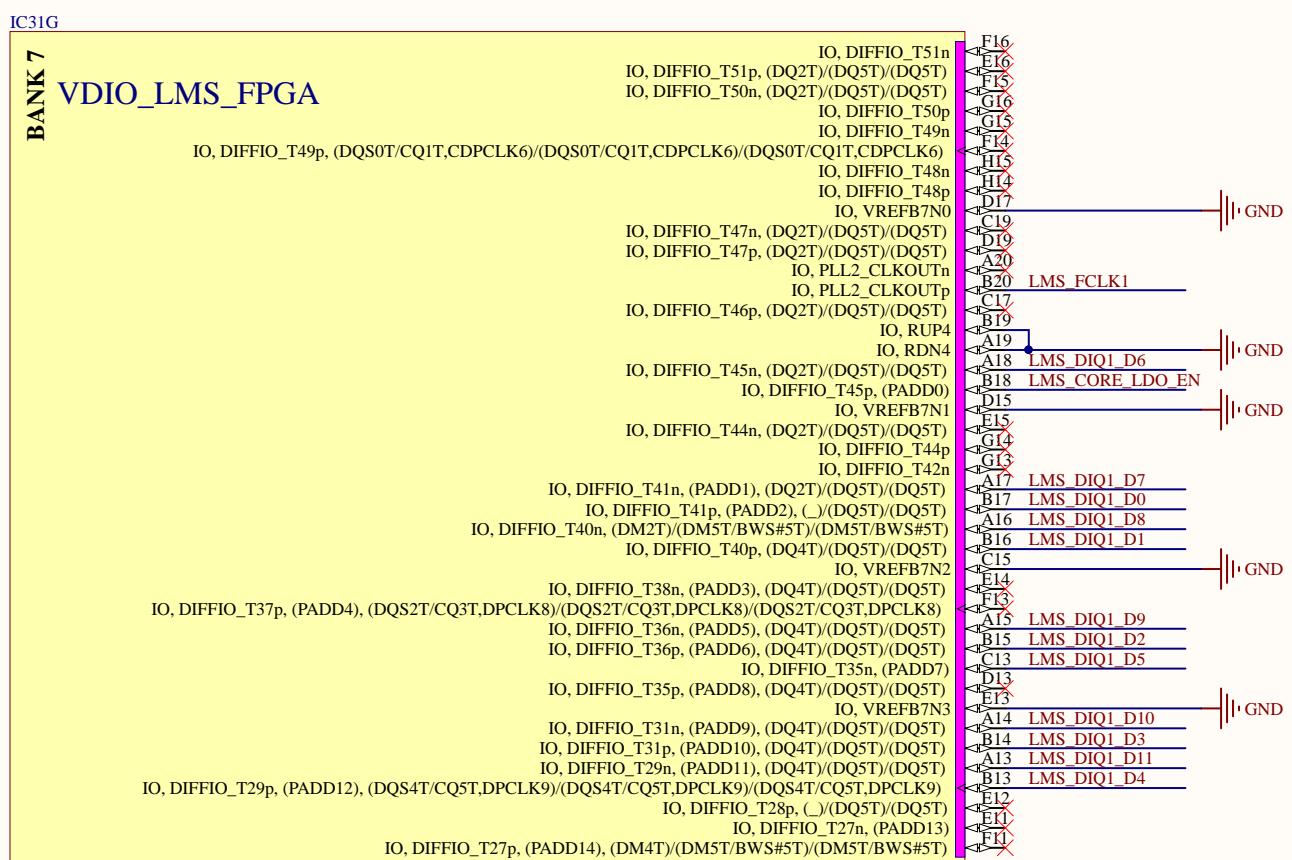
FPGA banks 5, 6, 7, 8



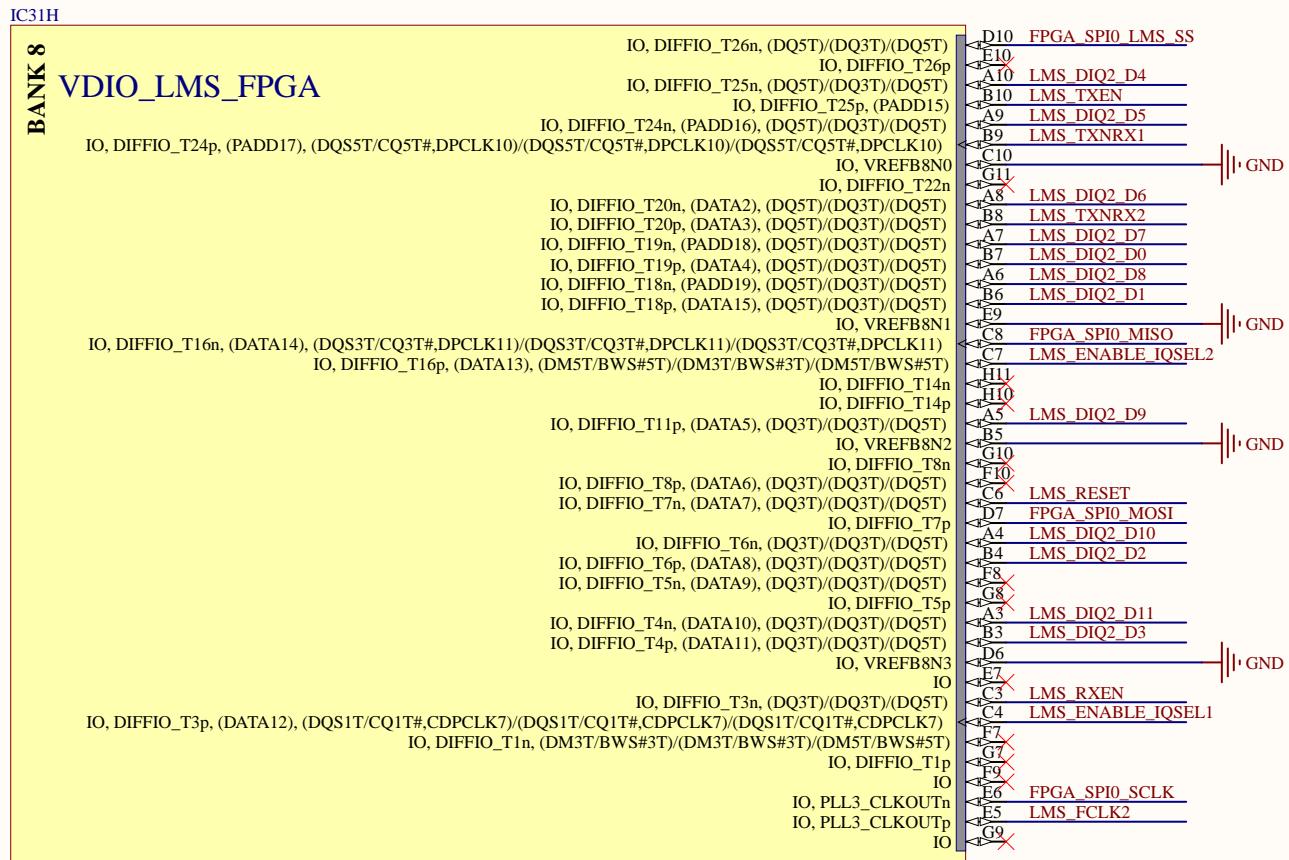
EP4CE40F23C8N



EP4CE40F23C8N



EP4CE40F23C8N



EP4CE40F23C8N

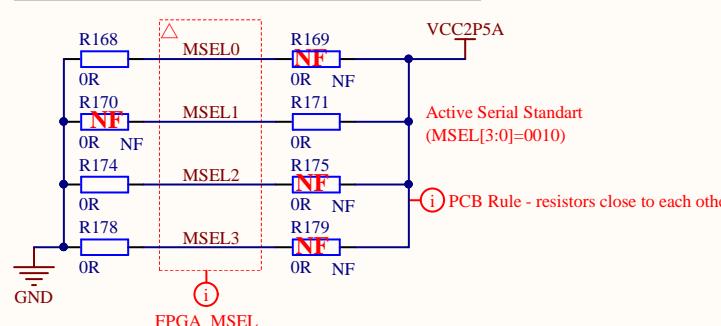
Project name: **LimeSDR_1v2.PrjPcb**

Title: FPGA banks 5, 6, 7, 8		<i>Lime Microsystems Surrey Tech Centre Guildford GU2 7YG Surrey United Kingdom</i>	 Lime microsystems
Size: A3	Revision: v1.2		
Date: 2016-04-21	Time: 10:29:16	Sheet 8 of 14	
File: 08_FPGA_banks_5_6_7_8.SchDoc			

NF elements on sheet: R169, R170, R173, R175, R179, R184, R185, J19, C321
Number of NF elements on sheet: 9

FPGA misc (power, clocks, config)

MSEL config



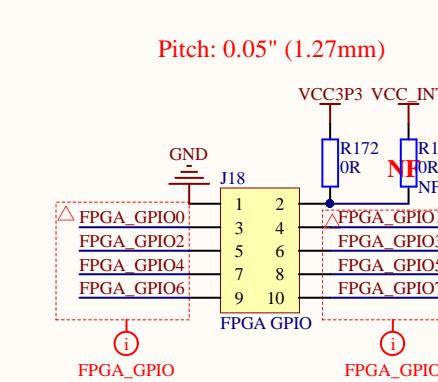
Pitch: 0.05" (1.27mm)

VCC2P5A

FPGA_JTAG

J17

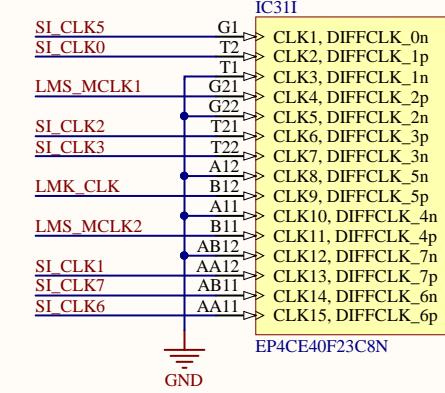
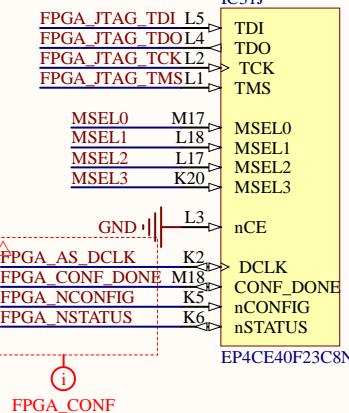
VCC2P5A



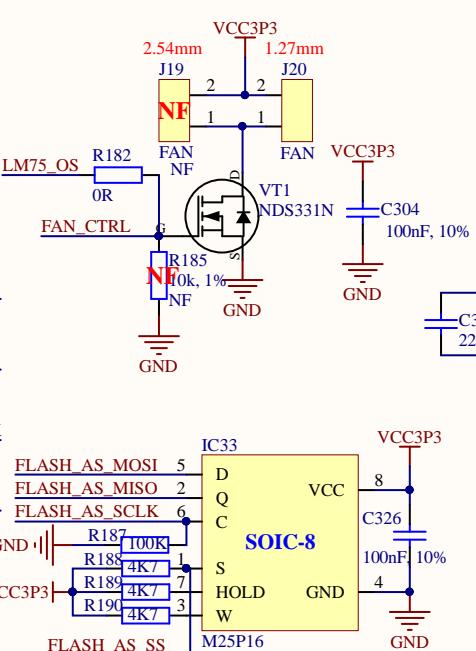
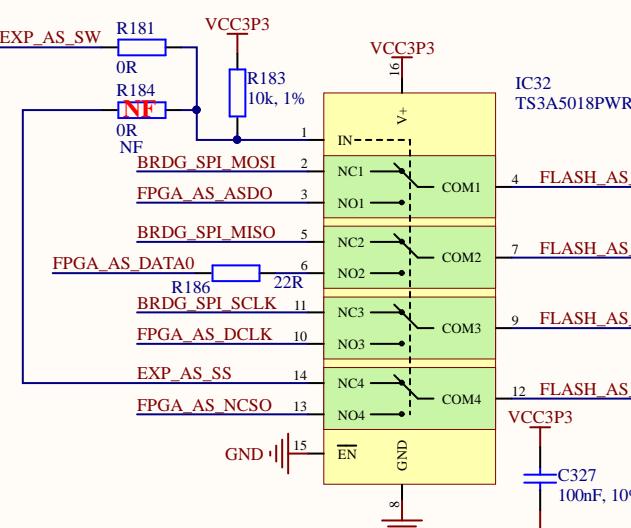
FPGA_GPIO

FPGA_GPIO

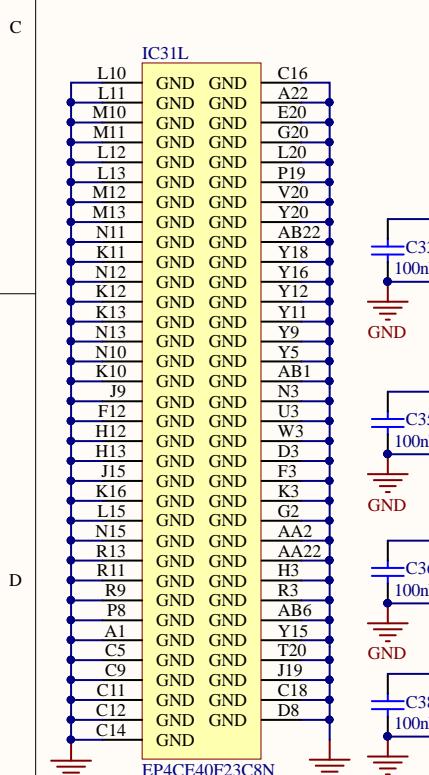
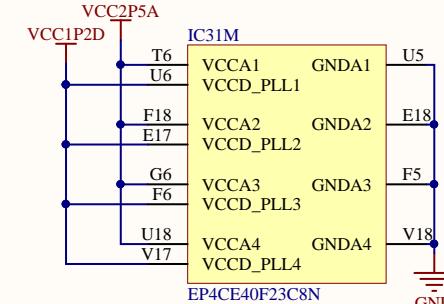
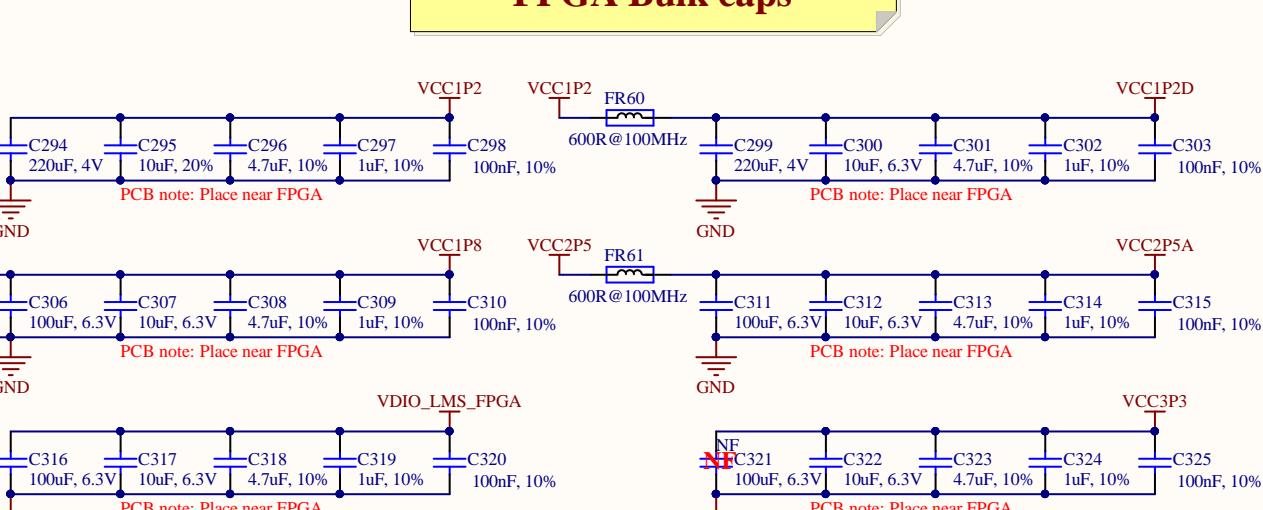
FPGA_GPIO



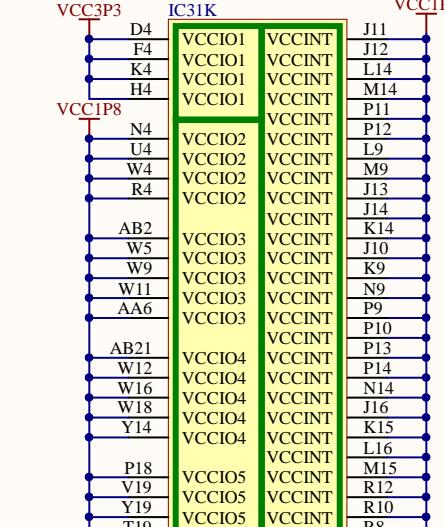
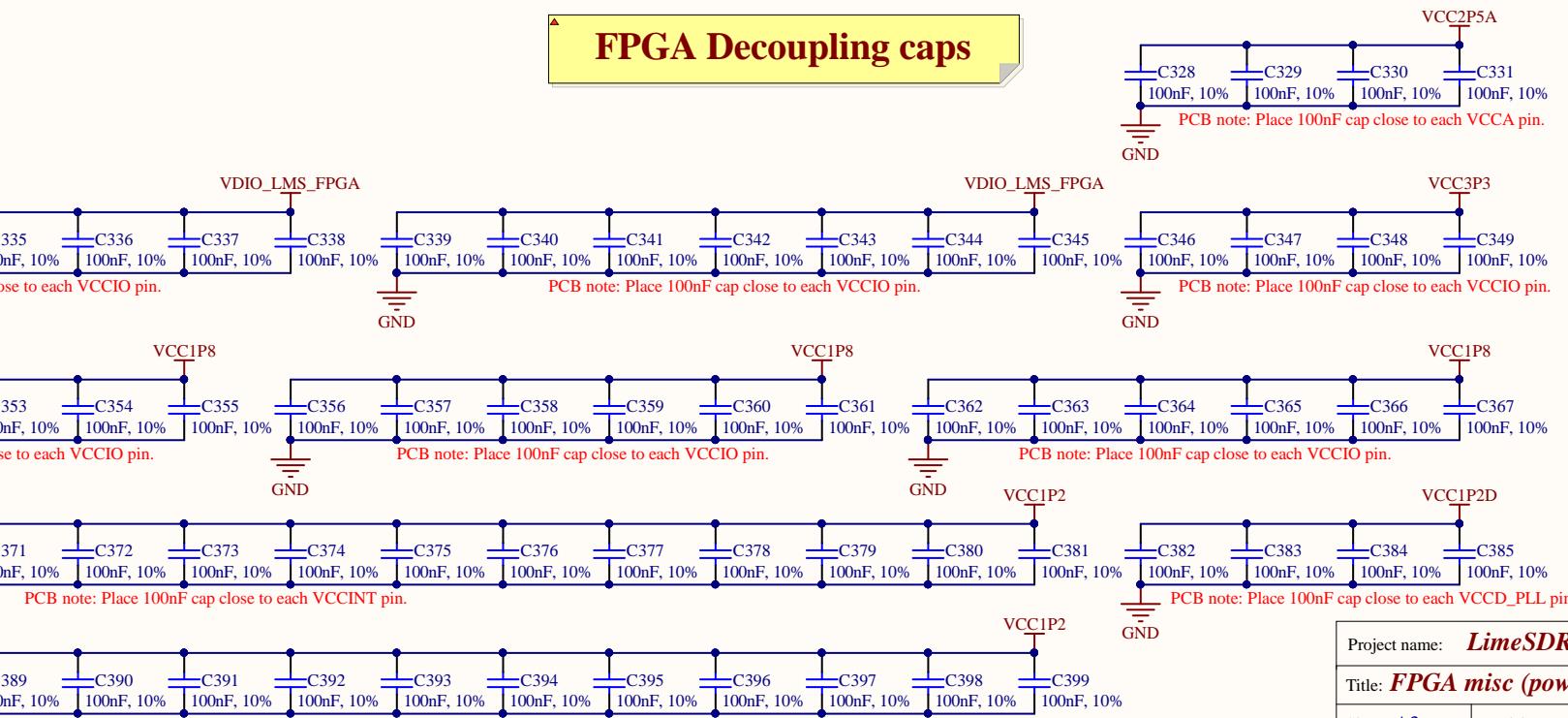
IN:
0: FLASH connected to FX3 (NC to COM)
1: FLASH connected to FPGA (NO to COM)



FPGA Bulk caps



FPGA Decoupling caps



Project name: LimeSDR_1v2.PjPcb

Title: FPGA misc (power, clocks, config)

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Size: A3 Revision: v1.2

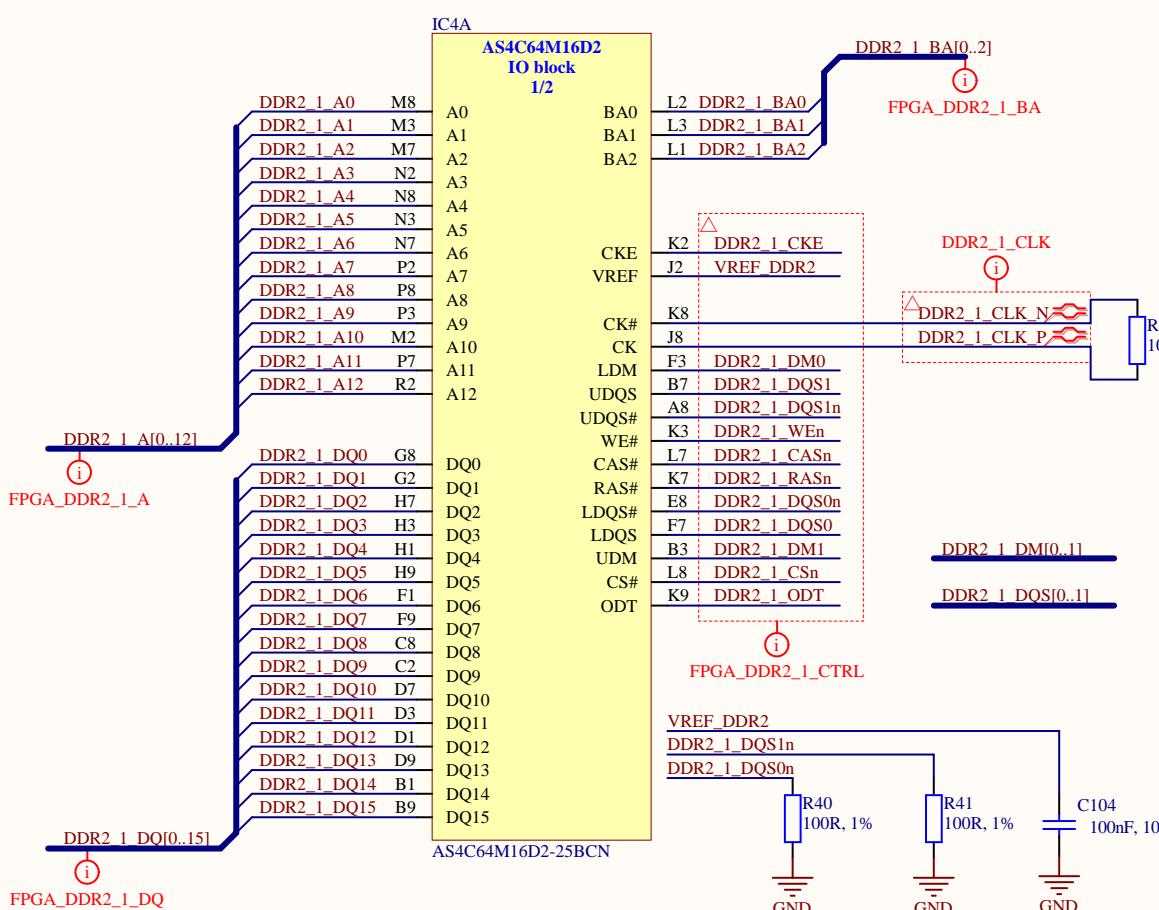
Date: 2016-04-21 Time: 10:29:20 Sheet 9 of 14

File: 09_FPGA_mis...SchDoc



NF elements on sheet: -
Number of NF elements on sheet: 0

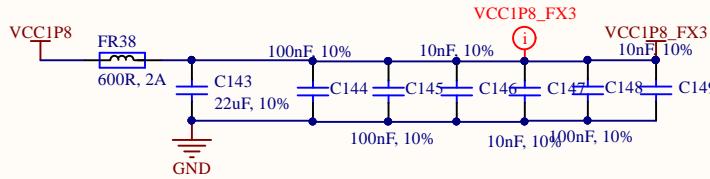
DDR2_1 (BOT L)



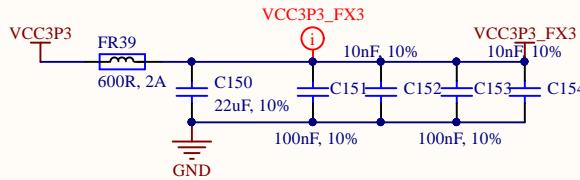
NF elements on sheet: FR40, FR41
Number of NF elements on sheet: 2

USB3 power block

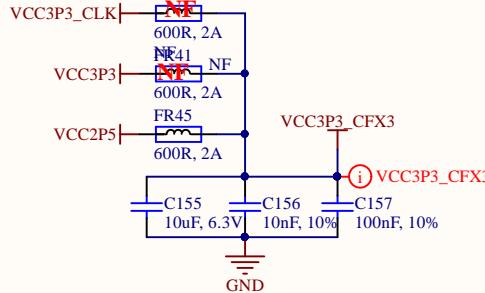
A



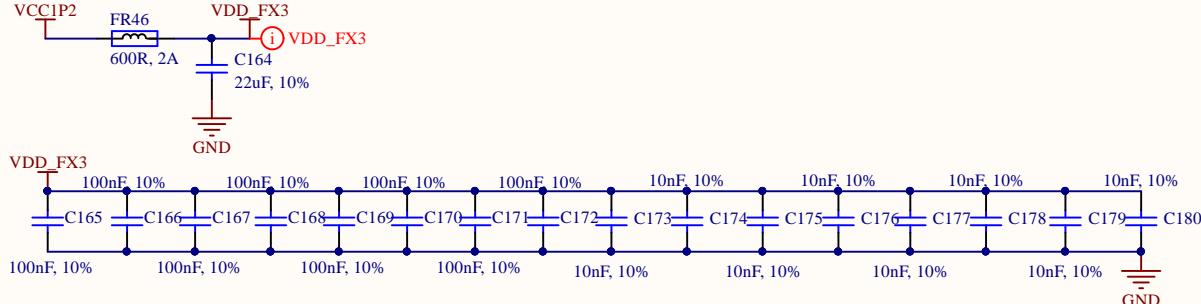
B



C



2



name: LimeSDR Jv2 PriPch

Title: *USB3.0 power*

Size: A4

Revision: v1.

Date: 2016-04-21 Time: 10:29:30 Sheet 12 of 14

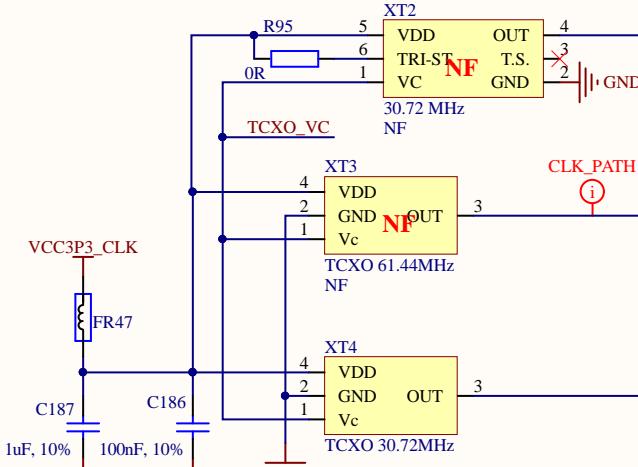
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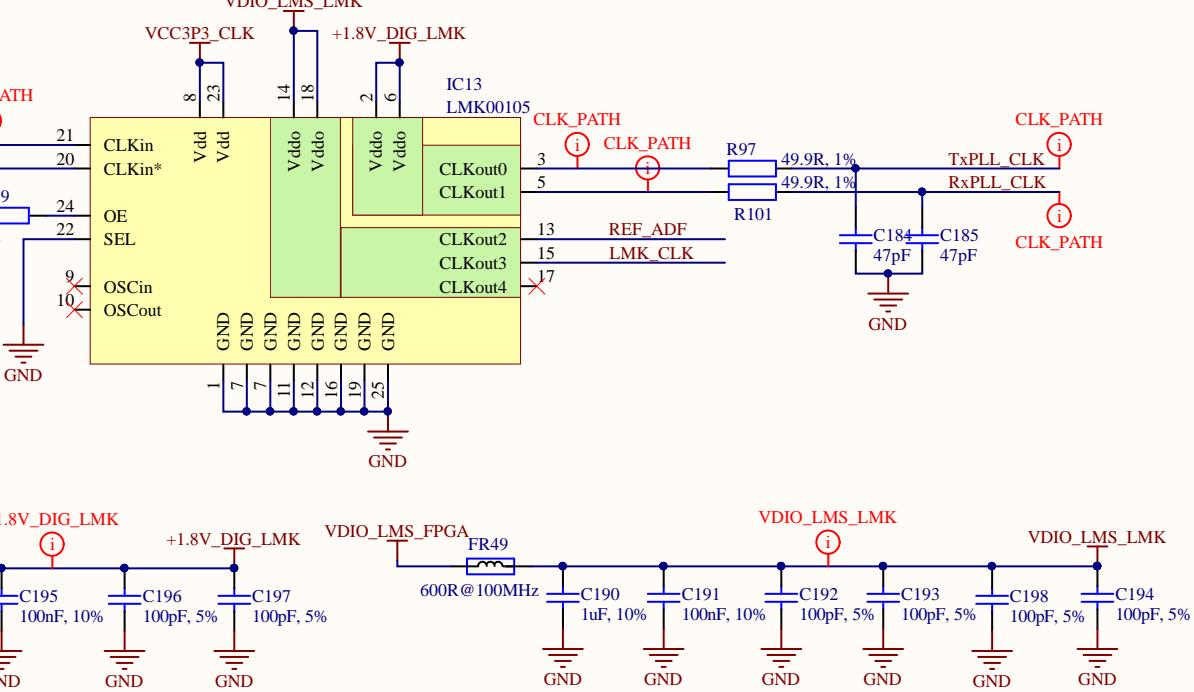
NF elements on sheet: XT2, XT3, R100, R102, R103, R104, R105, R106, R107, C199
Number of NF elements on sheet: 10

Clock circuits

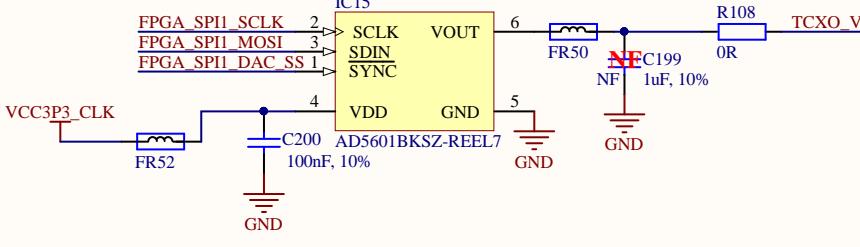
(VC)TCXO



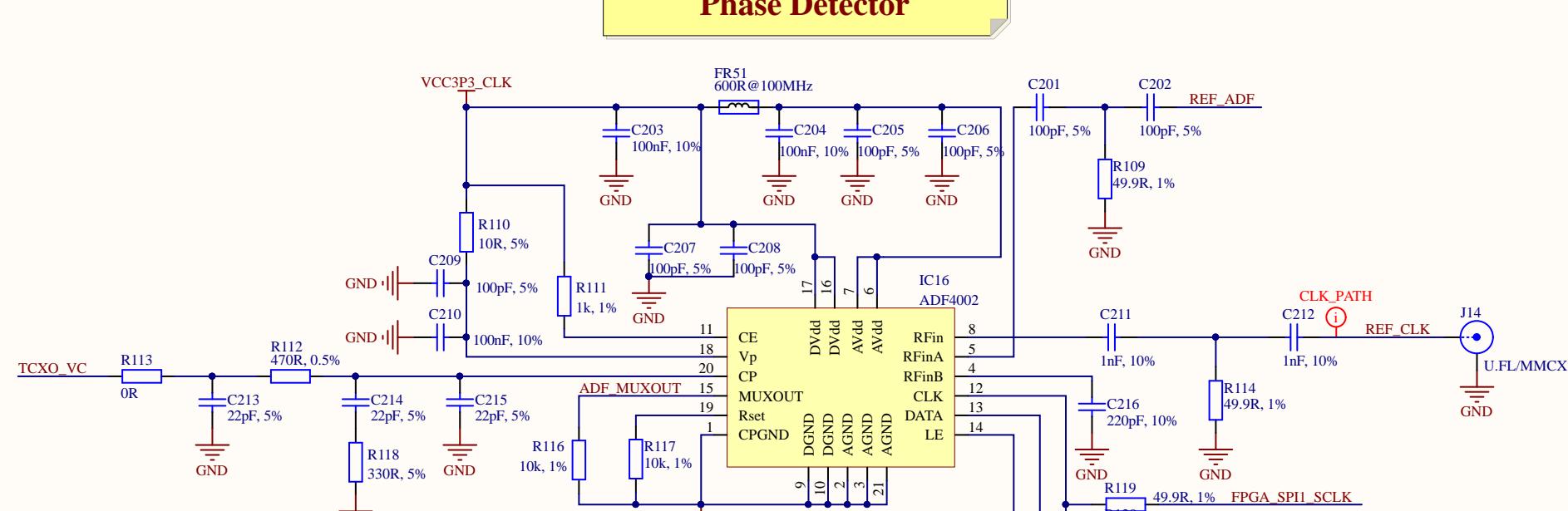
Clock buffer



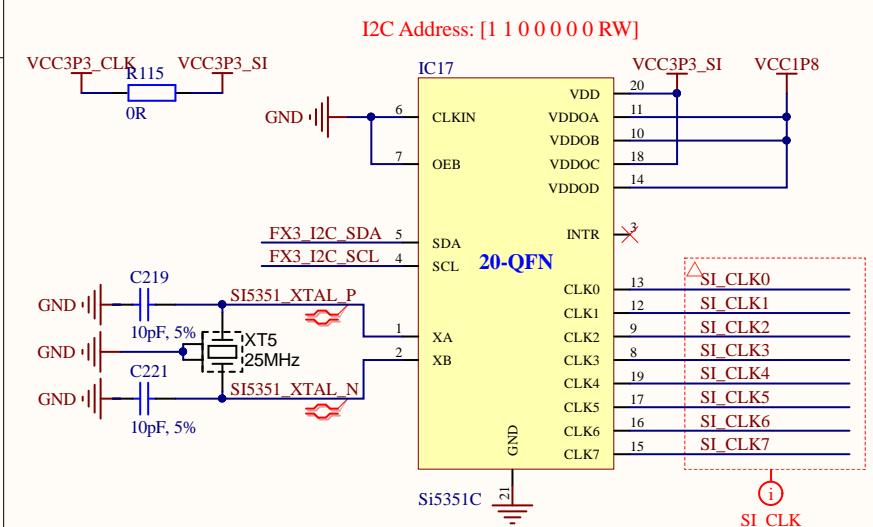
DAC



Phase Detector



Clock generator



Project name: LimeSDR_Iv2.PjPcb

Title: Clocks

Size: A3

Revision: v1.2

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Date: 2016-04-21 Time: 10:29:33

Sheet 13 of 14

File: 13_Clocks.SchDoc

1

2

3

4

5

6

7

8

NF elements on sheet: R122, R124, R125, R165, J16, LED2, LED3, LED6, LED7, LEDS1, LEDS2

Number of NF elements on sheet: 11

Total number of NF elements on all sheets: 46

Board power circuits

