Cache Replacement Policy

- On a cache miss, how do we choose which entry to replace?
 - Assuming the new entry is more likely to be used in the near future
 - In direct mapped caches, not an issue!
- Policy goal: reduce cache misses
 - Improve expected case performance
 - Also: reduce likelihood of very poor performance

MIN, LRU, LFU

· MIN

- Replace the cache entry that will not be used for the longest time into the future
- Optimality proof based on exchange: if evict an entry used sooner, that will trigger an earlier cache miss
- Least Recently Used (LRU)
 - Replace the cache entry that has not been used for the longest time in the past
 - Approximation of MIN
- Least Frequently Used (LFU)
 - Replace the cache entry used the least often (in the recent past)

LRU/MIN for Sequential Scan

							LRU								
Reference	·A	В	С	D	E	A	В	C	D	E	Α	В	С	D	E
1	A				E				D	, , , , , , , , , , , , , , , , , , ,			С		
2		В				A				E	- ,			D	
3			C				В				Α				E
4				D				C				В			
							MIN		*						
1	Α					+					+			+	
2		В					+					+	C		
3			C					+	D					+	
4				D	E					+					+

							LRU								
Reference	A	В	A	C	В	D	A	D	E	D	A	E	В	A	C
1	A		+			-	+				+			+	
2		В			+								+		
3				C					E			+			
4						D		+		+					C
							FIFO								
1 .	A		+				+		E						
2		В			+						A			+	
3				C								+	В		
4						D		+		+			,		C
							MIN								
1	A		+				+				+			+	
2		В			+								+		C
3				C					E			+			
4						D		+		+					

Belady's Anomaly

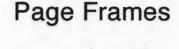
FIFO (3 slots)												
Reference	A	В	С	D	Α	В	E	A	В	C	D	E
1	Α			D			E					+
2		В			A			+		C		
3			C			В			+		D	
				FI	FO (4	slot	3)					
1	Α				+		E				D	
2		В				+		Α				E
3			C						В			
4				D						C		

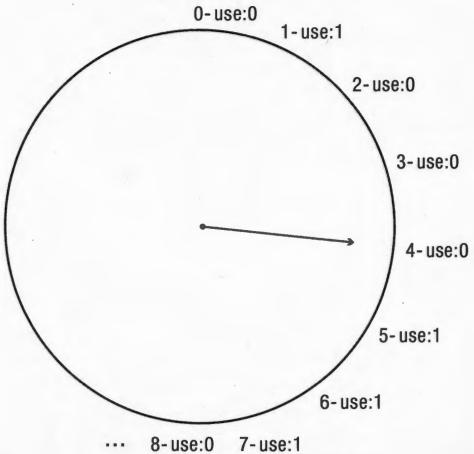
Question

- How accurately do we need to track the least recently/least frequently used page?
 - If miss cost is low, any approximation will do
 - Hardware caches
 - If miss cost is high but number of pages is large, any not recently used page will do
 - Main memory paging with small pages
 - If miss cost is high and number of pages is small, need to be precise
 - Main memory paging with superpages

Clock Algorithm: Estimating LRU

- Hardware sets use bit
- Periodically, OS sweeps through all pages
- If page is unused, reclaim
- If page is used, mark as unused





Recell: page frames in physical memory use bits in page table (virtually indexed)

core map: 1.3+ of virtual pages for each page free

Nth Chance: Not Recently Used

- Instead of one bit per page, keep an integer
 notInUseSince: number of sweeps since last use
- Periodically sweep through all page frames if (page is used) {

```
if (page is used) {
    notInUseForXSweeps = 0;
} else if (notInUseForXSweeps < N) {
    notInUseForXSweeps++;
} else {
    reclaim page; write modifications if needed
}</pre>
```

Implementation Note

- Clock and Nth Chance can run synchronously
 - In page fault handler, run algorithm to find next page to evict
 - Might require writing changes back to disk first
- Or asynchronously
 - Create a thread to maintain a pool of recently unused, clean pages
 - Find recently unused dirty pages, write mods back to disk
 - Find recently unused clean pages, mark as invalid and move to pool
 - On page fault, check if requested page is in pool!
 - If not, evict page from the pool

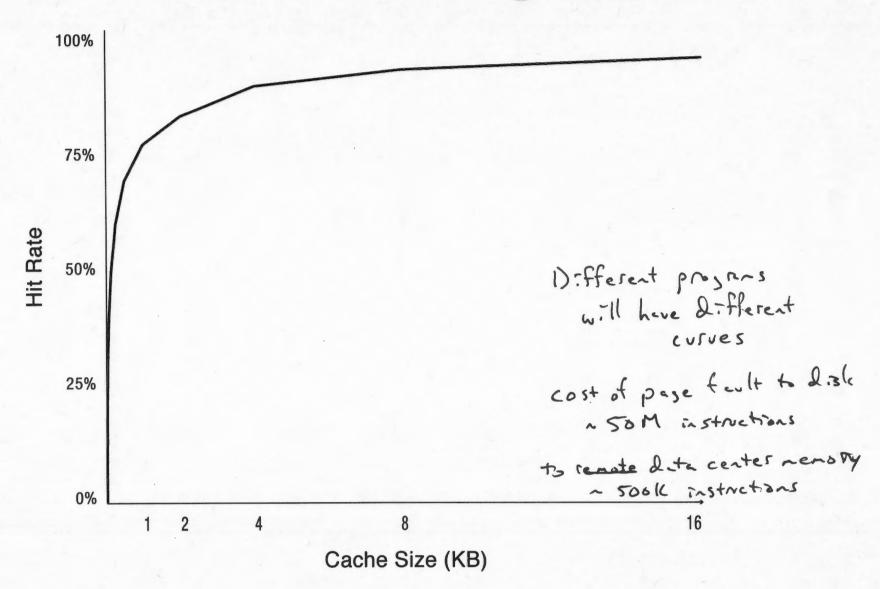
Recap

- MIN is optimal
 - replace the page or cache entry that will be used farthest into the future
- LRU is an approximation of MIN
 - For programs that exhibit spatial and temporal locality
- Clock/Nth Chance is an approximation of LRU
 - Bin pages into sets of "not recently used"

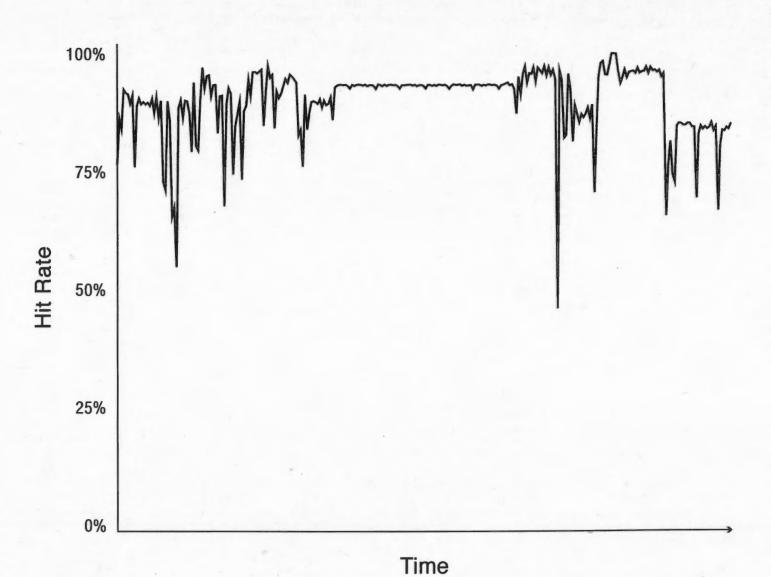
Working Set Model

- Working Set: set of memory locations that need to be cached for reasonable cache hit rate
- Thrashing: when system has too small a cache

Cache Working Set



Phase Change Behavior



Question

- What happens to system performance as we increase the number of processes?
 - If the sum of the working sets > physical memory?

