## **CPU** \_mem\_byte\_enable= —256'b mem\_rdata256 bus\_adapter L1 256'b mem\_wdata256 **CACHE** 32'b mem\_byte\_enable256 L1 control (duplicate) L1 control **DESCRIPTION** word aligned/ 3 bits for word in line/ 3 ovalid1\_read 1'b valid2\_read 1'b dirty1\_read 1'b dirty2\_read 1'b lru\_read 1'b tag\_ld1 mem\_address 3'b index 1'b valid1\_load 1'b dirty1\_load 1'b dirty2\_load 1'b lru\_load index bits/ 24 tag 1'b tag\_ld2 3'b index 1'b datast\_rd 8 sets with 2 ways 1'b tag\_read 1'b dirty1\_data 3'b index 1'b way 2'b data\_bus\_mux\_sel Each way holds an 8-word cache line 1'b dirty2\_data \_\_256'b line\_o\_ Write-back with a TAG STORE write allocate policy LRU replacement tag\_array1.sv (tag tag\_array2.sv (tag data\_array1.sv data\_array2.sv Read/Write hits (data store) (data store) 26'b 26'b must take exactly two clock cycles to complete DATA STORE Set/index bits must come from the address bits cache/data line directly adjacent to mux 256'b the offset bits (I chose to use the format tag/index/word) ABOUT SIGNALS/ LEGEND L1 - write\_en (32 bits each for a byte of each way) DATAPATH -internal signals are black -output wires are the same color as the origin -The thick lines from the metadata stores combine multiple signals - anything wtthout a bit marker (i.e X'b ) can be \_156'b line\_o---1'b .L1\_mem\_read(mem\_read) assumed to be ${f 1}$ memory arrays 1'b resp\_i bus\_adapter\_mu 1b .L1\_mem\_write(mem\_write) - tag\_array is of 26 of 1'b write\_i array.sv instances 1'b read\_i - then you need 5 instances of array.sv for the metadata 32'b mem\_address —⊉56' .L1\_evicted\_cacheline(line\_i) cacheline\_adapter mem\_line Mux \_\_1'b resp\_o\_ victimcache \_256'b .datain\_from\_mem(line\_o) **Main Memory** pmem\_resp 64'b 1'b 256'b .datain\_from\_vc(vc\_swap\_rdata)

## SAMUEL CHEUNG