High Speed Digital Receivers for Electronic Warfare Applications

Mike Groden, Lamberto Raffaelli

LNX Corporation, Salem, NH, USA

ABSTRACT

This paper describes the design, fabrication and test results of a dual channel high speed data acquisition and real-time Digital Signal Processing module. The board incorporates two Atmel TS83102, 2 Gsa/sec, 10-bit analog to digital converters and up to three Virtex-II Field Programmable Gate Arrays (FPGAs); the board also has two high-speed serial (Hotlink) interfaces and a VME64 interface. Typical applications include Electronic Warfare, radar, and software defined radios.

Introduction

Digital Receivers are rapidly replacing traditional analog receivers such as heterodyne receivers, interferometers, filter-bank receivers and others for military applications such as Electronic Warfare and Radars. In addition, their ability to be software driven enables the operator to change key parameters such as carrier frequency or modulation in real time. This feature makes digital receivers ideal for applications such as secure communications and software defined radio.

Design Concept

Critical military applications including Electronic Warfare and Electronic Intelligence require continuously searching for electronic signals over a wide range of frequencies. SETI, the project to search for signals from outer space, requires similar searching, on a grander scale. This paper describes a novel approach to optimizing the architectures of FPGA-based channelized receivers used for these types of applications.

In the past, signal search problems have been solved using a bank of RF filters to reduce the sampling and processing requirements, or by constructing specialized multi-processor systems. These are typically constructed using arrays of Digital Signal Processors. Using multiple RF filters requires the output of each filter bank to be down converted to baseband for subsequent processing. This results in a bulky solution. DSP processing arrays can be large, and transferring large amounts of data between devices presents its own challenges.

Today's very high speed A/D converters can perform sampling at rates in excess of 2 Gsa/sec. Field Programmable Gate Arrays (FPGAs) have likewise grown in capacity and speed. FPGAs are now available with large amounts of memory and features like multipliers and MACs. These embedded features enable these devices, with sufficient RTL coding, to implement the FFTs and other elements needed to construct a high performance channelized receiver.

Figure 1.LNX 's Digital Products, Including Single and Dual Channel Digital Receivers.

Item Description

A/D

The board incorporates two TS83102 A/Ds from Atmel. This device has a maximum sample rate of 2 Gsa/sec at 10-bits with a 3 GHz full power input bandwidth. Spurious free dynamic range is 58 dBc (7.4 effective bits at F_S = 1.4 Gsa/sec, f_{IN} = 700 MHz). A companion device, the TS81102 demultiplexes the high speed, 10-bit ECL A/D outputs onto an 80-bit, single-ended bus running at 1/8 of the sample rate. The A/D's sampling delay and gain can be adjusted to support synchronizing and interleaving multiple A/D boards. The output of the demultiplexer is connected to a Virtex-II FPGA using an 80-bit single-ended data bus and a differential clock.

FPGAs

There are sites for three Virtex-II FPGAs; each site can support devices ranging from 2 to 8 million gates. The FPGAs are also used to implement the Hotlink and VME interfaces. Two devices also have a CPU bus for direct communication with an on-board CPU.

CPU

An on-board CPU module is used to provide a user interface, local control, and FPGA configuration. This module also provides an RS232 interface. There are 32 megabytes of Flash memory that can be used to store FPGA configuration data. A simple command set is used to configure and control data collection and processing.

Hotlink Interface

High speed serial links are implemented using the CYP15G0101DXA HOTLink II™ Transceiver from Cypress Semiconductor. It contains all of the logic to support the serialize/de-serialize (SERDES) function and clock recovery and supports data rates from 200-1500 Mbaud.

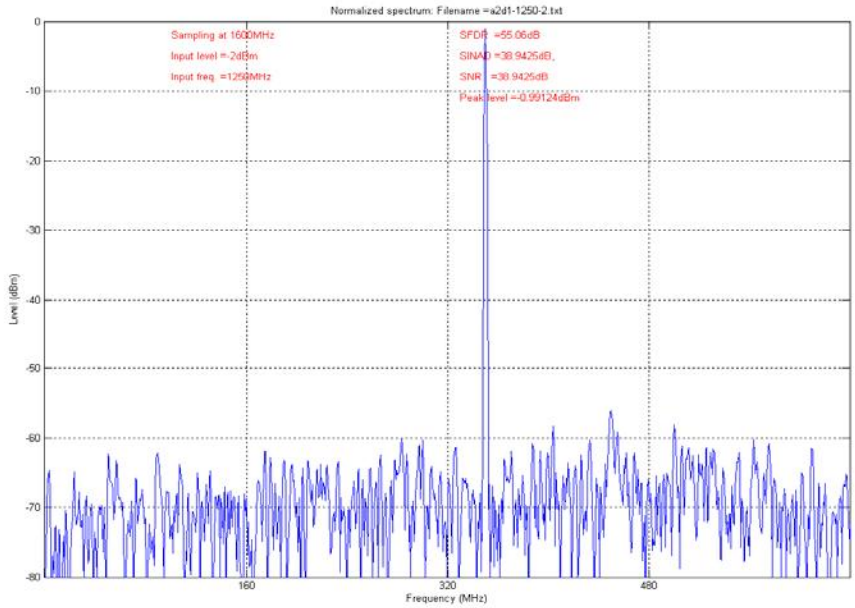

Figure 2 Direct downconversion of 1250 MHz signal, sampled at 1600 Gsa/sec. Spurious free dynamic range exceeds 55 dB.

VME Interface

The VMEbus interface is designed to conform to the VME64x specification and requires the 160 pin connectors with the added ground pins and +3.3 volt power pins. The interface was designed to support A32/D32 slave data transfer.

Power

Power can be supplied through a 10-pin terminal block for bench top operation or the VME backplane. The special power supply voltages, that are not part of the VME specification, are supplied through user defined pins. Typical power consumption is 60W.

Conclusion

We have developed a very high speed data acquisition and real-time DSP processing platform. With the tools and capabilities we have in house, we can easily tailor the design, using lower cost design techniques, as necessary to implement new requirements.