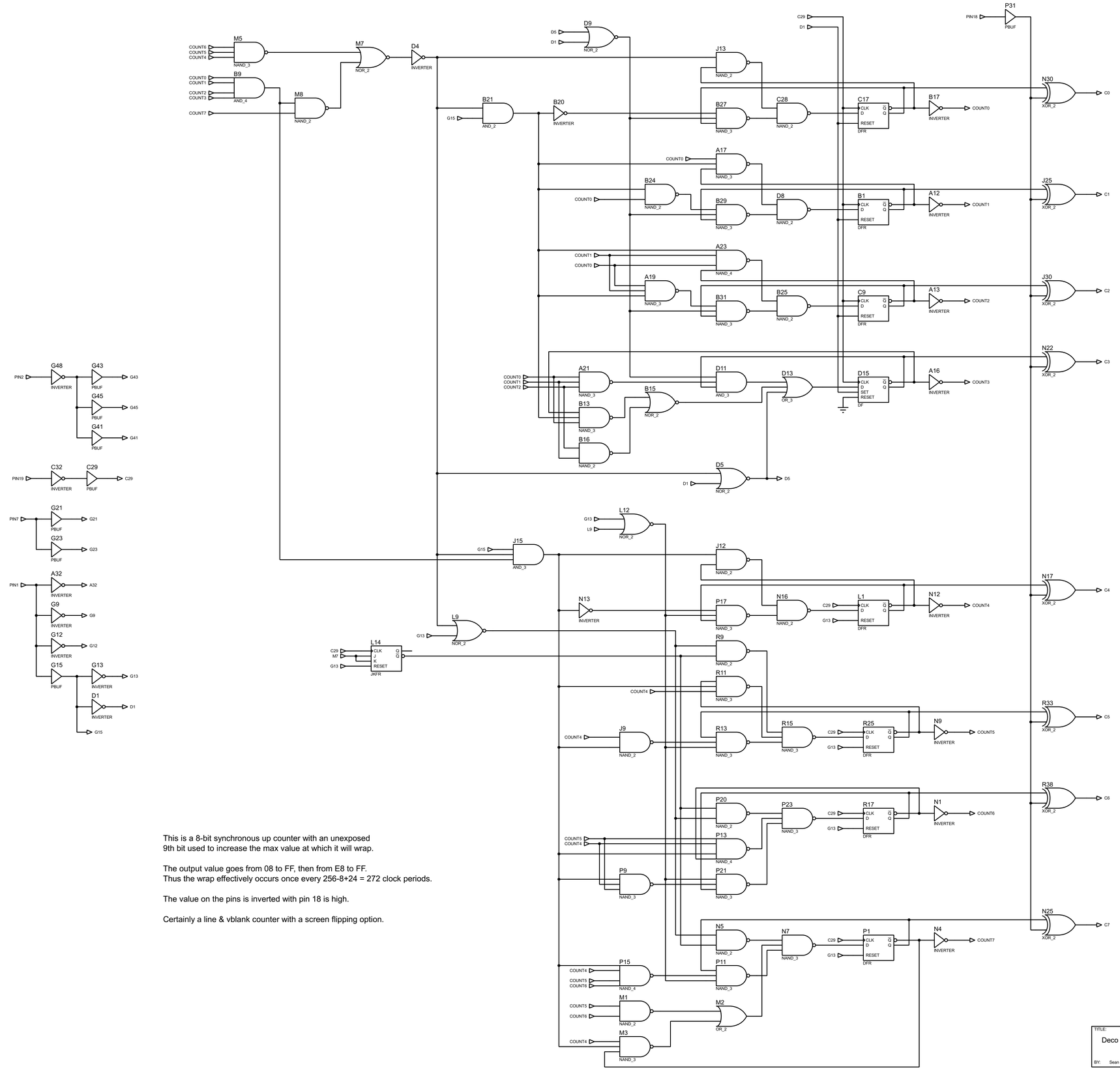

This is a 8-bit synchronous up counter with an unexposed
9th bit used to increase the max value at which it will wrap.

The output value goes from 08 to FF, then from E8 to FF.
Thus the wrap effectively occurs once every 256-8+24 = 272 clock periods.

The value on the pins is inverted with pin 18 is high.

Certainly a line & vblank counter with a screen flipping option.

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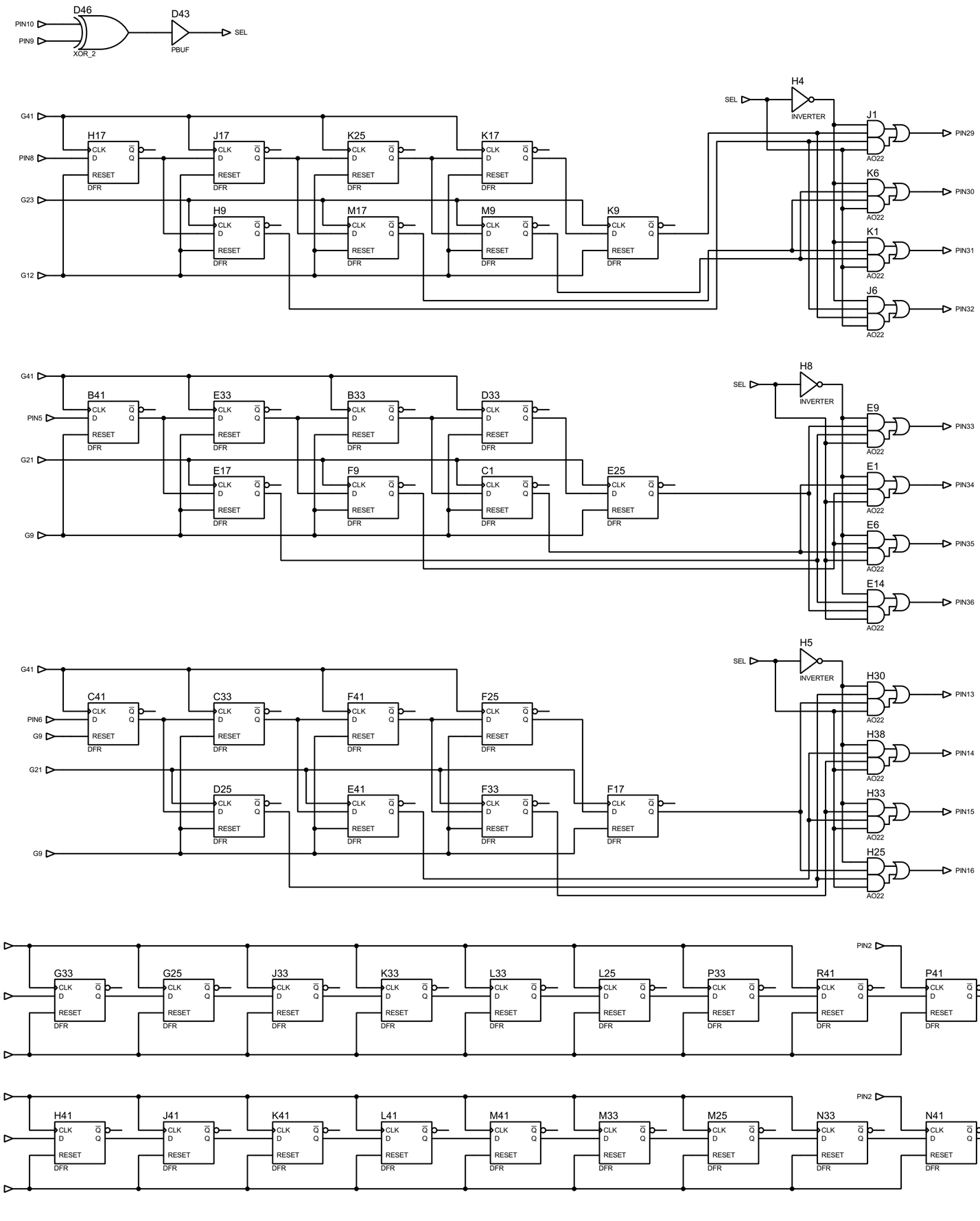

Three 4-bit shift registers, with separate registers to "catch" their output. The value is then output normally or backwards depending on pin 9 and 10.

Possibly graphics SIPO with flipping.

Two 8-bit delay lines with a final register.

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