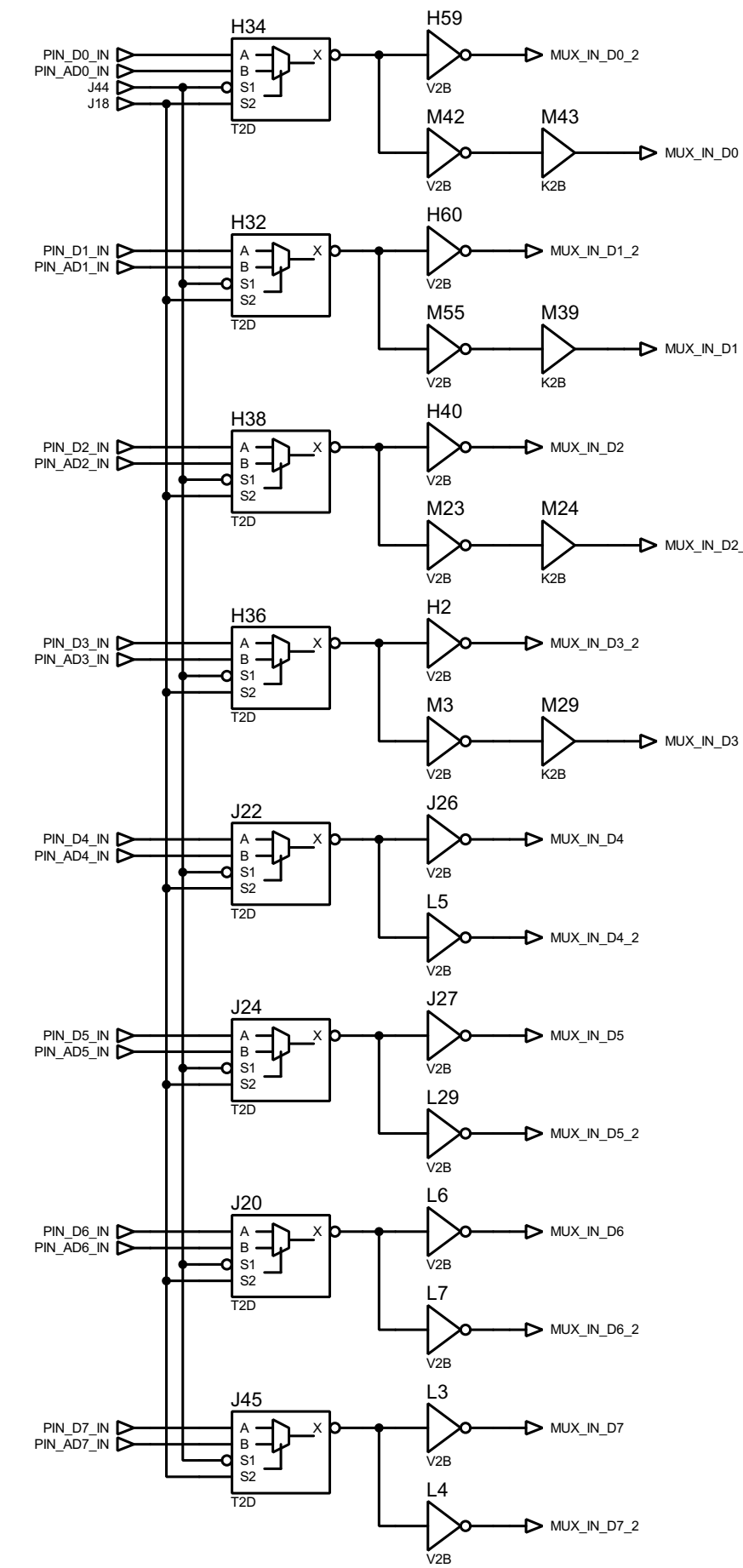
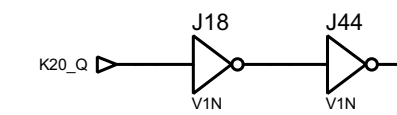
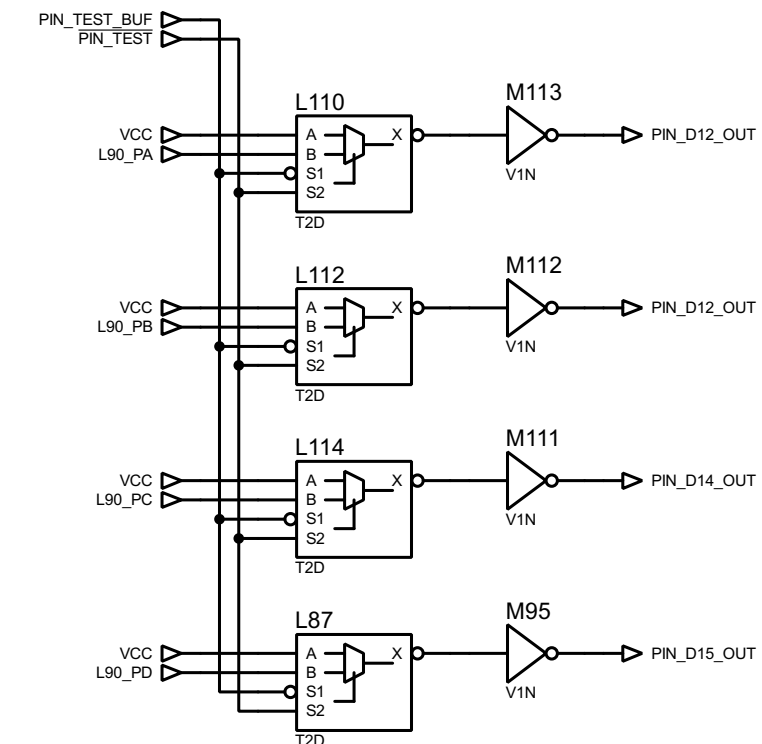
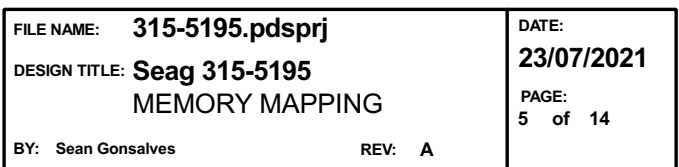
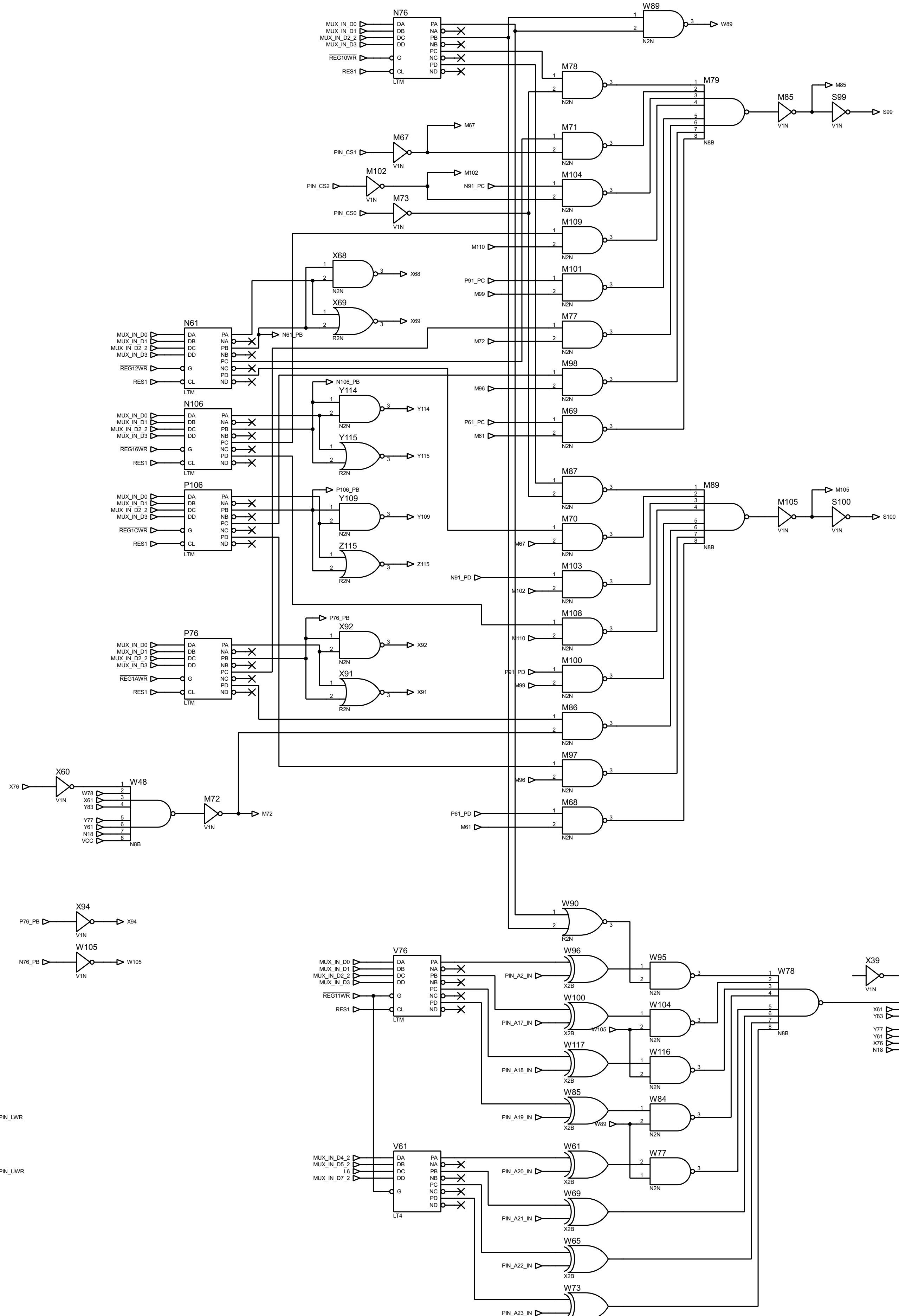
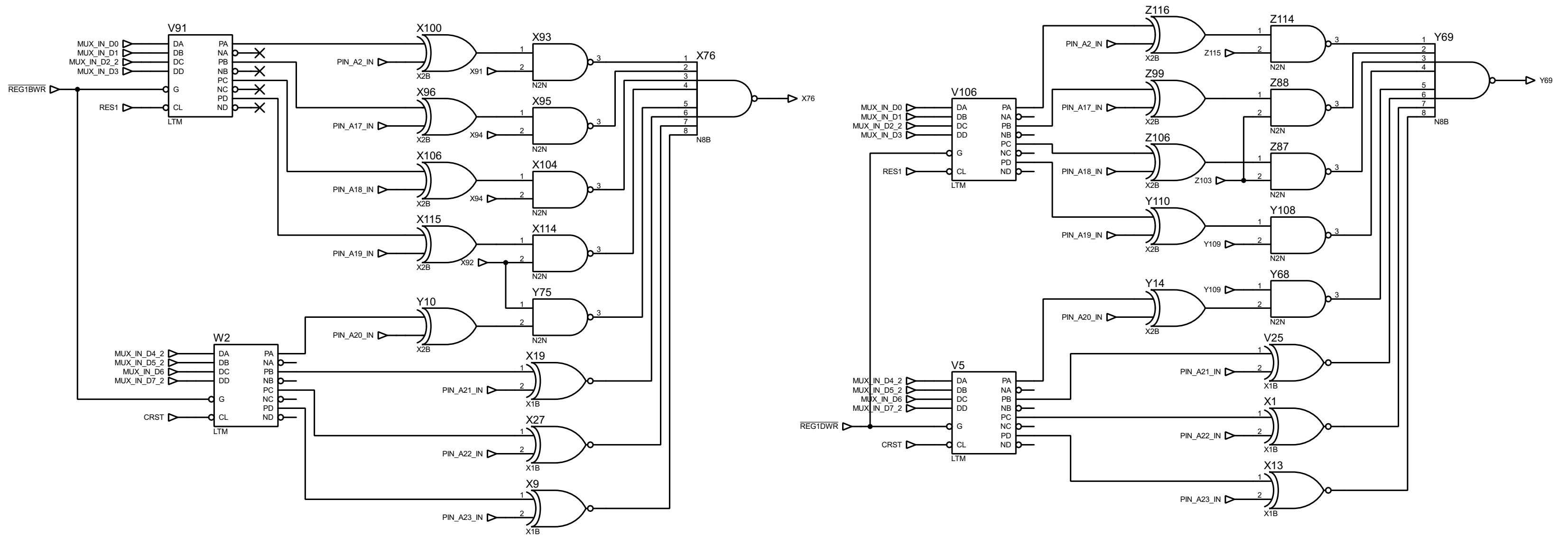
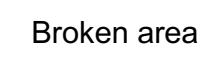
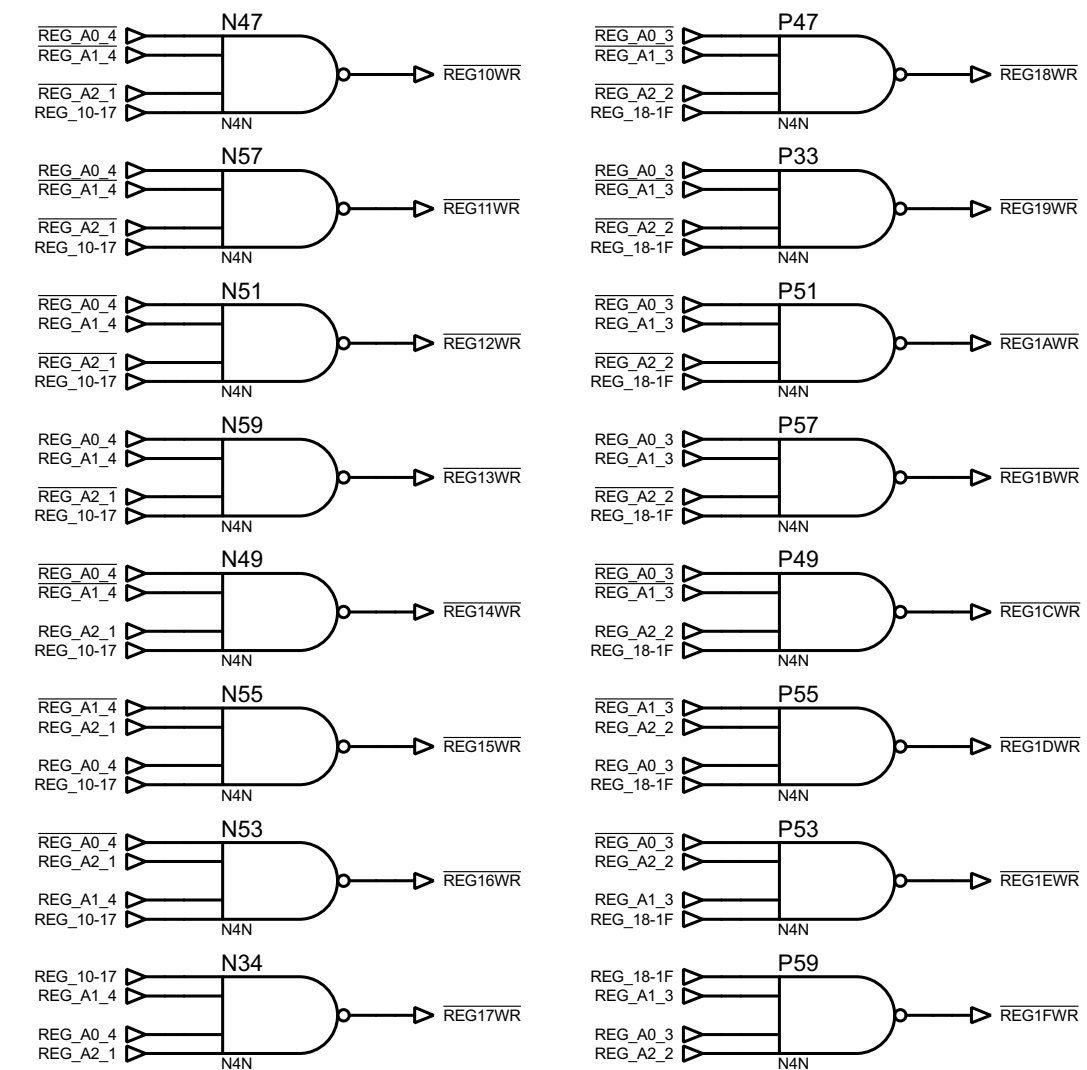
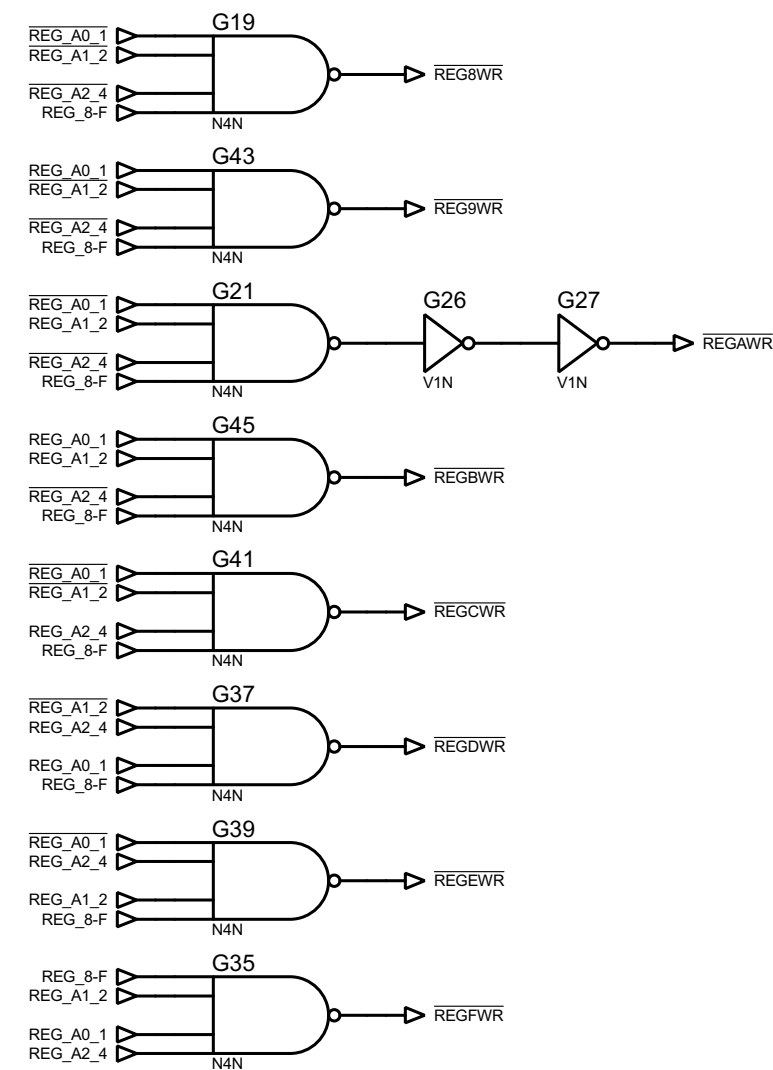
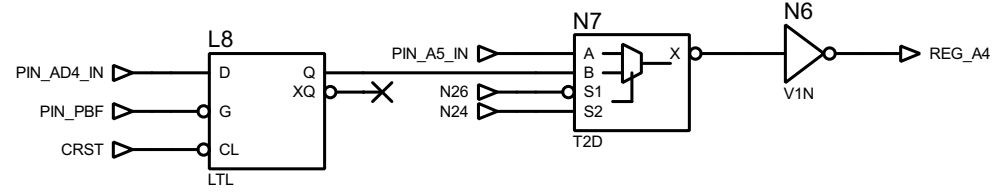


Read 02:
 Bit 0: REST pin
 Bit 1: HALT pin
 Bit 2: BERR pin
 Bit 3: IPL pins direction
 Bit 4: IRQ in
 Bit 5: P pins direction
 Bit 6: Busy with R/W
 Bit 7:

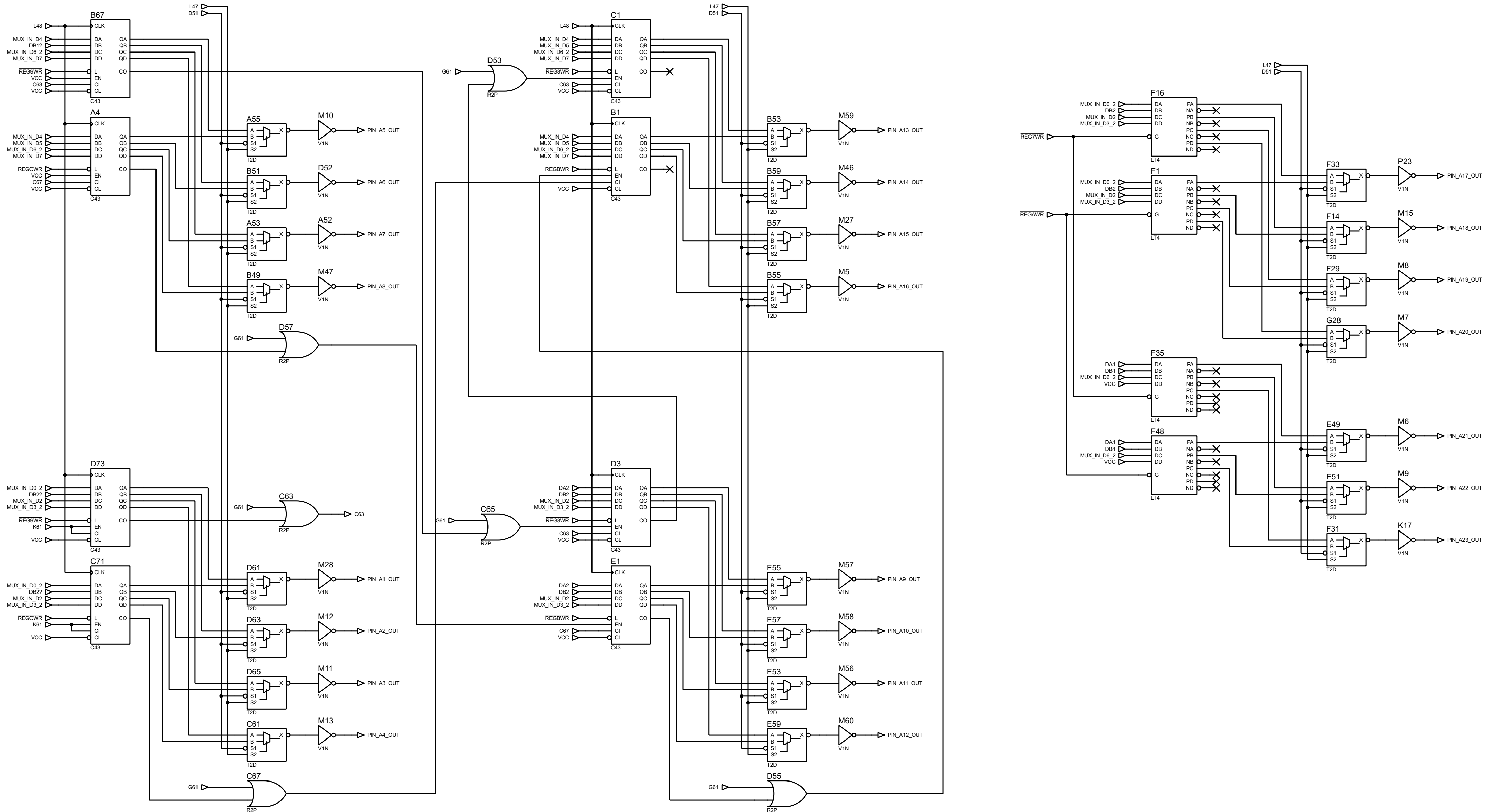


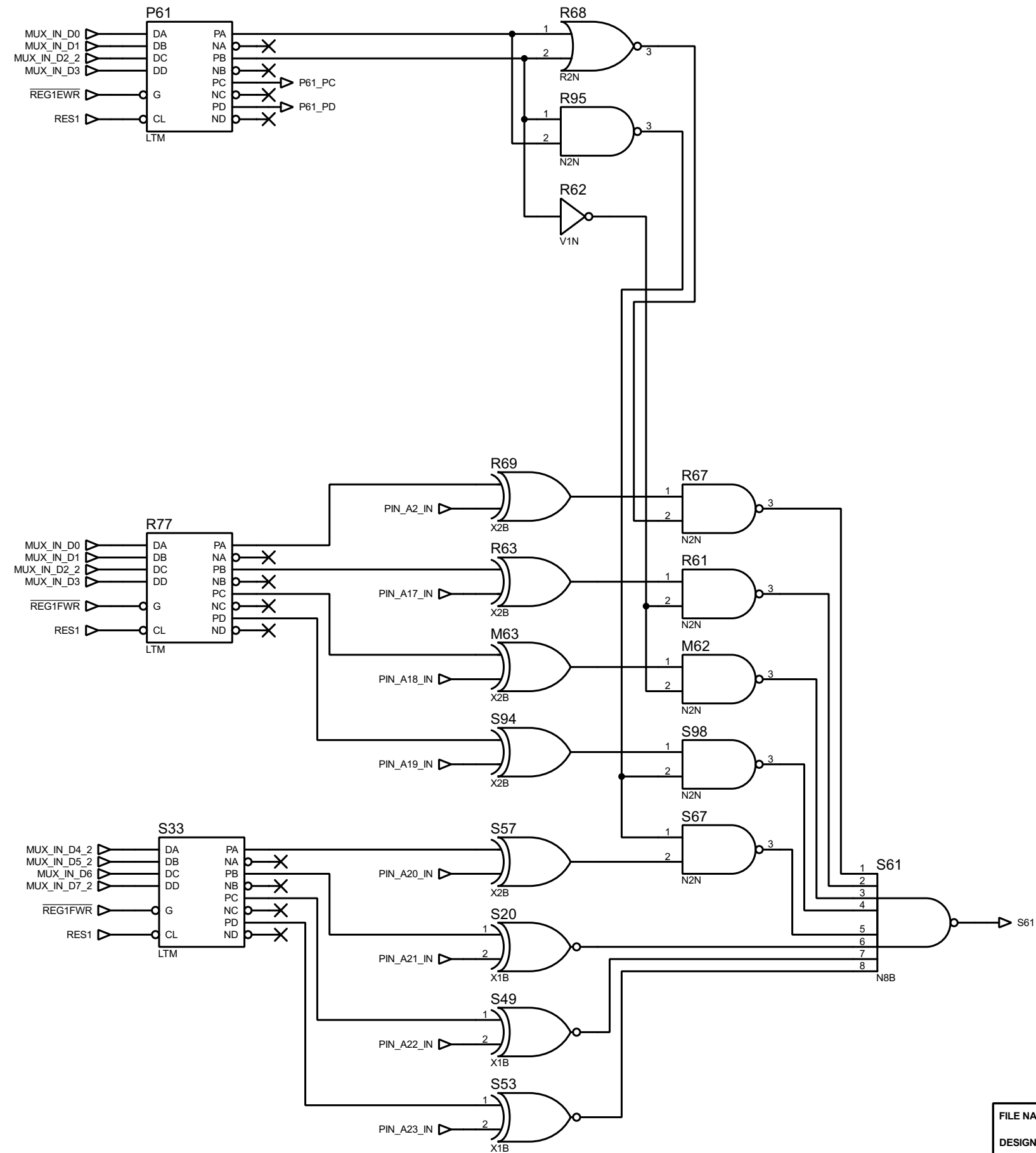


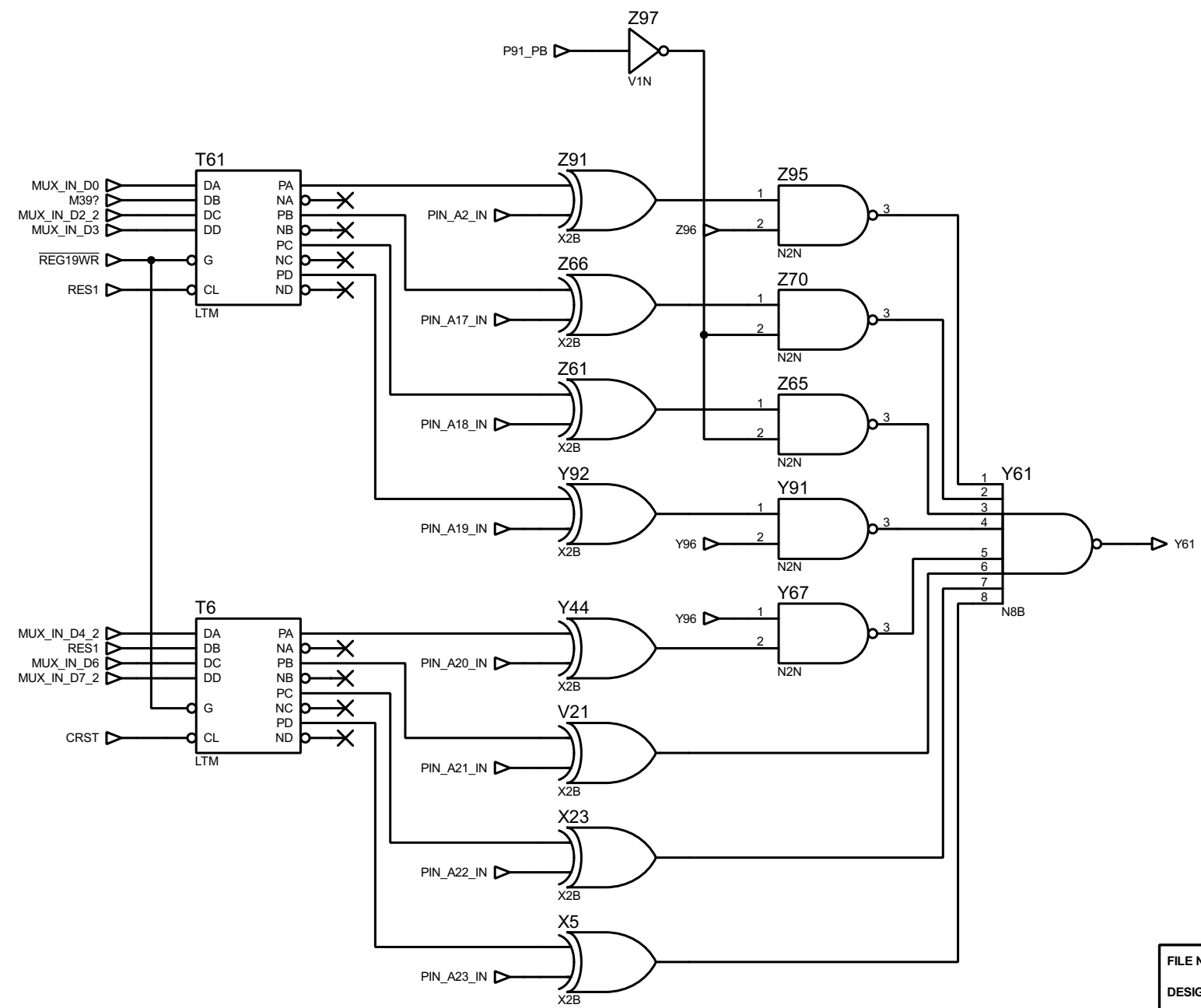
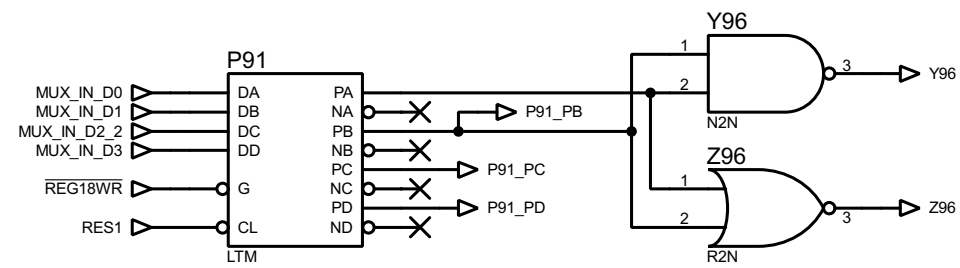


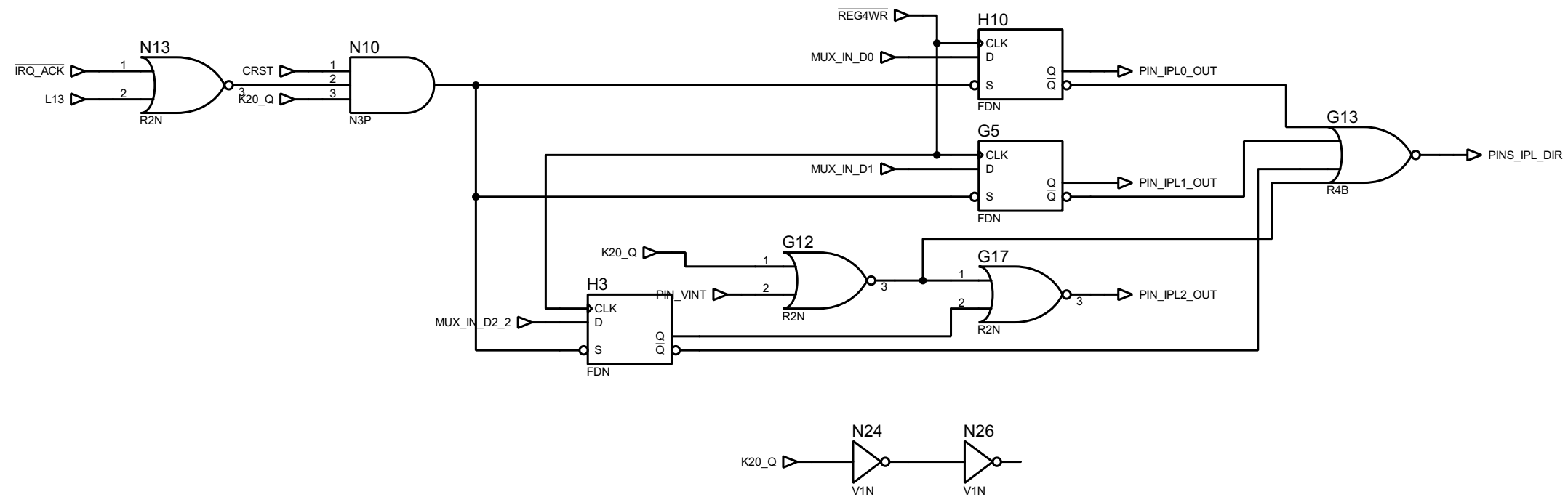
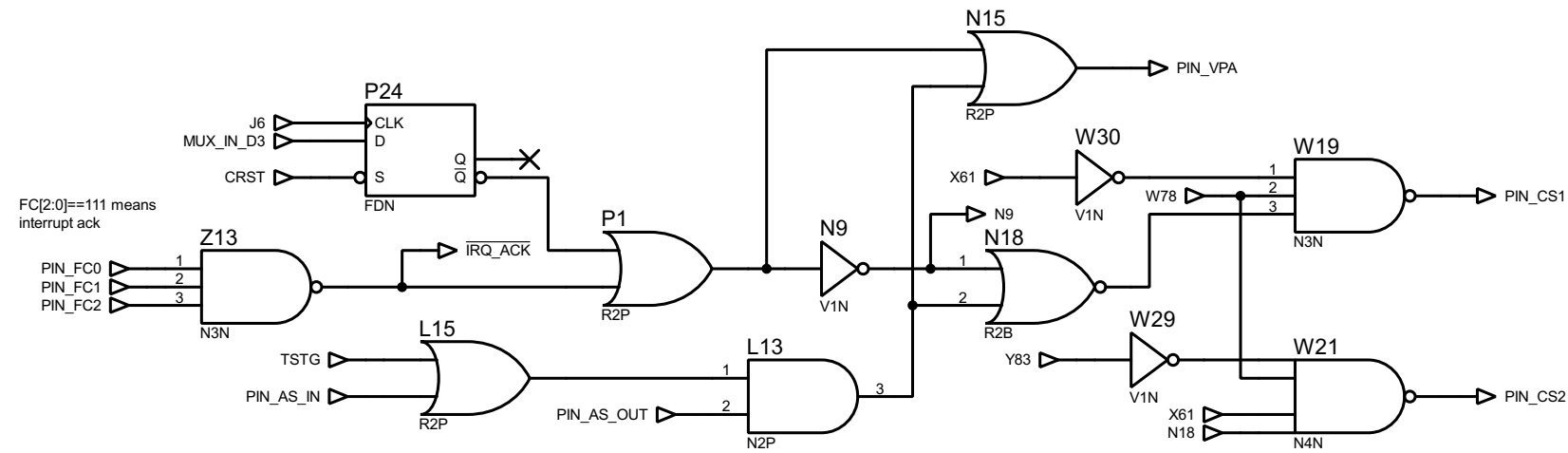
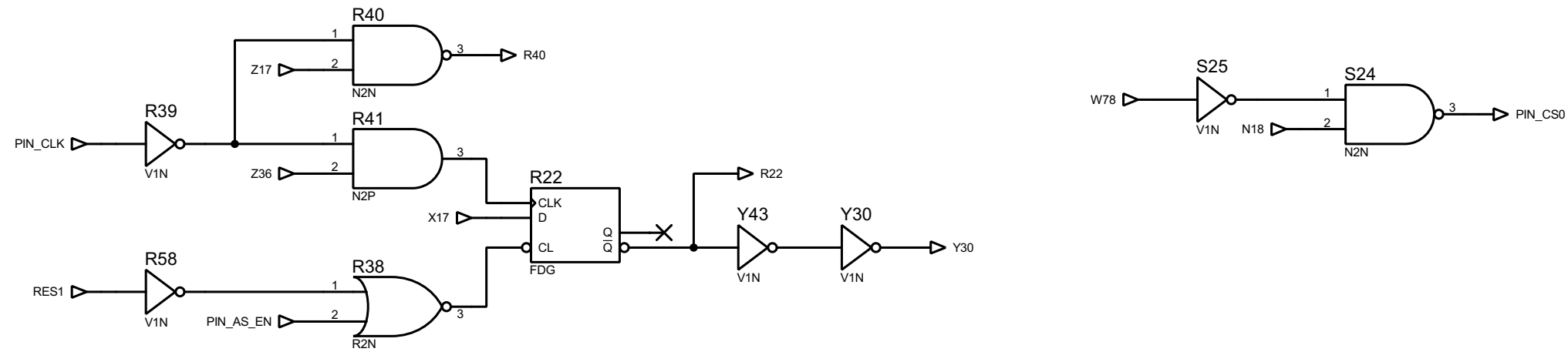


Reg	Decoder	Write
0	J30	Data to write
1	J13	Data to write
2	J32	Half/reset control
3	J28 xx	68k -> Z80
4	J6	Set 68k IPL lines
5	J3	R/W control
6	J18	?
7	J11 xx	Write address
8	G19 xx	
9	G43 xx	
A	G21 xx	Read address
B	G45 xx	
C	G41 xx	
D	G37 x	?
E	G39 xx	
F	G35	
10	N47 x	Size mask
11	N57 x	Base...
12	N51 x	Size mask
13	N59 xx	Base...
14	N45 x	
15	N55 xx	
16	N53 x	
17	N34 xx	
18	P47 x	
19	P33 xx	
1A	P51 x	
1B	P57 xx	
1C	P49 x	
1D	P55 xx	
1E	P53 x	
1F	P59 xx	

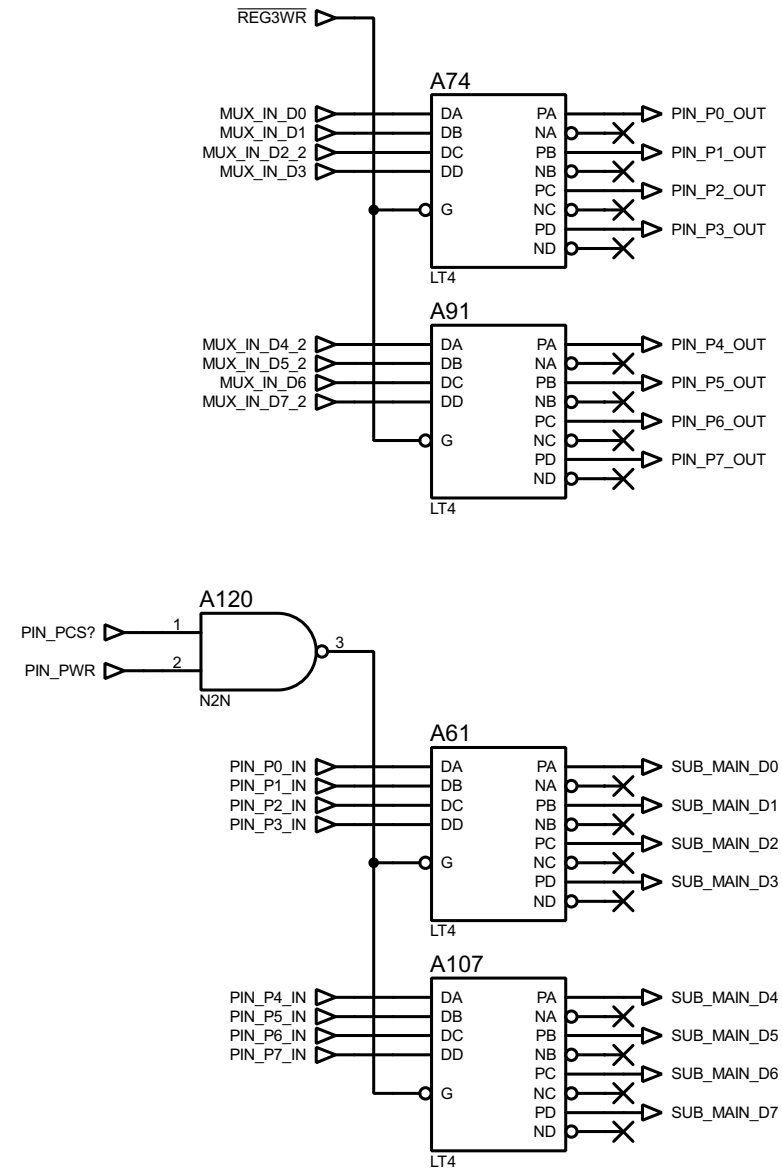




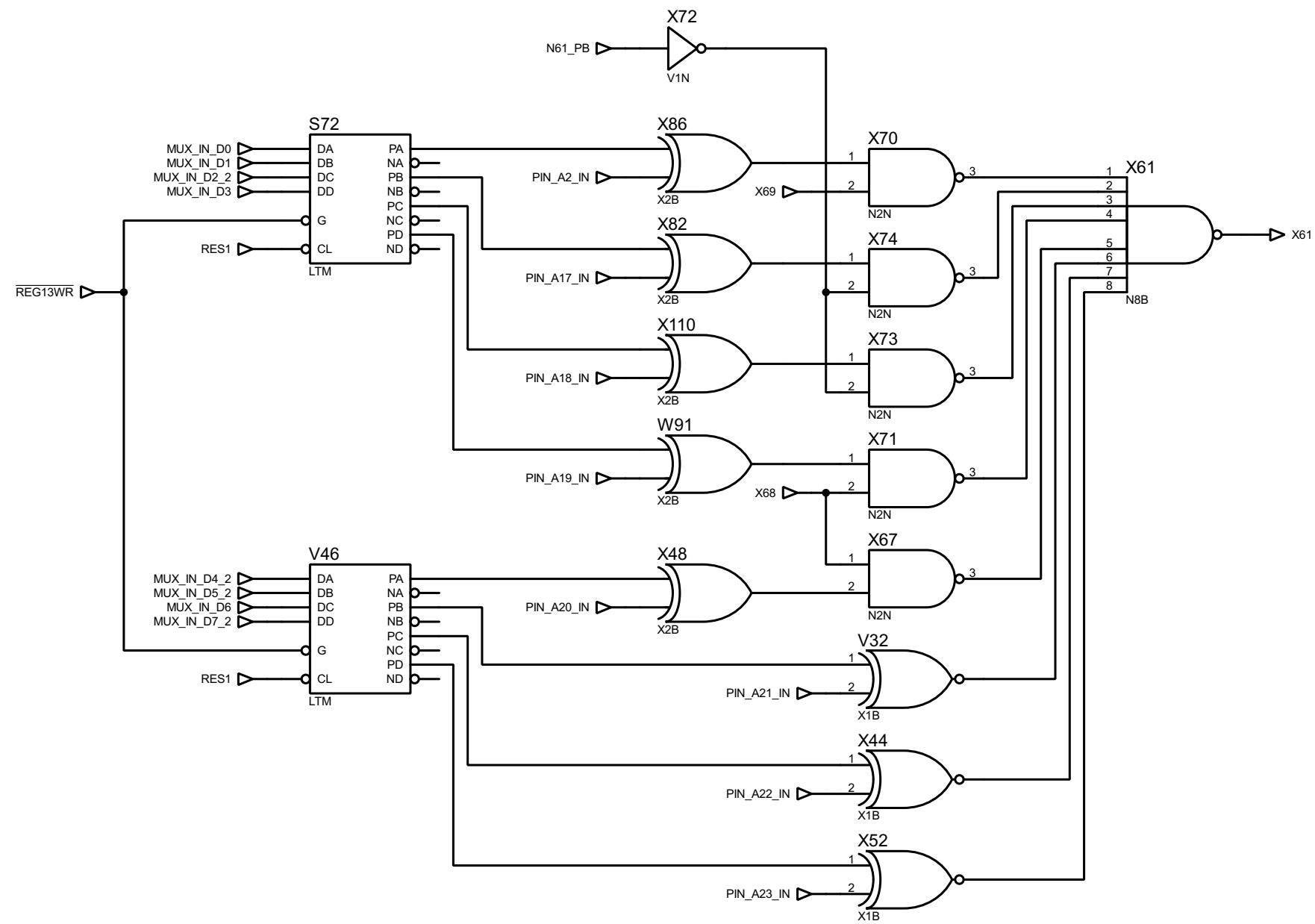




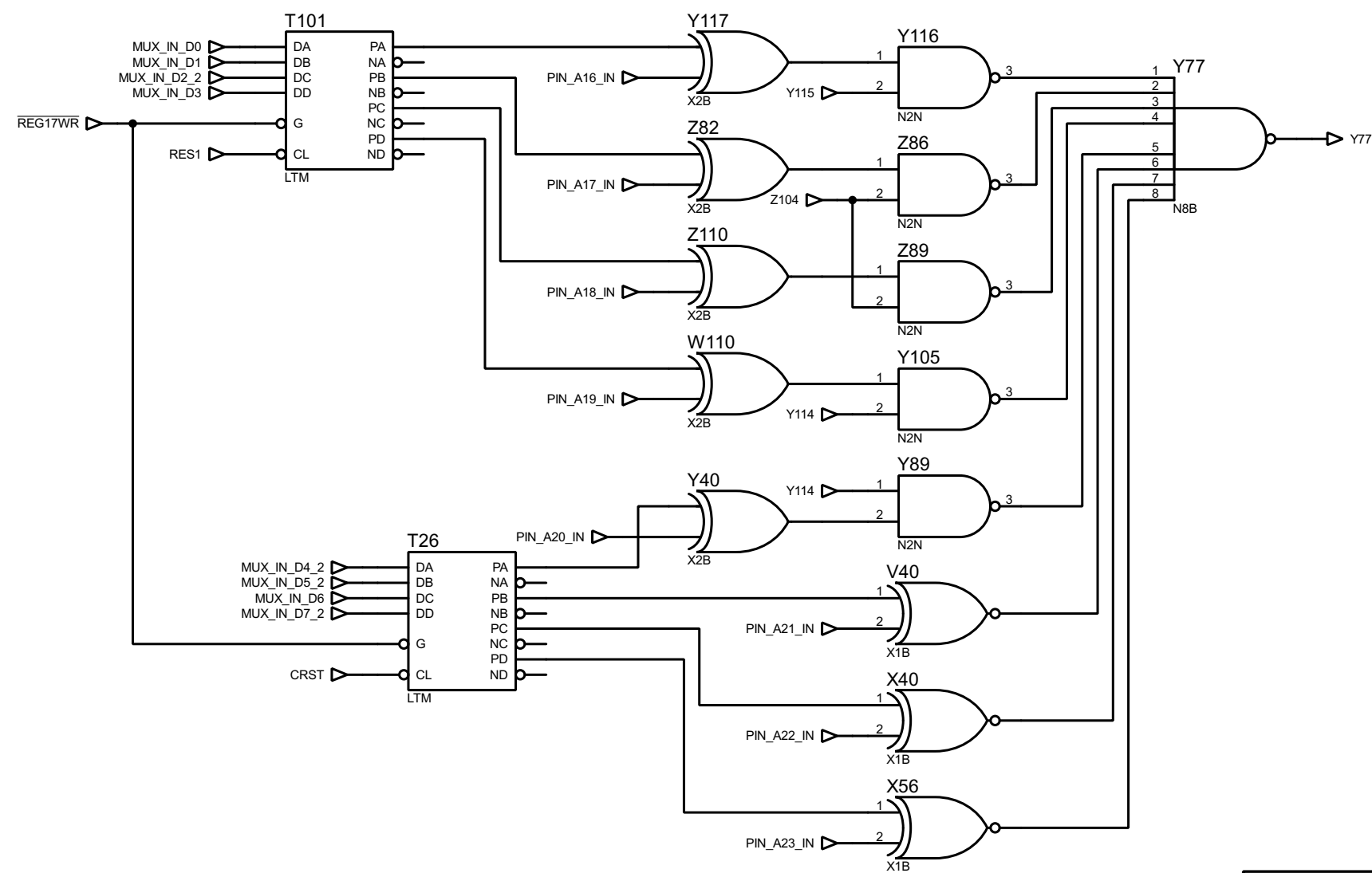
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DESIGN TITLE: Seag 315-5195 CS OUTPUTS	PAGE: 11 of 14
BY: Sean Gonsalves	REV: A



FILE NAME: 315-5195.pdsprj	DATE: 23/07/2021
DESIGN TITLE: Seag 315-5195 MAIN / SUB COMM	PAGE: 12 of 14
BY: Sean Gonsalves	REV: A



FILE NAME: 315-5195.pdsprj	DATE: 23/07/2021
DESIGN TITLE: Seag 315-5195	PAGE: 13 of 14
MAPPING REGS BANK 6	
BY: Sean Gonsalves	REV: A



FILE NAME:	315-5195.pdsprj	DATE:	23/07/2021
DESIGN TITLE:	Seag 315-5195 MAPPING REGS BANK 3	PAGE:	14 of 14
BY:	Sean Gonsalves	REV:	A