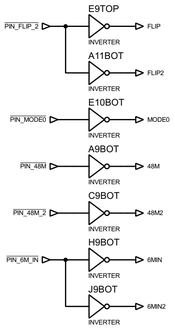
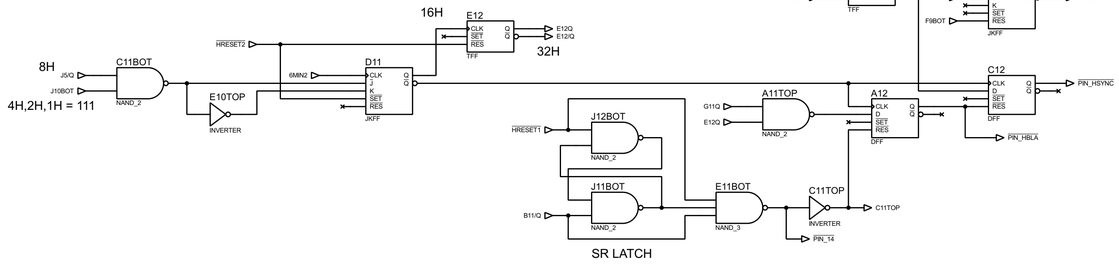
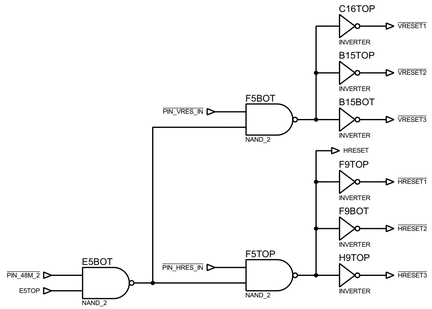
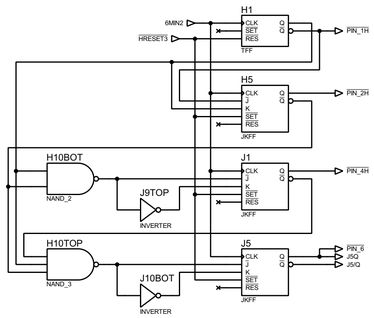
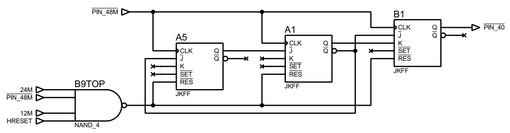
All IO blocks have embedded NANDs with max 3 inputs.
All unconnected inputs considered as in HIGH state.

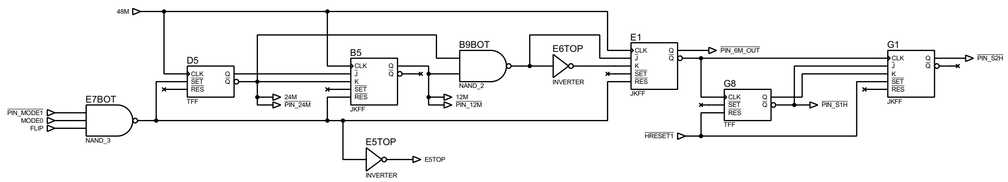


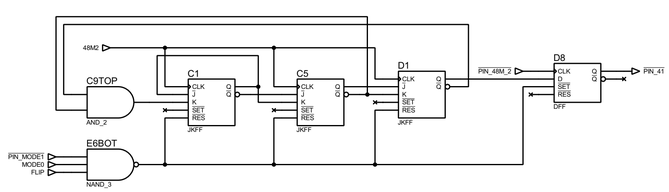


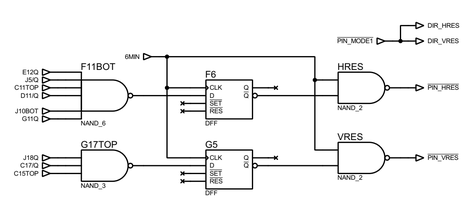










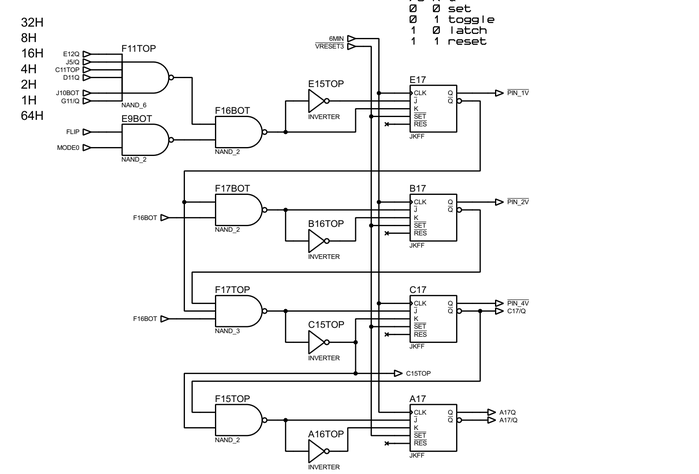


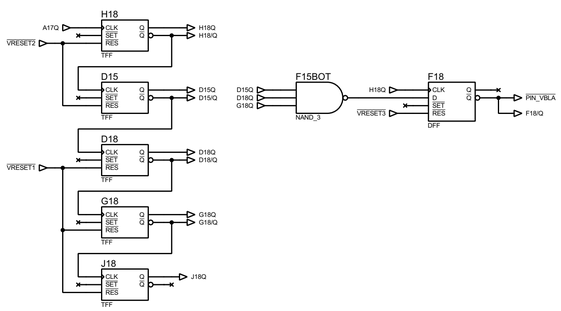
TITLE:	DATE:
Namco CUS27	27/06/2022
	PAGE: 1/1
BY: Sean Gonsalves	REV: A

V counters

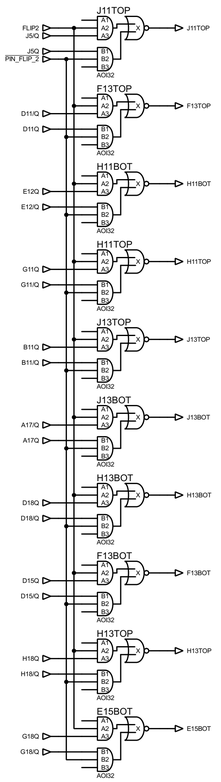
32H
8H
16H
4H
2H
1H
64H

/J	K	Q
0	0	set
0	1	toggle
1	0	latch
1	1	reset

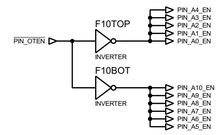




Flipping muxes



OTEN enables output on pins A0~A10



All PIN_Ax_y lines are NANDed together in the IO block of each respective pin