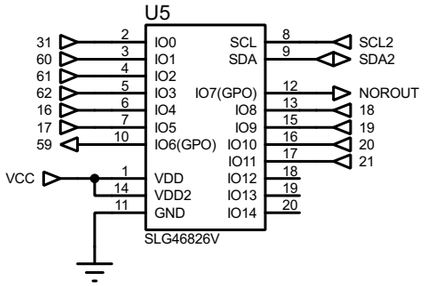
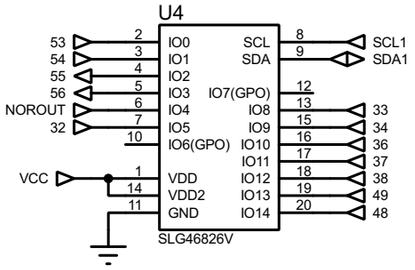
Changes:
Replaced the 4078 and the AND gate by a second SLG46826V
It's slightly cheaper, reduces the BOM, and eases routing
Routed (NOR U9 pin 13, now in new SLG46826V) to IO4 (pin 6)
Routed NEO-E0 pin 32 to IO5 (pin 7)

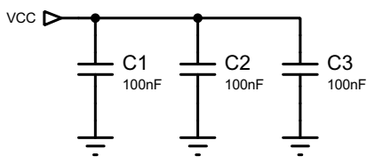
2



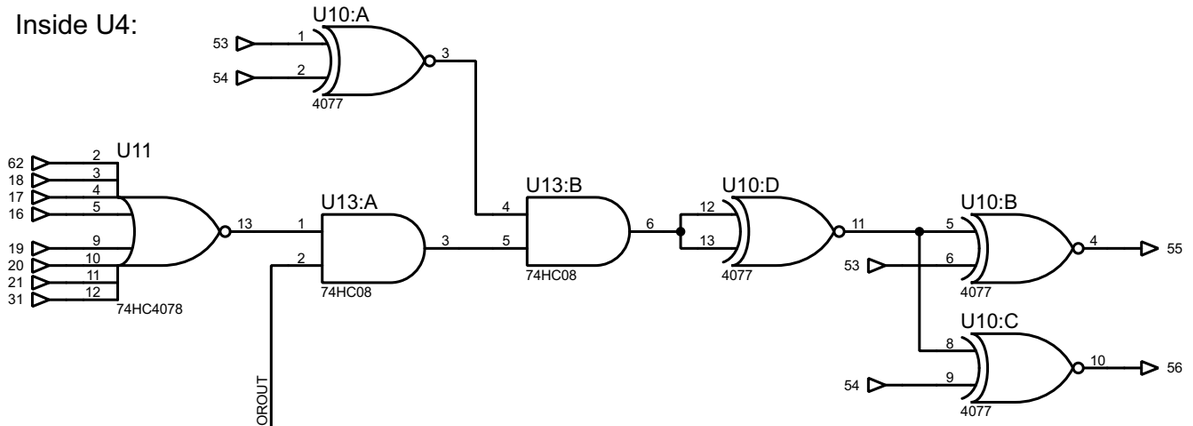
1



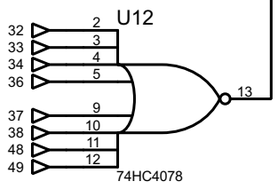
Required GPIOs:
8 in OR
1 in 8OR ext
(2 in AND)
(1 out AND)
2 in A22 A23
2 out A22Z A23Z
16 total



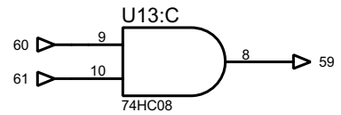
Inside U4:



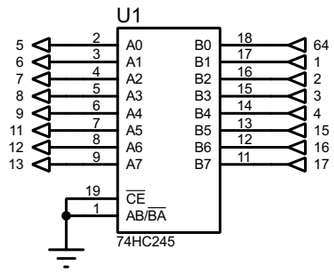
Inside U5:

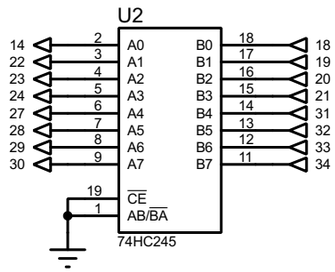


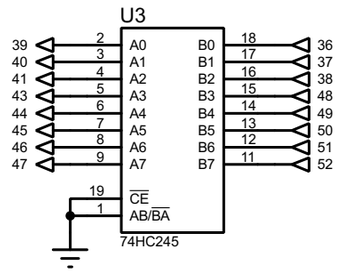
Individual AND gate



Plain buffers







FILE NAME: NEO-E0_B.pdsprj	DATE: 10/11/2022
DESIGN TITLE: NEO-E0	PAGE: 1 of 1
BY: Sean Gonsalves REV: B	