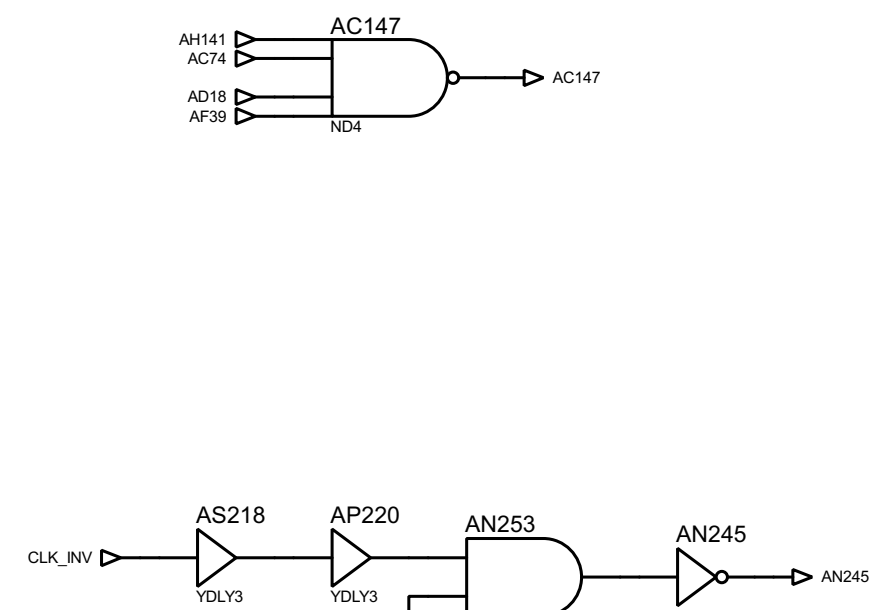
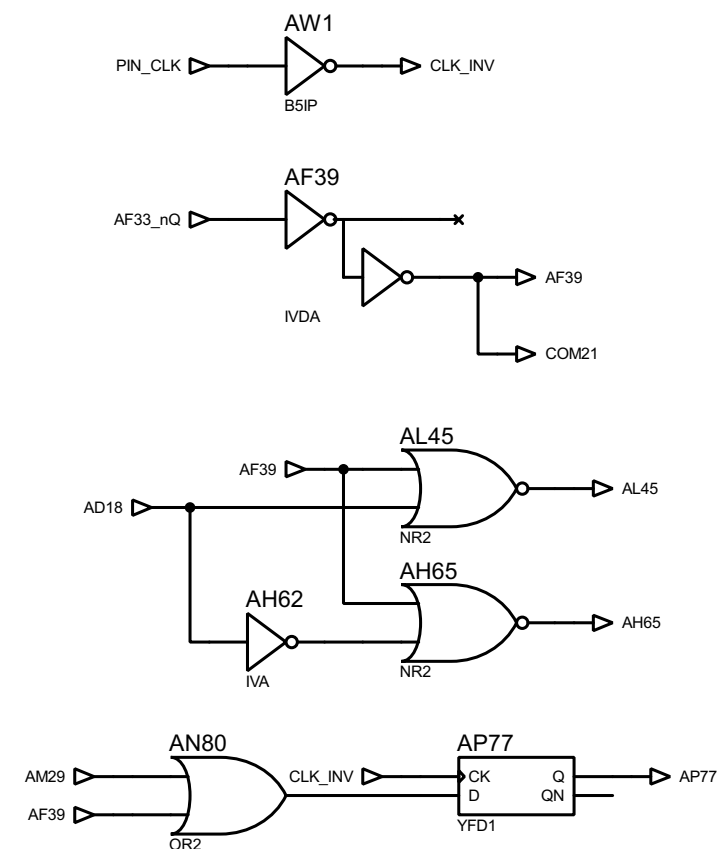
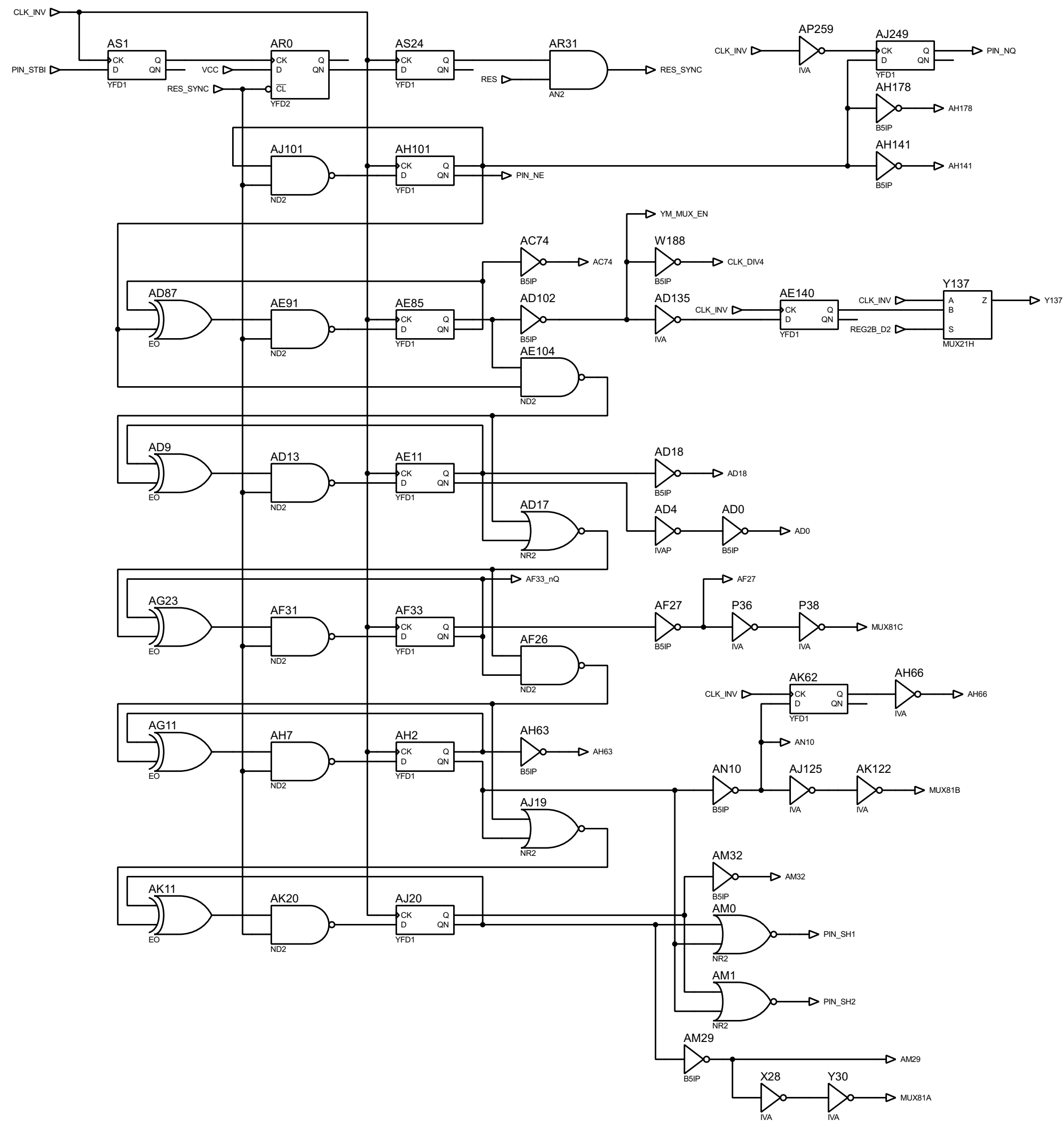
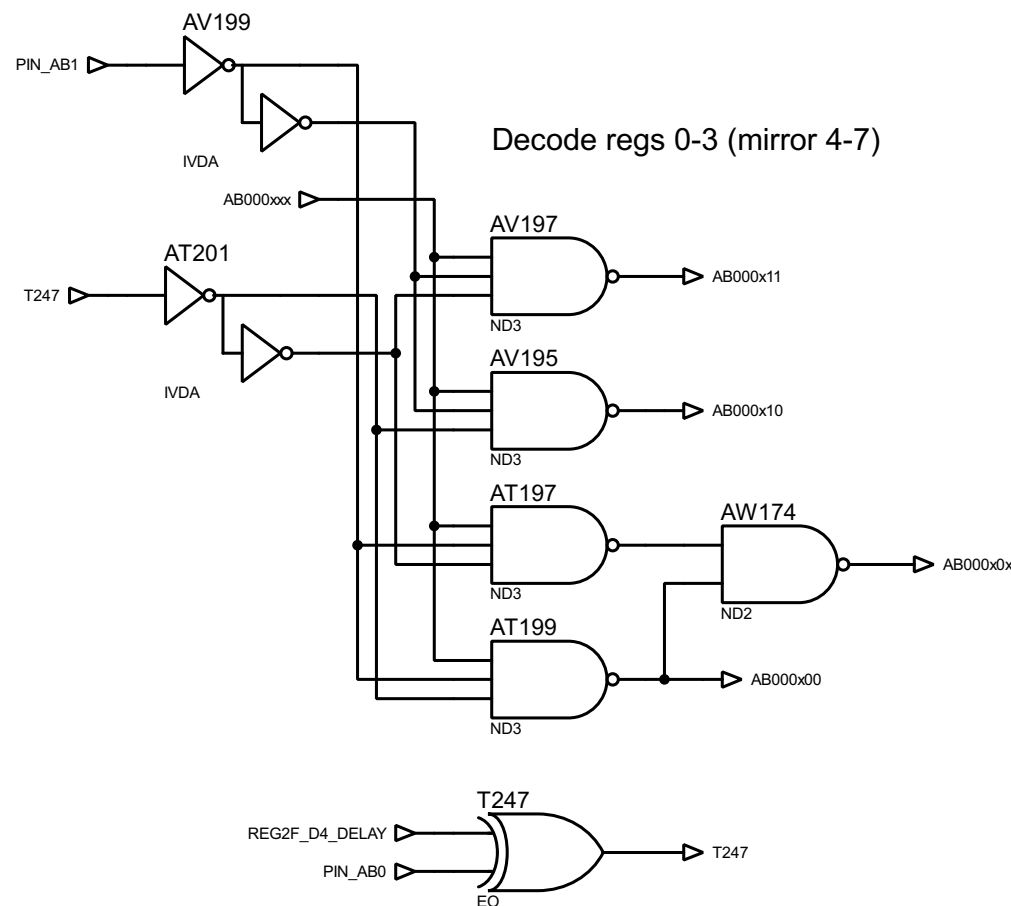
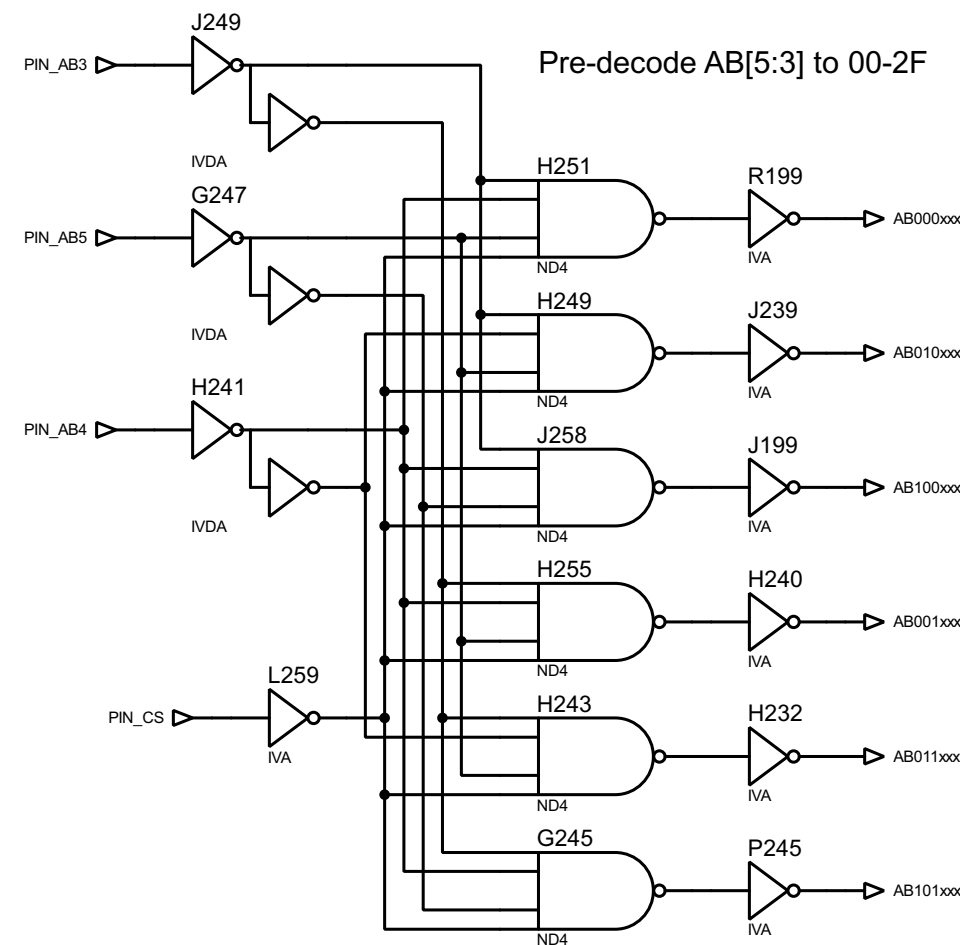
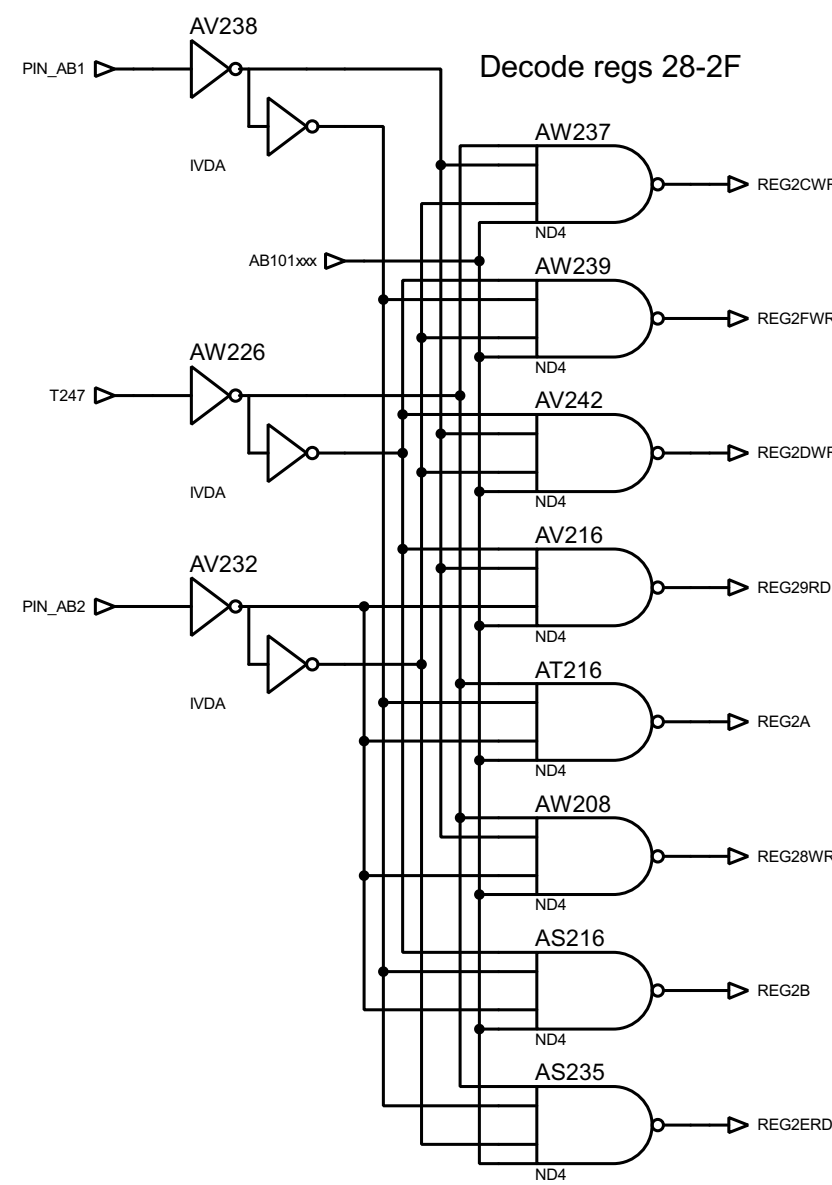
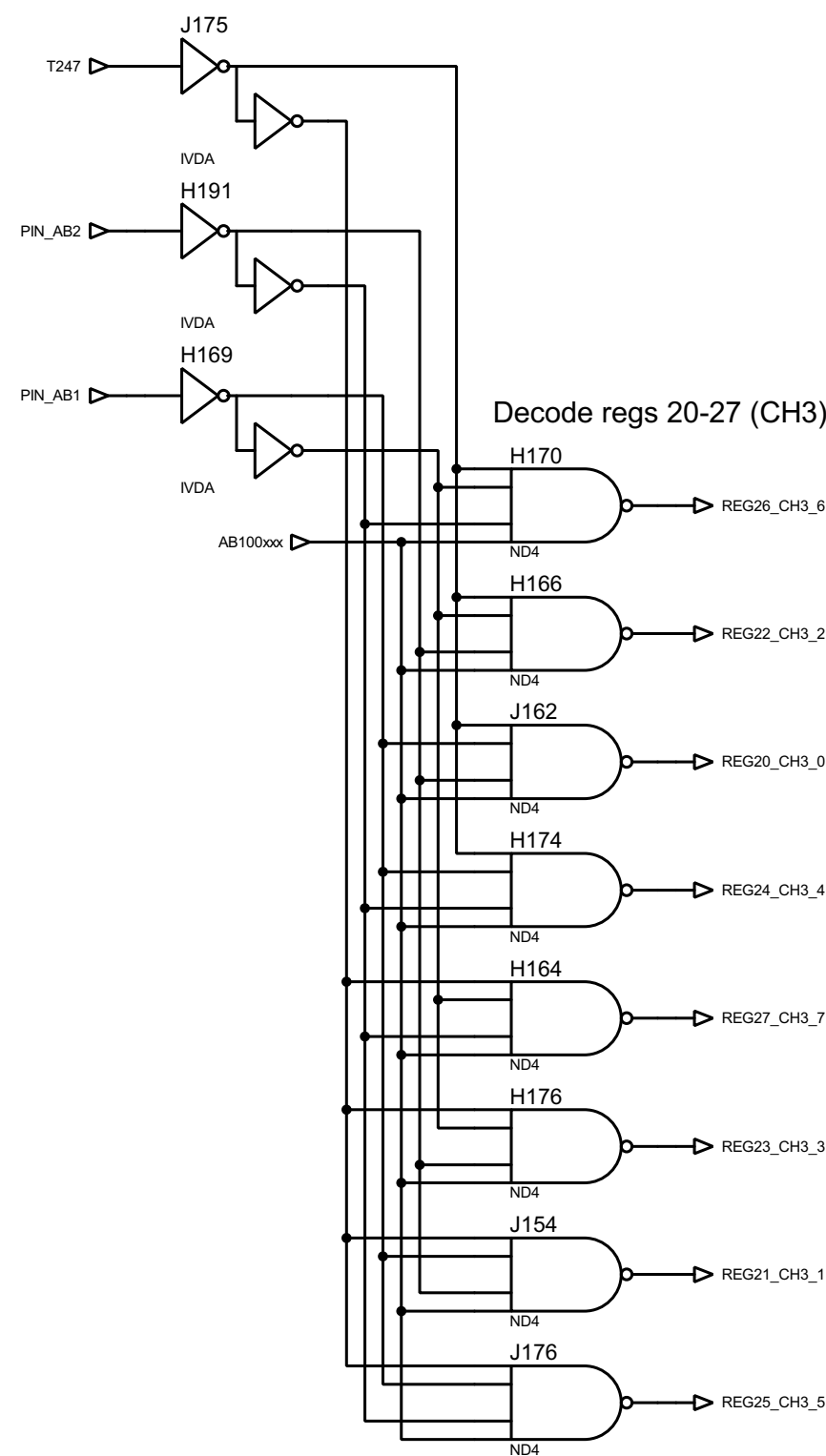
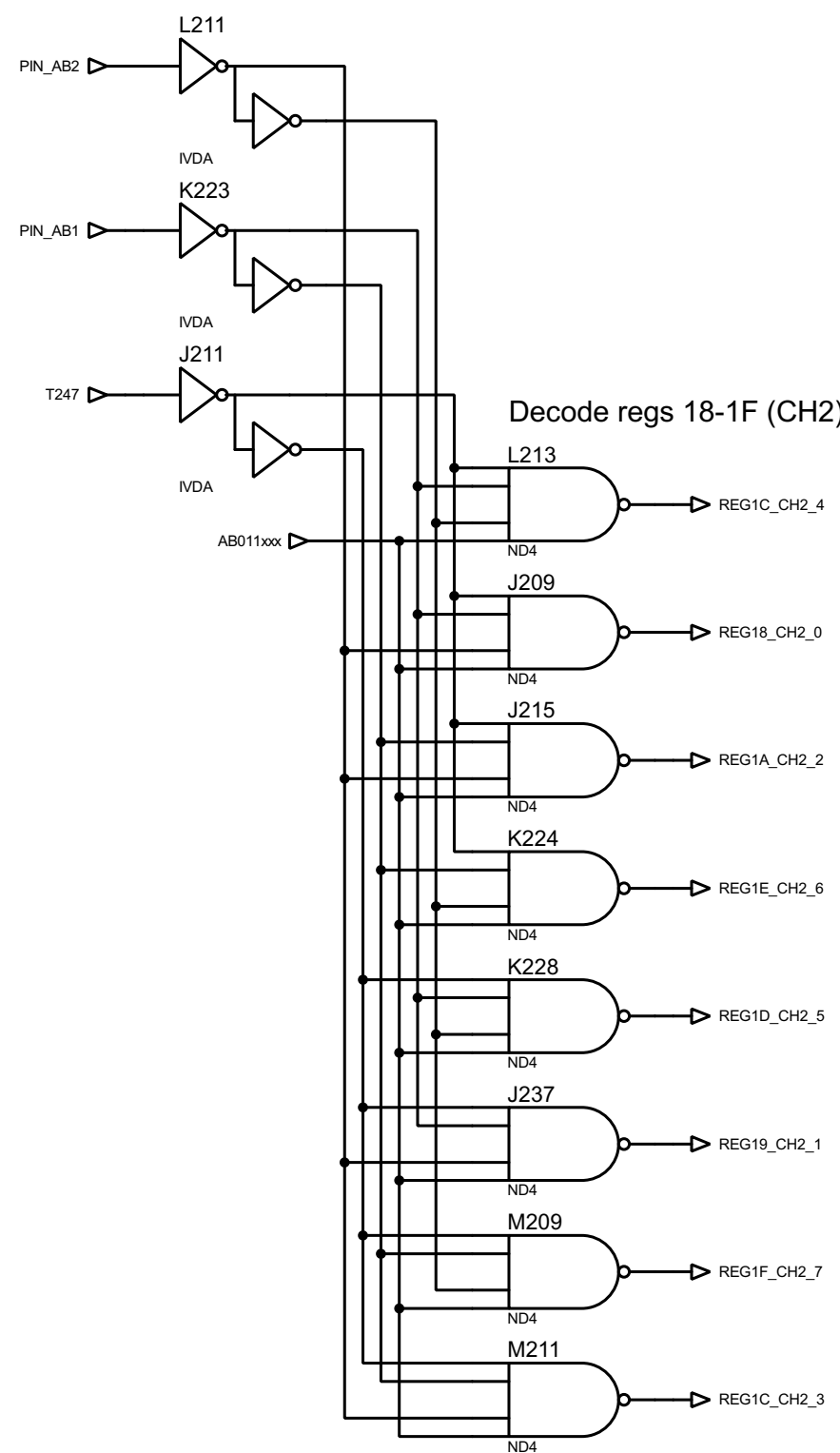
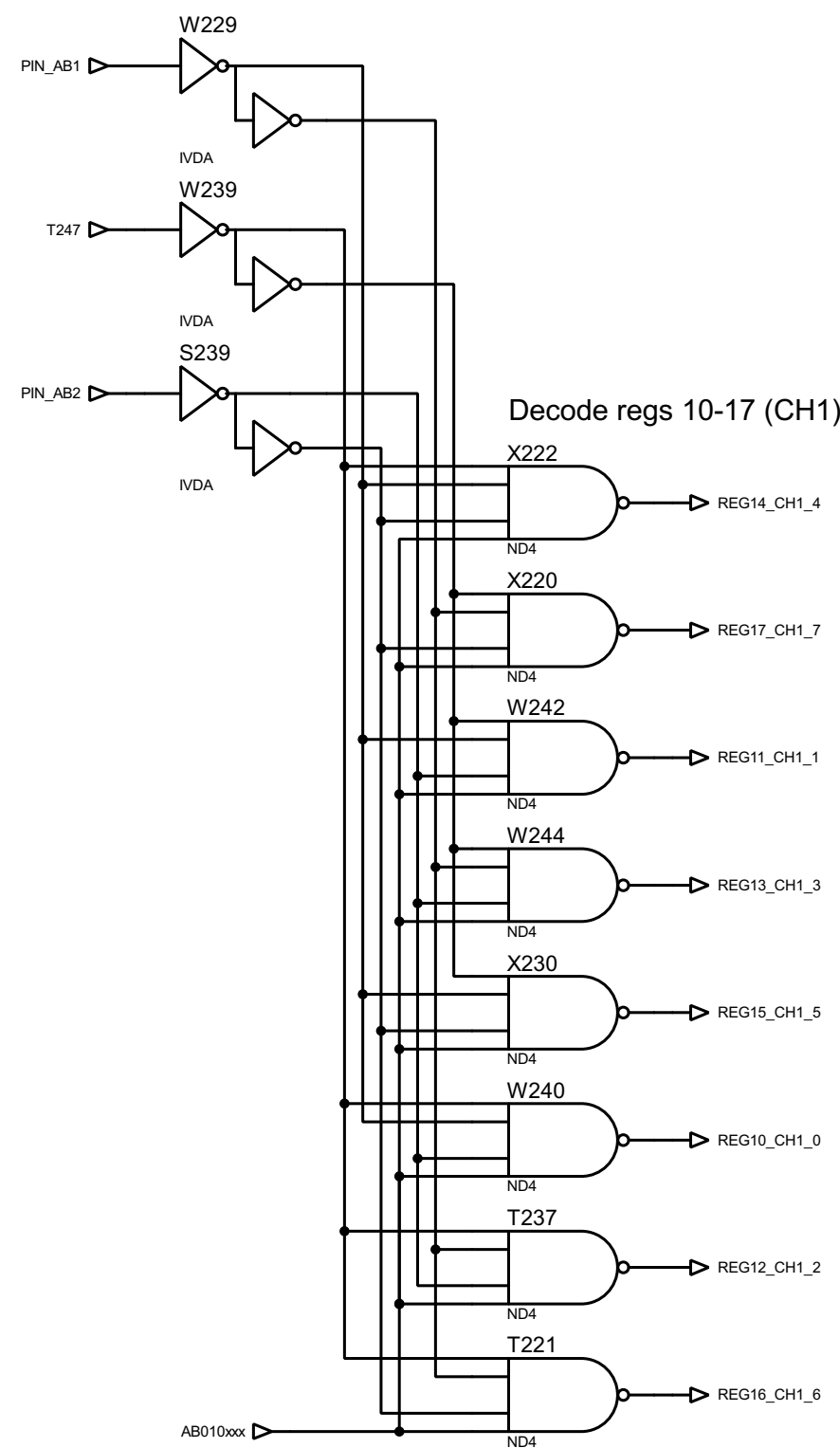
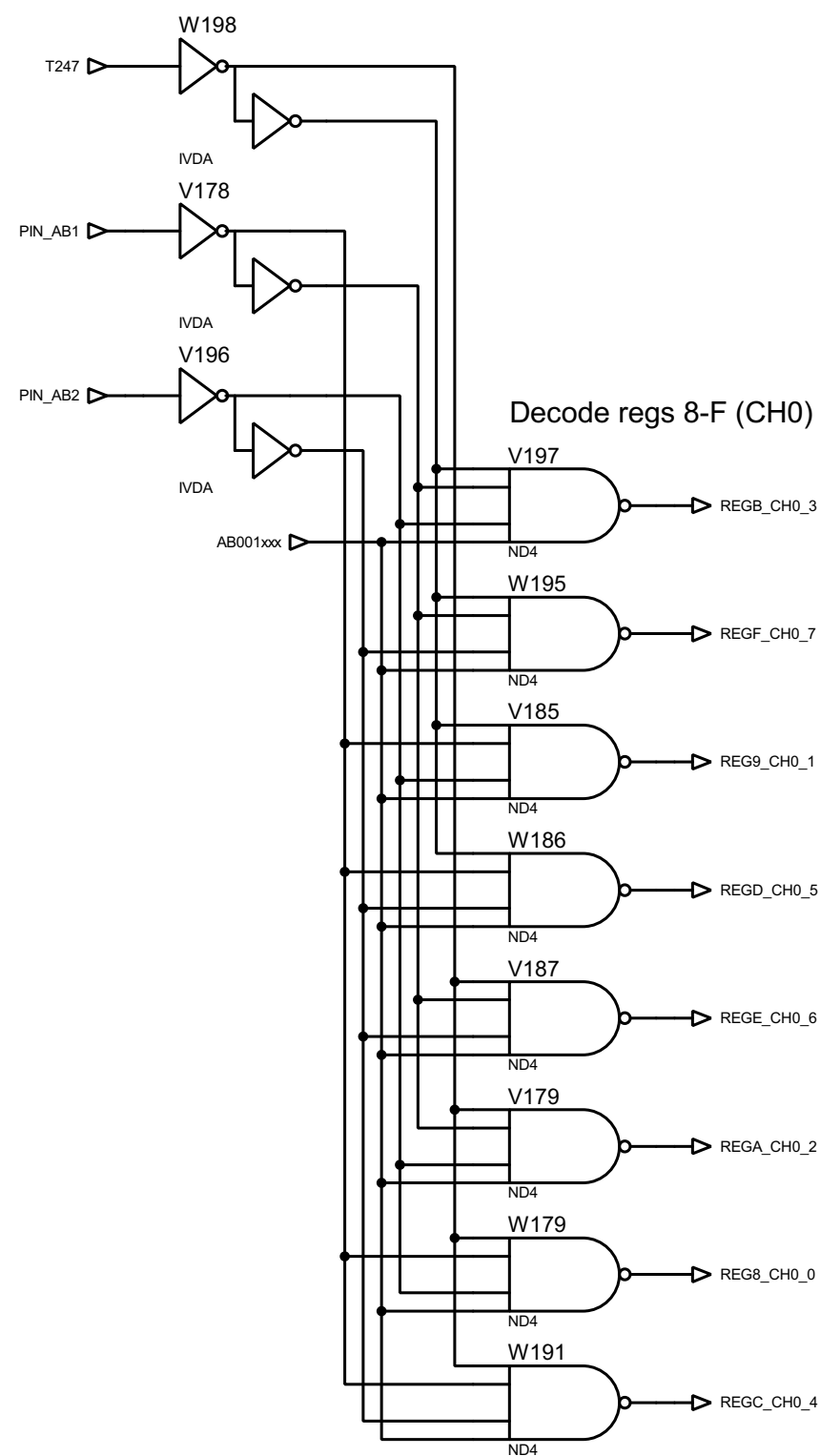


Clock distribution:  
AH141 /2 invert  
AC74 /4  
AD18 AD0 /8  
AF27 /16 invert  
AN10 /32  
AH63 /32 invert  
AM29 AM32 /64 invert

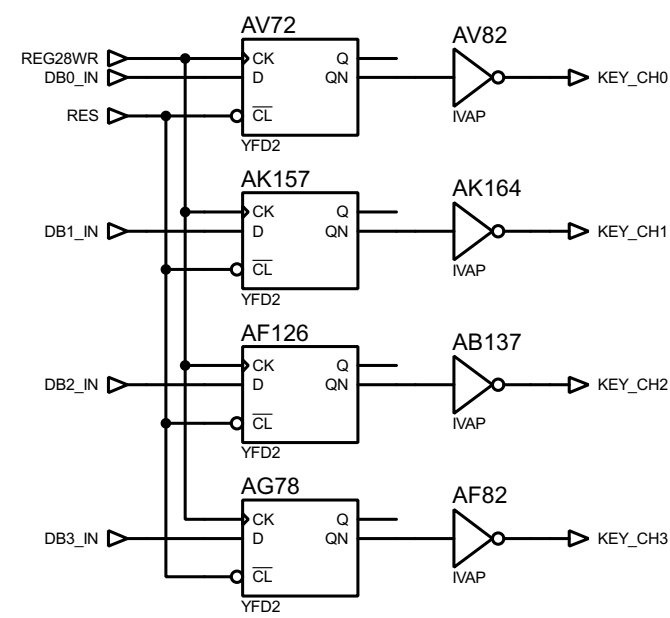




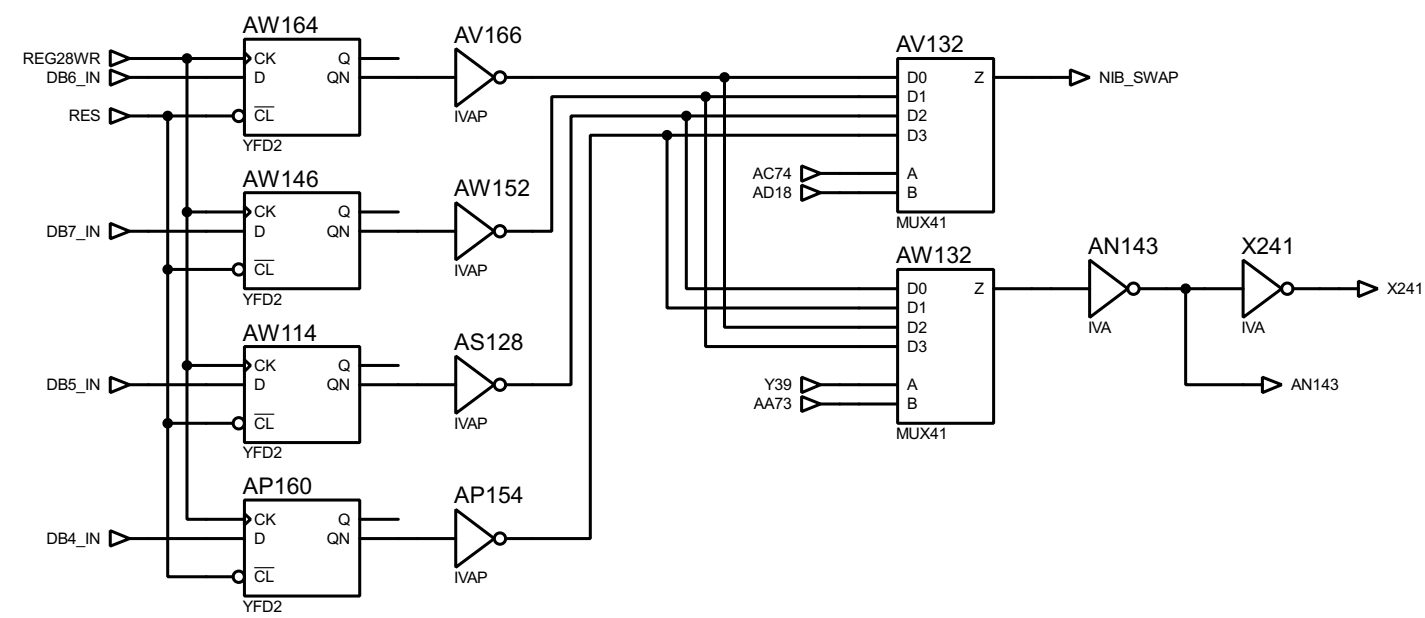
Reg  
00: Sub-to-main A WR  
01: Sub-to-main B WR  
02: Main-to-sub A RD  
03: Main-to-sub B RD  
04: Mirror of 0 ?  
05: Mirror of 1 ?  
06: Mirror of 2 ?  
07: Mirror of 3 ?  
  
4x the following group (08-27)  
08: Pitch low WR  
09: [3:0] Pitch high WR  
0A: Length low WR  
0B: Length high WR  
0C: Start low WR  
0D: Start middle WR  
0E: [4:0] Start high WR  
0F: [6:0] Volume WR  
  
28: [3:0] key on WR  
[7:4] ?  
29: [3:0] Ch status RD  
2A: [7:4] sample format, [3:0] loop en  
2B: Test modes  
2C: [7:4] CH1 pan, [3:0] CH0 pan  
2D: [7:4] CH3 pan, [3:0] CH2 pan  
2E: ROM data  
2F: 0: ROM read en  
1: Enable sound output  
2: Enable aux input ?  
3: ?



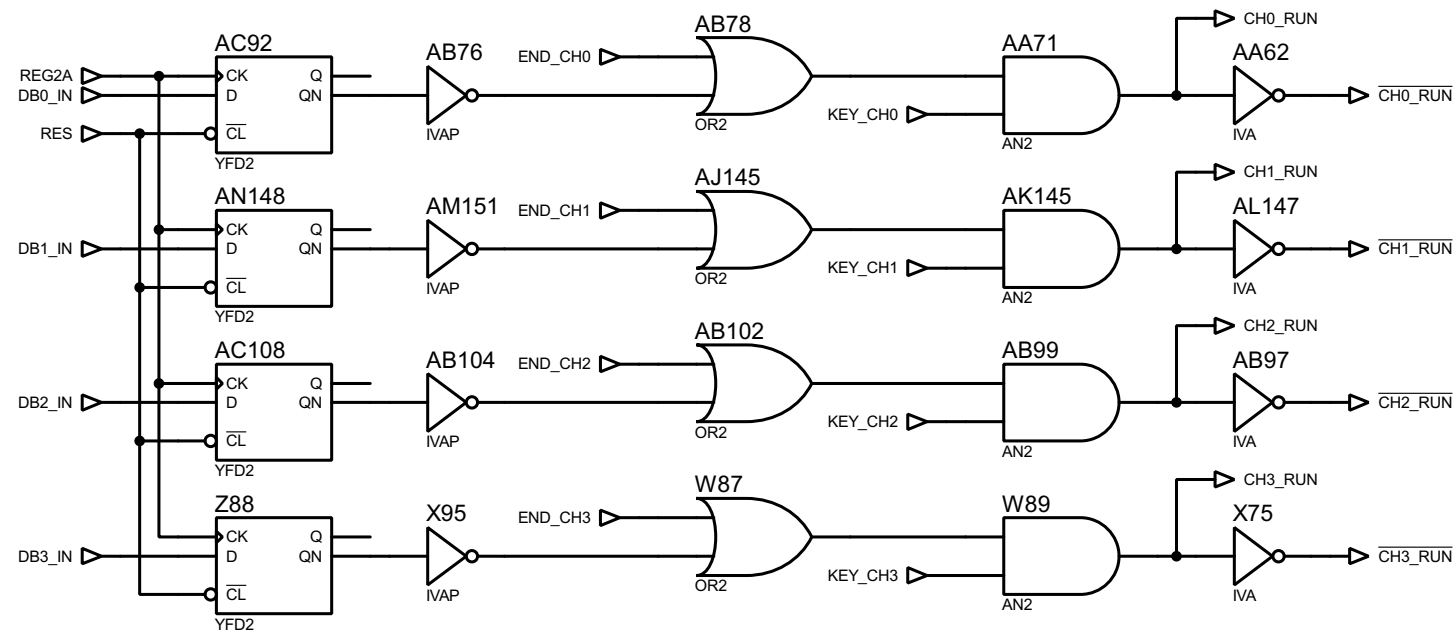
Reg key on/off



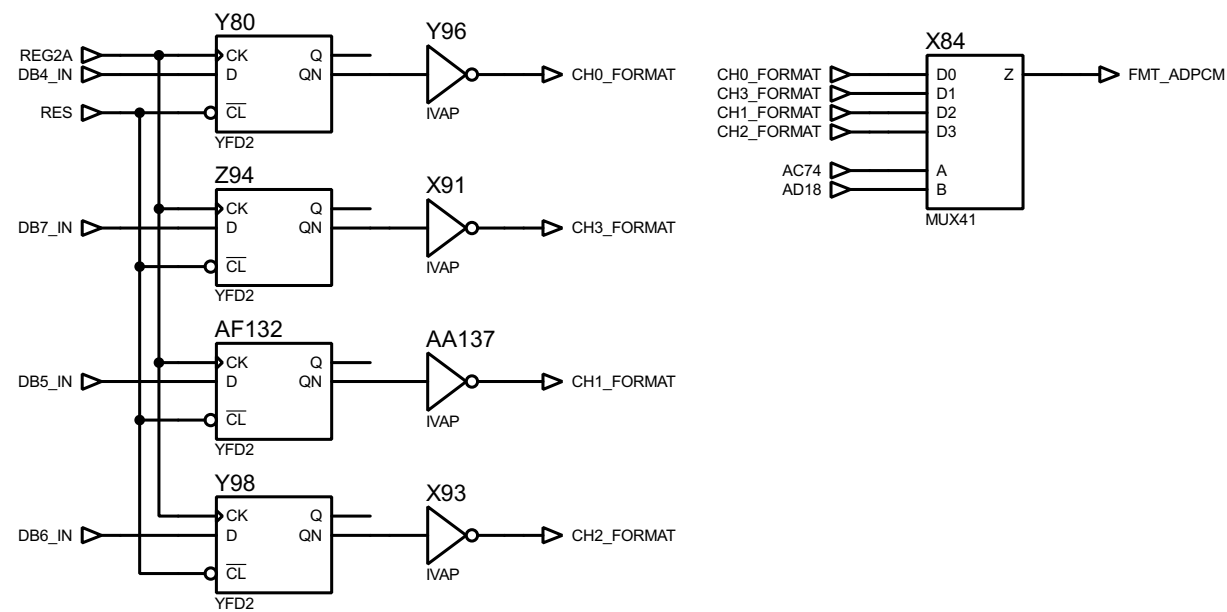
Play channel backwards ?

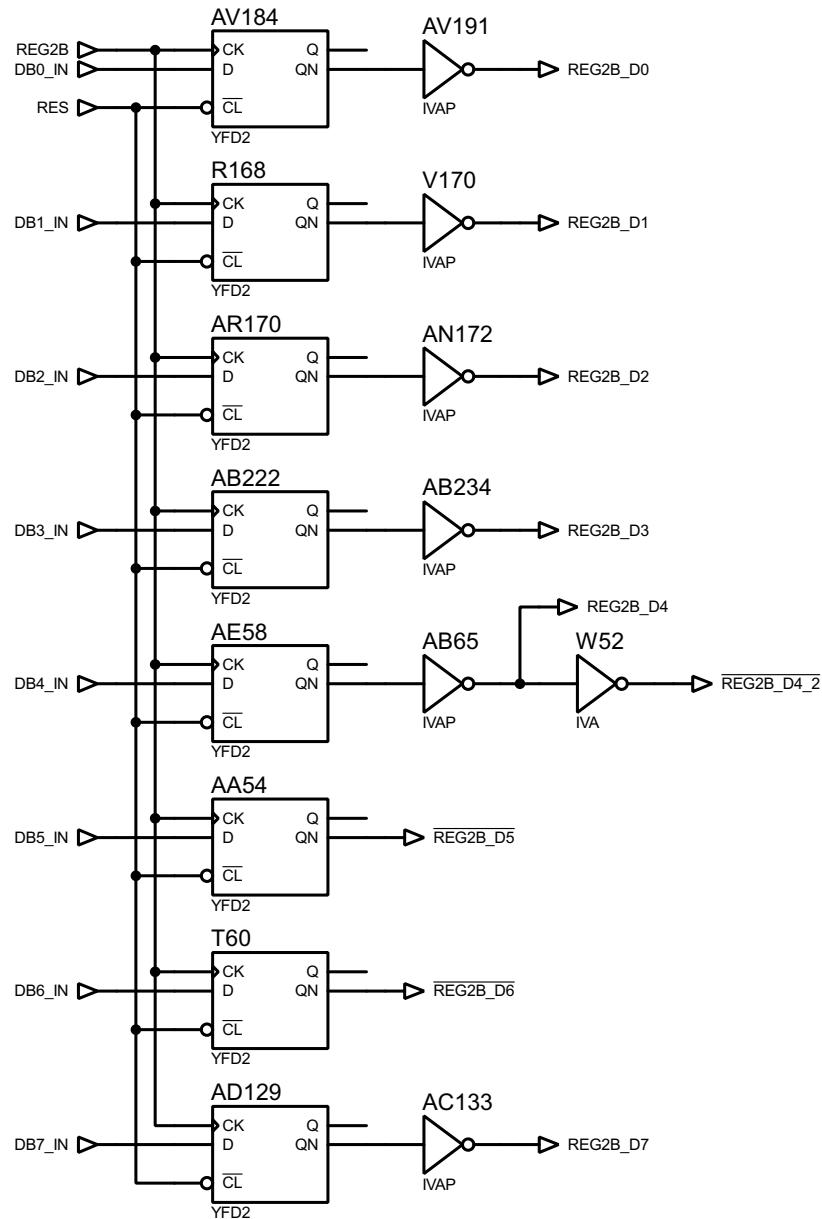


Loop flags



Format flags

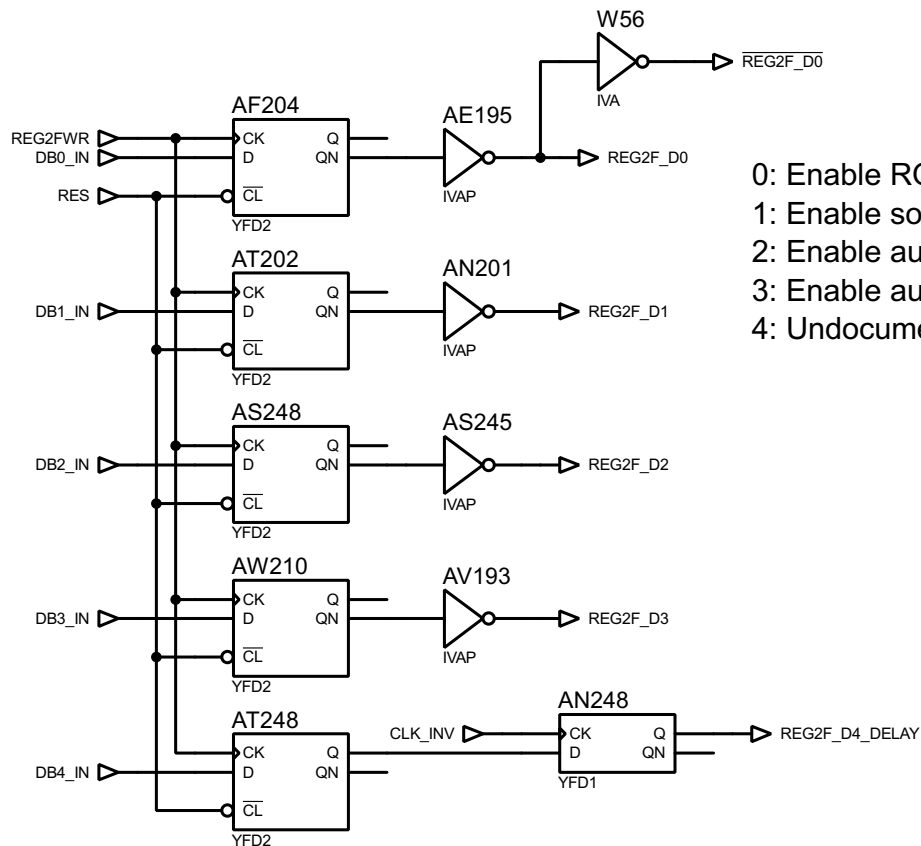




Test stuff. Setting this register to anything other than zero may cause irreversible damage.

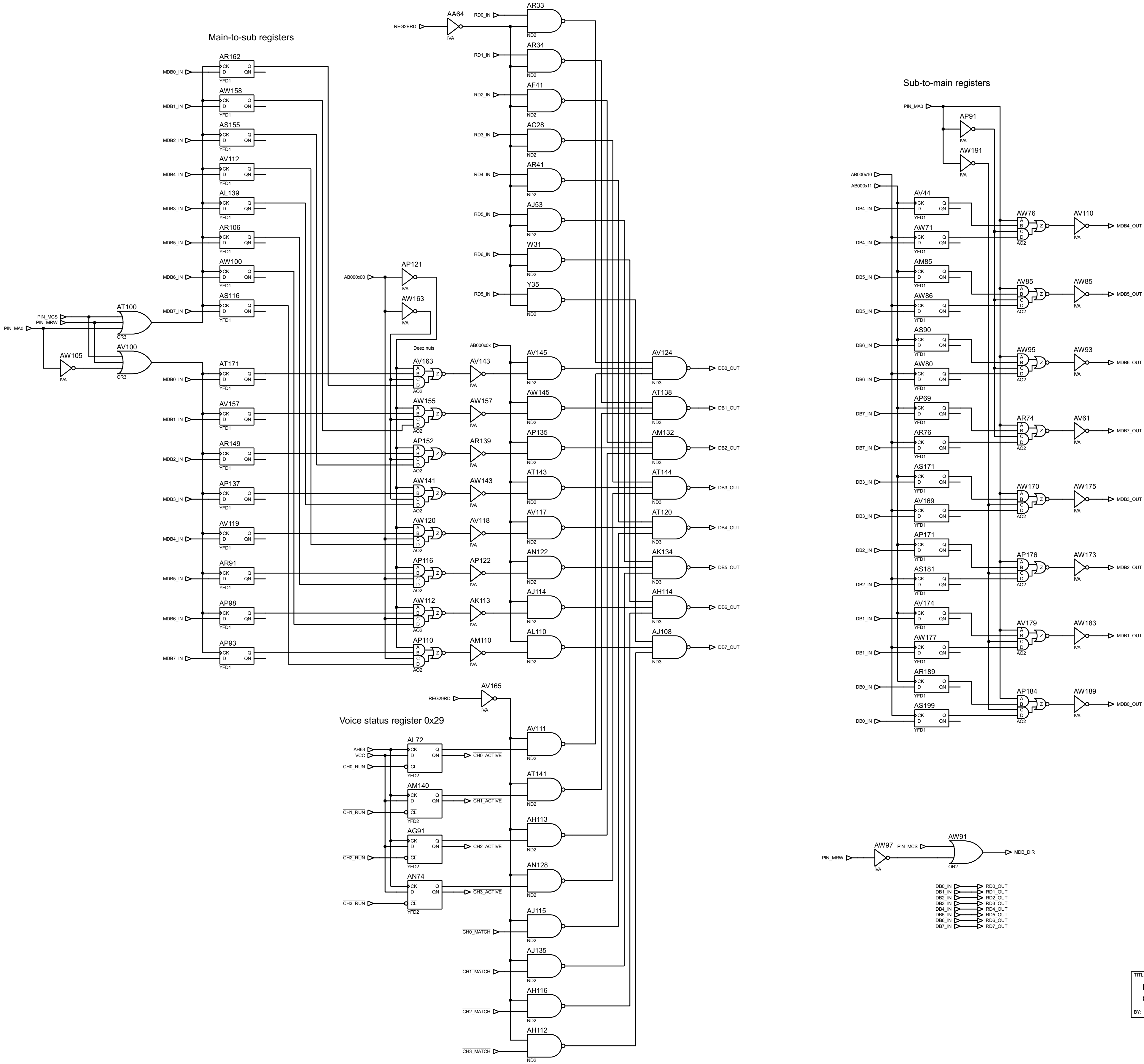
- 0: Bypass counters
- 1: ROM address mux select
- 2: Multiplier input select
- 3: Clock related
- 4: Enable channel selection
- 5: Channel select A
- 6: Channel select B
- 7: Clock for some ROM addr

TITLE:		DATE:
Konami 053260		22/03/2023
REG 2B		PAGE:
BY: Sean Gonsalves	REV: A	5/34



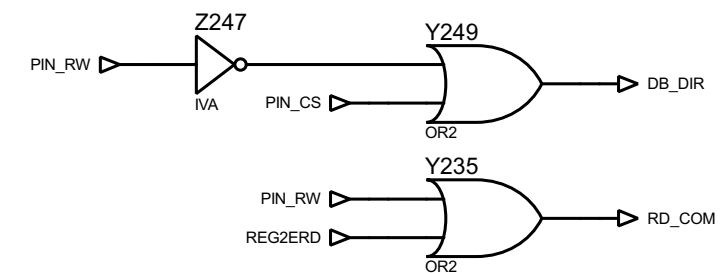
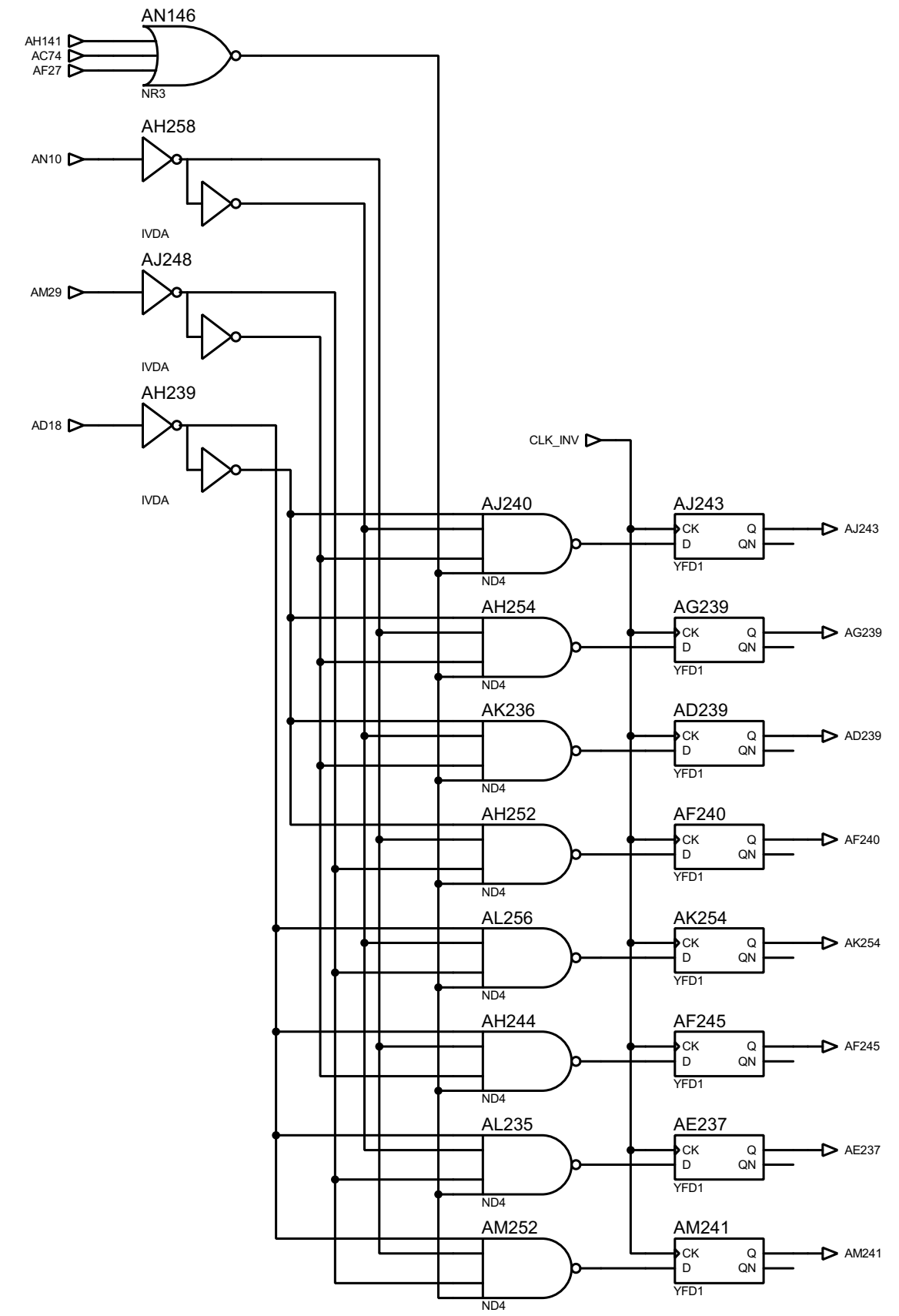
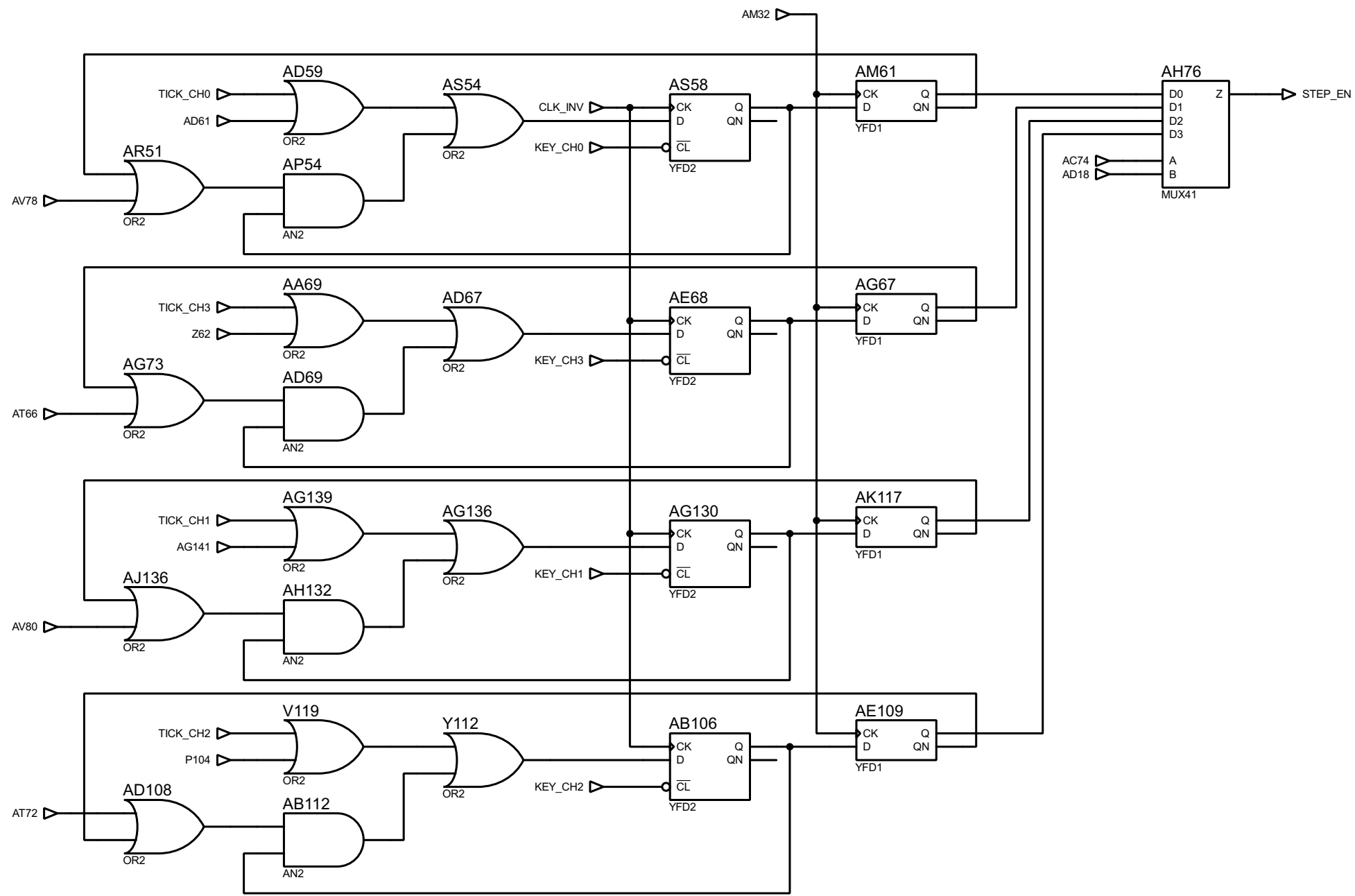
TITLE: Konami 053260 REG 2F BY: Sean Gonsalves	DATE: 22/03/2023 PAGE: 6/34
REV: A	

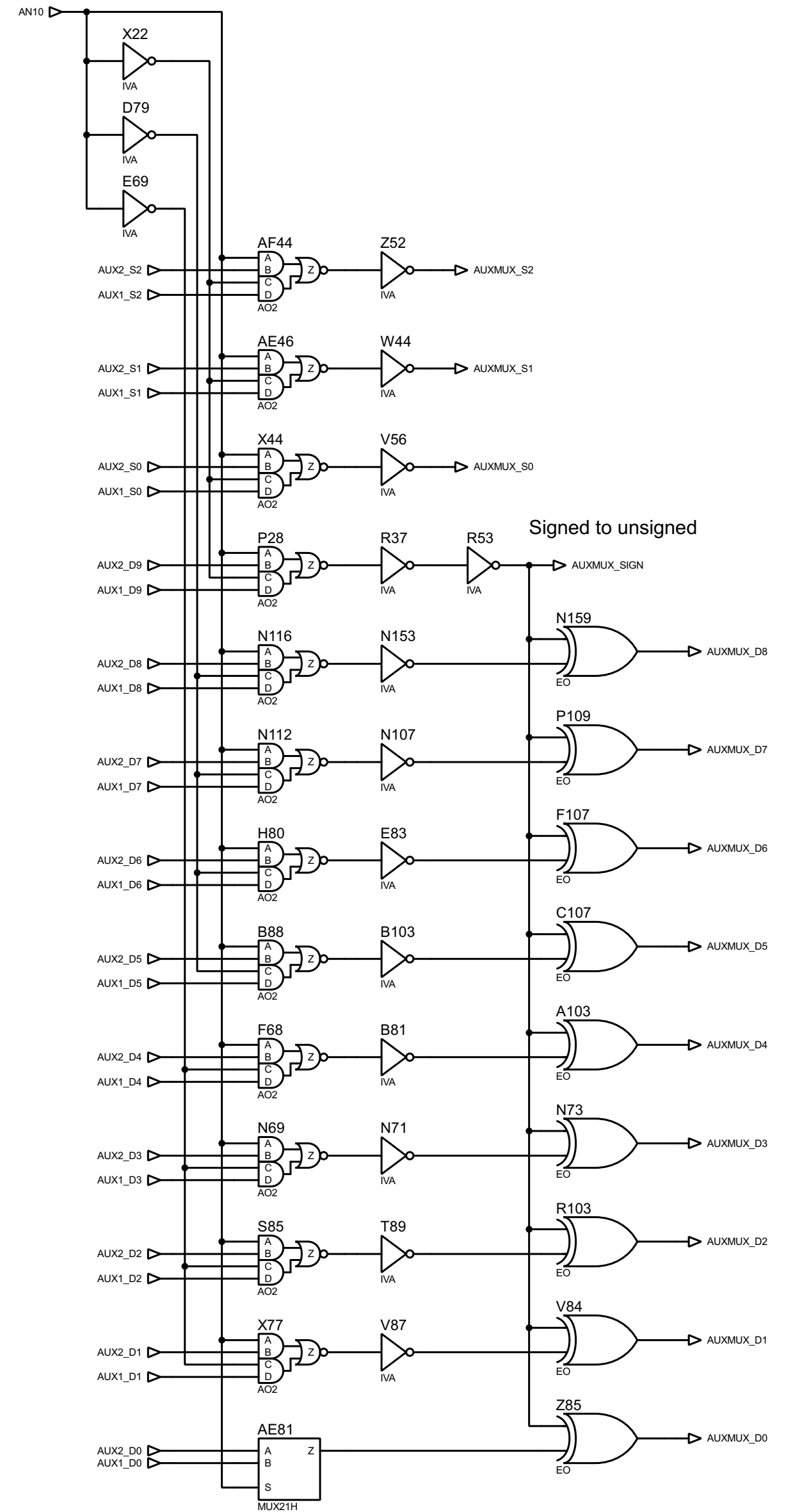
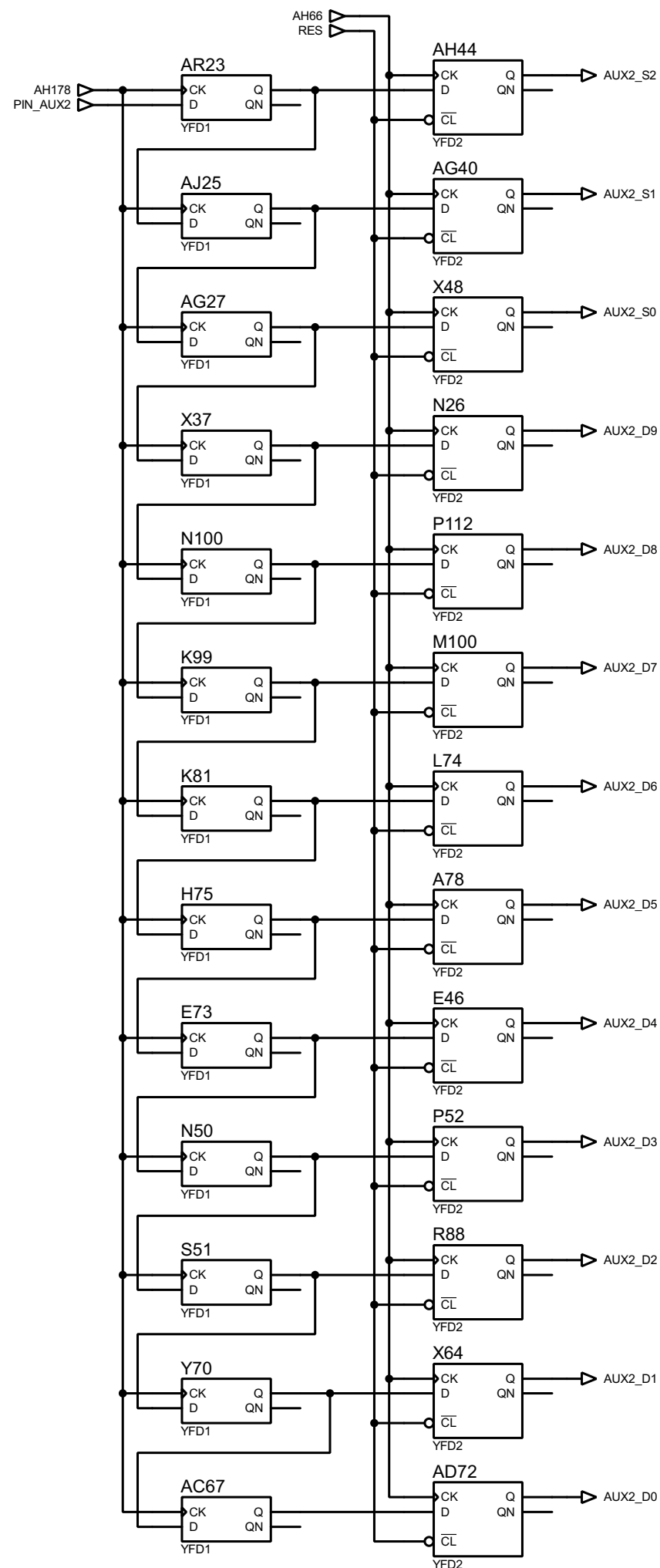
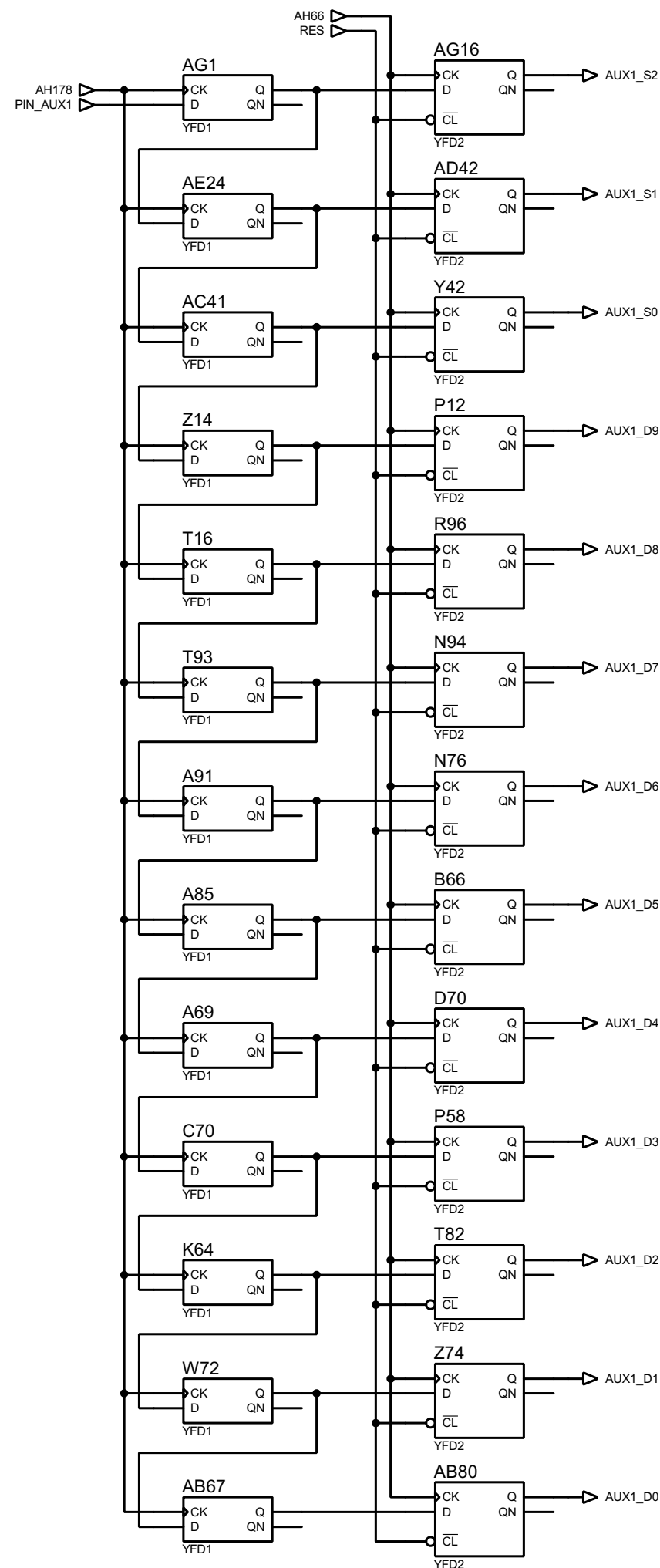
Sample ROM to sub CPU readback

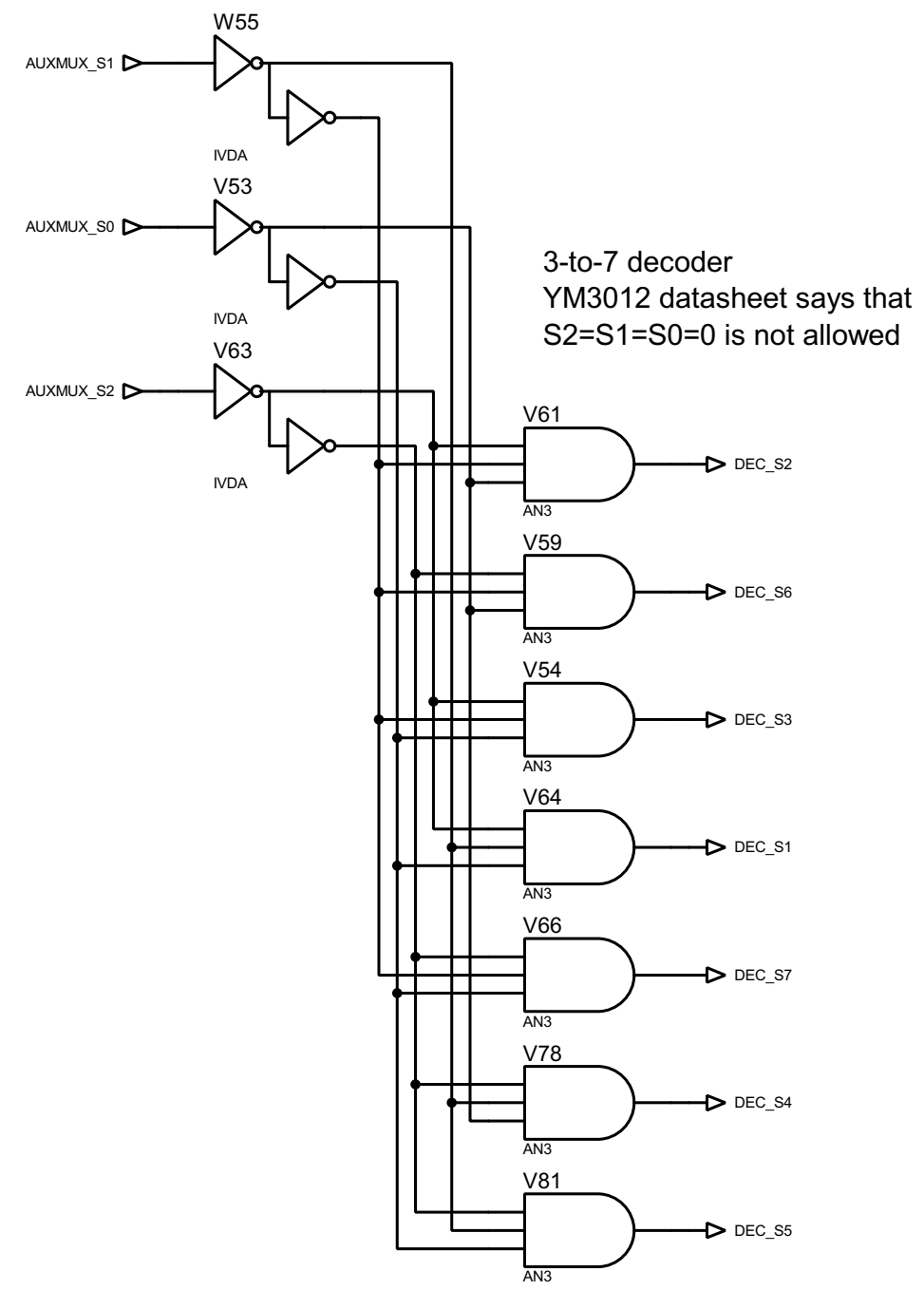




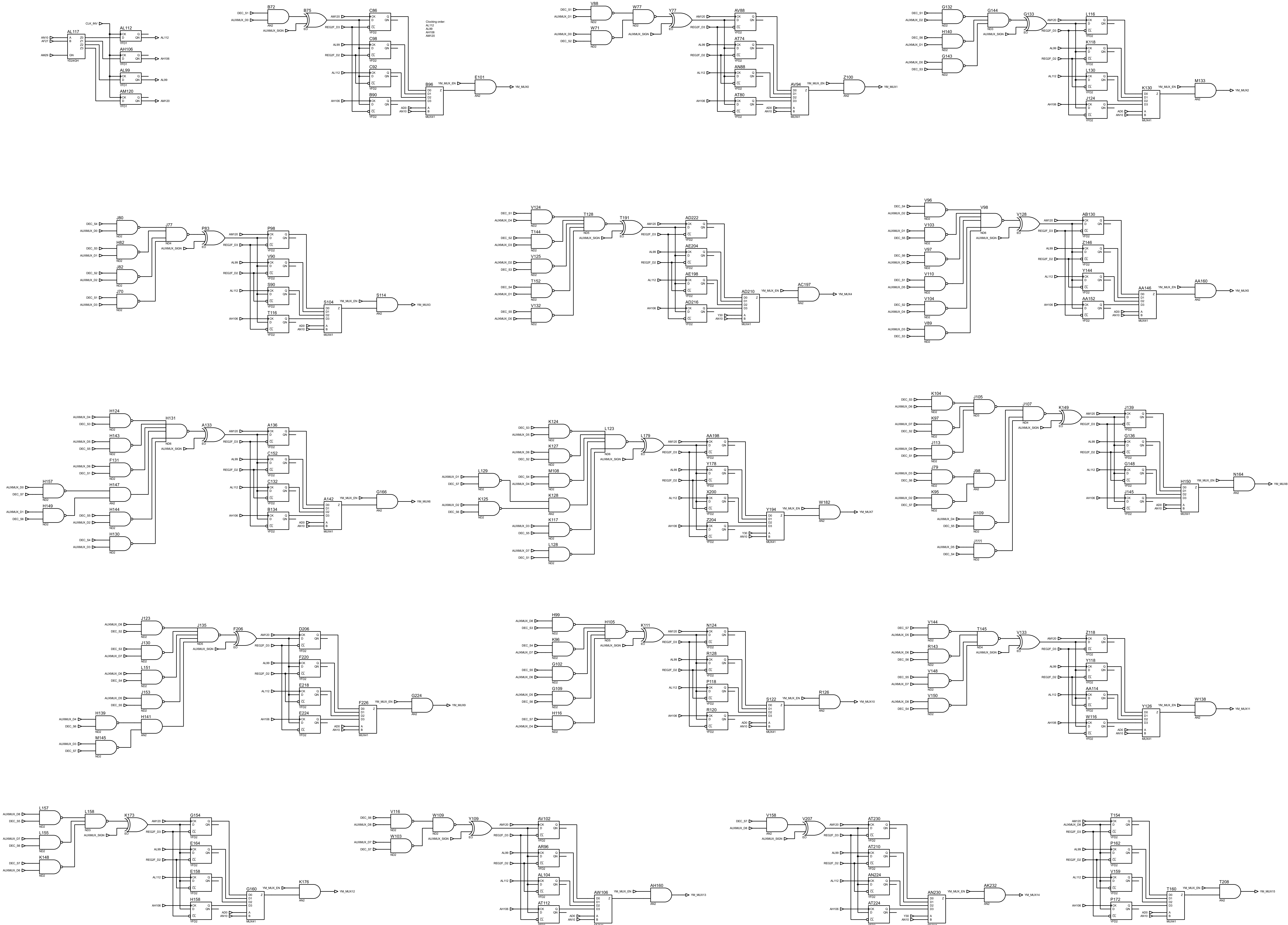


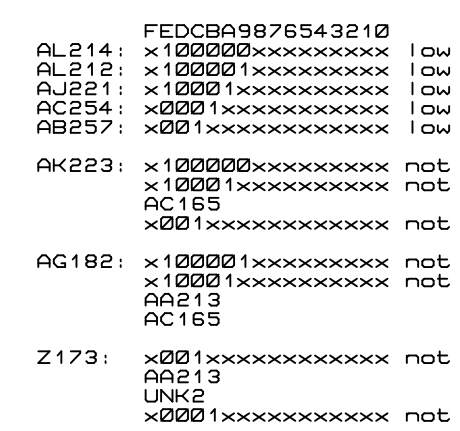
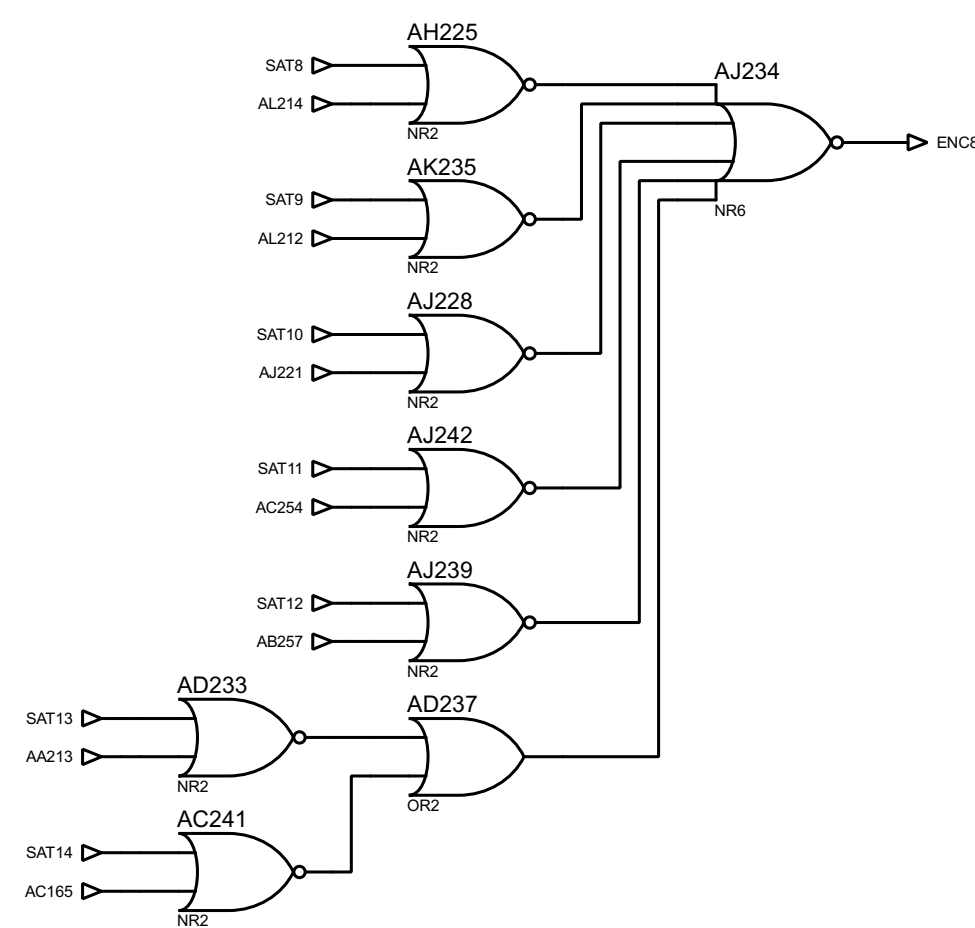
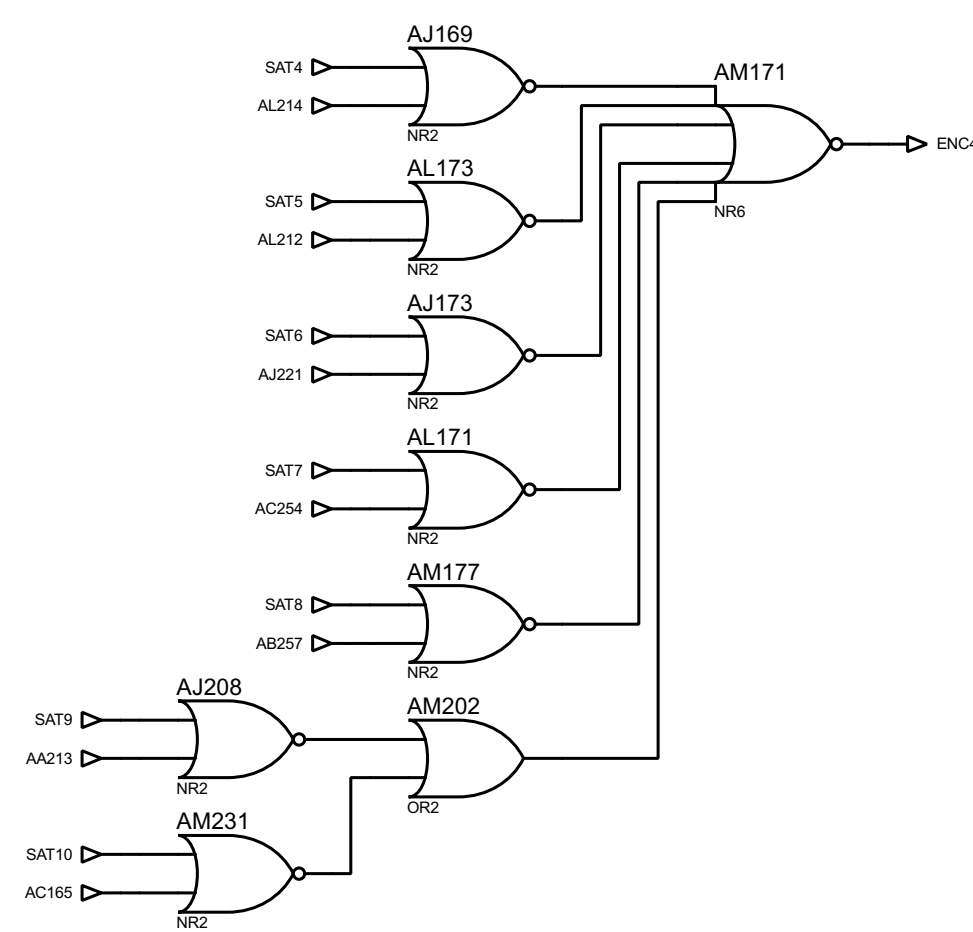


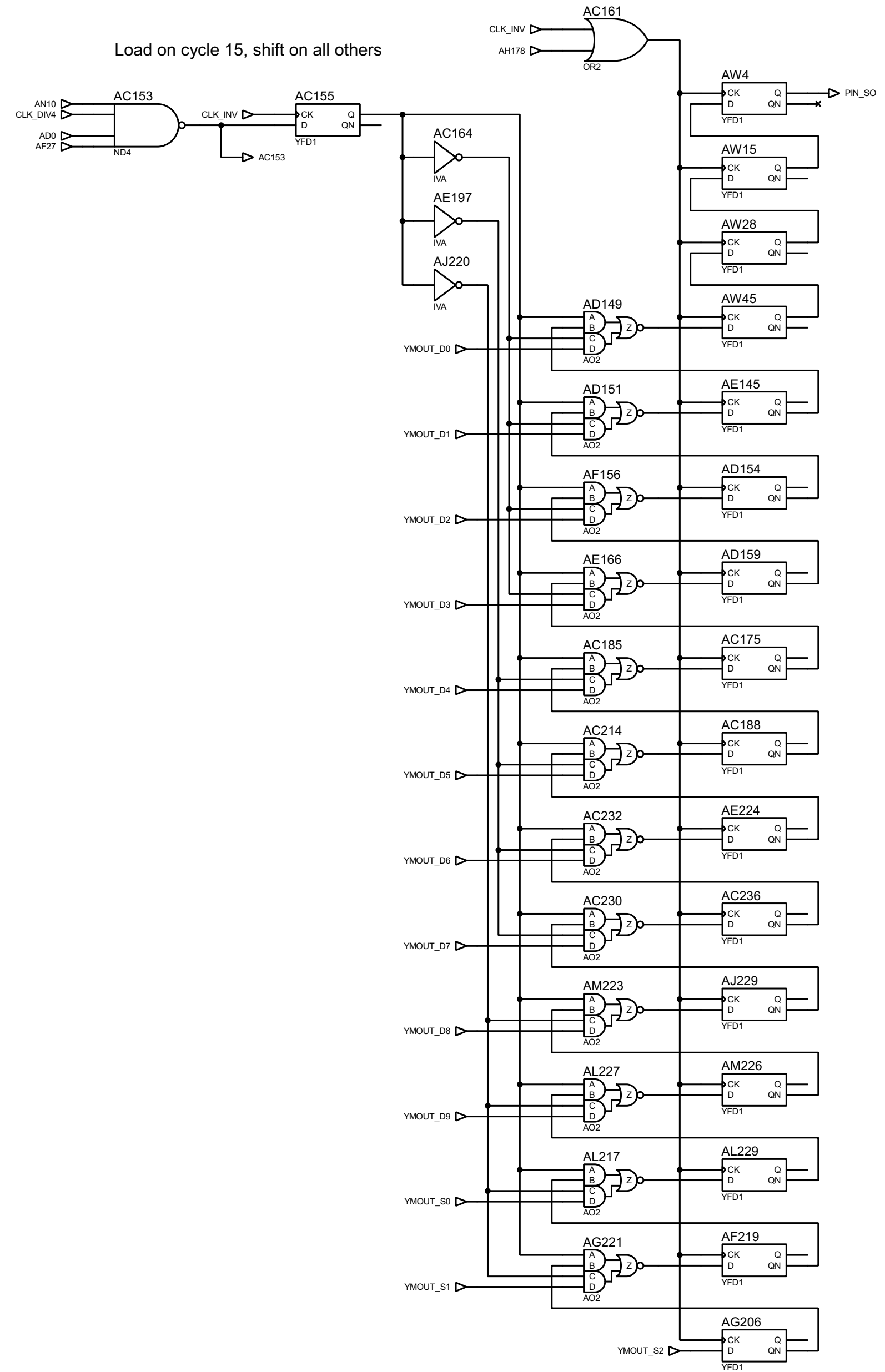
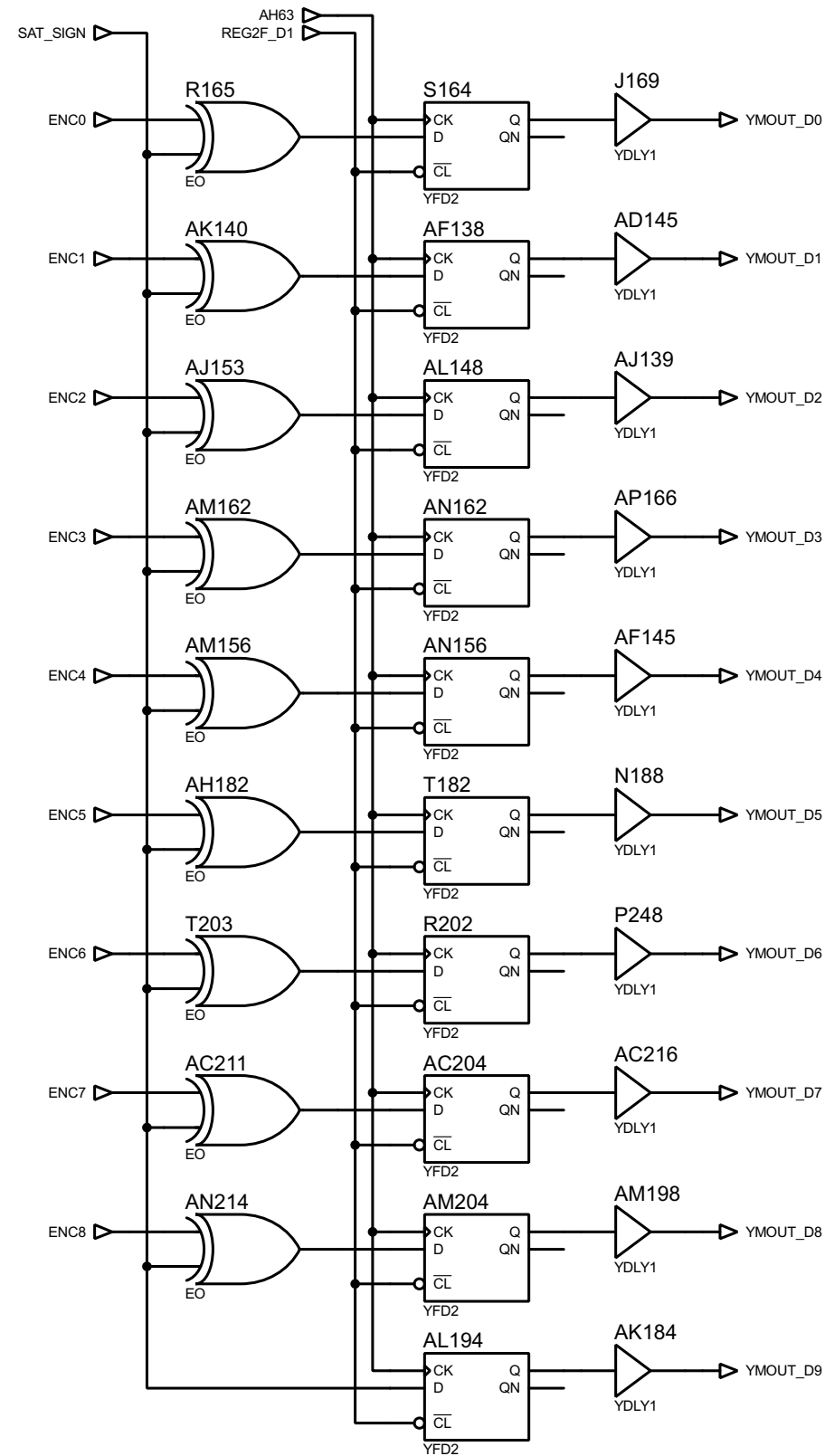


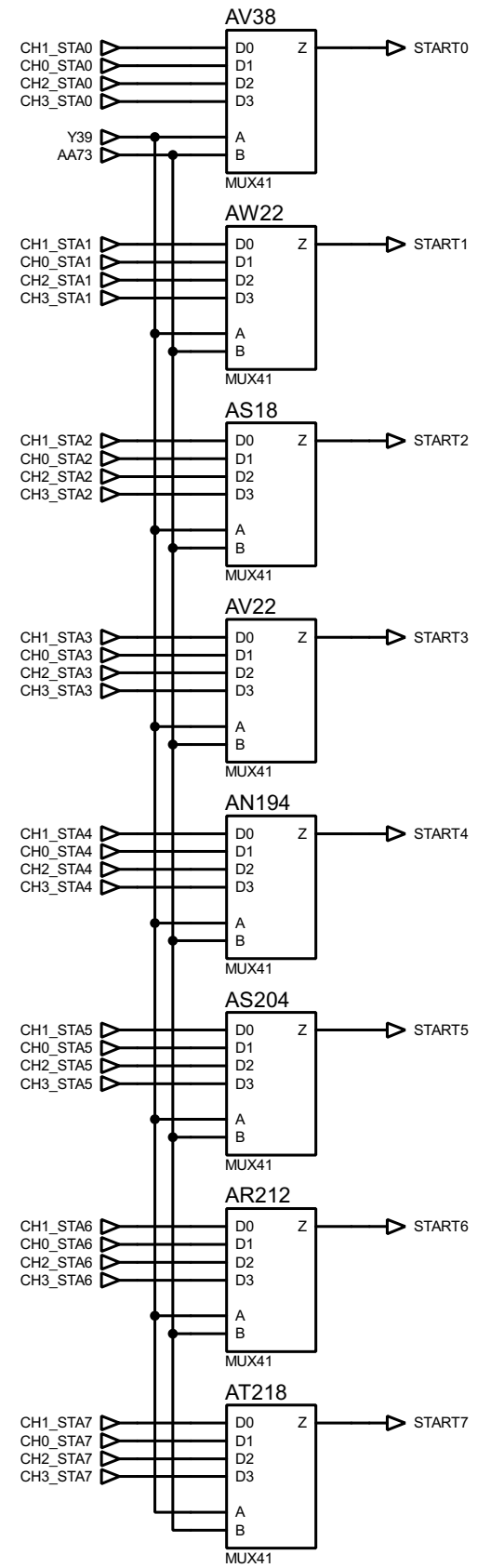
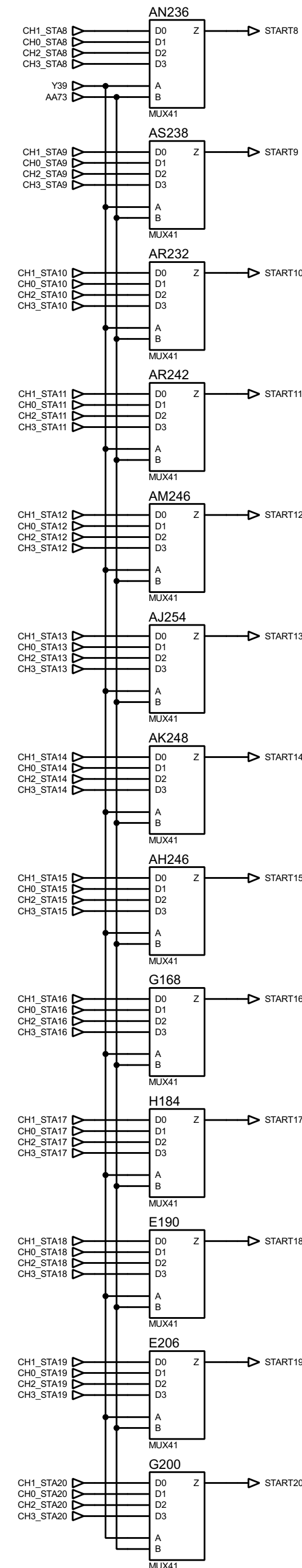
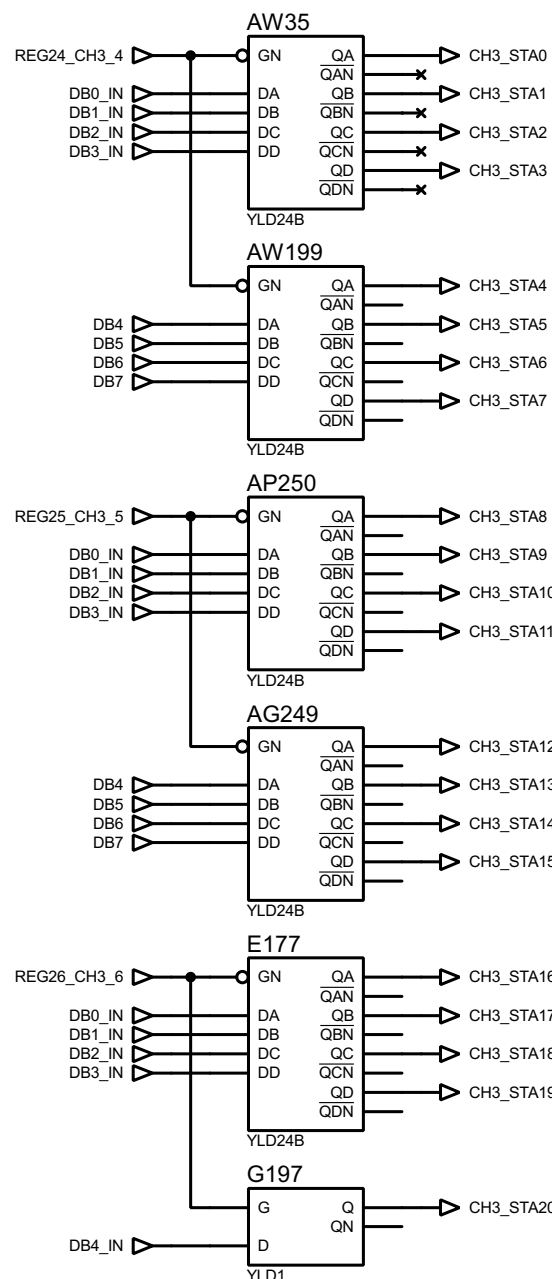
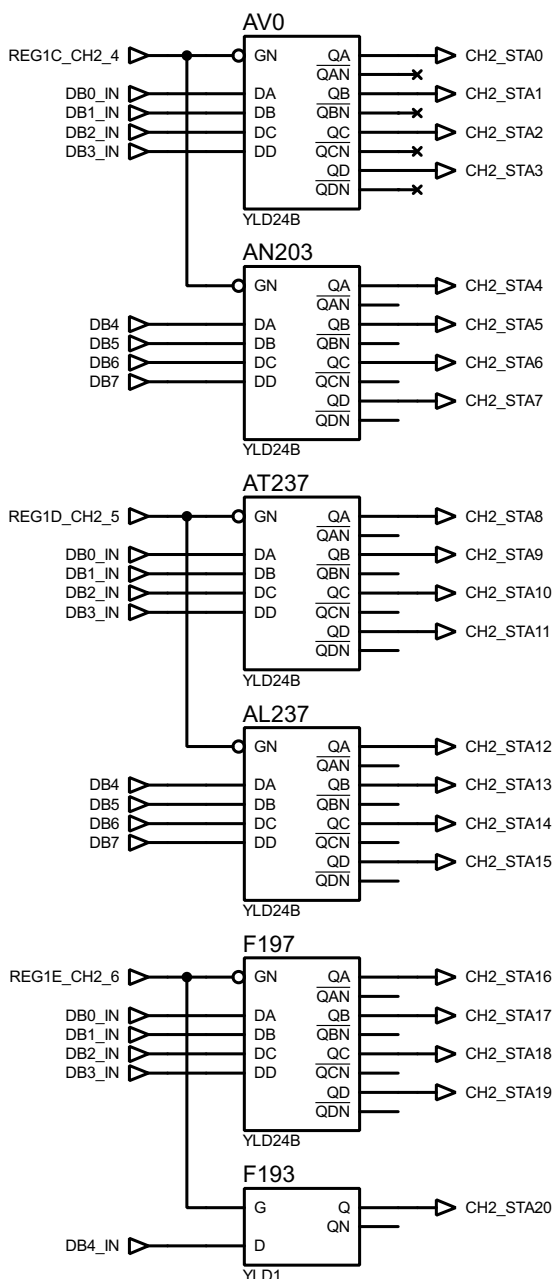
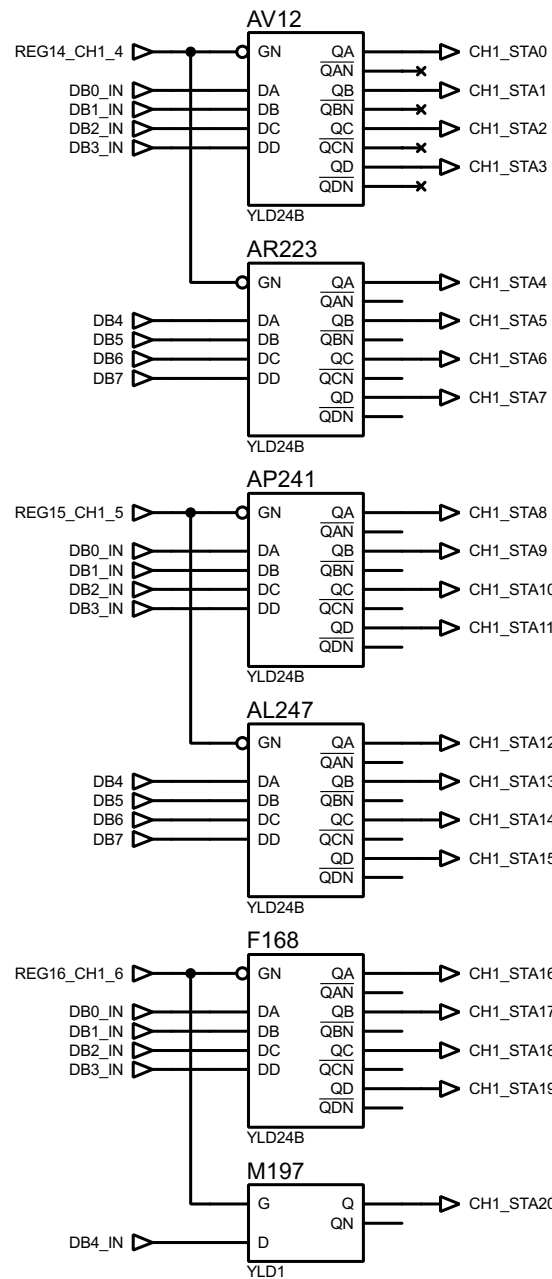
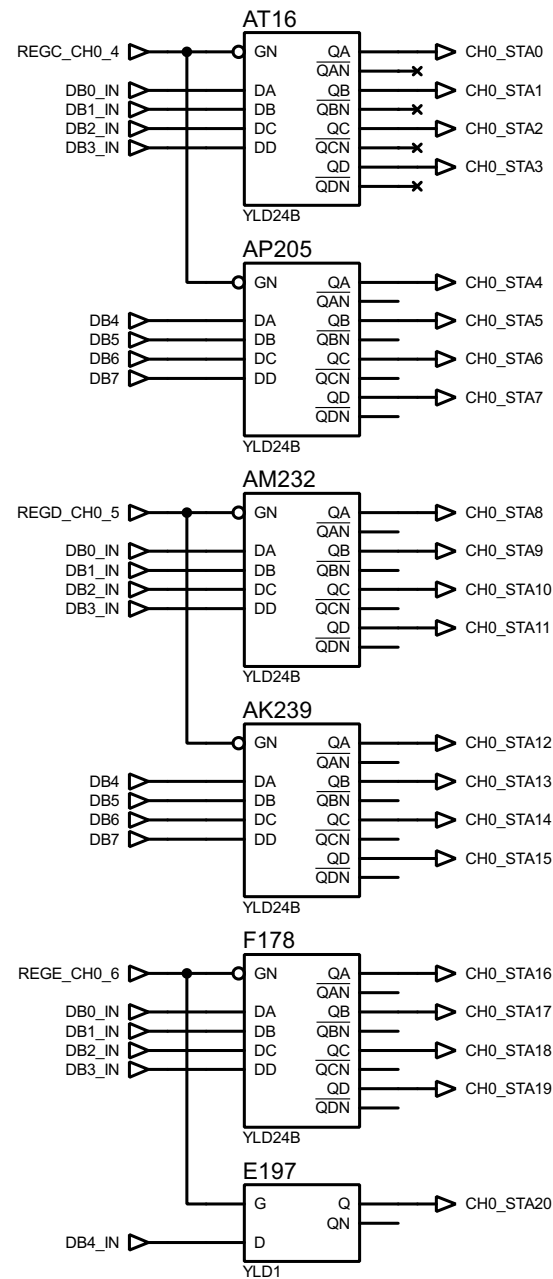


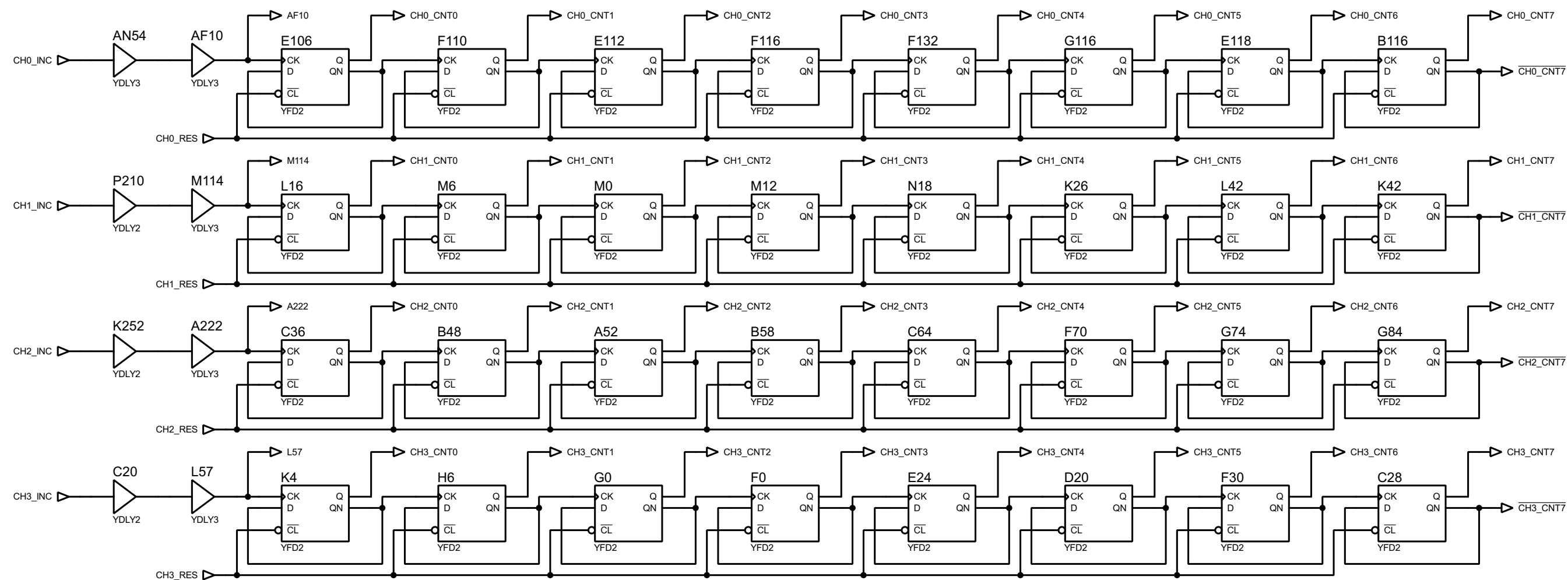
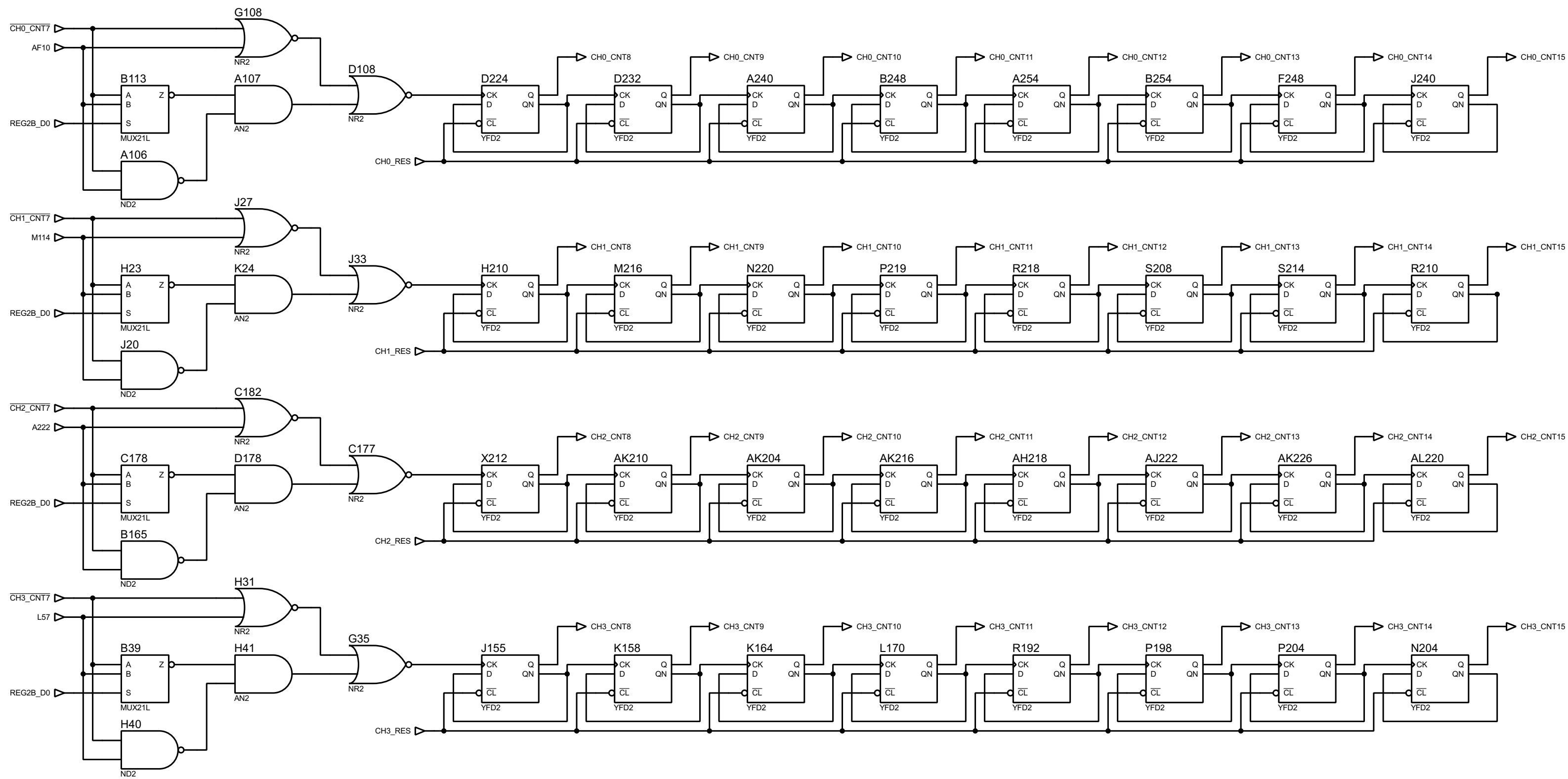
Muxes used to select AUX1/AUX2 and L/R channels ?





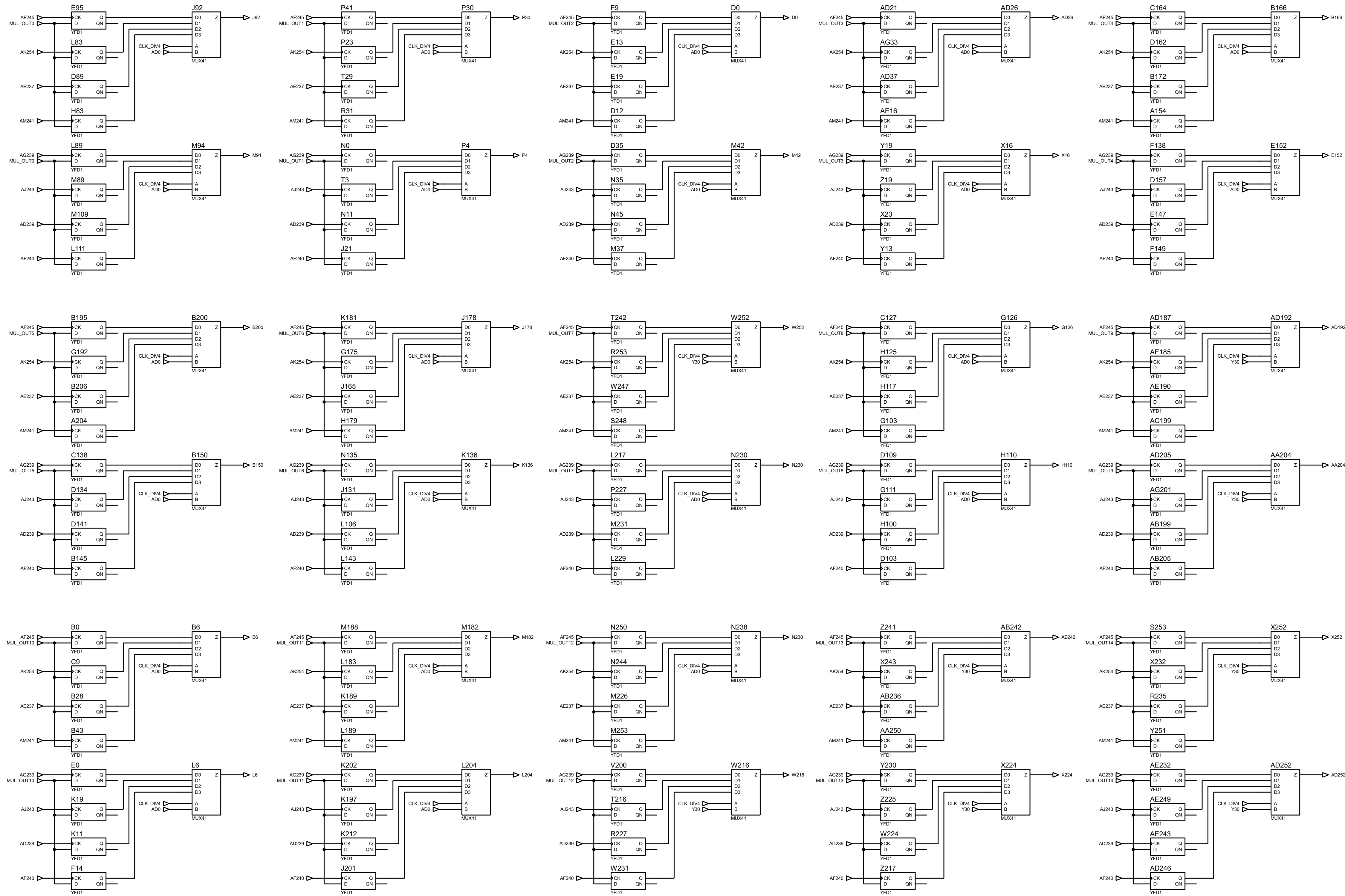


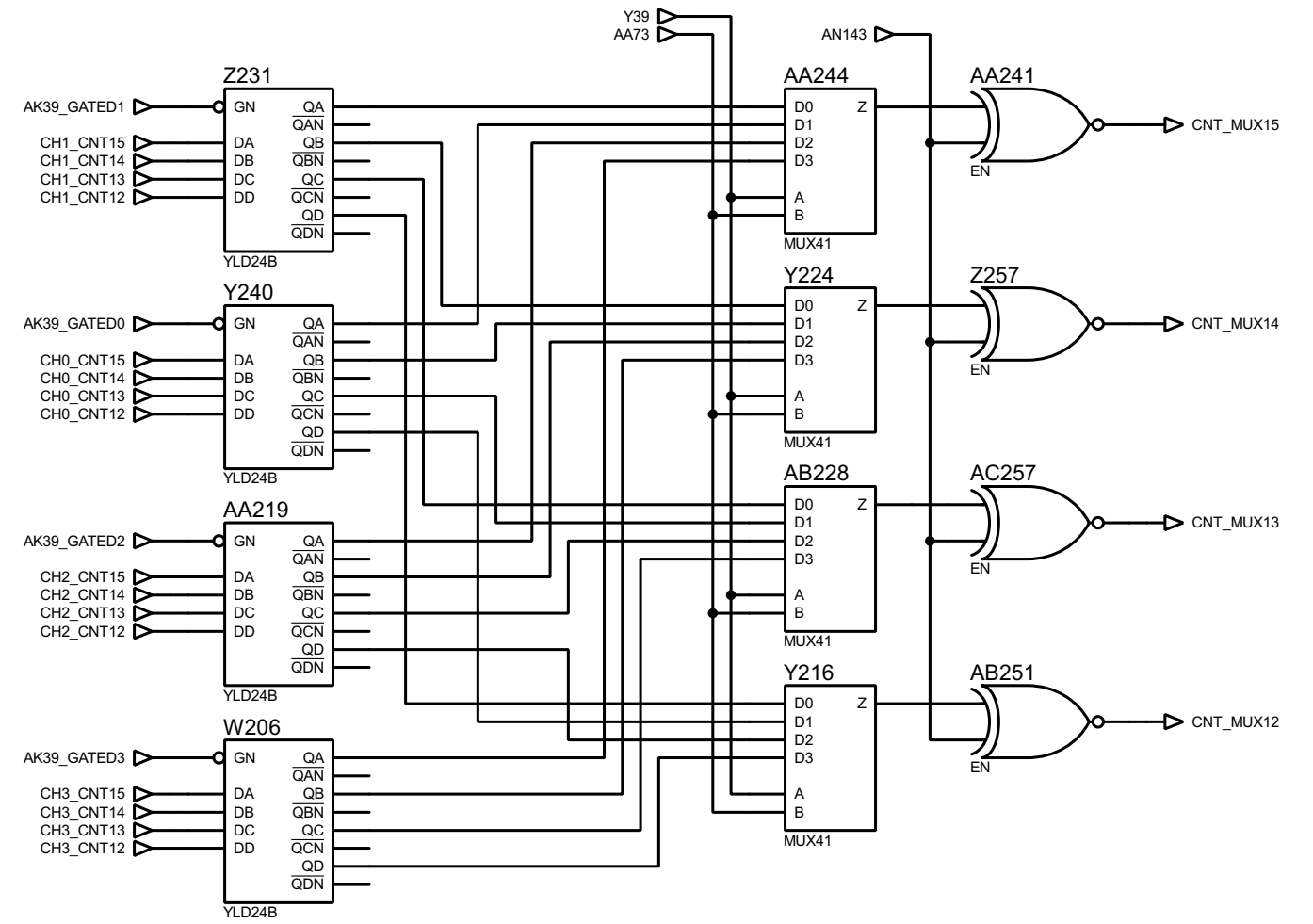
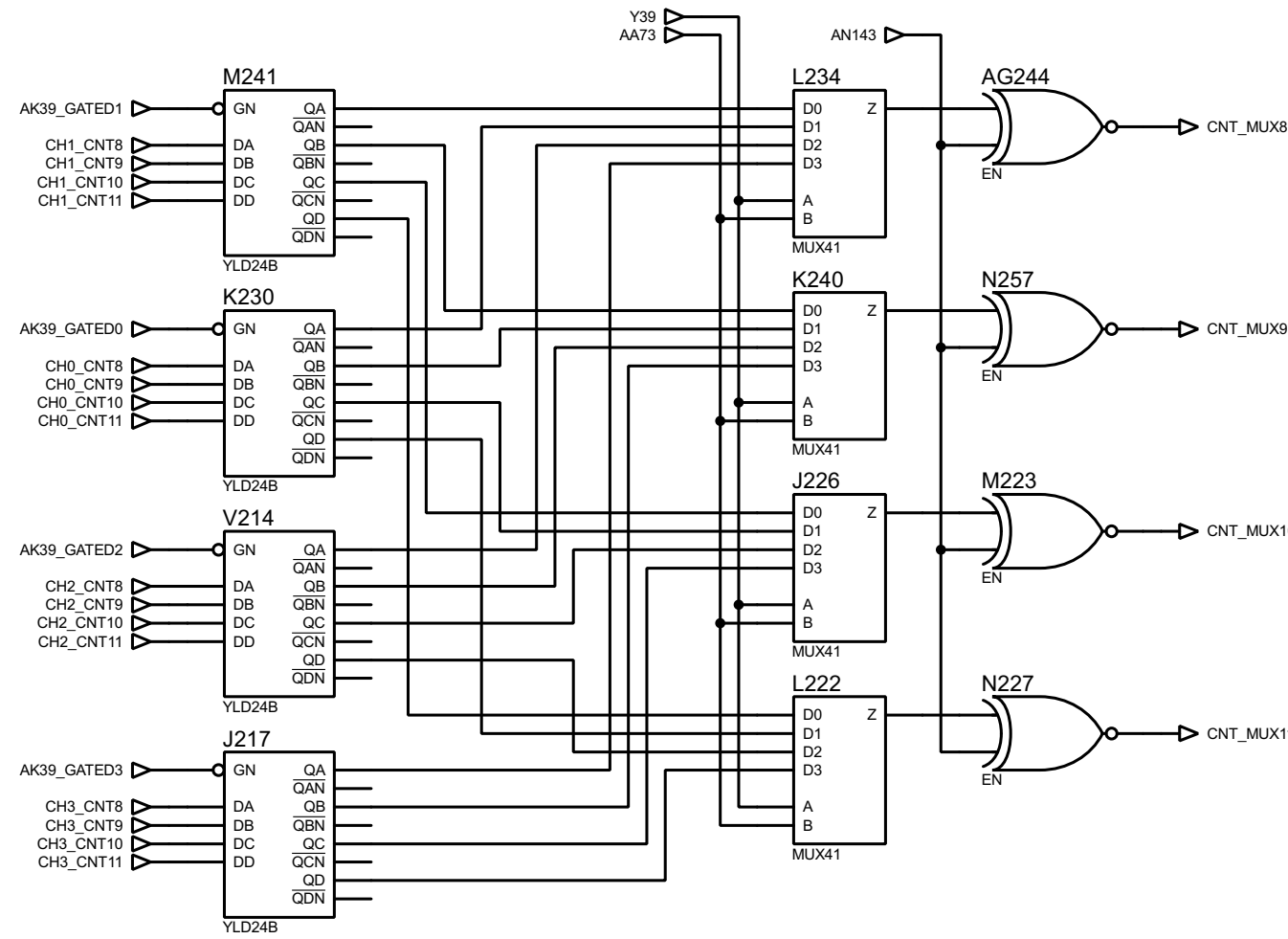
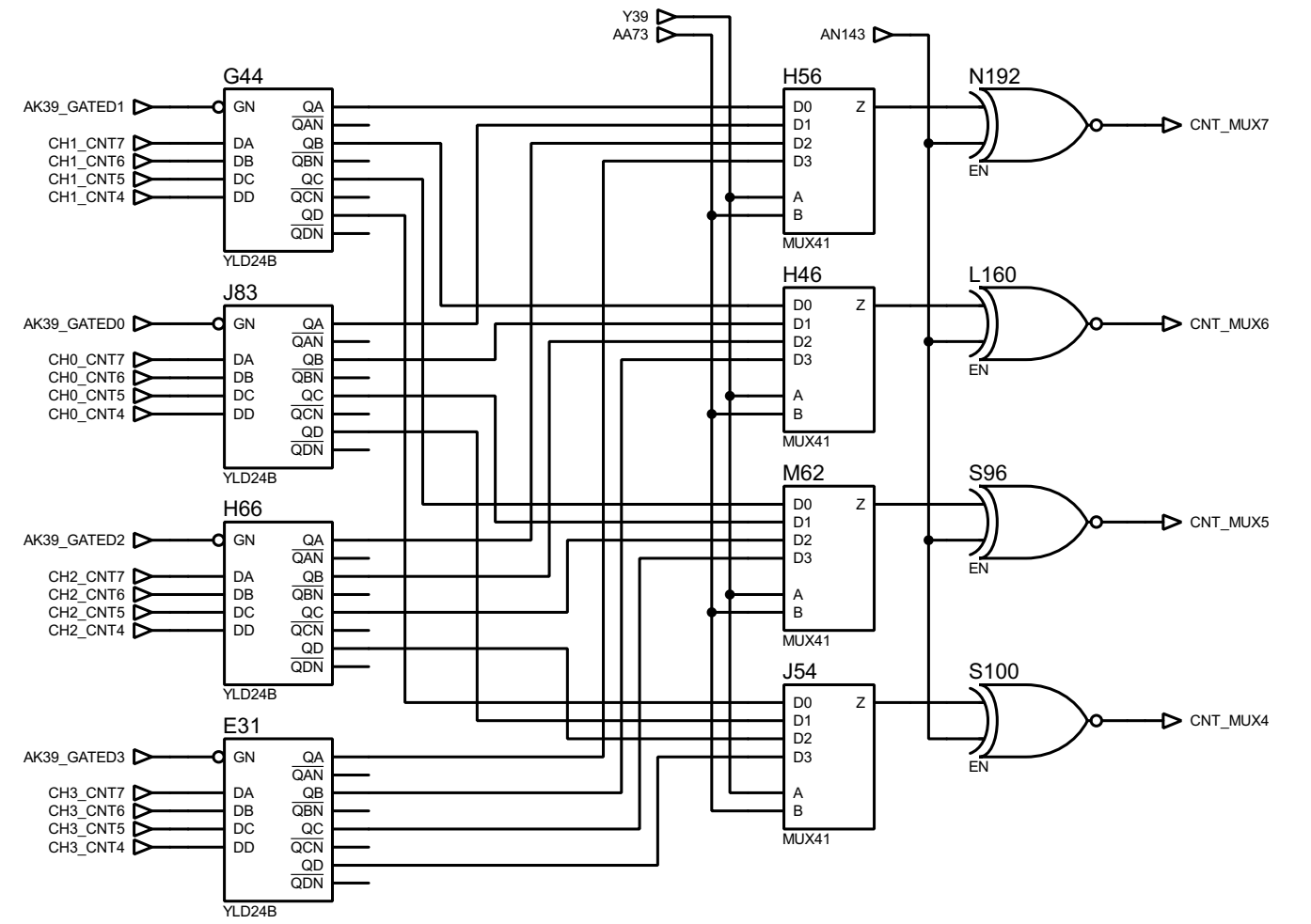
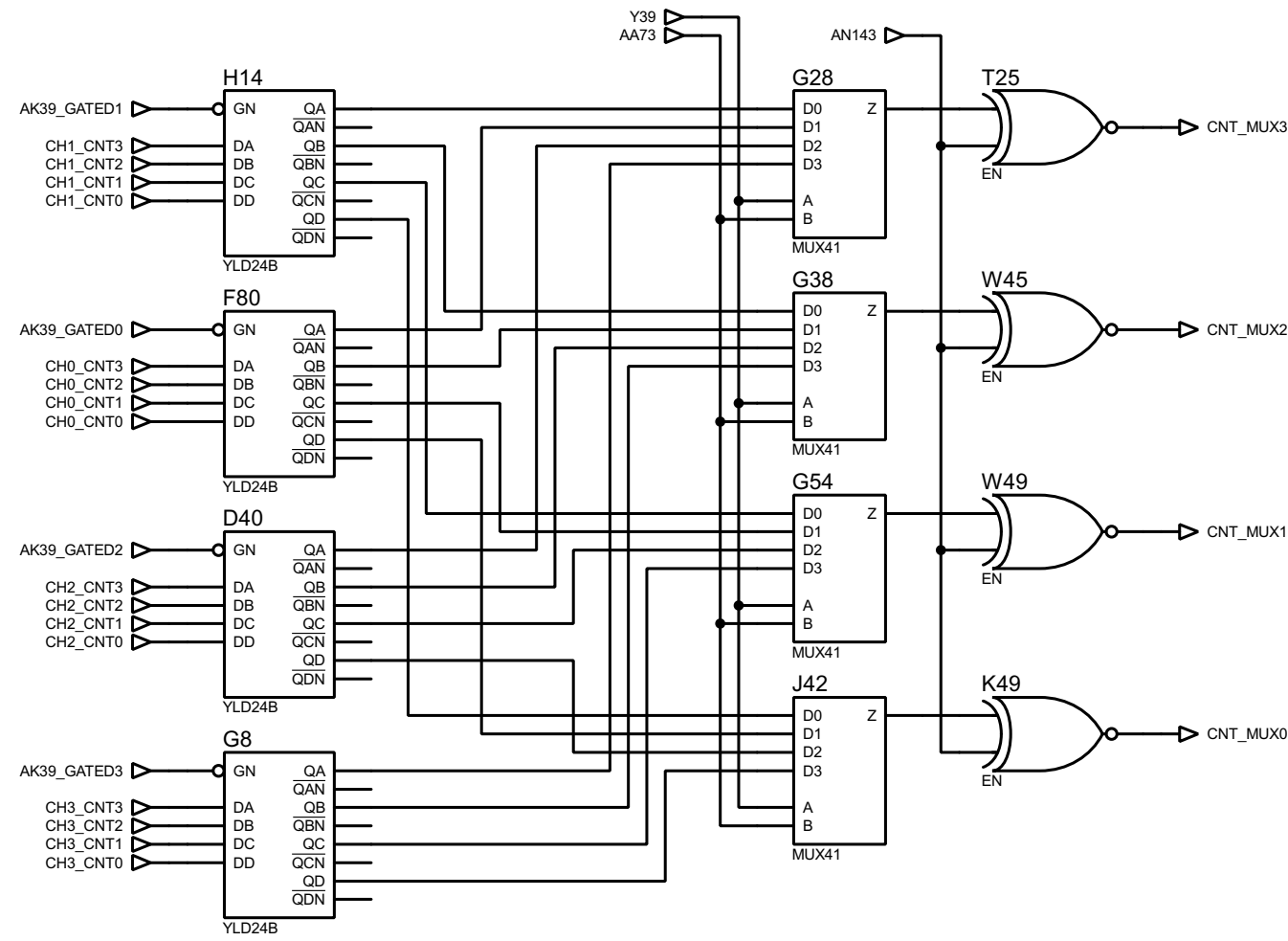
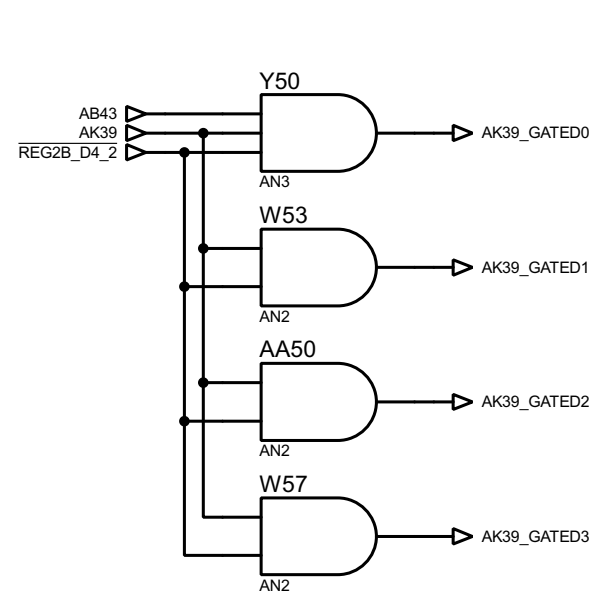


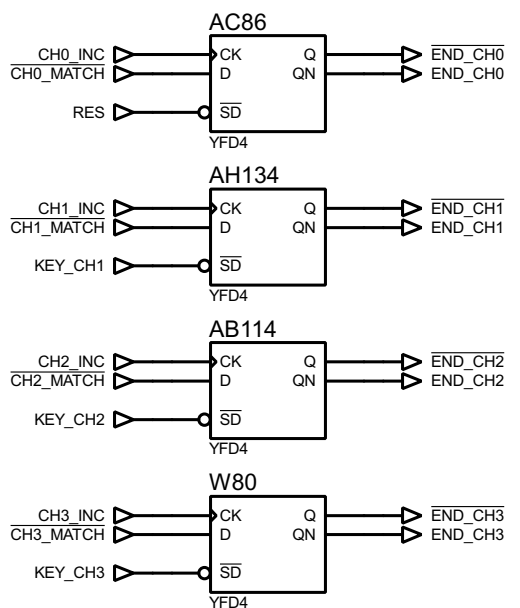
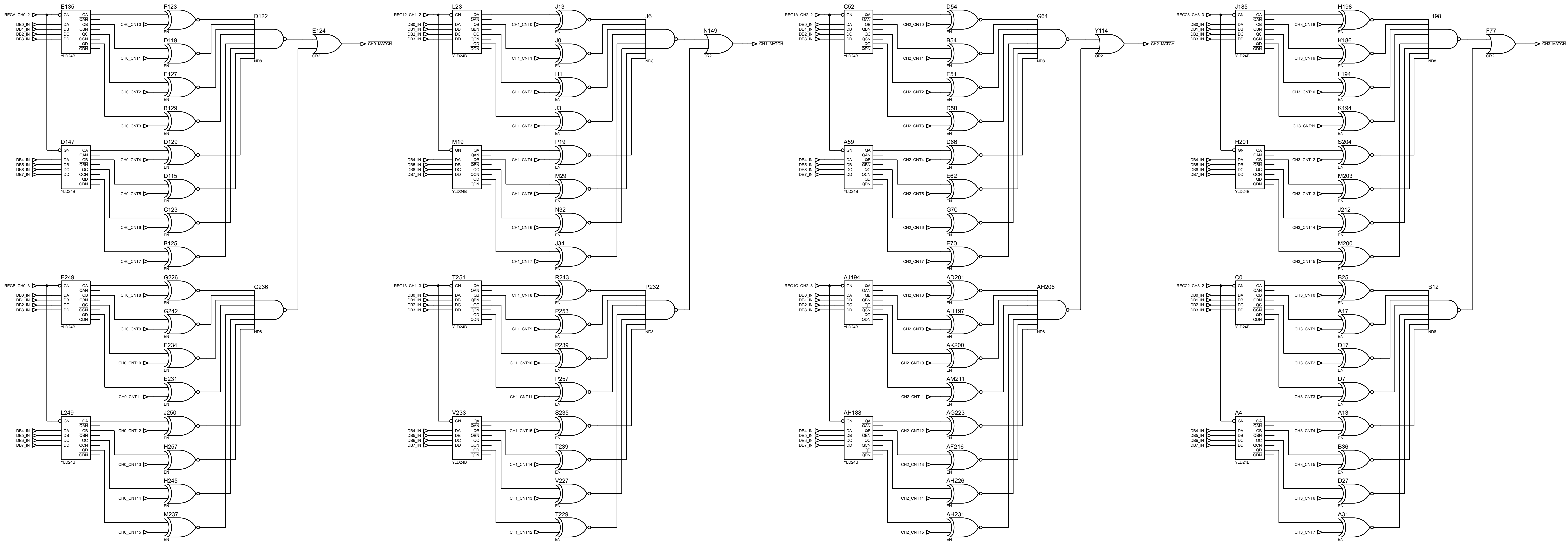


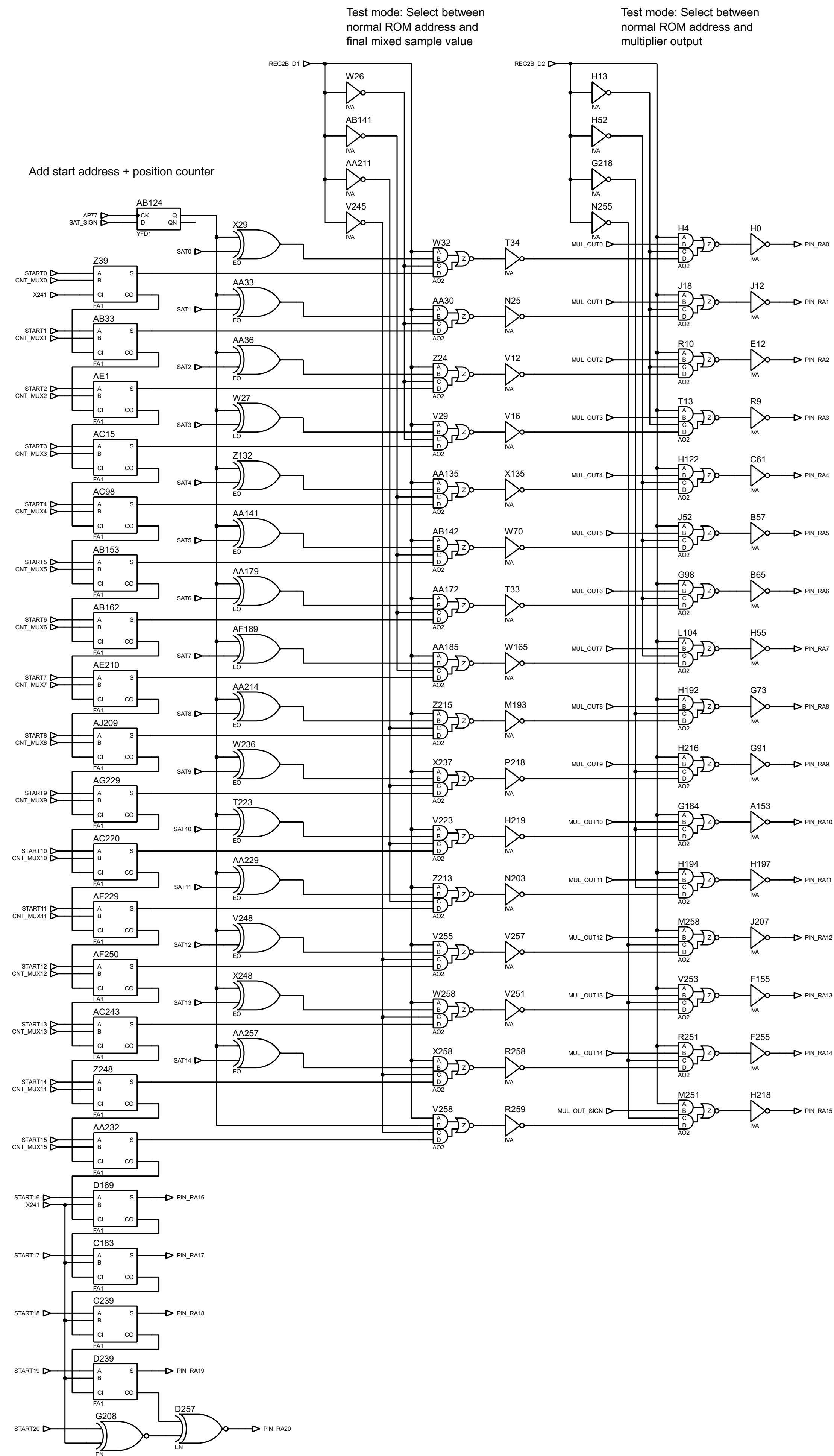
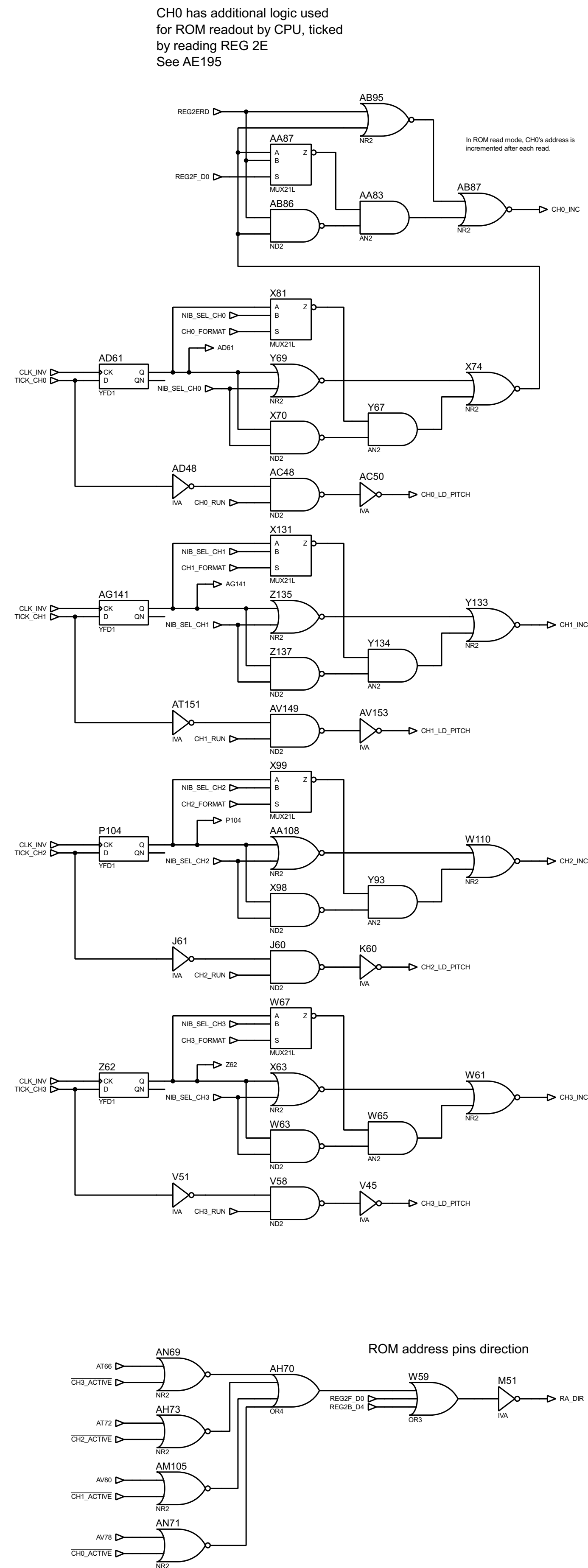


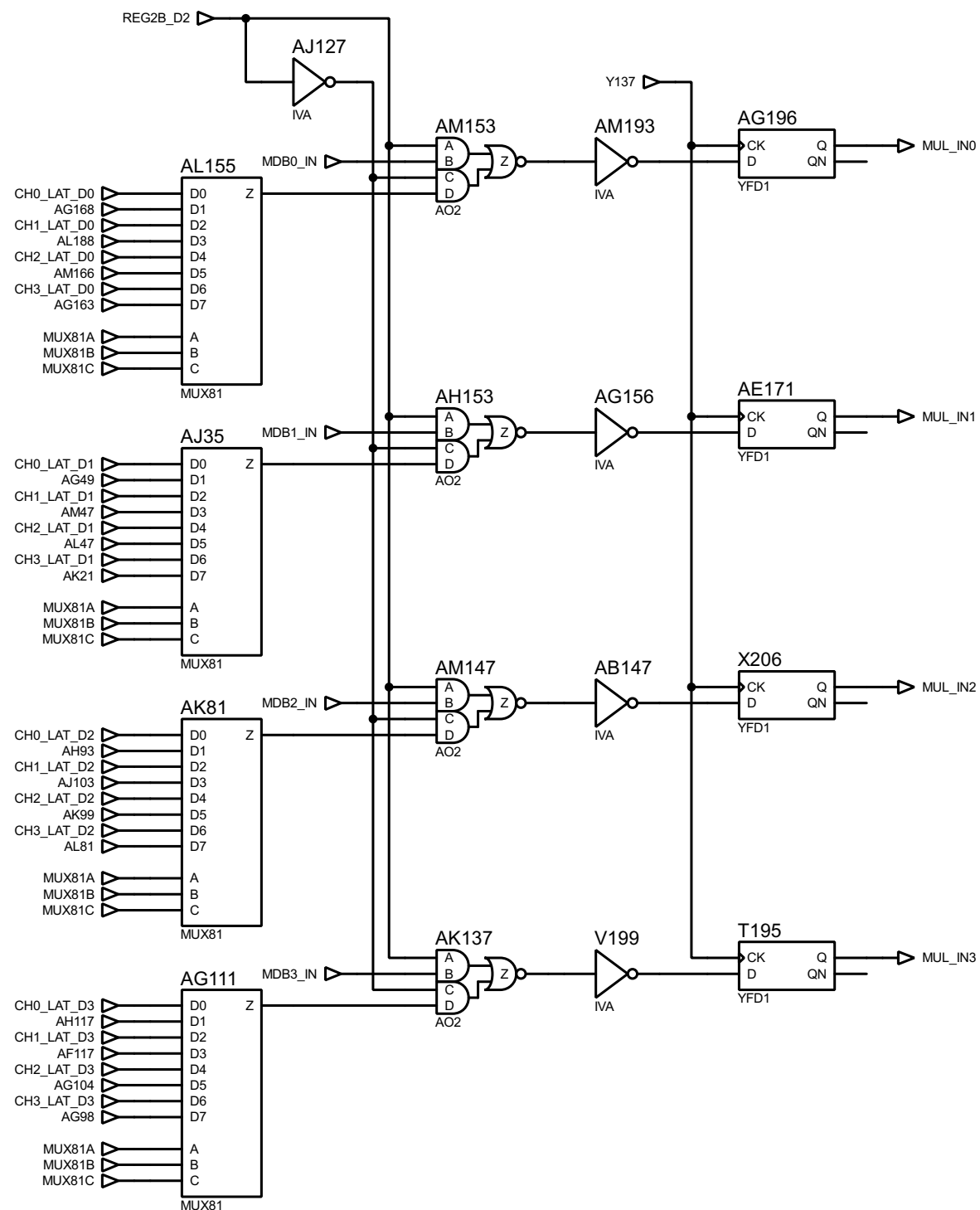
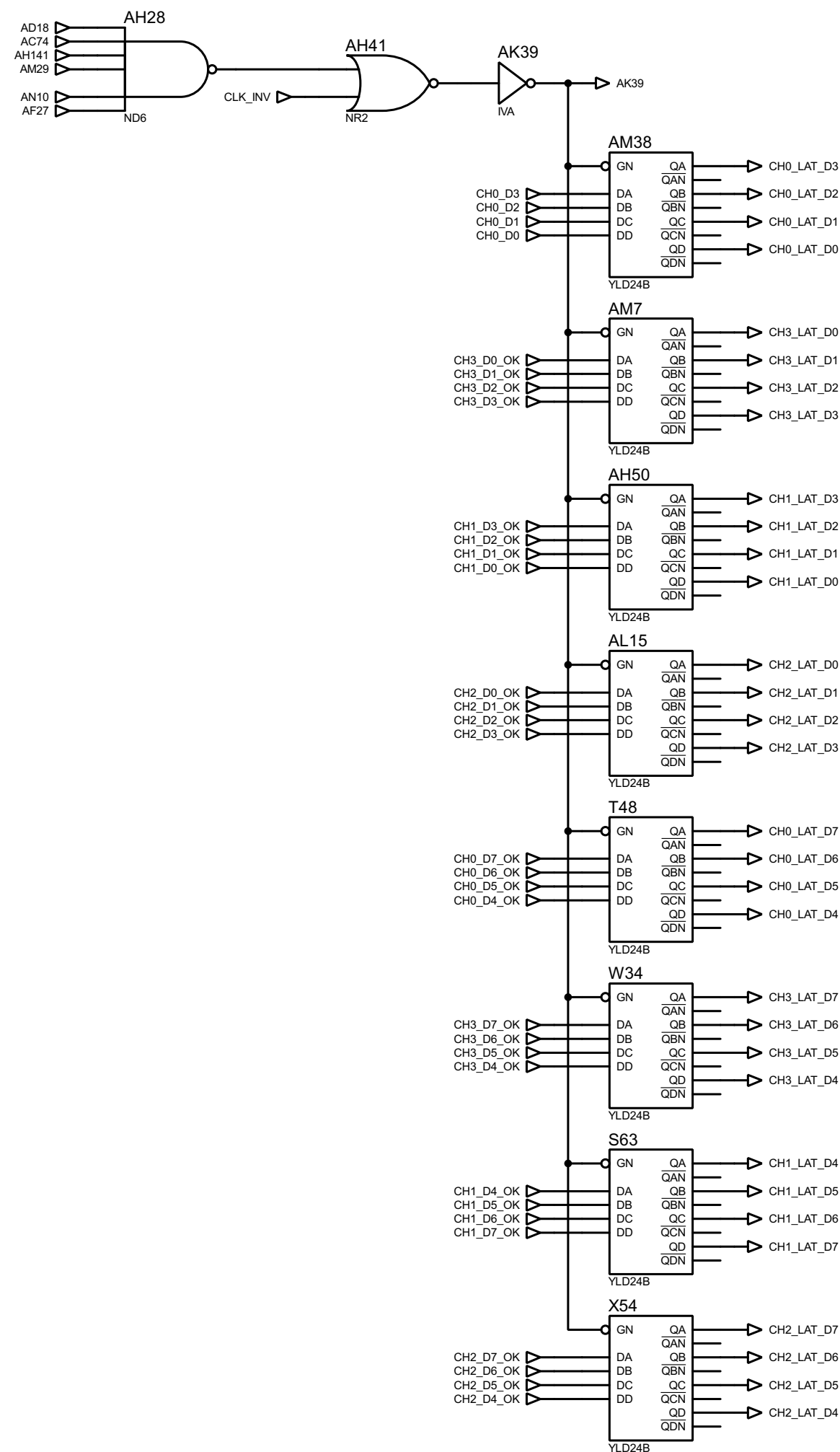
16 bits for 4 channels in stereo



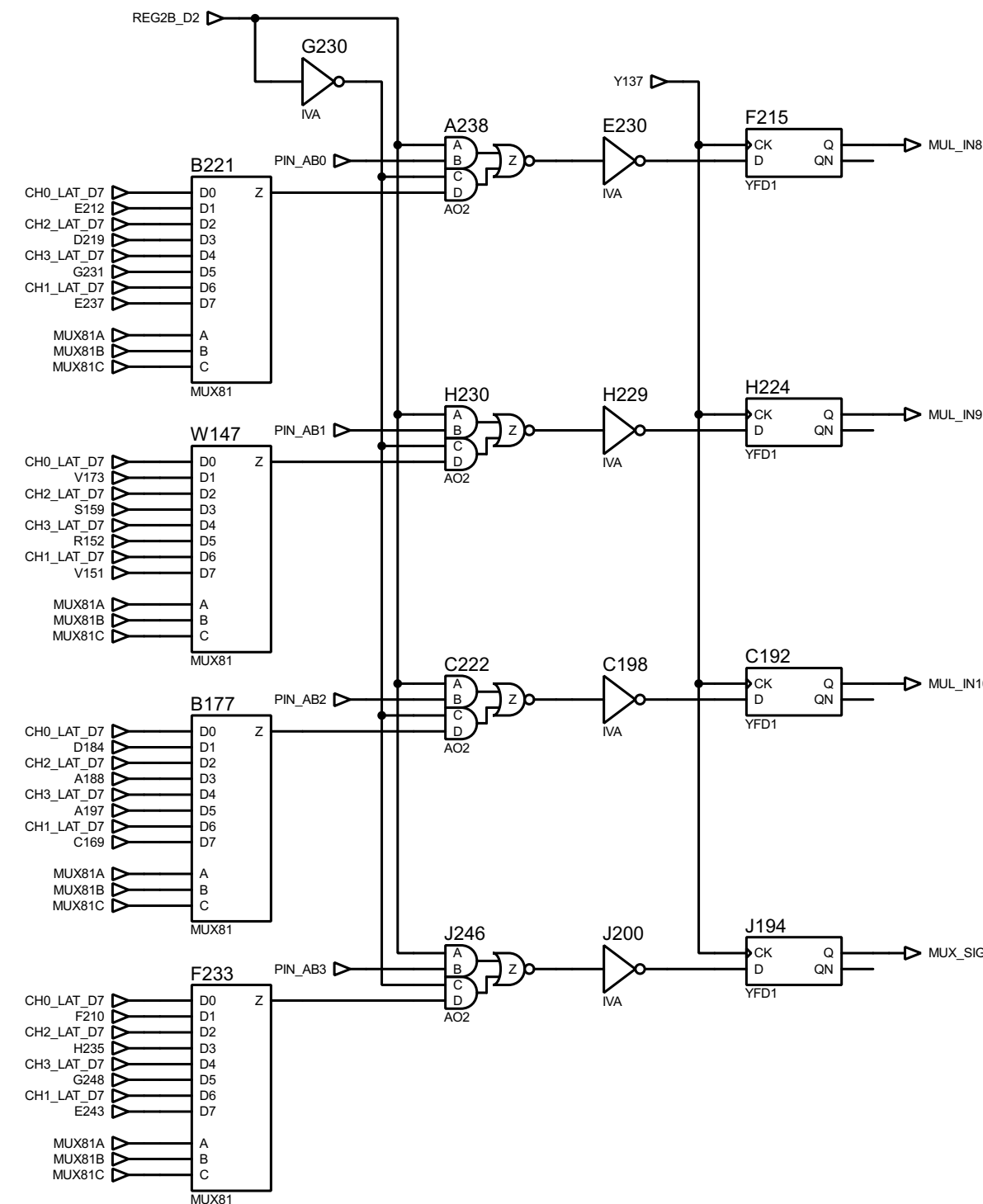
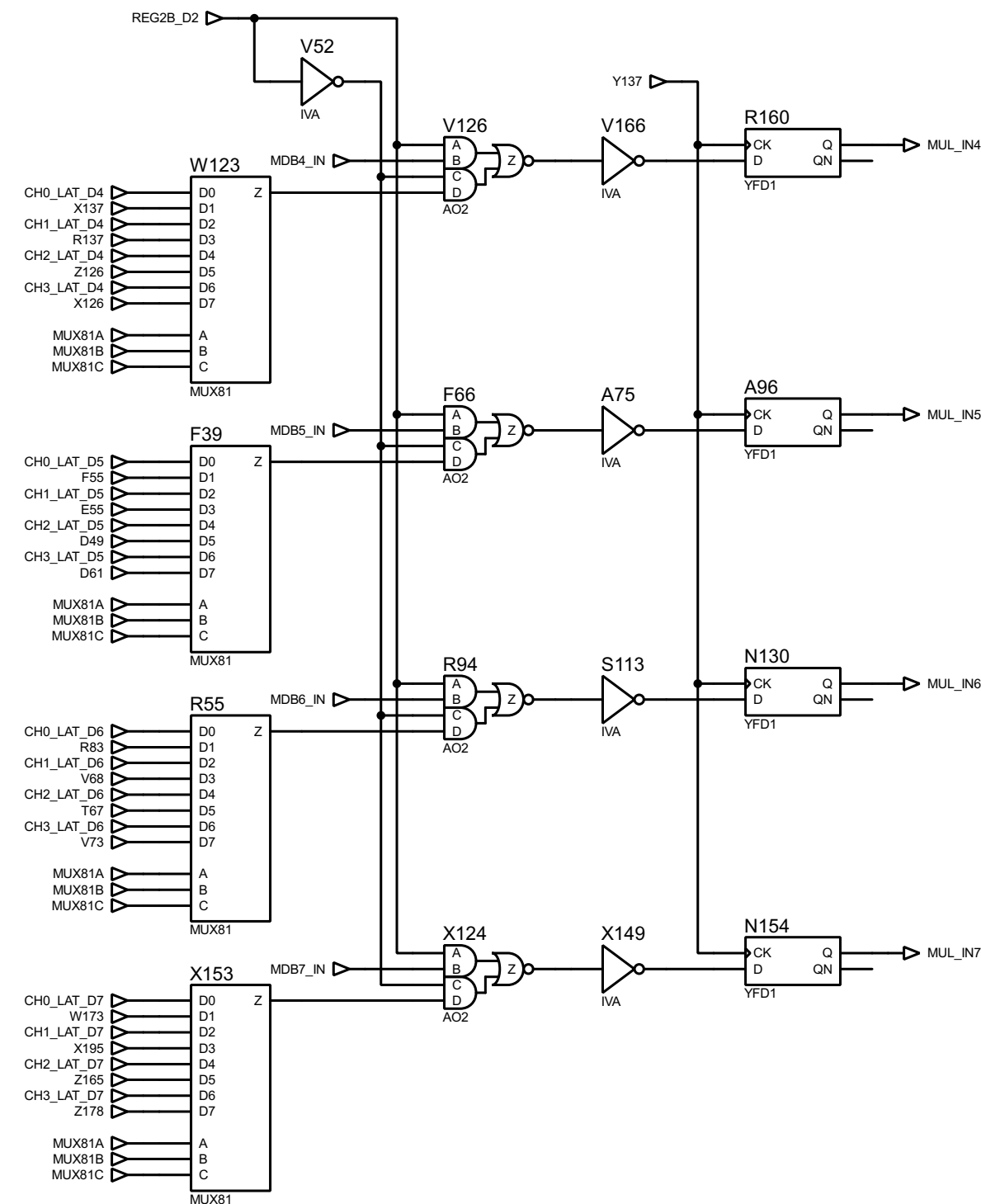




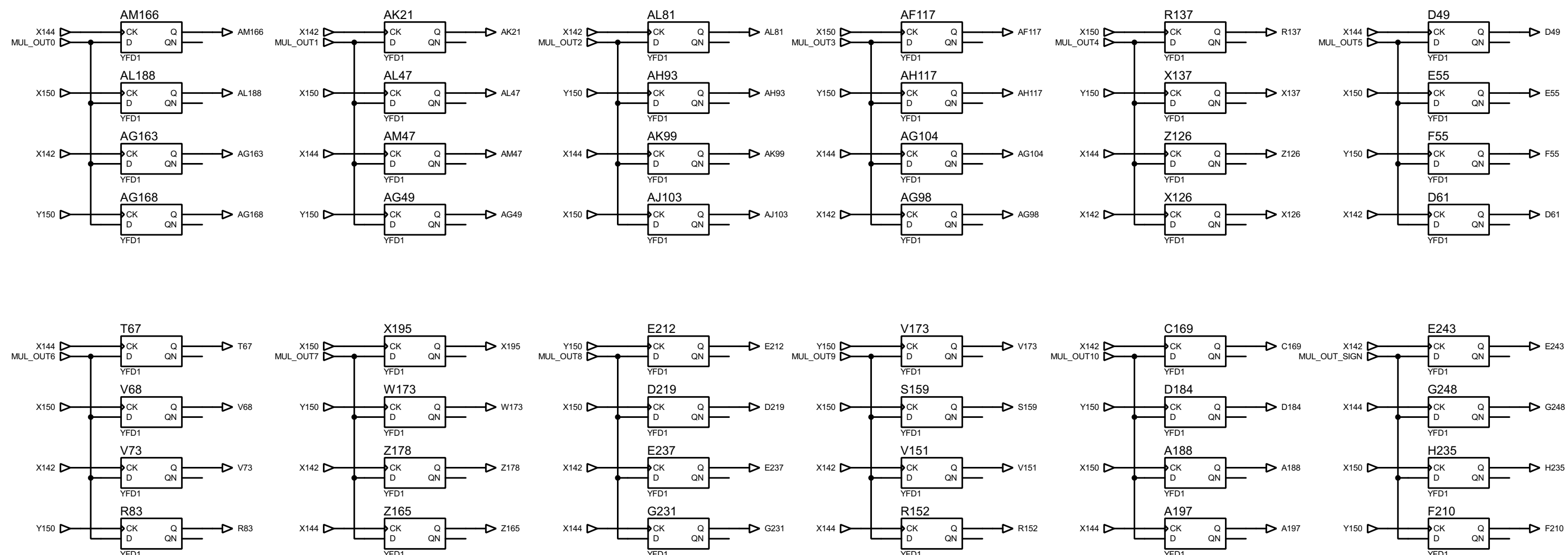
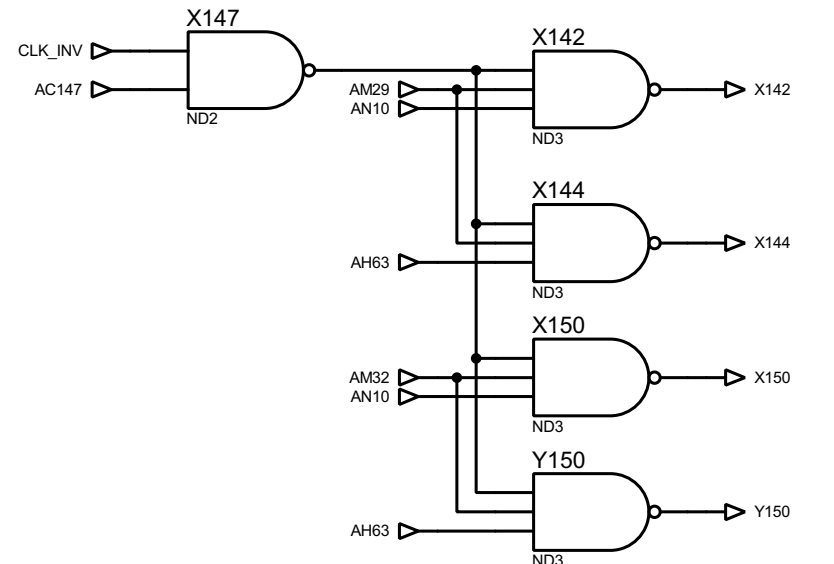




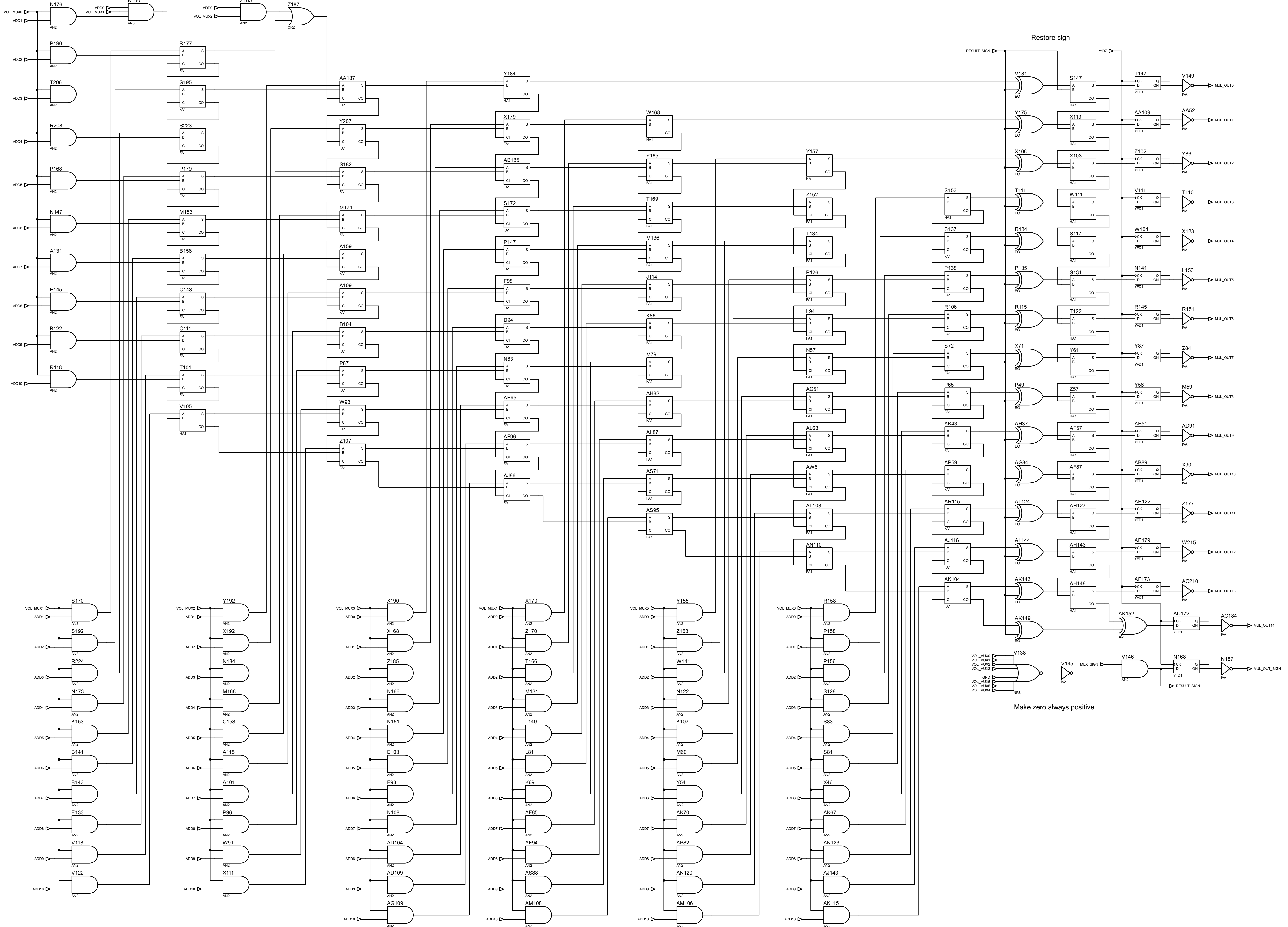
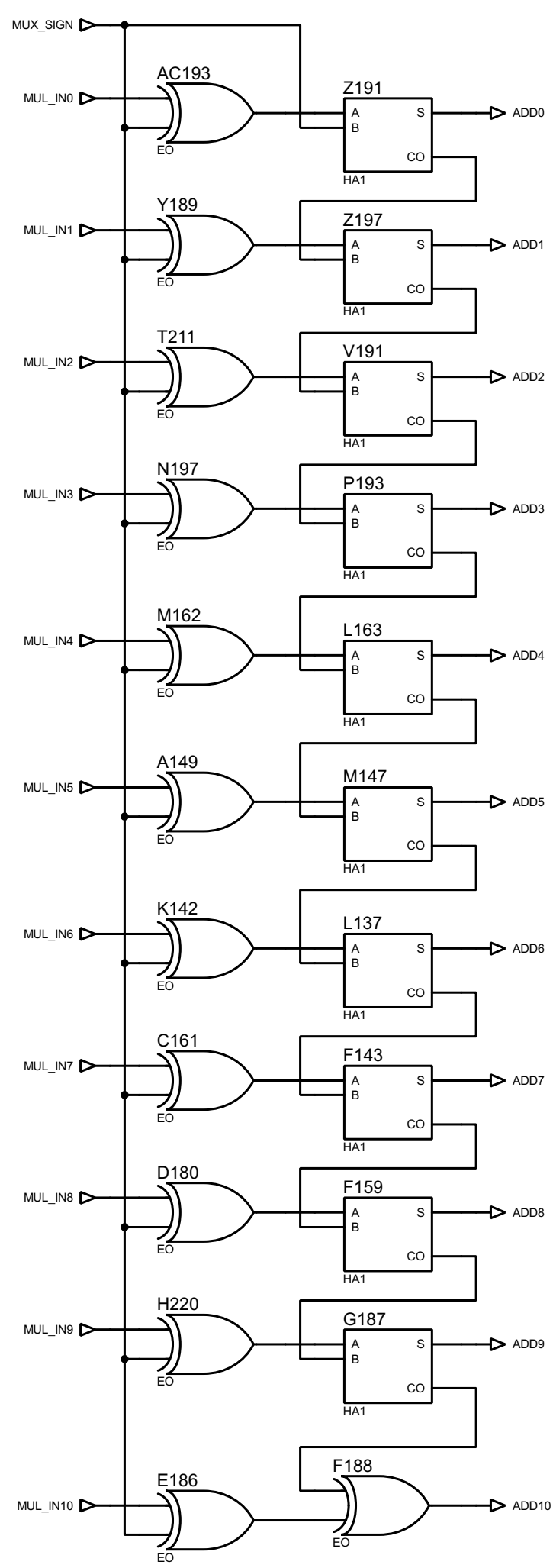
4 PCM channels L/R sample value mux to feed volume multiplier ?  
Sign extend 8 to 12 bits

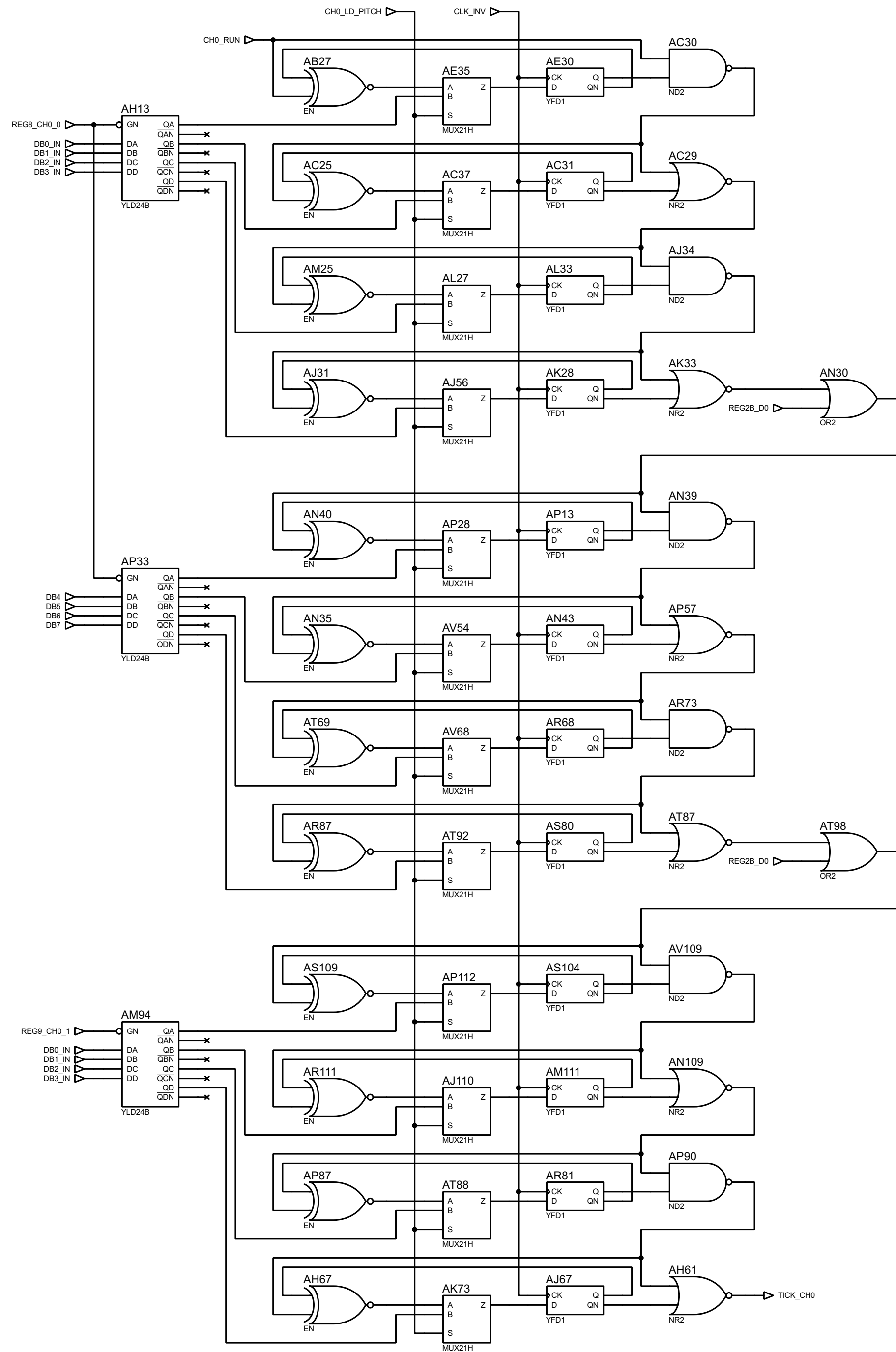


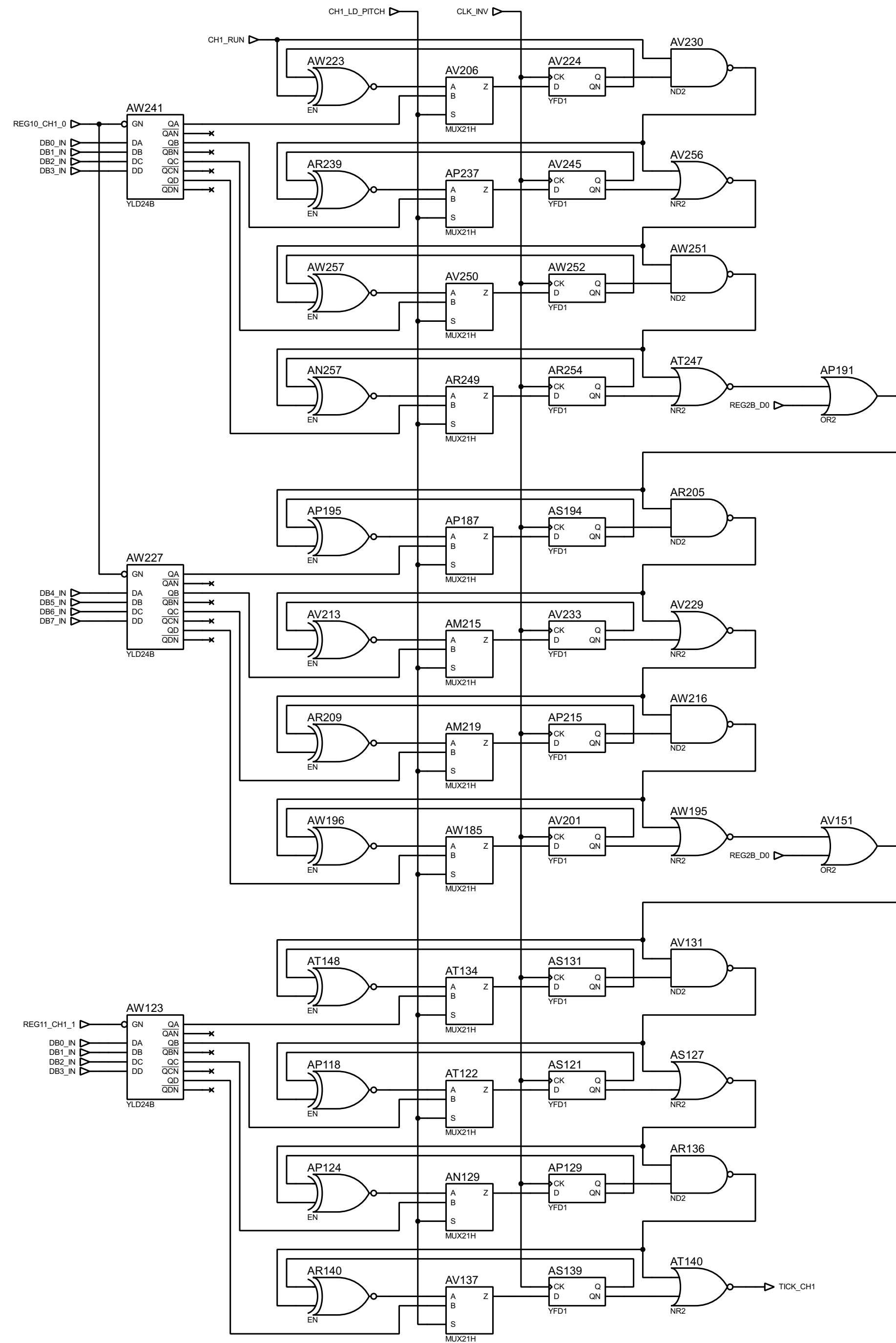
What are these used for ?  
They allow feeding back the result of a multiplication back into the multiplier.  
Only connected to 12 bits instead of 16.  
Is it panning related ?



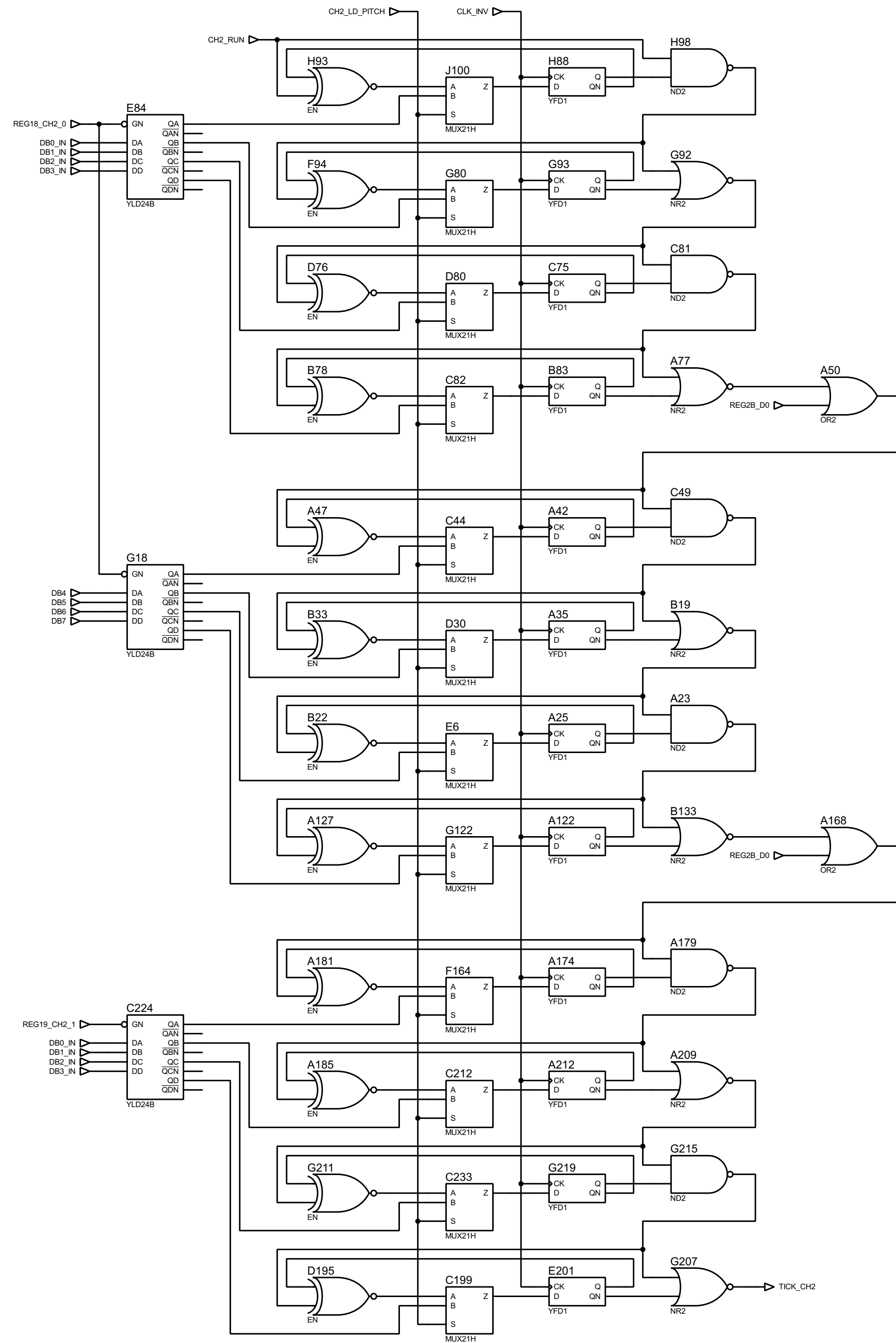
Get absolute value

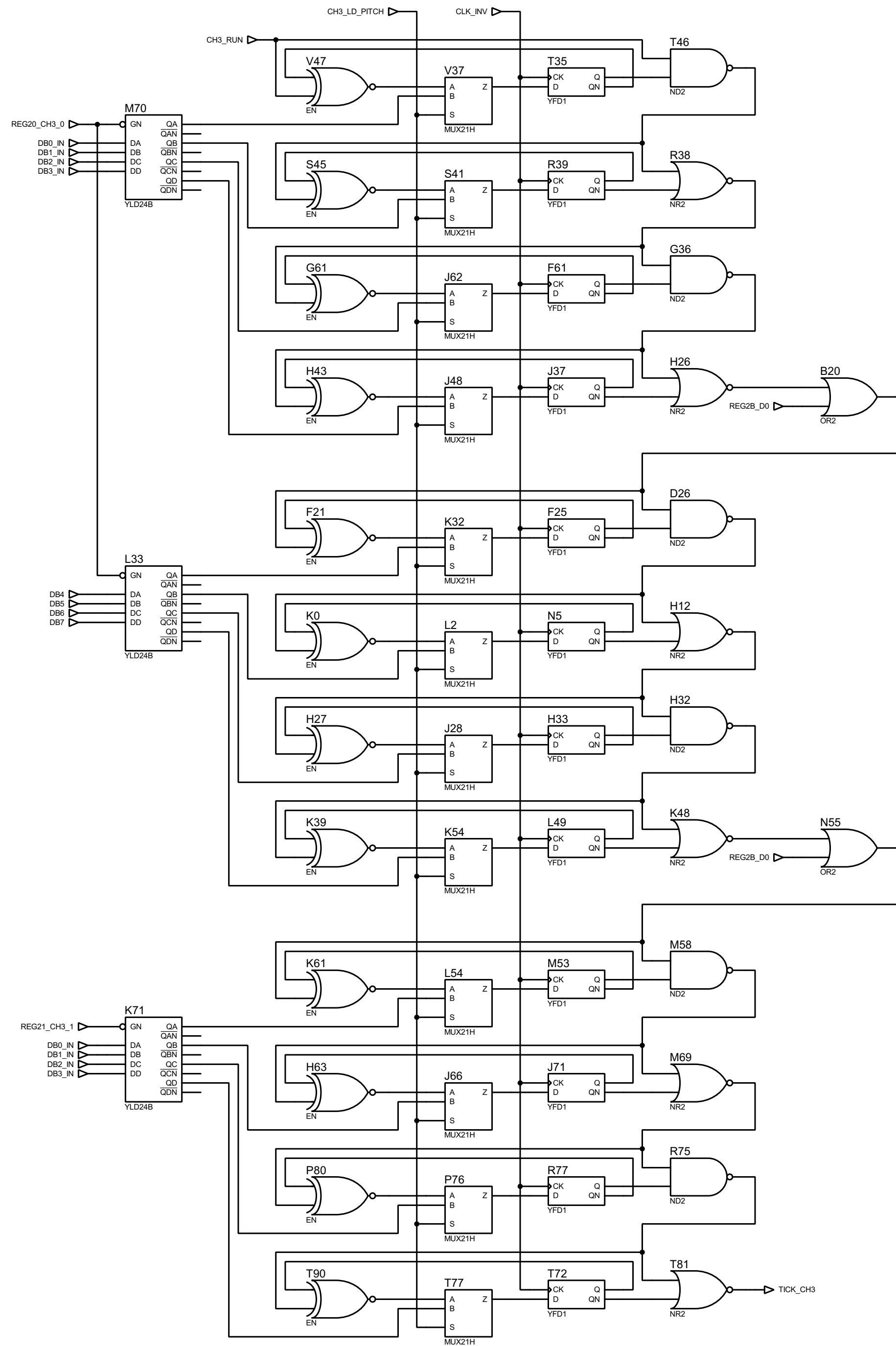


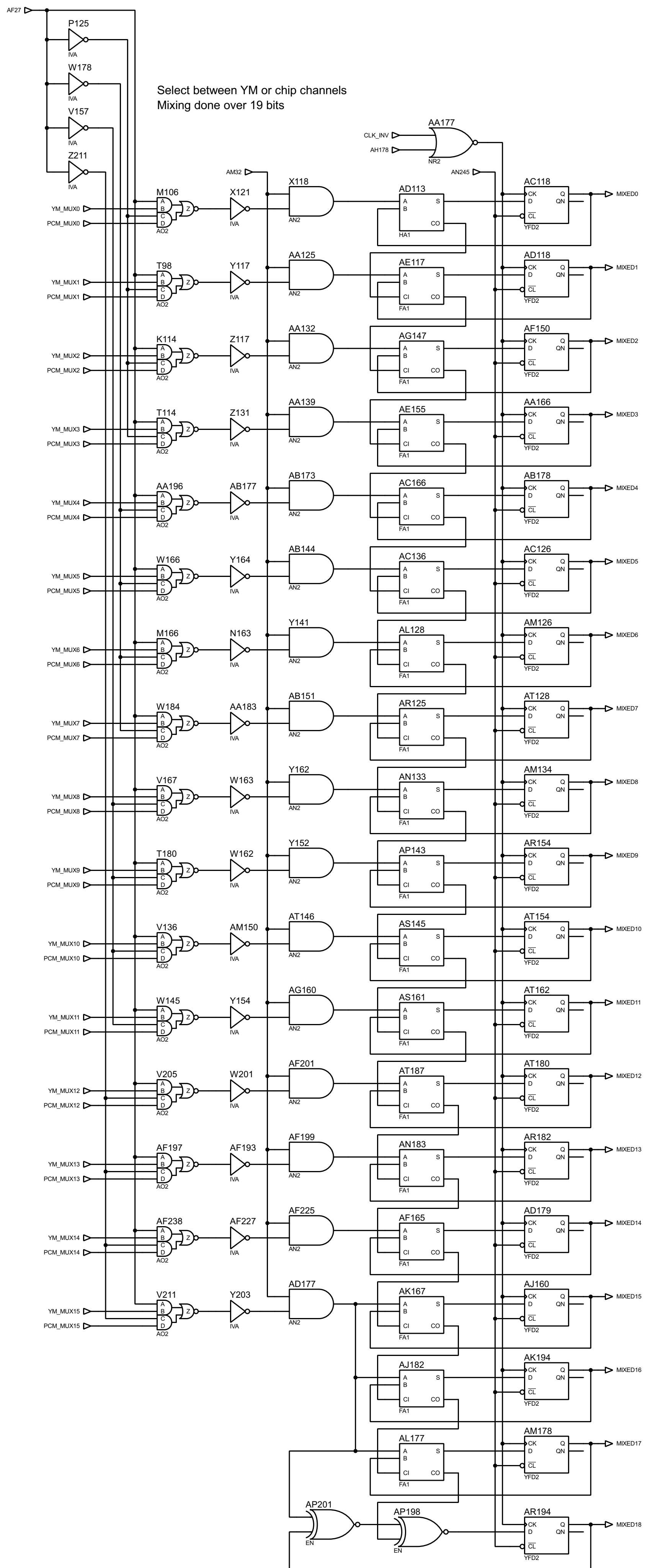




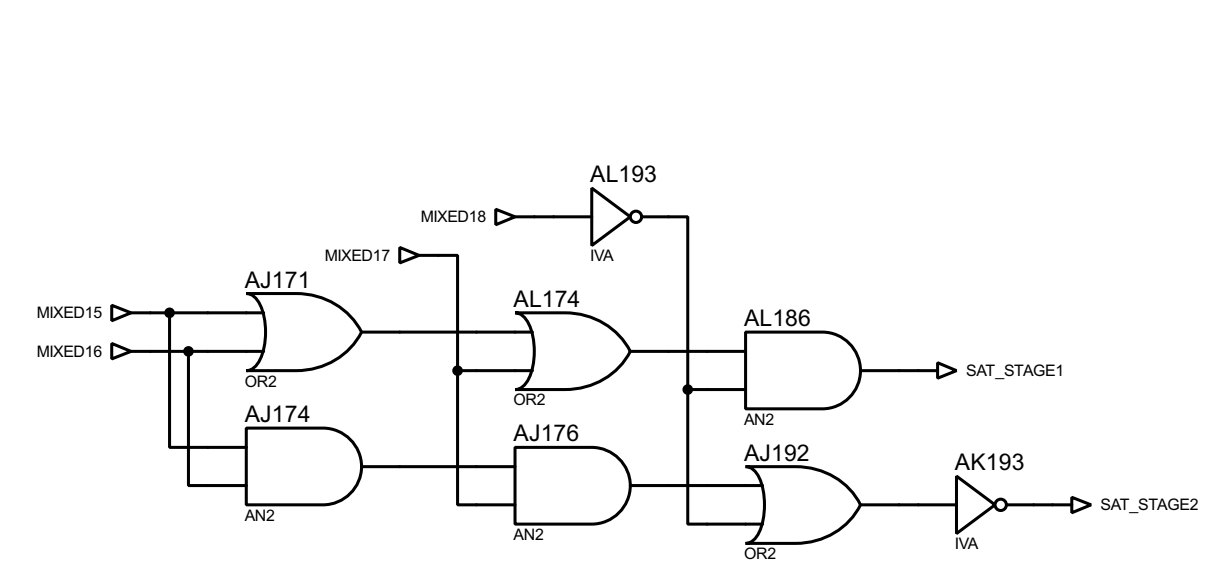
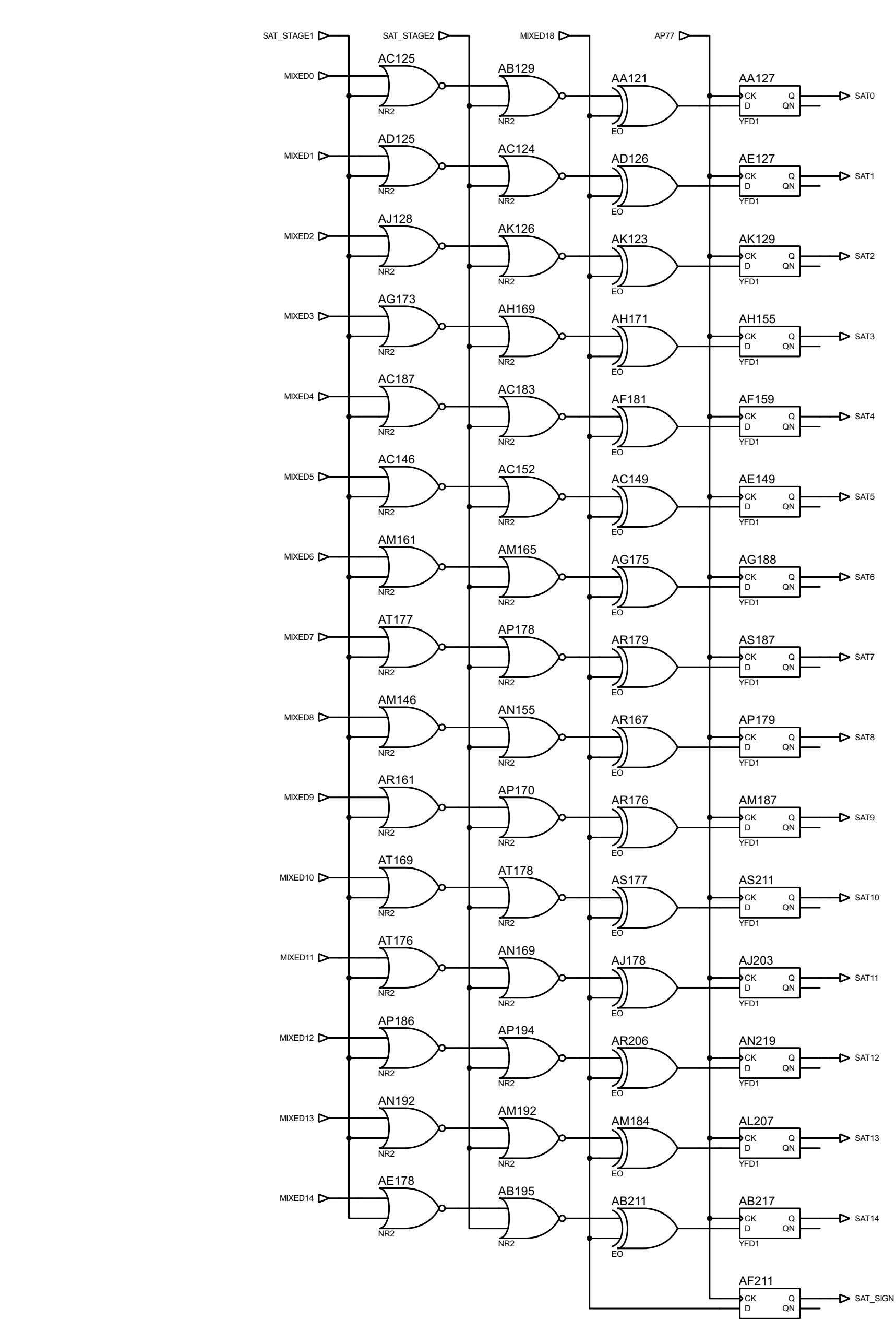








Saturation  
Unsigned to signed



Saturation

EDCBA98 76543210

111 11111111 11111111 = 7FFFF = -255144 0 0

011 11111111 11111111 = 3FFFF = -255143 0 1

First stage:

18 17 16 15 AL186

0 0 0 0

1 x x x 0

Second stage:

18 17 16 15 AK193

x 1 1 1 0

0 x x x 0

00: through

01: 0000

10: 1111

11: 0000

0000 0 0 through (between 0 and 32767)

0001 1 0 max

0010 1 0 max

0011 0 max

0100 1 0 max

0101 1 0 max

0110 1 0 max

0111 1 0 max

1000 0 1 min

1001 0 1 min

1010 0 1 min

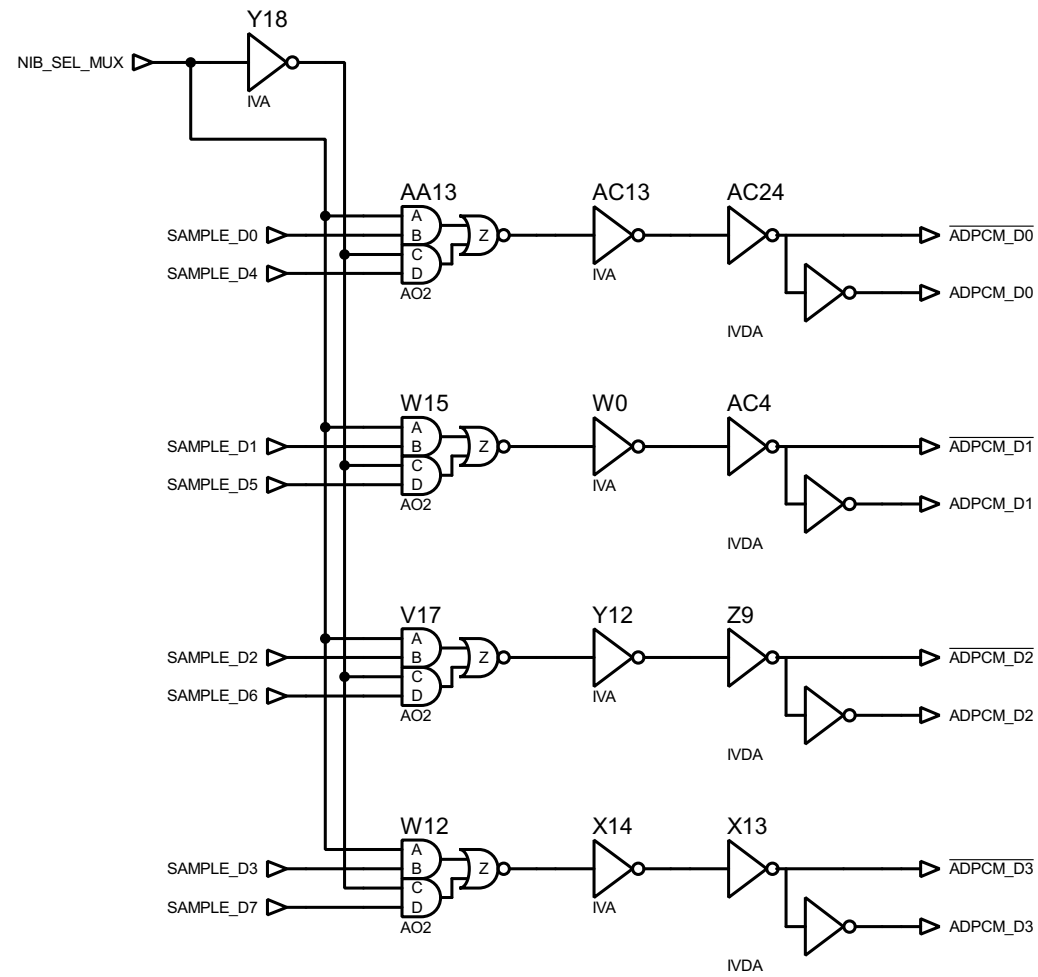
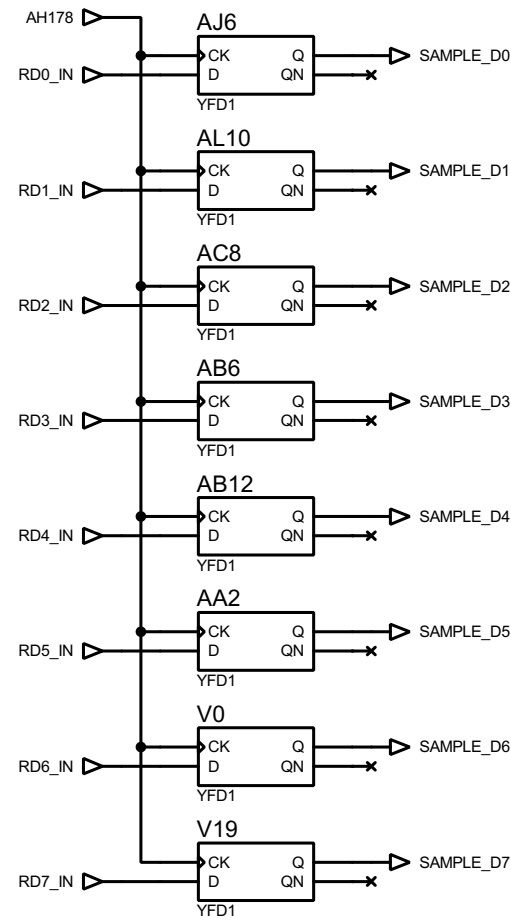
1011 0 1 min

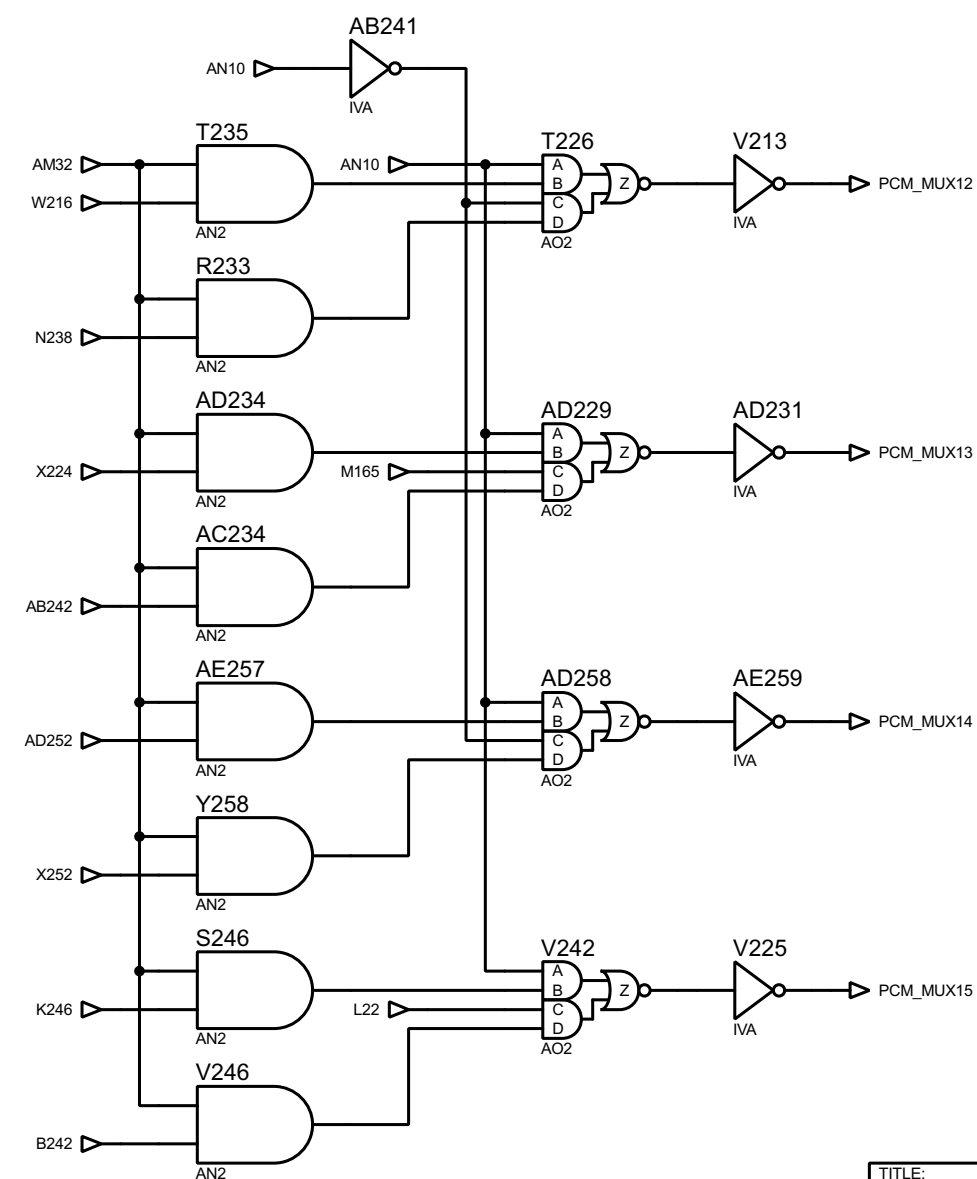
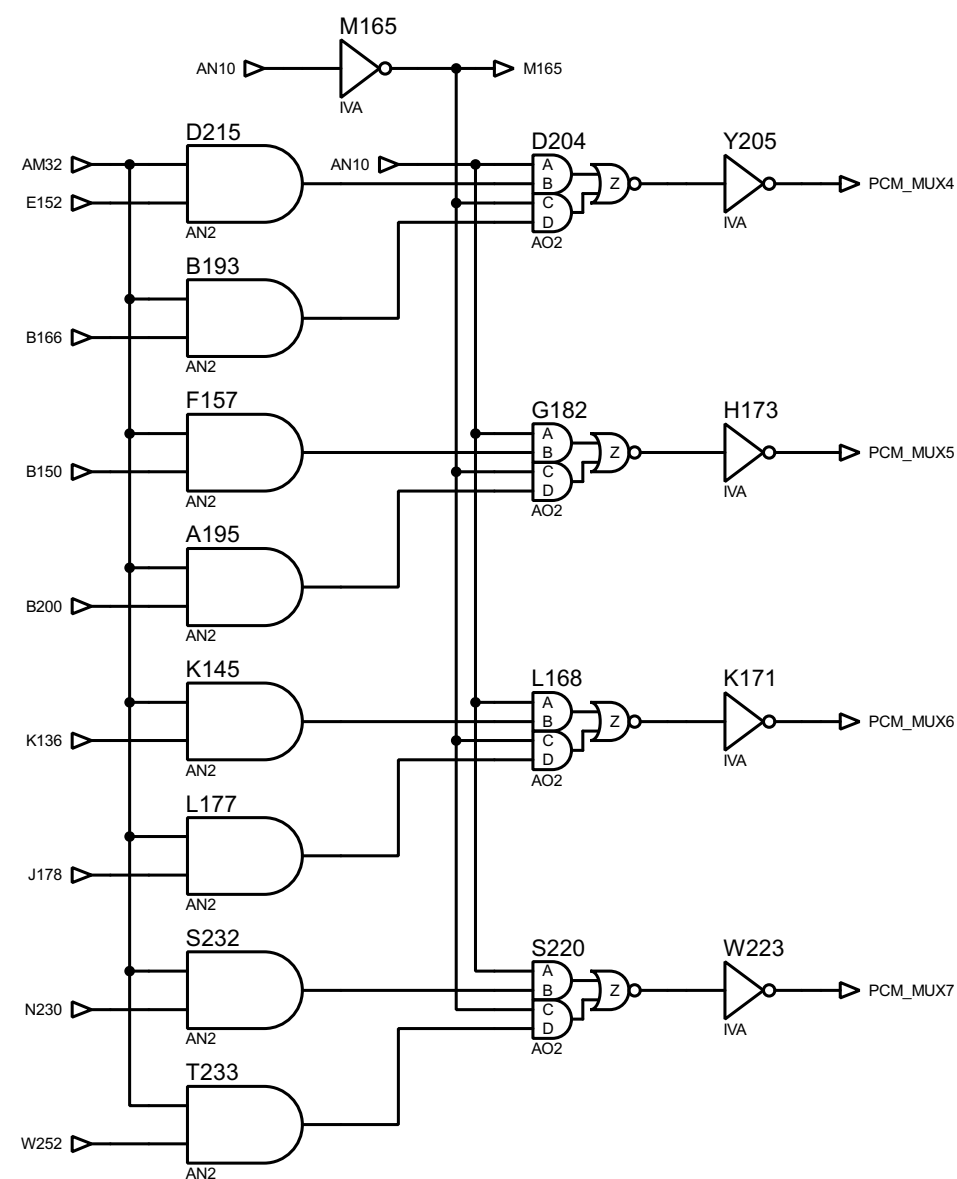
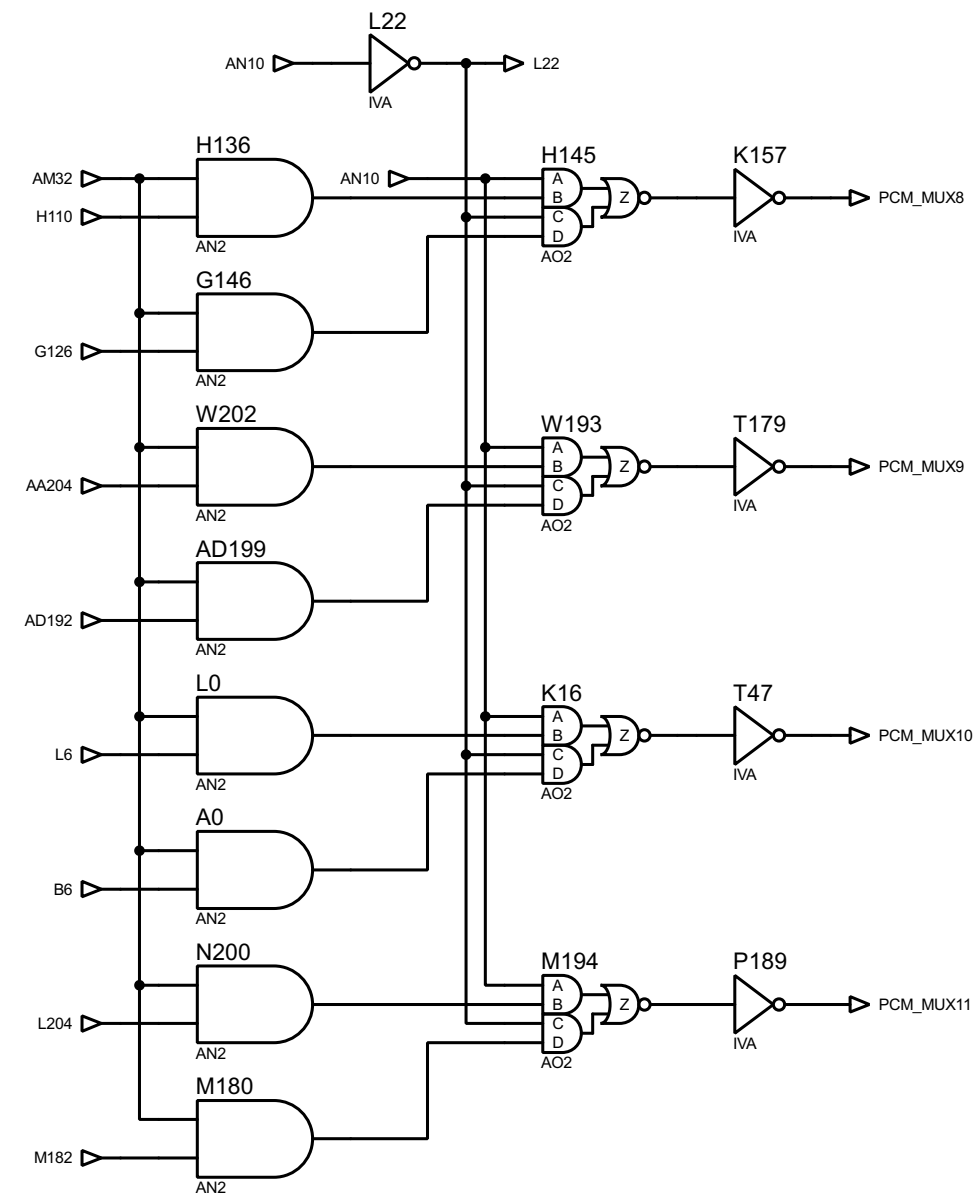
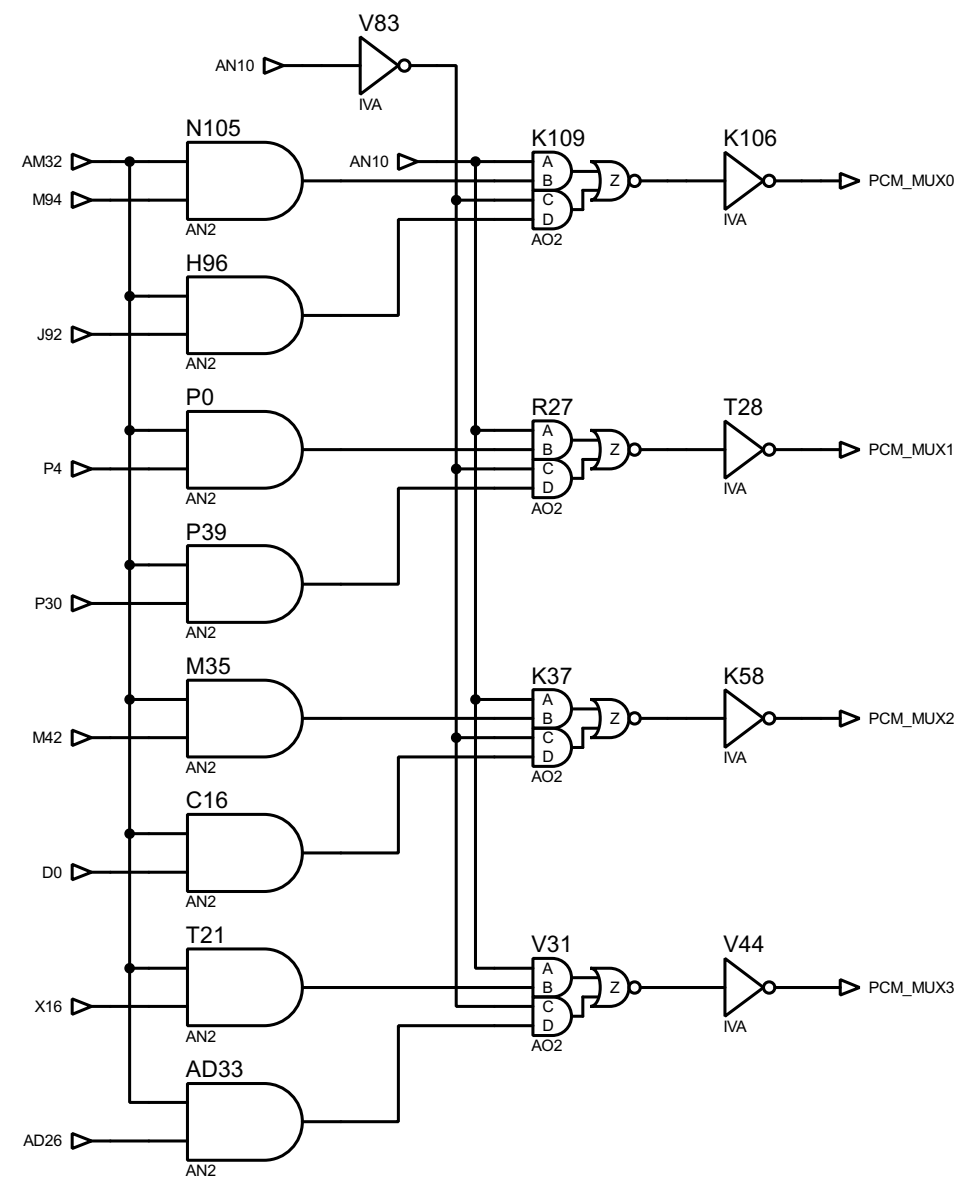
1100 0 1 min

1101 0 1 min

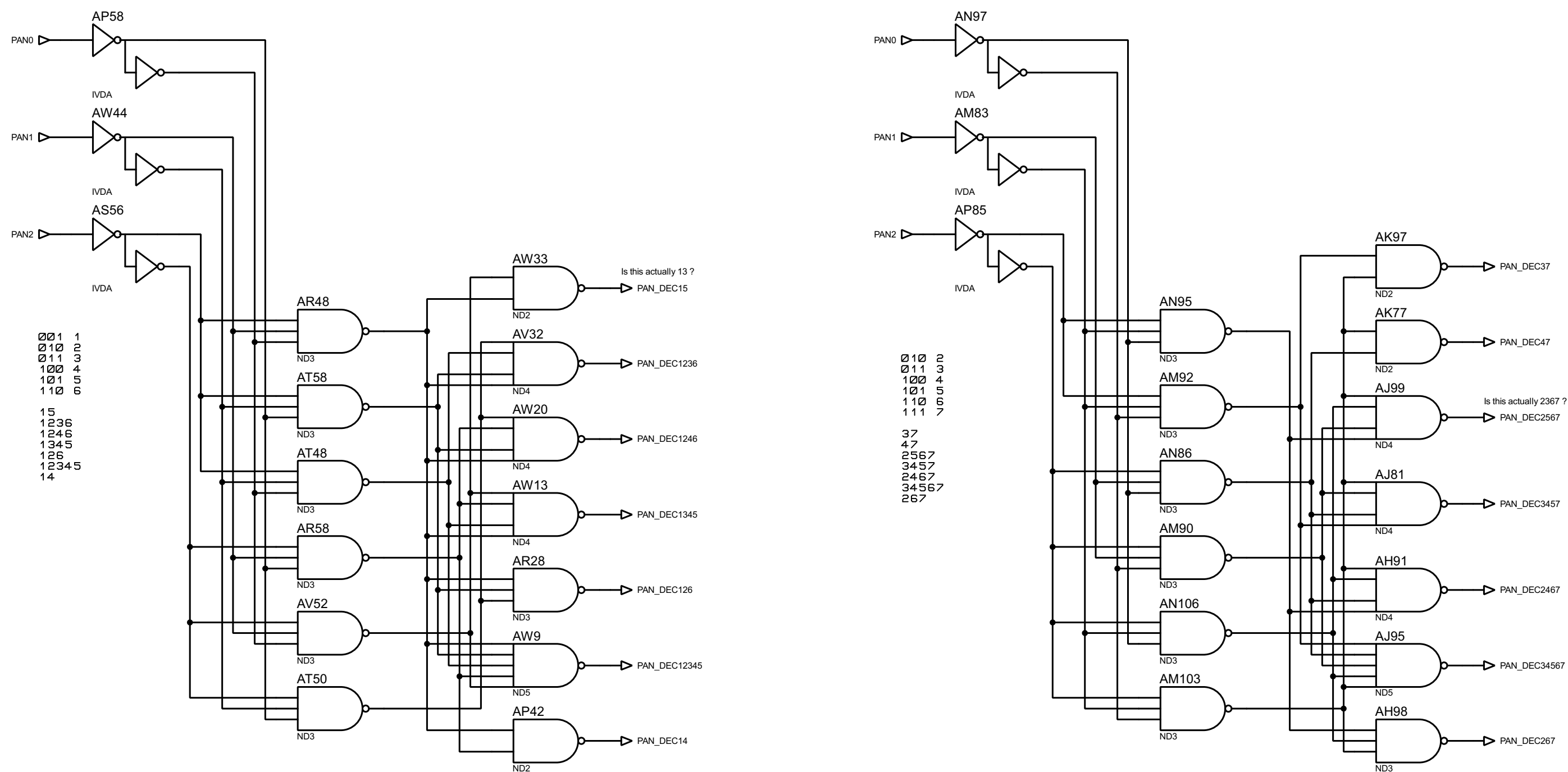
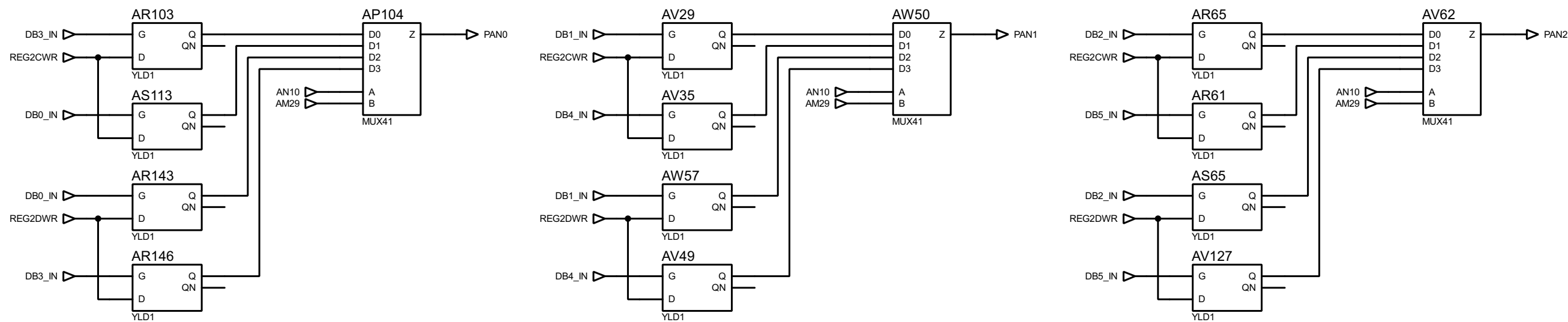
1110 0 1 min

1111 0 0 through (between -1 and -32768)

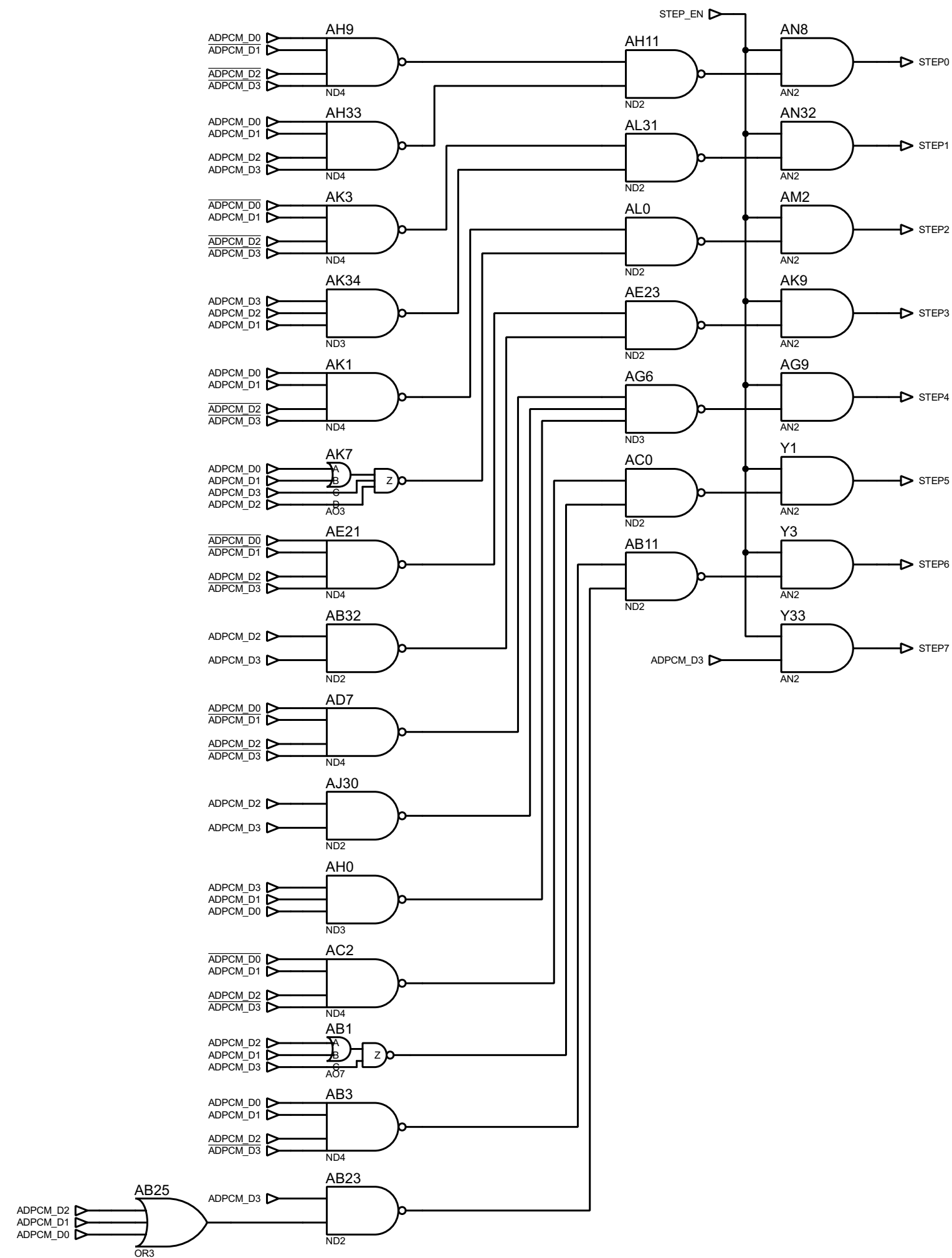




Shouldn't these two be swapped ?



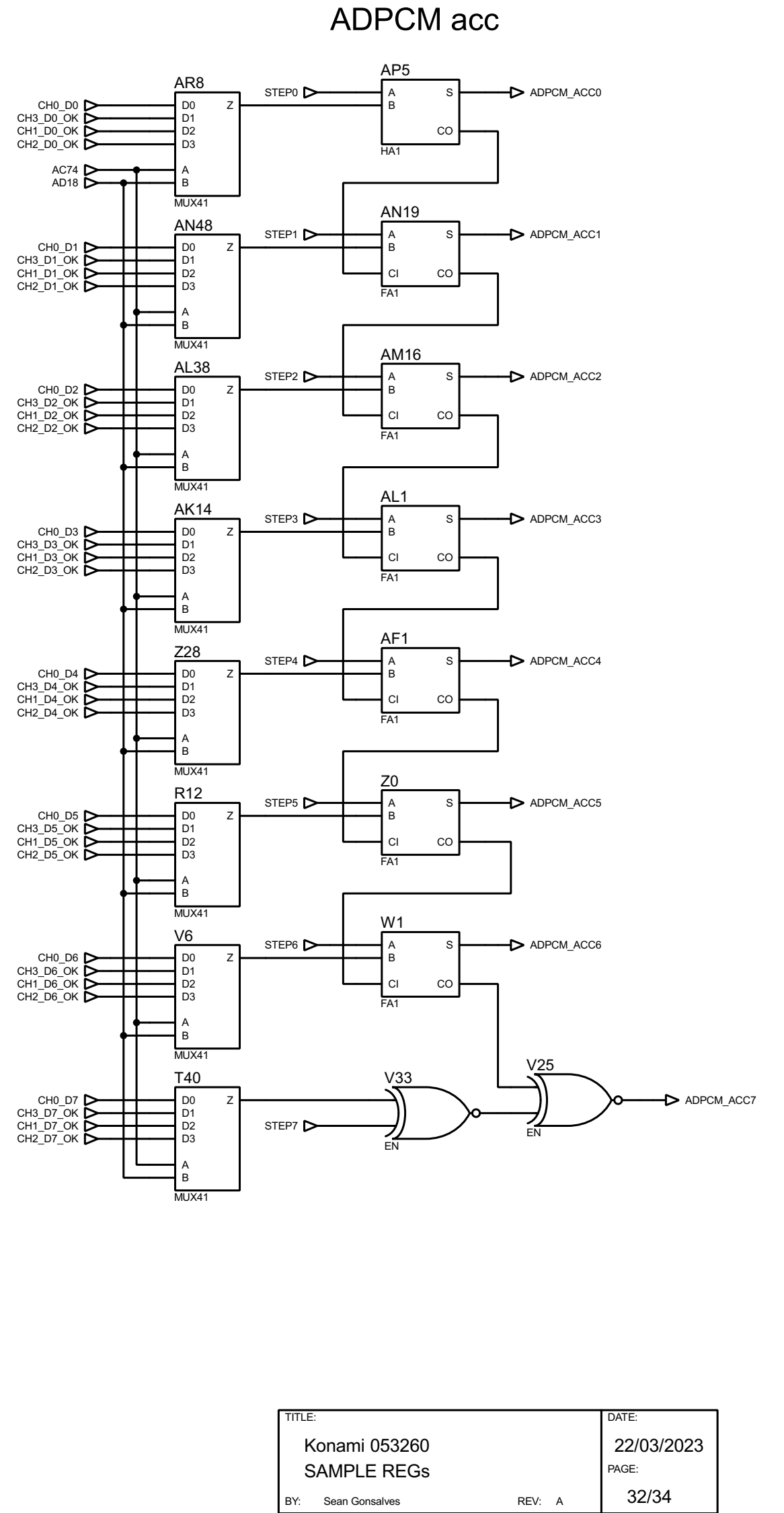
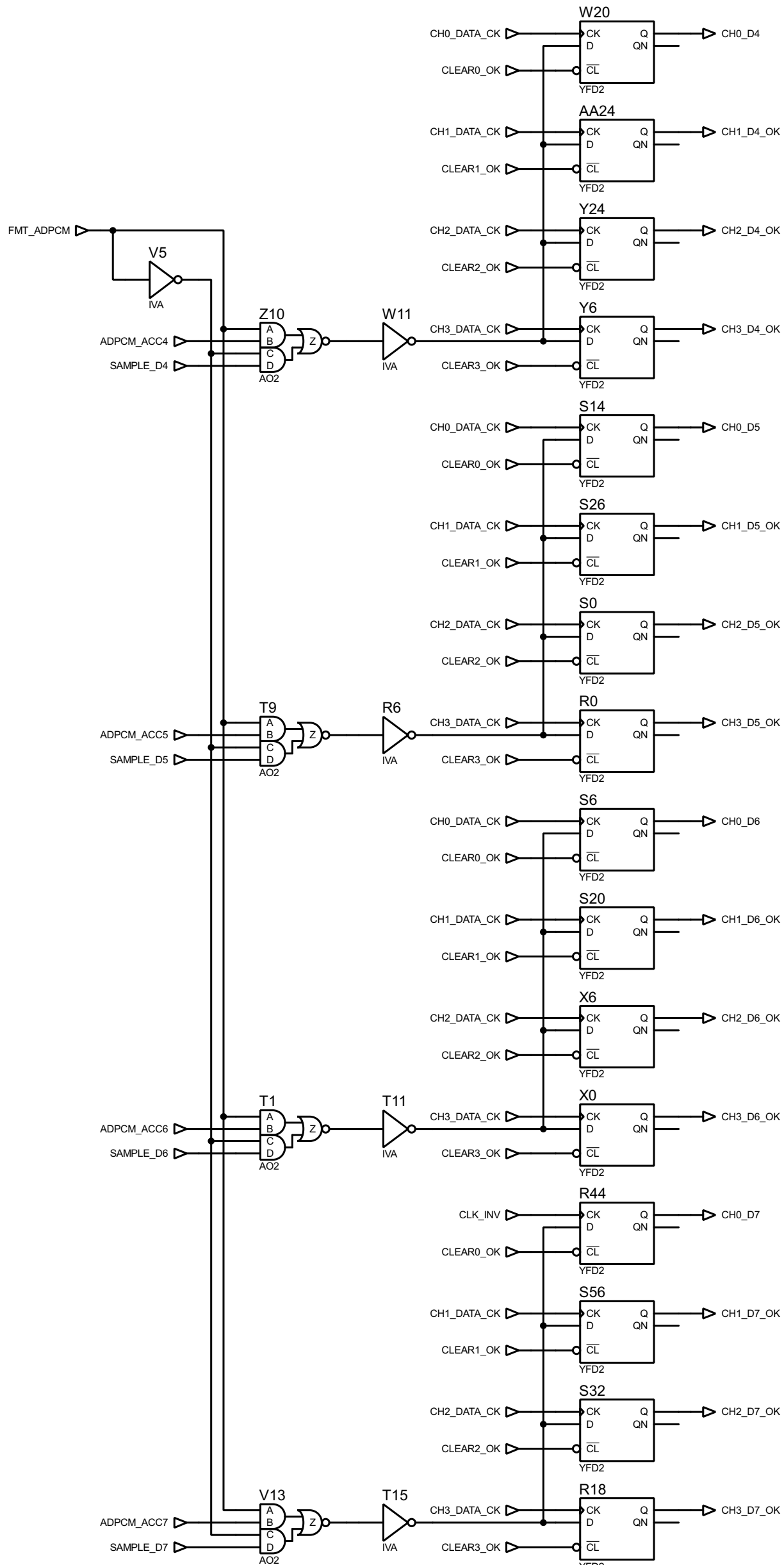
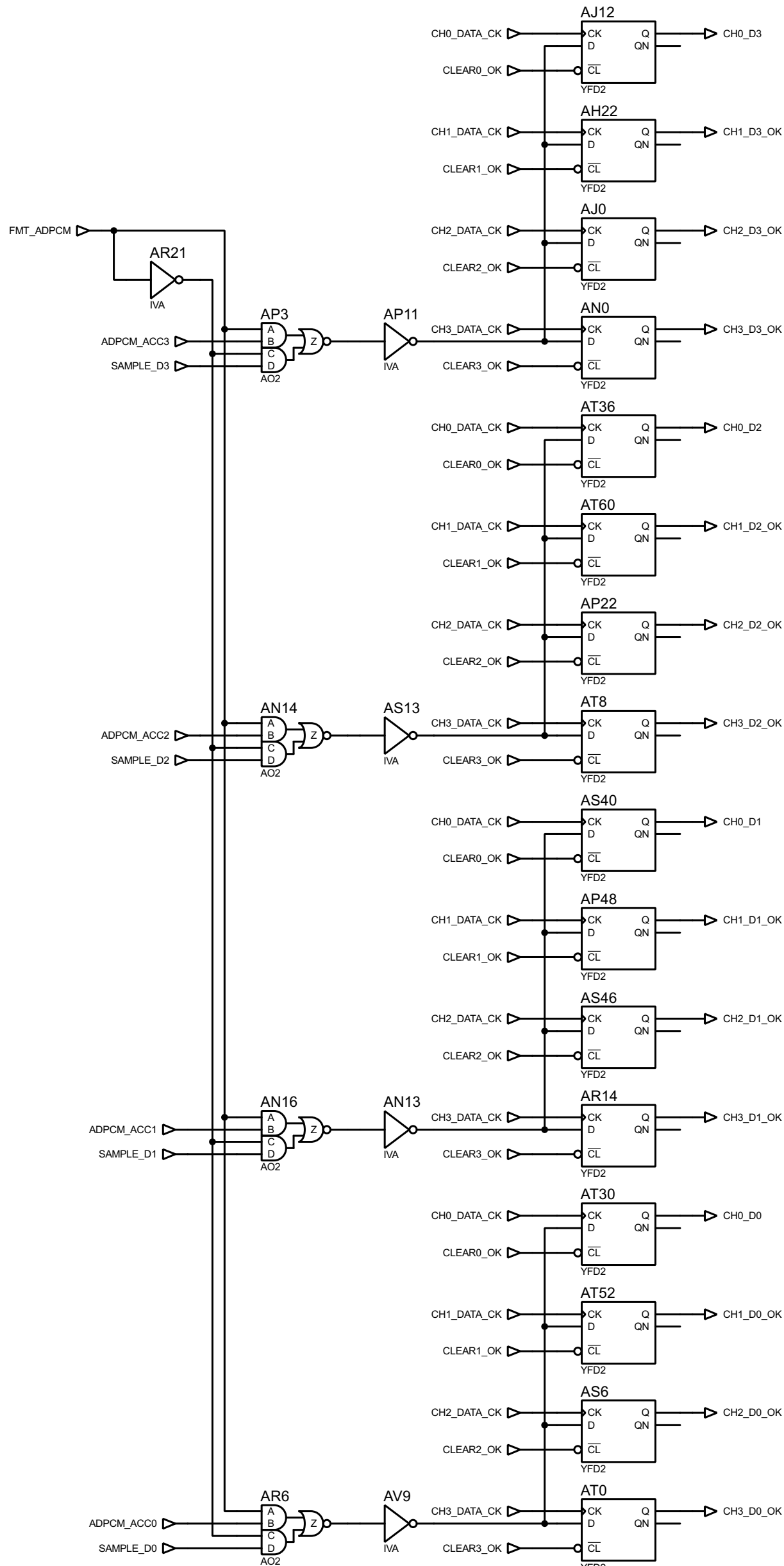
This stuff decodes the 8 possible pan values to a 16 signals used to modify the channel's volume setting



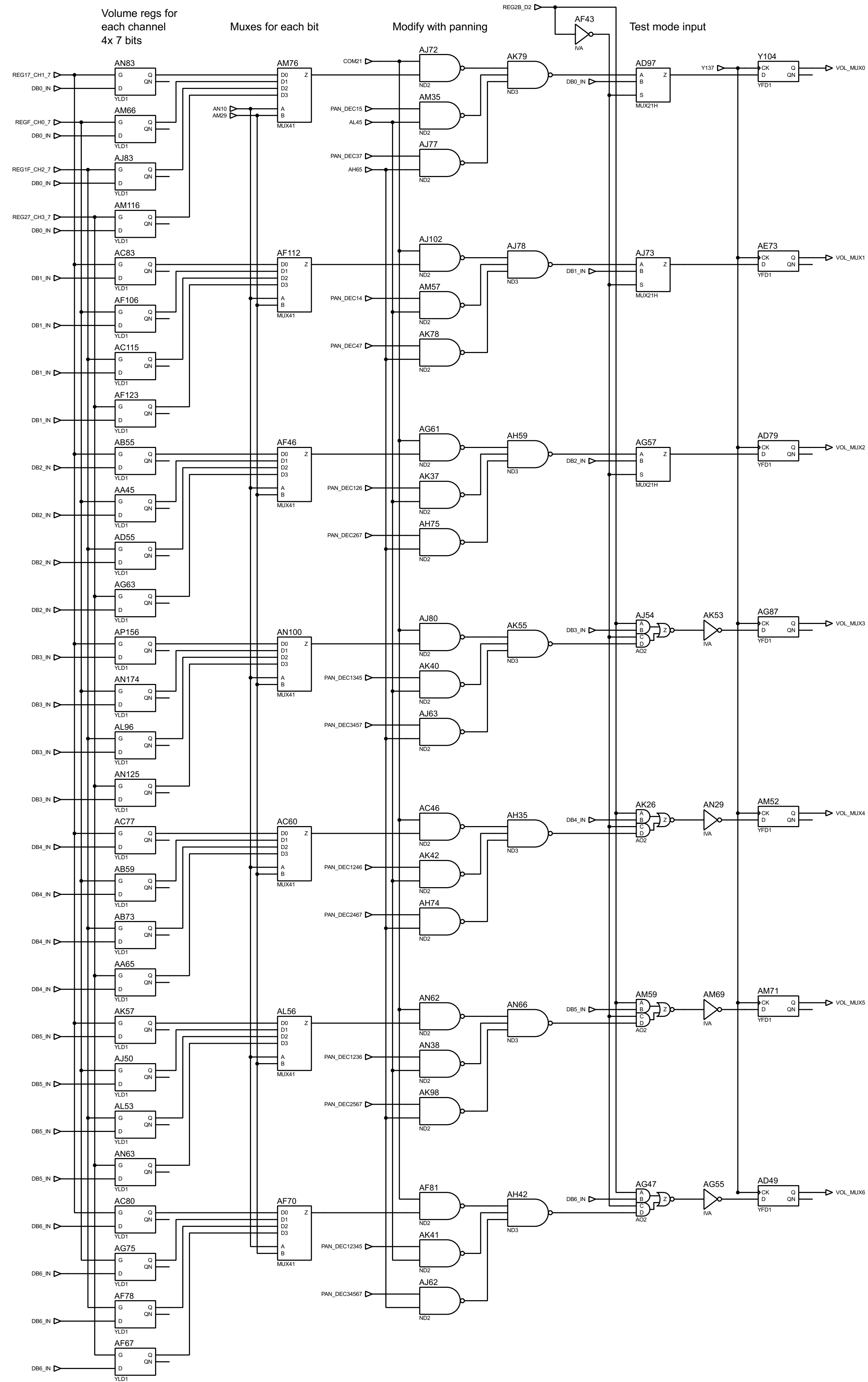
This translates the 4-bit ADPCM sample to a signed value that must be added to the channel's accumulator. Should match MAME's kadpcm\_table[].

IN:OUT  
 0:0  
 1:1  
 2:2  
 3:4  
 4:8  
 5:16  
 6:32  
 7:64  
 8:-128  
 9:-64  
 A:-32  
 B:-16  
 C:-8  
 D:-4  
 E:-2  
 F:-1

4 CH x 8-bit regs for sample values  
Either load from ROM, or acc ADPCM







## Further clock division for TIM2 output

