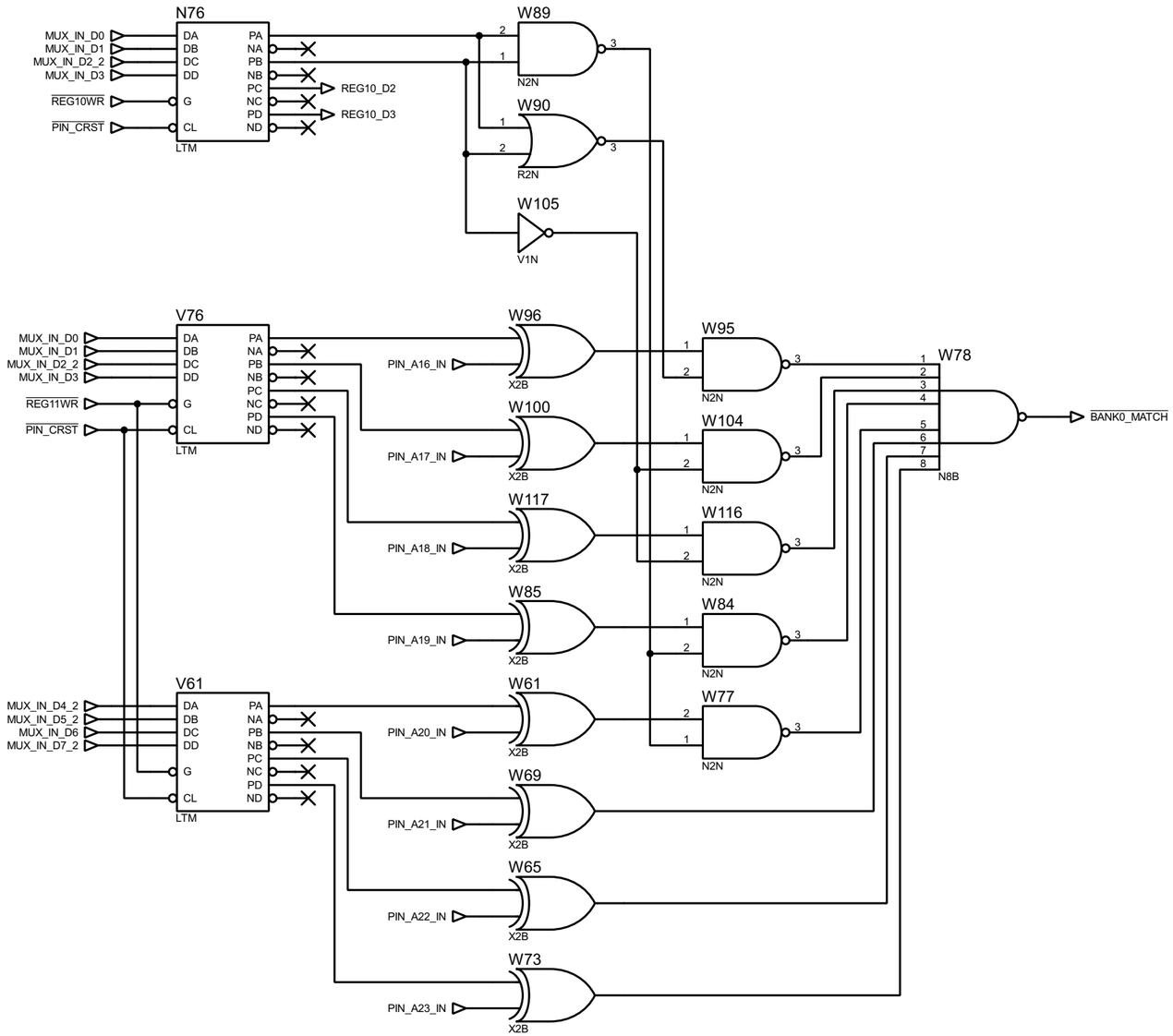
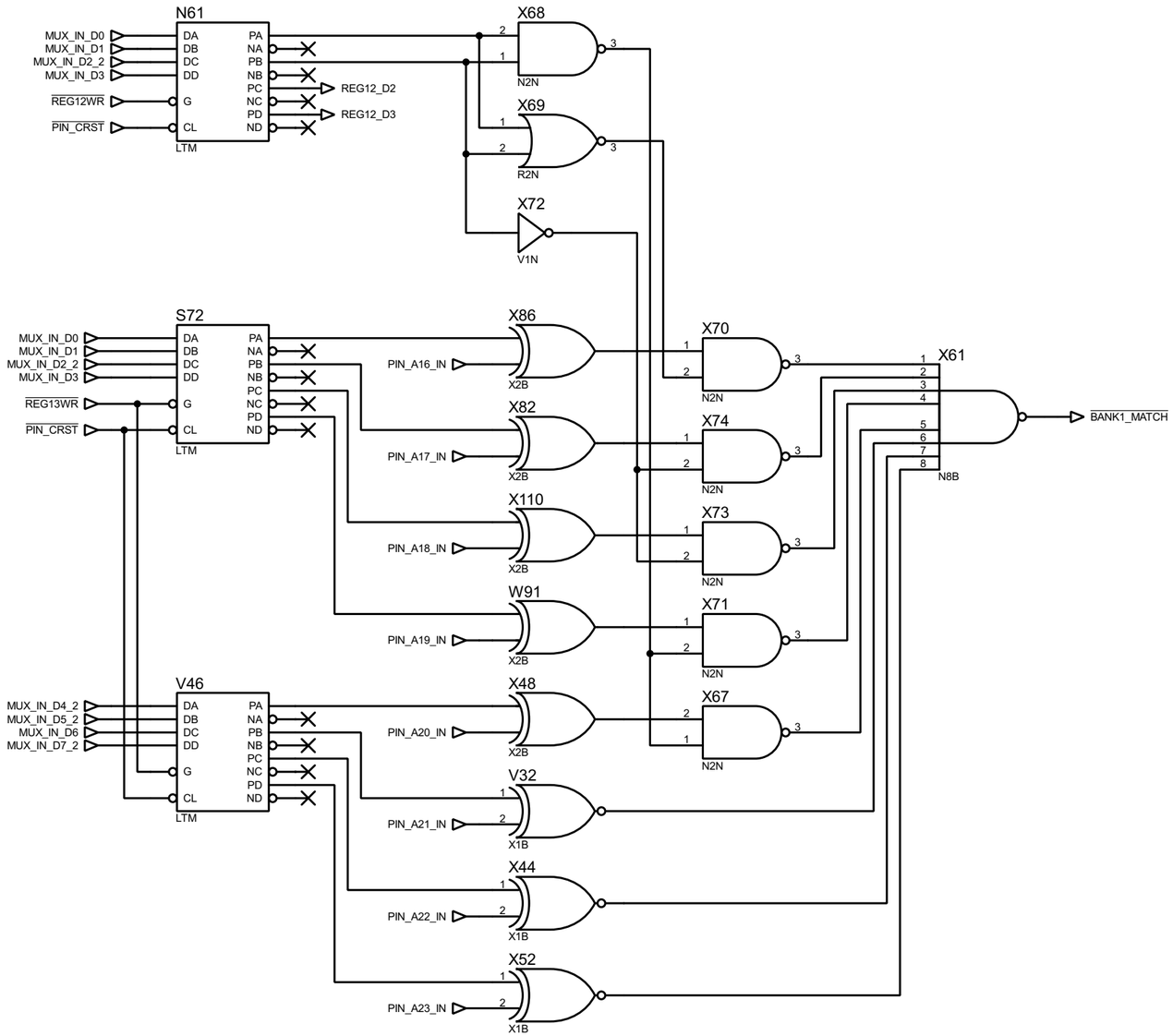
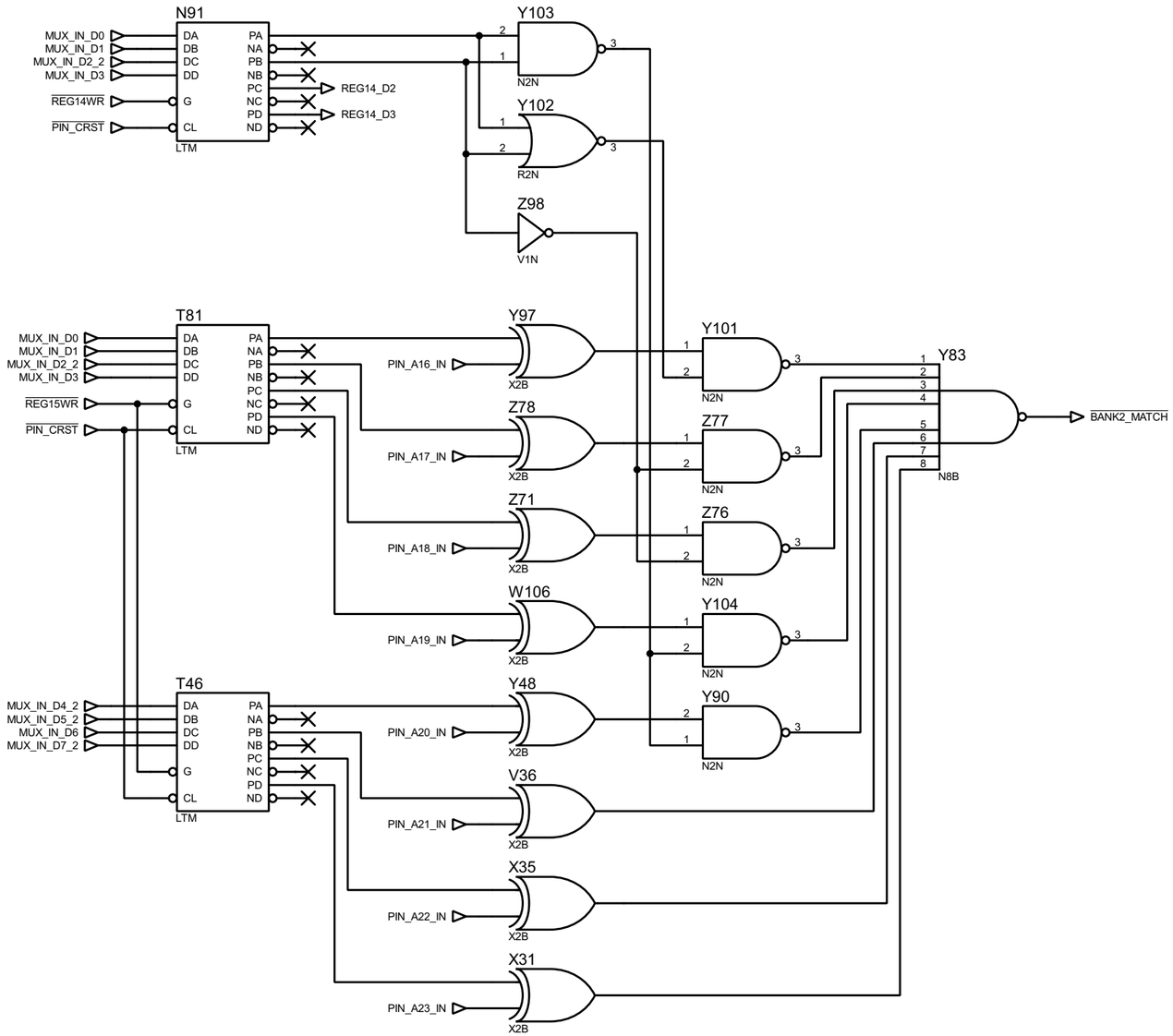


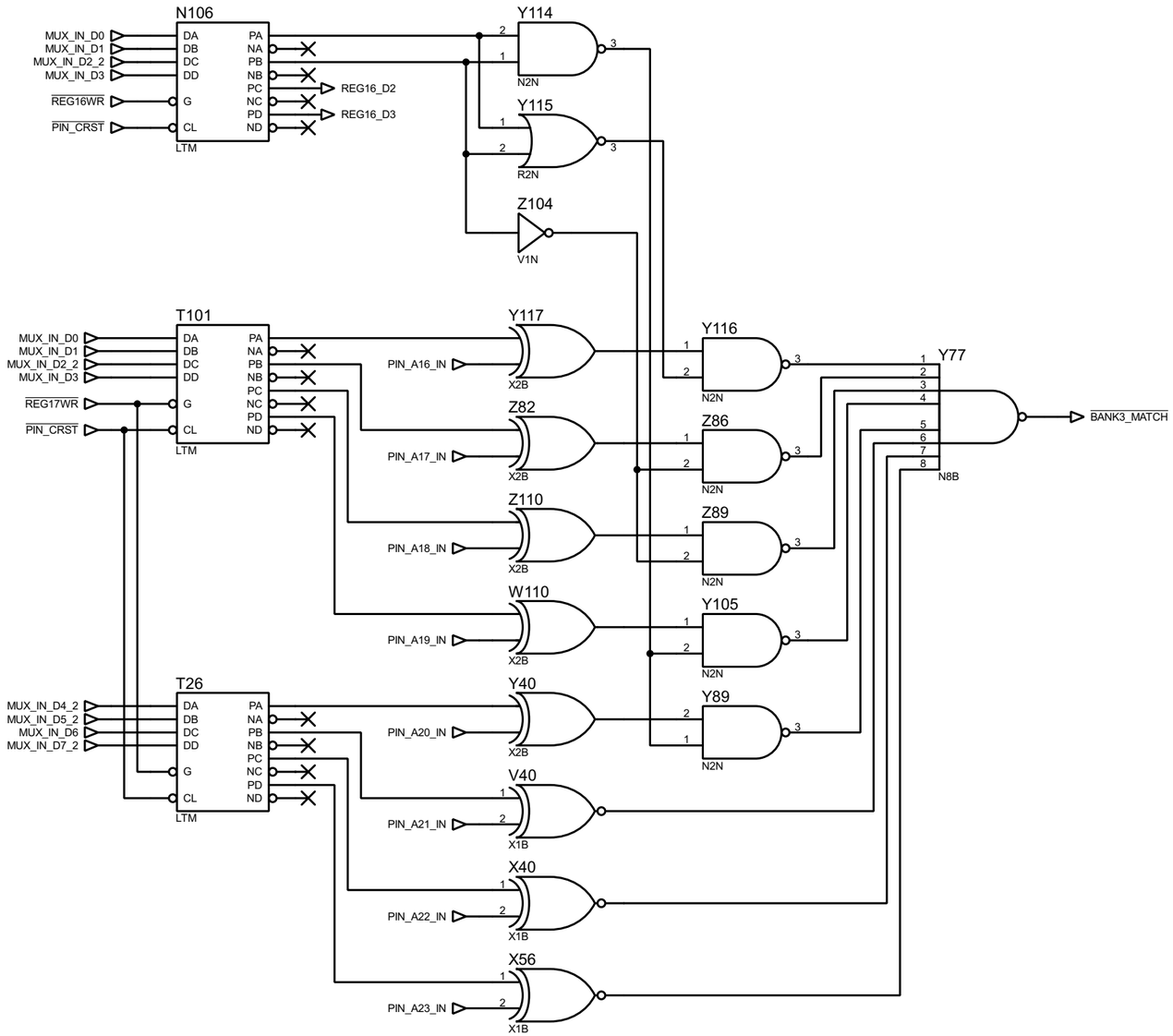
FILE NAME: **315-5195.pdsprj**		DATE: **02/08/2022**
DESIGN TITLE: **Sega 315-5195** MAPPING REGS BANK 0		PAGE: **1 of 18**
BY: **Sean Gonsalves**	REV: **A**	



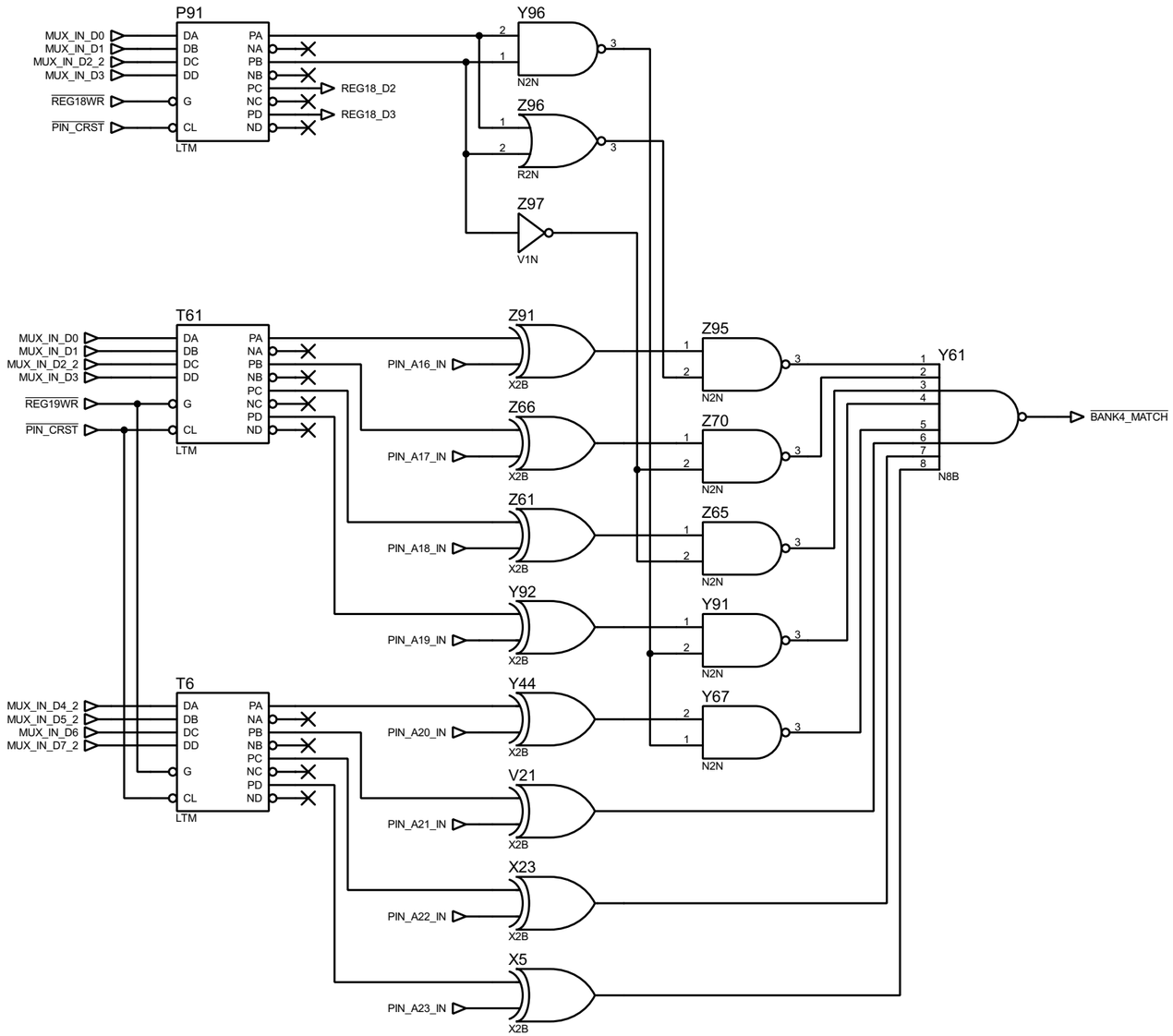
FILE NAME: **315-5195.pdsprj**		DATE: **02/08/2022**
DESIGN TITLE: **Sega 315-5195** MAPPING REGS BANK 1		PAGE: **2 of 18**
BY: **Sean Gonsalves**	REV: **A**	



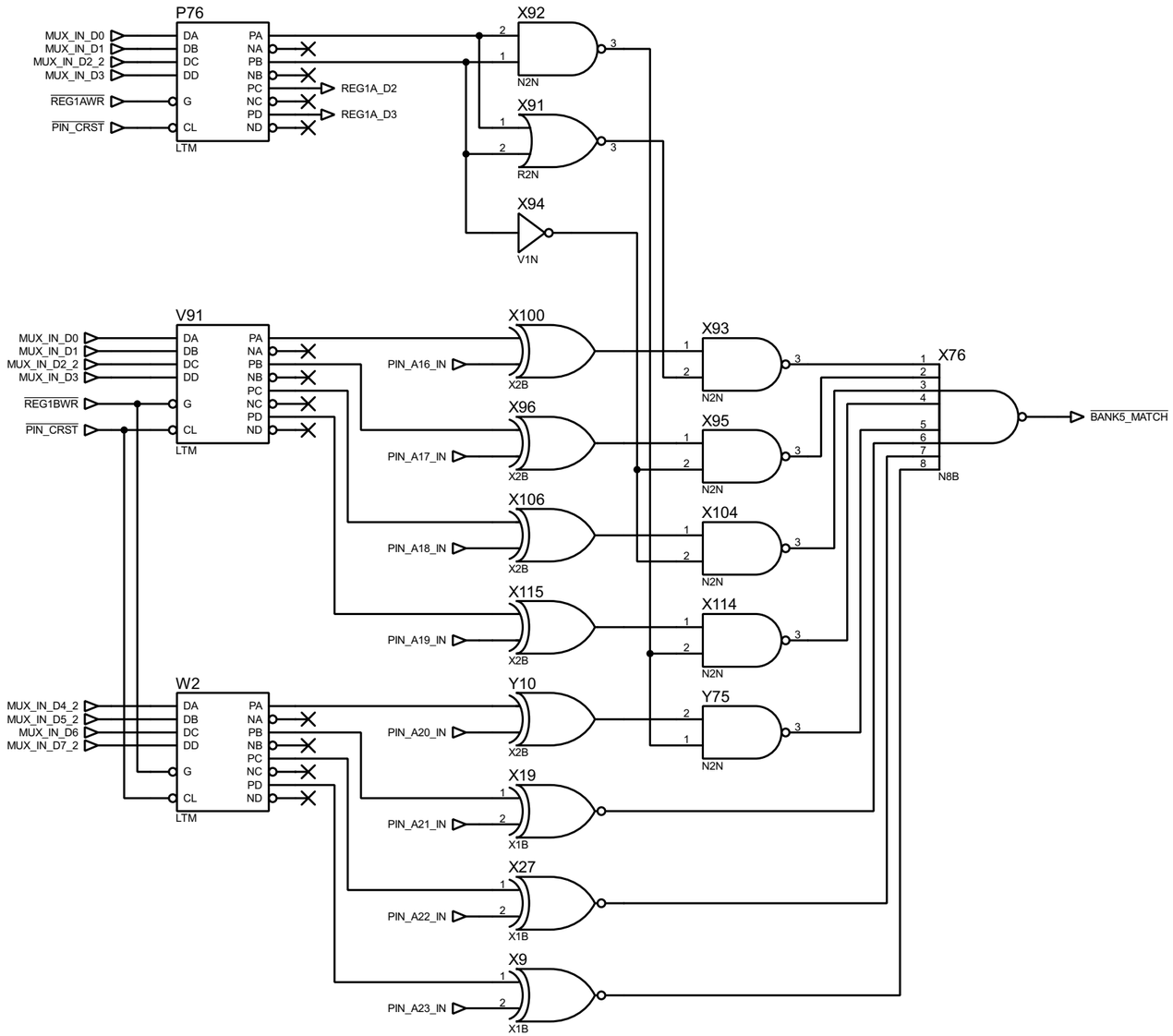
FILE NAME: **315-5195.pdsprj**		DATE: **02/08/2022**
DESIGN TITLE: **Sega 315-5195** MAPPING REGS BANK 2		PAGE: **3 of 18**
BY: **Sean Gonsalves**	REV: **A**	



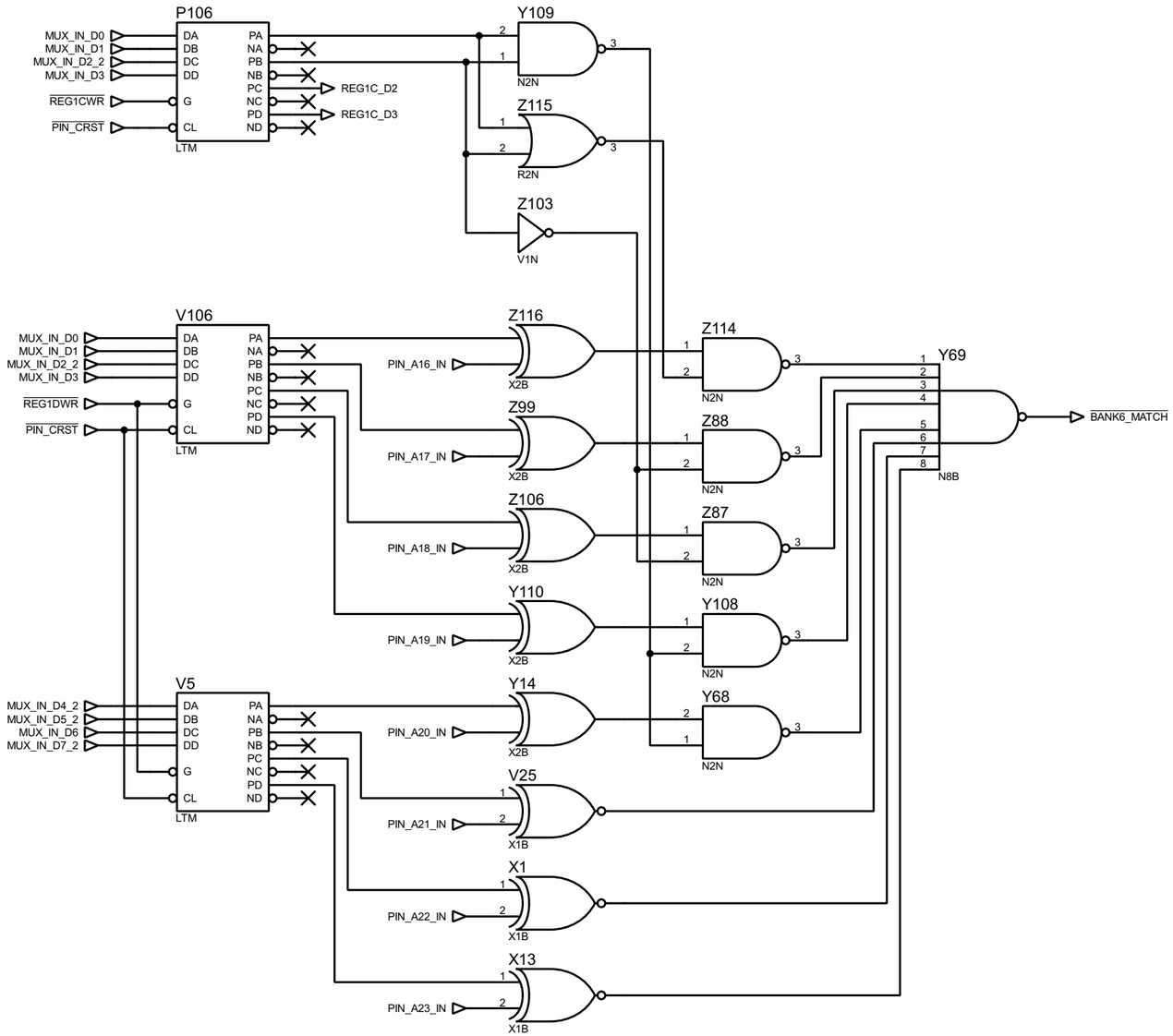
FILE NAME: **315-5195.pdsprj**		DATE: **02/08/2022**
DESIGN TITLE: **Sega 315-5195** MAPPING REGS BANK 3		PAGE: **4 of 18**
BY: **Sean Gonsalves**	REV: **A**	



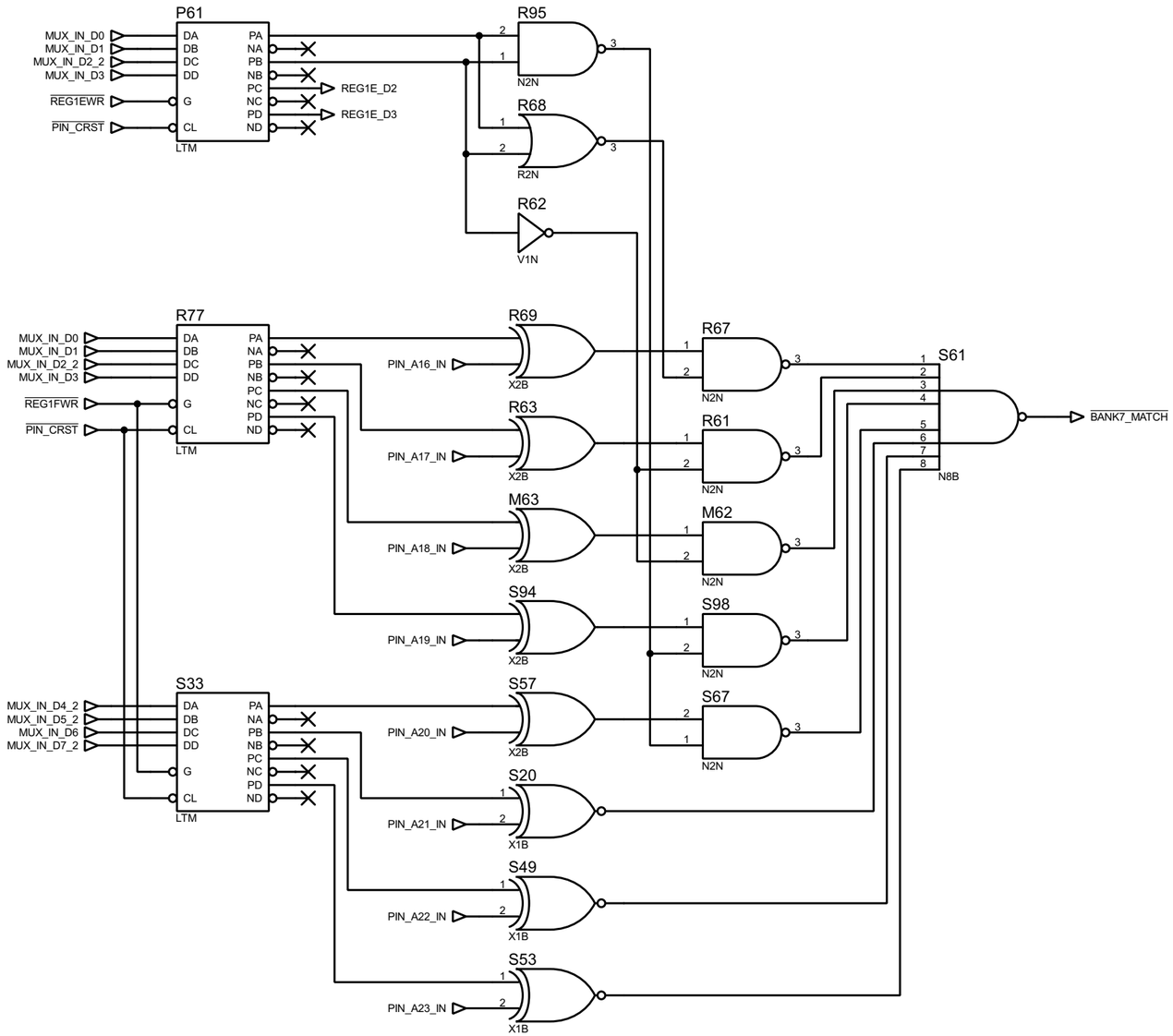
FILE NAME: **315-5195.pdsprj**		DATE: **02/08/2022**
DESIGN TITLE: **Sega 315-5195** MAPPING REGS BANK 4		PAGE: **5 of 18**
BY: **Sean Gonsalves**	REV: **A**	



FILE NAME: **315-5195.pdsprj**		DATE: **02/08/2022**
DESIGN TITLE: **Sega 315-5195** MAPPING REGS BANK 5		PAGE: **6 of 18**
BY: **Sean Gonsalves**	REV: **A**	

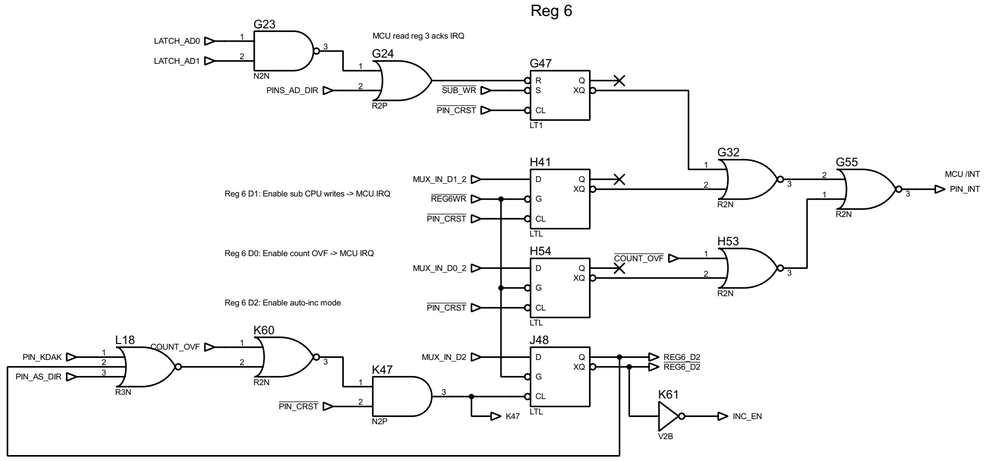


FILE NAME: **315-5195.pdsprj**		DATE: **02/08/2022**
DESIGN TITLE: **Sega 315-5195** MAPPING REGS BANK 6		PAGE: **7 of 18**
BY: **Sean Gonsalves**	REV: **A**	

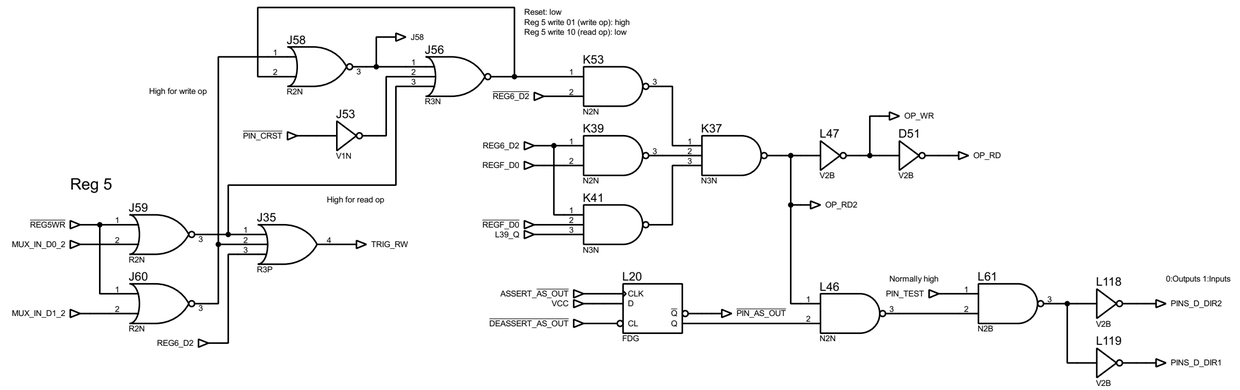


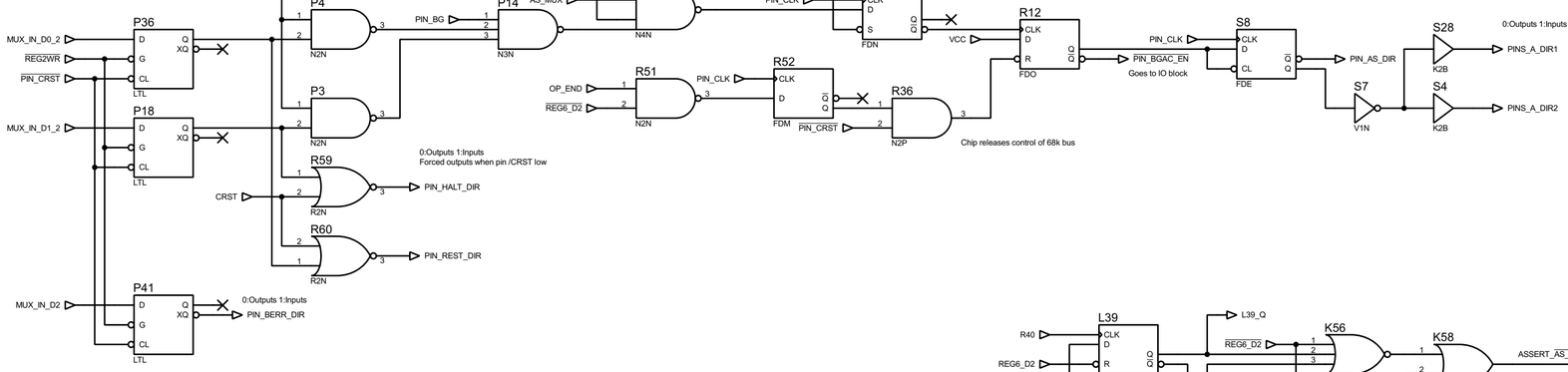
FILE NAME: **315-5195.pdsprj**		DATE: **02/08/2022**
DESIGN TITLE: **Sega 315-5195** MAPPING REGS BANK 7		PAGE: **8 of 18**
BY: **Sean Gonsalves**	REV: **A**	

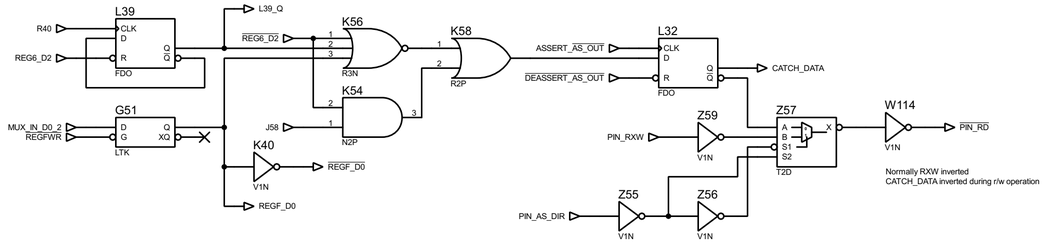
Reg 6



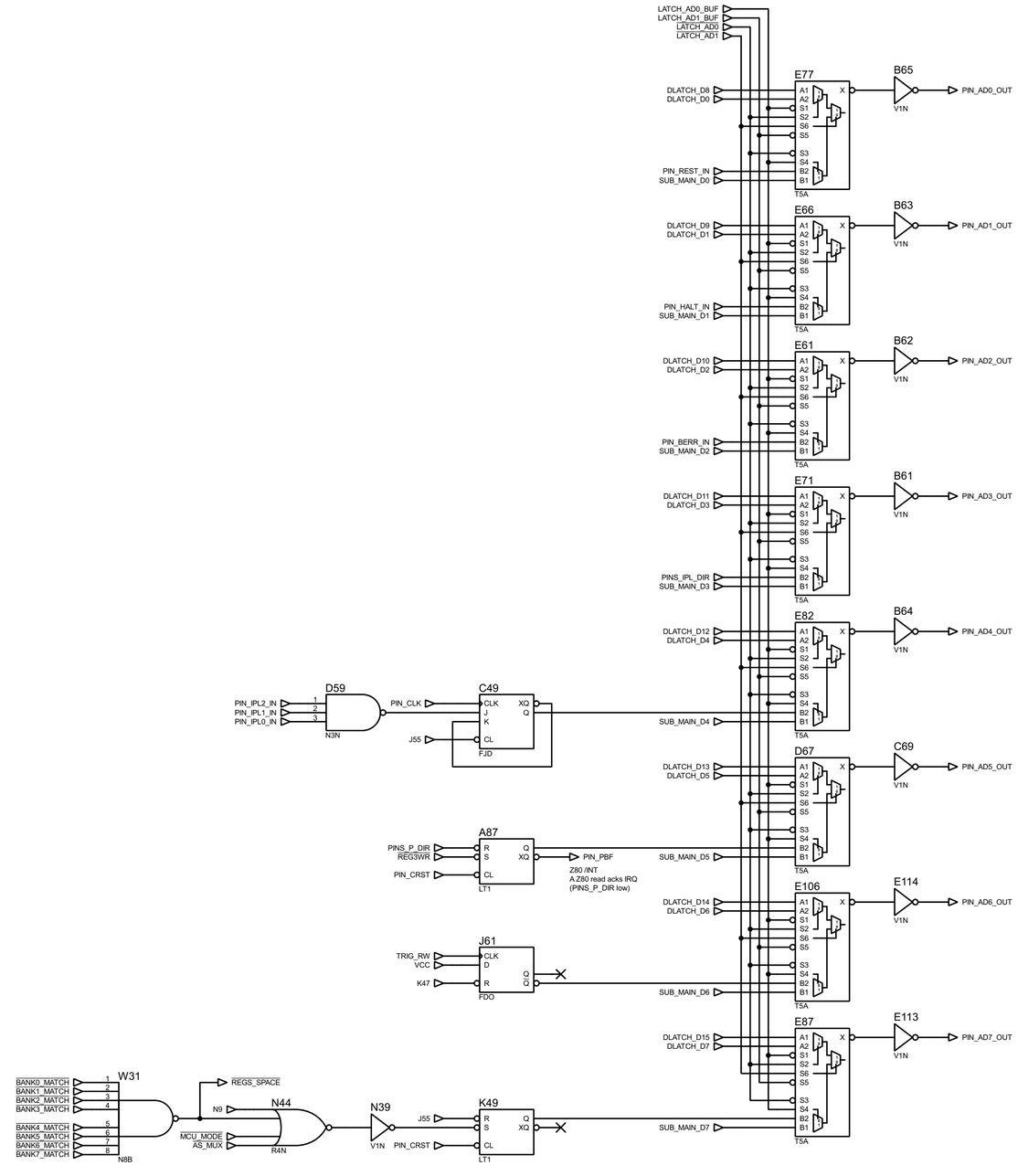
Reg 5





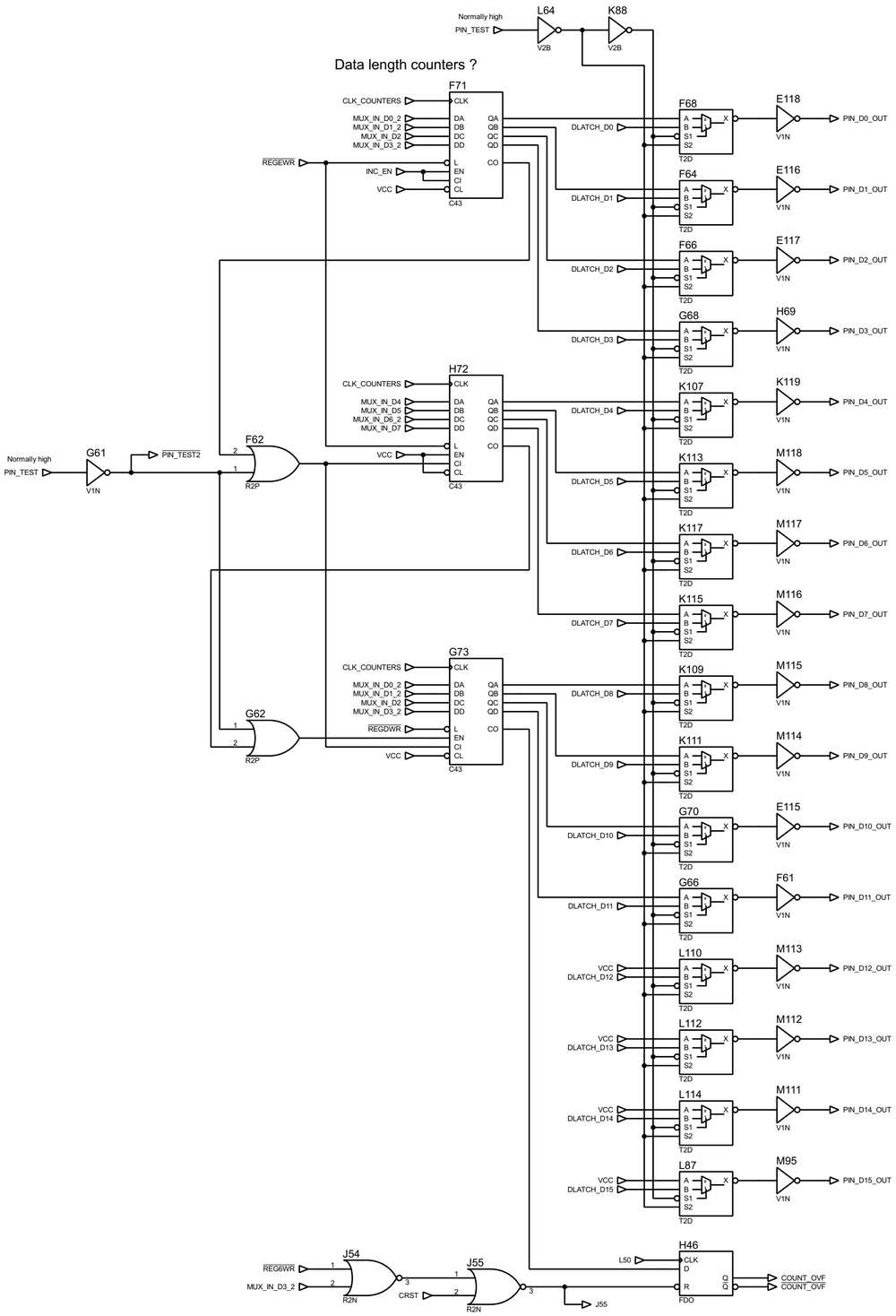


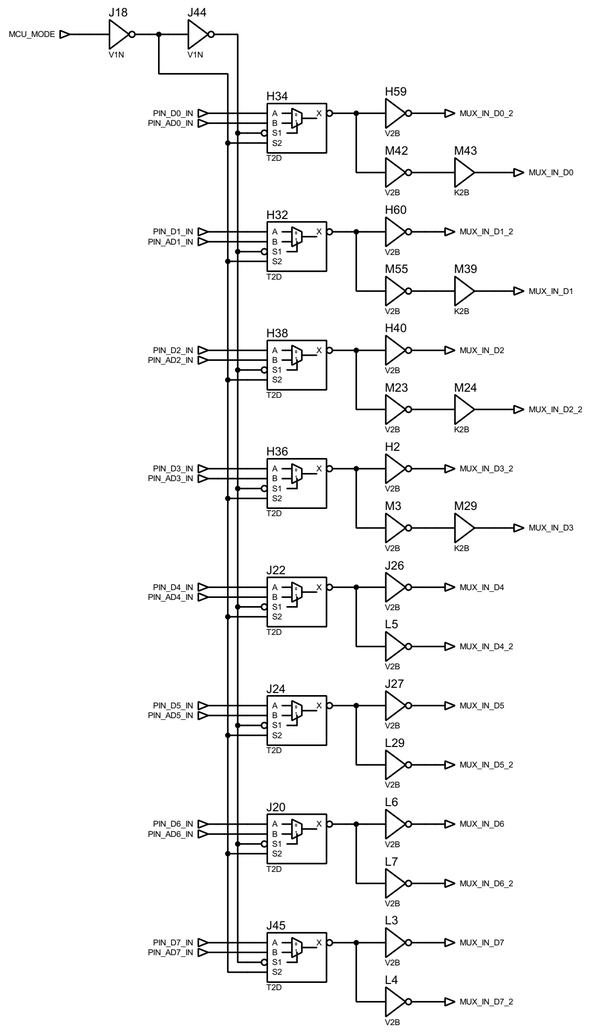
FILE NAME: 315-5195.pdsprj	DATE: 02/08/2022
DESIGN TITLE: Sega 315-5195 MISC	PAGE: 9 of 18
BY: Sean Gonsalves REV: A	



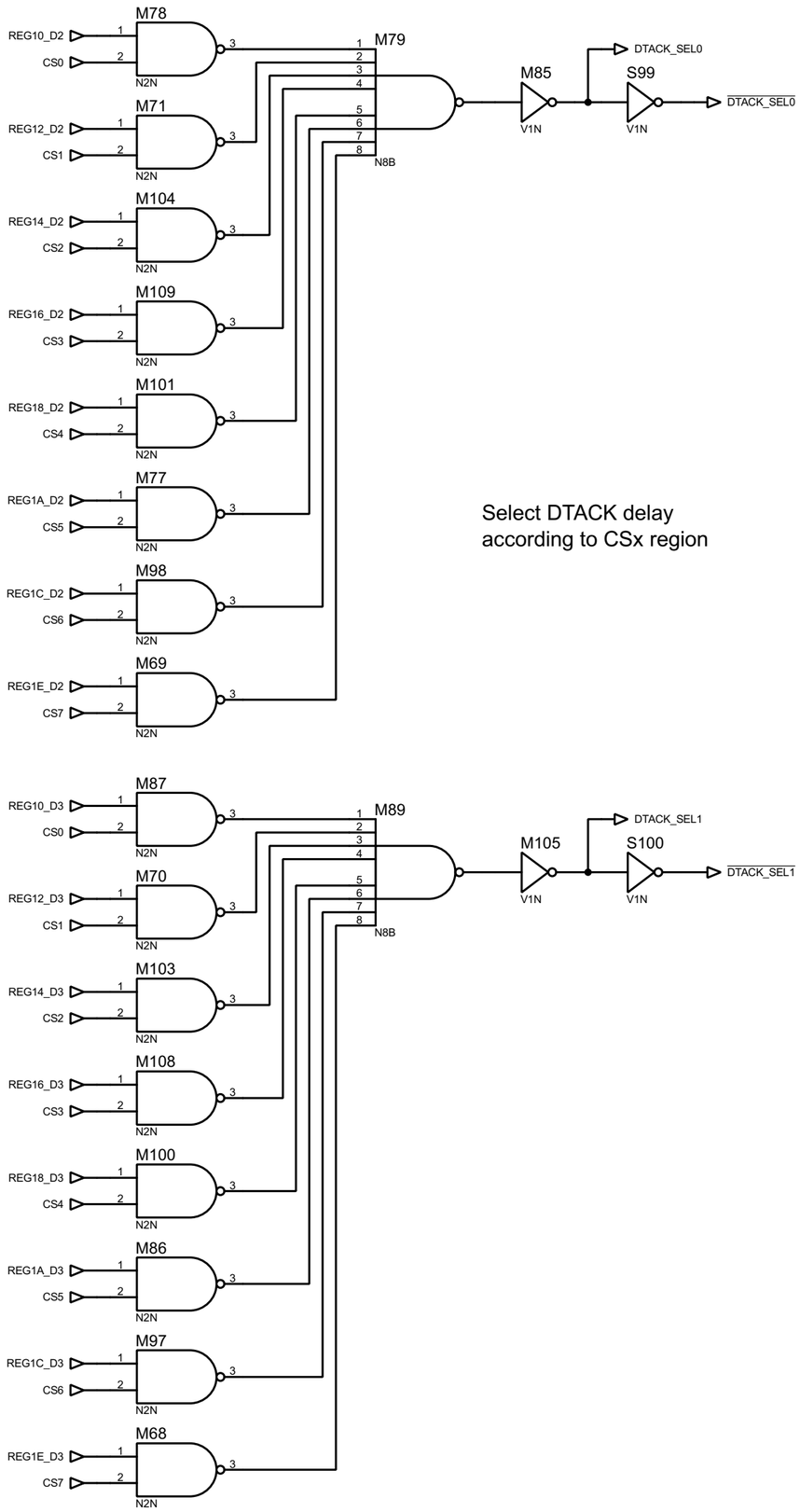
MCU read muxes:
00: Latch MSB
01: Latch LSB
02: Various 68k lines and status
03: Sub CPU latch data

FILE NAME: 315-5195.pdsprj		DATE: 02/08/2022
DESIGN TITLE: Sega 315-5195 MCU READ		PAGE: 10 of 18
BY: Sean Gonsalves	REV: A	



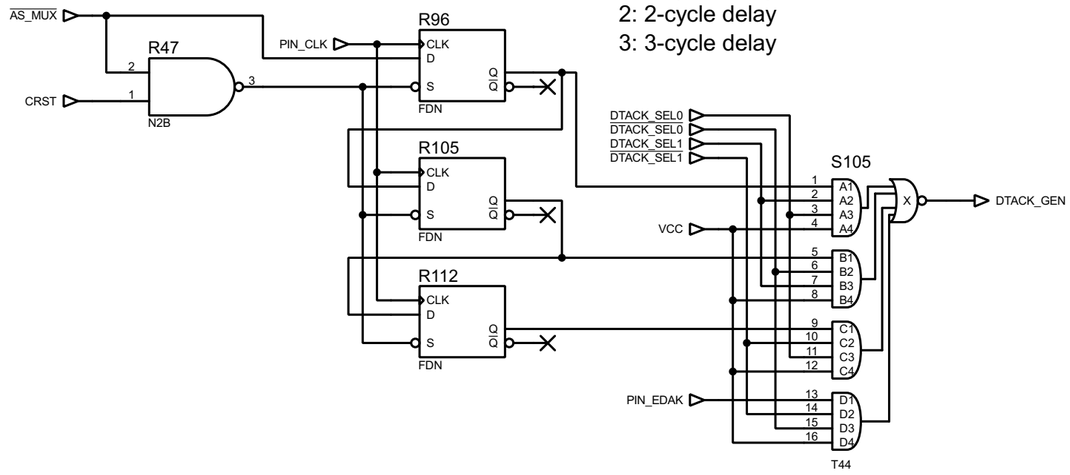


FILE NAME: 315-5195.pdsprj		DATE: 02/08/2022
DESIGN TITLE: Sega 315-5195 MAIN DATA OUT		PAGE: 11 of 18
BY: Sean Gonsalves	REV: A	



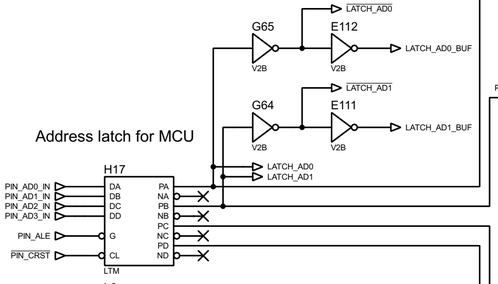
Select DTACK delay
according to CSx region

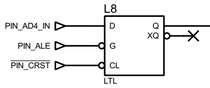
Bits [3:2] in configuration registers:
0: Use PIN_EDAK
1: 1-cycle delay
2: 2-cycle delay
3: 3-cycle delay

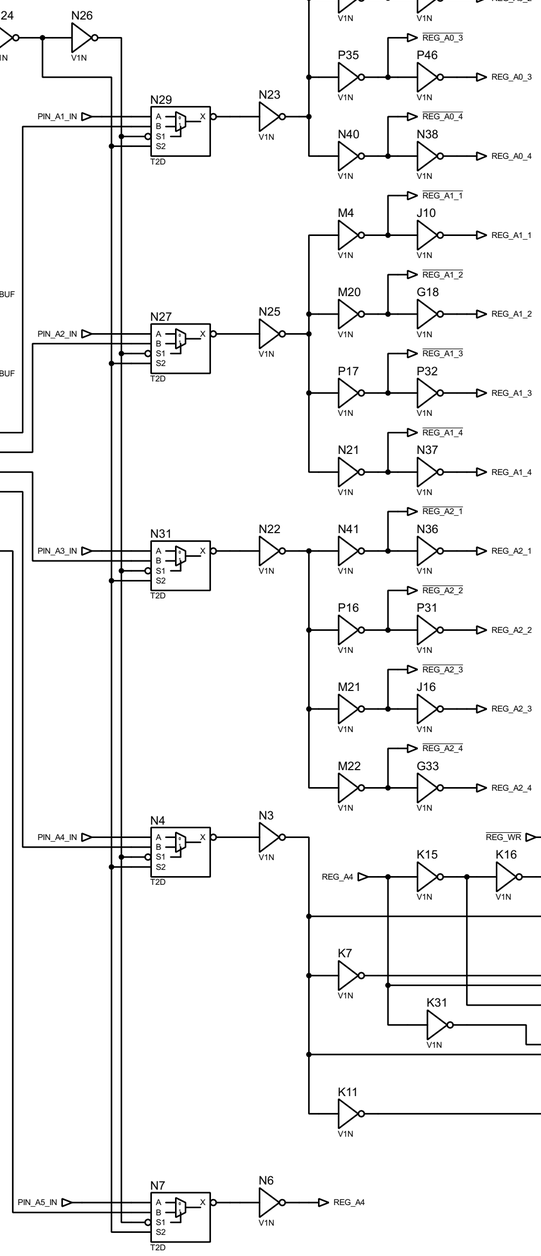


FILE NAME: 315-5195.pdsprj		DATE: 02/08/2022
DESIGN TITLE: Sega 315-5195 DTACK GEN		PAGE: 12 of 18
BY: Sean Gonsalves	REV: A	

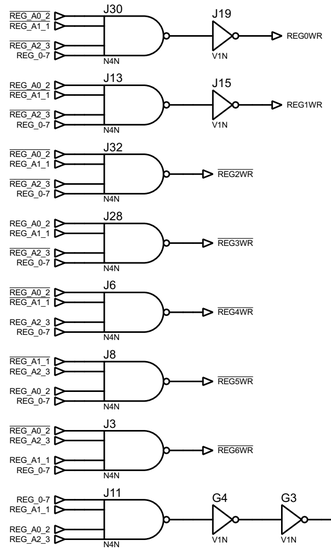
Address latch for MCU

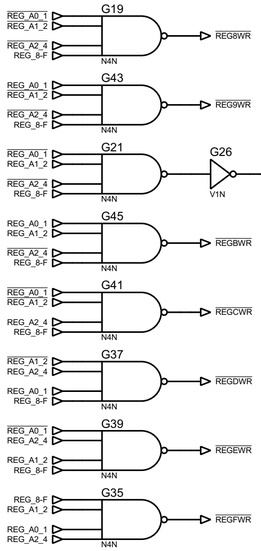


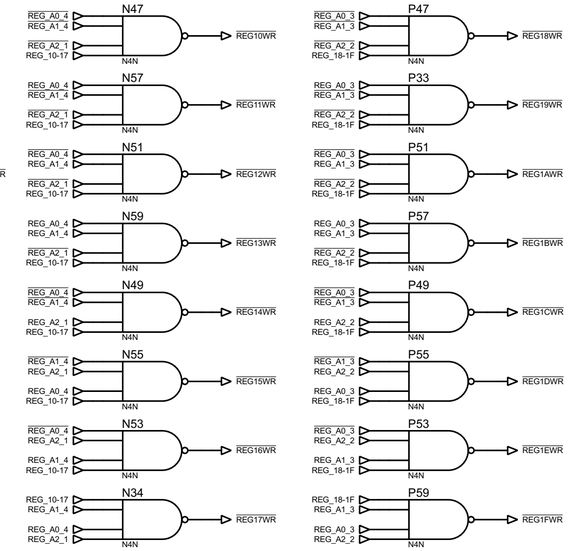




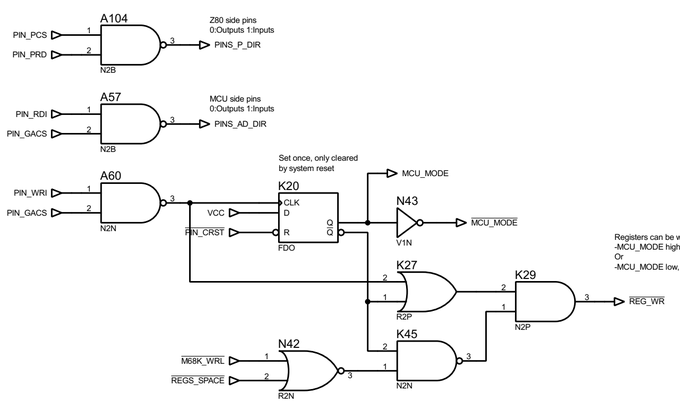

```
Reg Decoder Write
Ø   J30     Data to write
1   J13     Data to write
2   J32     Halt/reset control
3   J28 xx  68k -> Z80
4   J6      Set 68k IPL lines
5   J8      R/W control
6   J3      Op config

7   J11 xx  Write address
8   G19 xx
9   G43 xx

A   G21 xx  Read address
B   G45 xx
C   G41 xx

D   G37 x   Data length [11:8]
E   G39 xx  Data length [7:0]
F   G35     ??? Only D0 used

1Ø  N47 x   Size mask
11  N57 xx  Base
12  N51 x   Size mask
13  N59 xx  Base...
14  N49 x
15  N55 xx
16  N53 x
17  N34 xx
18  P47 x
19  P33 xx
1A  P51 x
1B  P57 xx
1C  P49 x
1D  P55 xx
1E  P53 x
1F  P59 xx
```



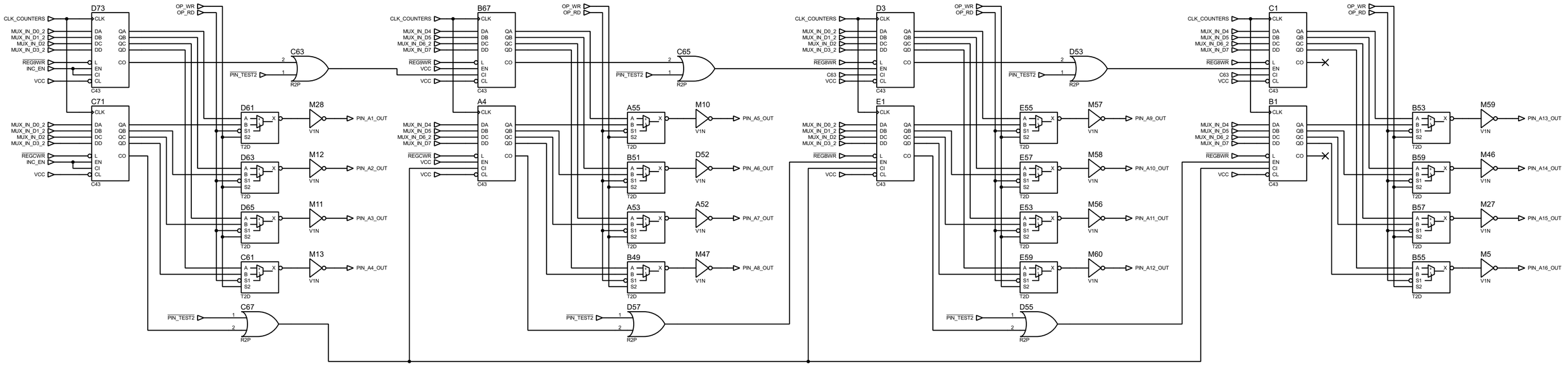


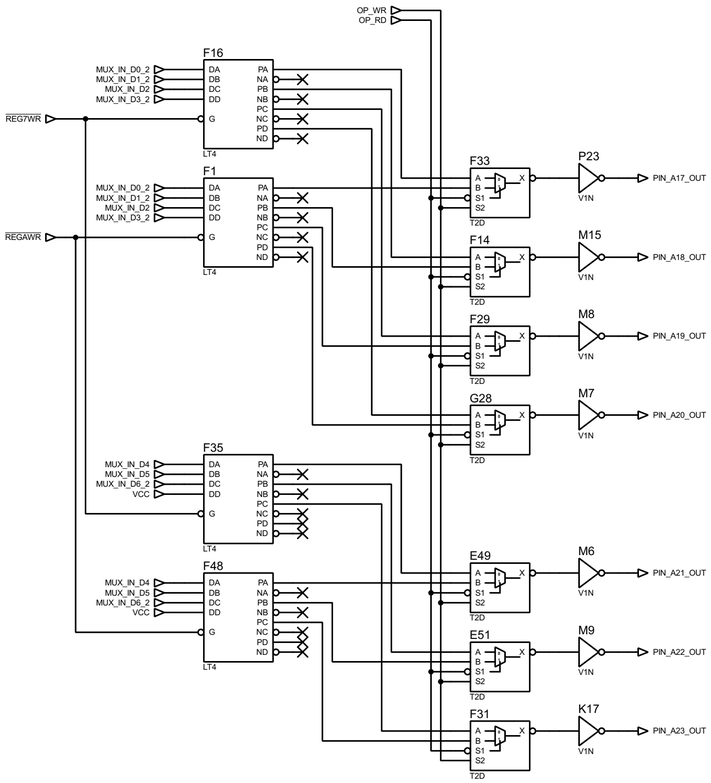


Broken area guesses

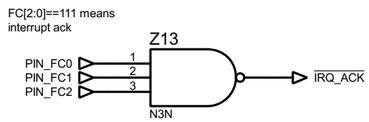


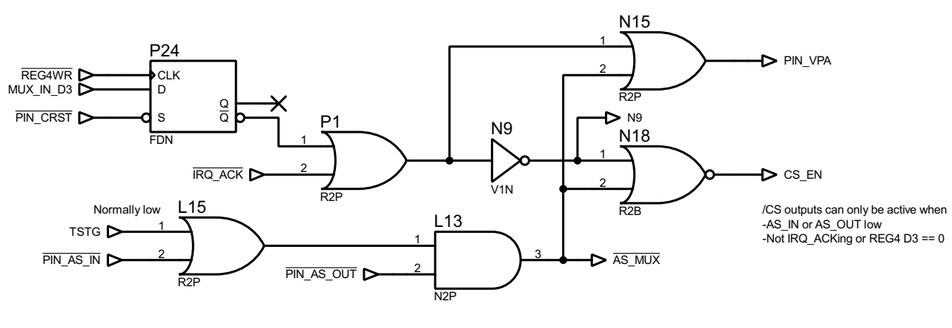
FILE NAME: 315-5195.pdsprj		DATE: 02/08/2022
DESIGN TITLE: Sega 315-5195 ADDRESS DECODING		PAGE: 13 of 18
BY: Sean Gonsalves	REV: A	

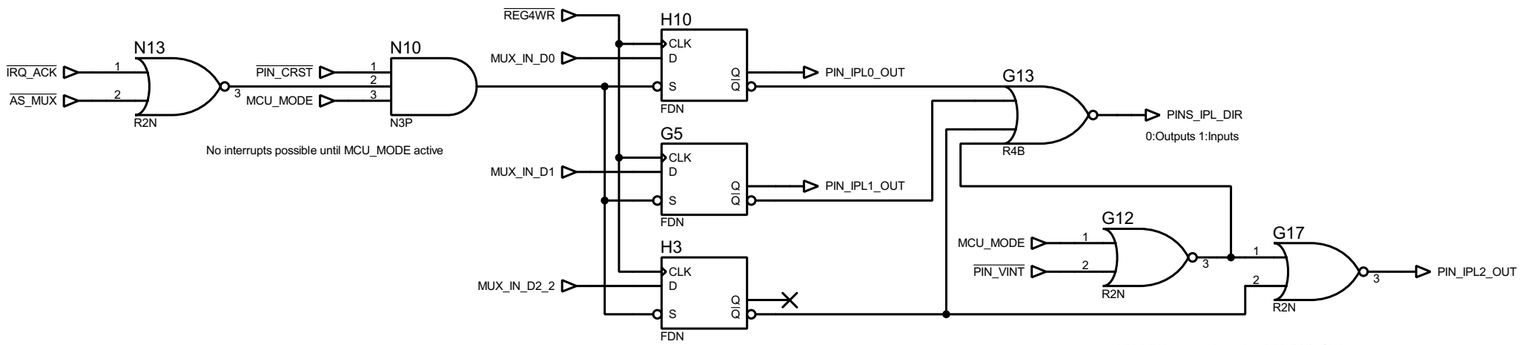


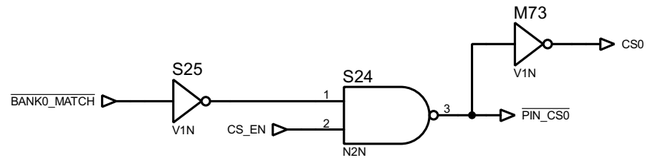


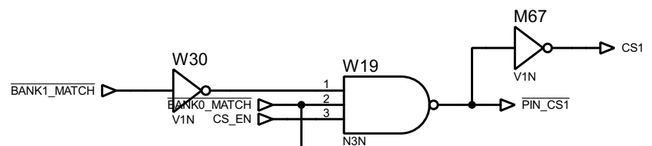
FILE NAME: **315-5195.pdsprj**		DATE: **02/08/2022**
DESIGN TITLE: **Sega 315-5195** ADDRESS COUNTERS		PAGE: **14 of 18**
BY: **Sean Gonsalves**	REV: **A**	

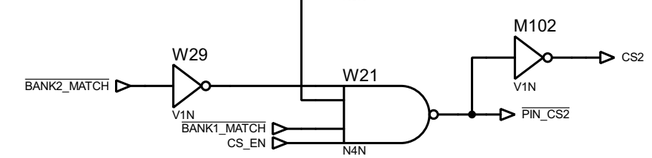


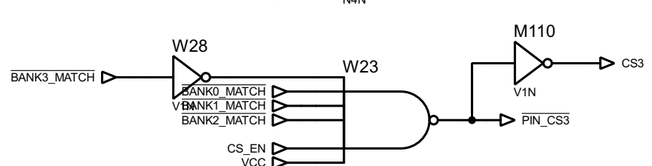


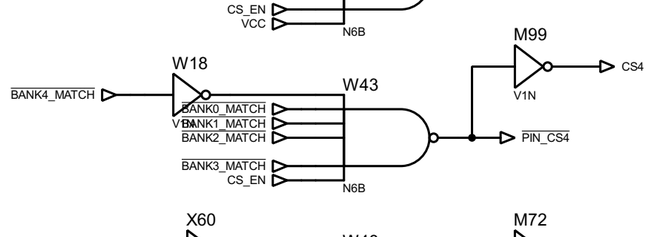


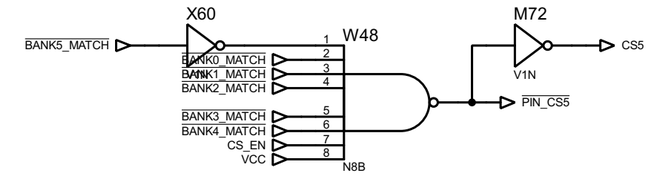


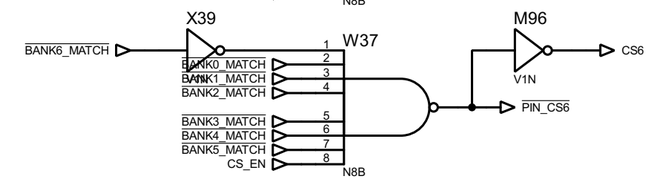


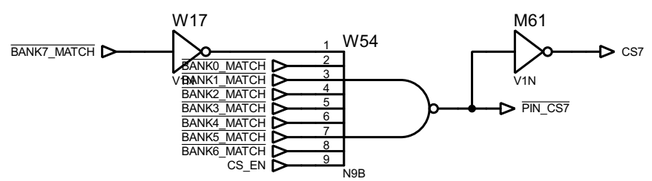




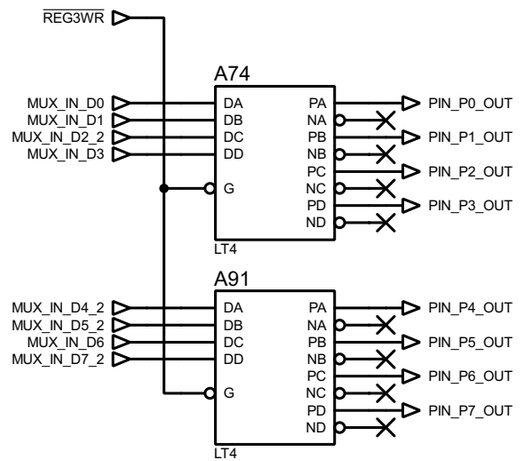


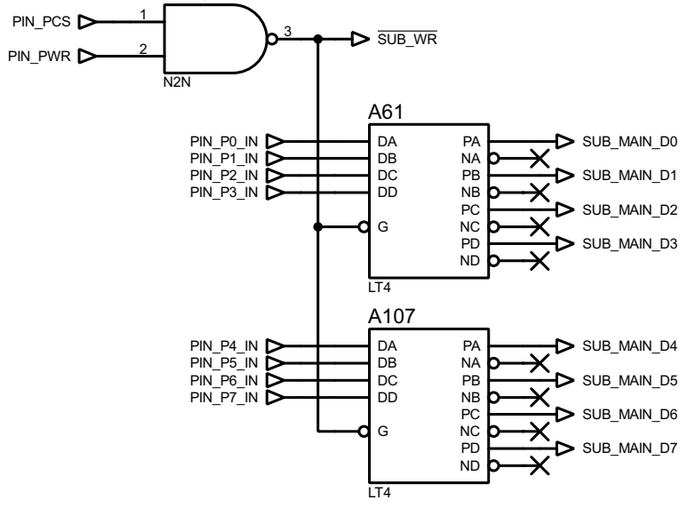




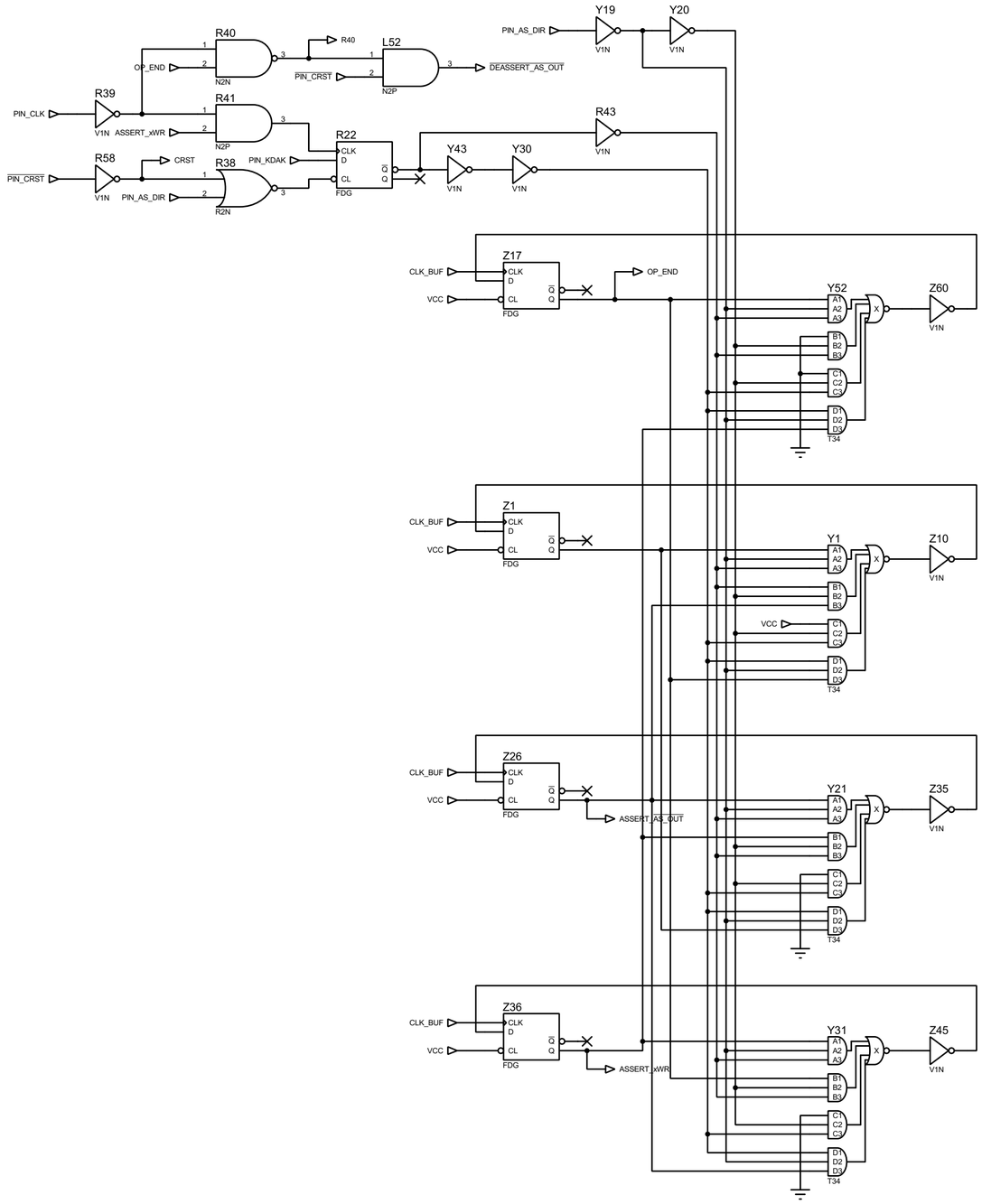


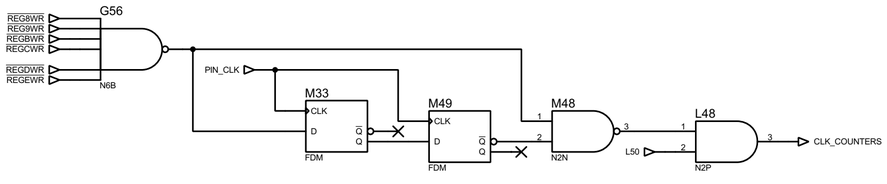
FILE NAME: **315-5195.pdsprj**		DATE: **02/08/2022**
DESIGN TITLE: **Sega 315-5195** CS AND INTERRUPTS		PAGE: **15 of 18**
BY: **Sean Gonsalves**	REV: **A**	

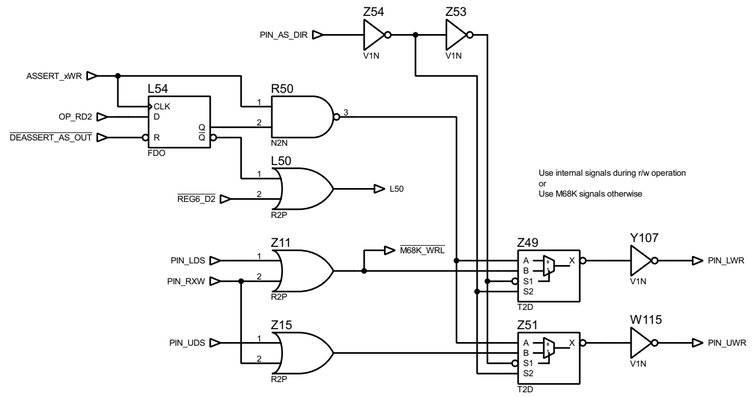




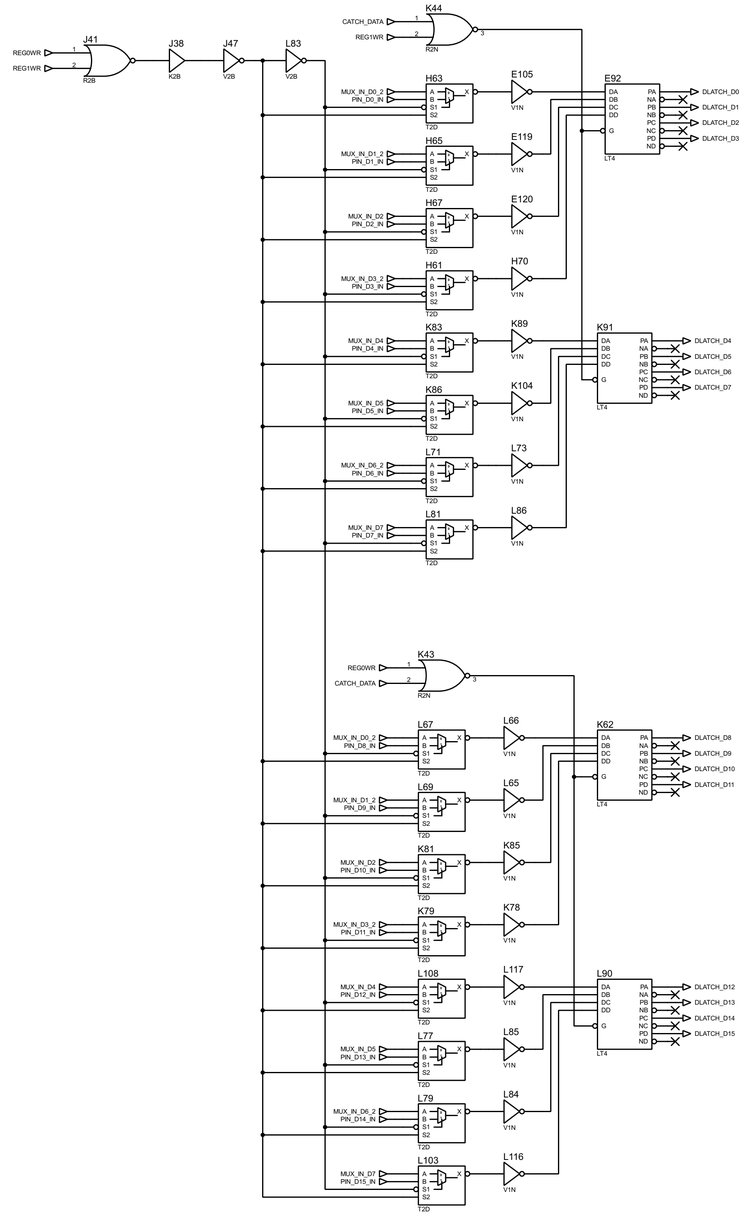
FILE NAME: **315-5195.pdsprj**	DATE: **02/08/2022**
DESIGN TITLE: **Sega 315-5195** MAIN / SUB COMM	PAGE: **16 of 18**
BY: **Sean Gonsalves** REV: **A**	







FILE NAME: 315-5195.pdsprj		DATE: 02/08/2022
DESIGN TITLE: Sega 315-5195 R/W STATE MACHINE		PAGE: 17 of 18
BY: Sean Gonsalves	REV: A	



FILE NAME: 315-5195.pdsprj	DATE: 02/08/2022
DESIGN TITLE: Sega 315-5195 DATA REGISTER	PAGE: 18 of 18
BY: Sean Gonsalves REV: A	