Name : Dipesh Digwal

Roll No. : 170121015

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Nano Sensor Data processor(NSDP) using quantum-dot cellular

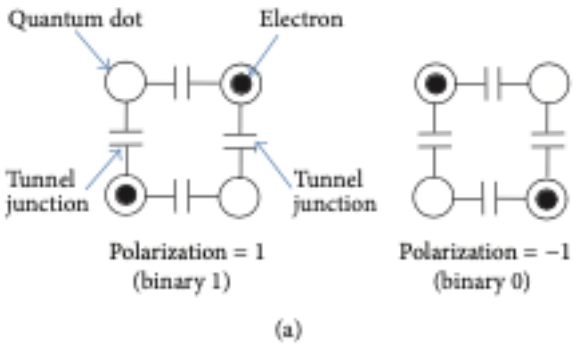
Objectives

- Analyse the structure of quantum-dot cellular automata(which is used the represent analogous bits of a classical computer)
- Using the QCA(Quantum-dot cellular automata) as a building blocks for the construction of a simple data processor(4-bit) which can be used in nano sensor data processing
- Compare the traditional MOSFET based data processors with the QCA processor.

Structure

QCA(Quantum-Dot Cellular Automata)

A QCA cell analogous to a MOSFET in operation, contains four quantum dots arranged at the corners of a cube. A QCA cell is given two electrons which by the properties of nanoscale quantum structures to tunnel can change there positions within quantum dots present in a QCA cell in two different ways which are restricted by Coulombic repulsions.



(a)

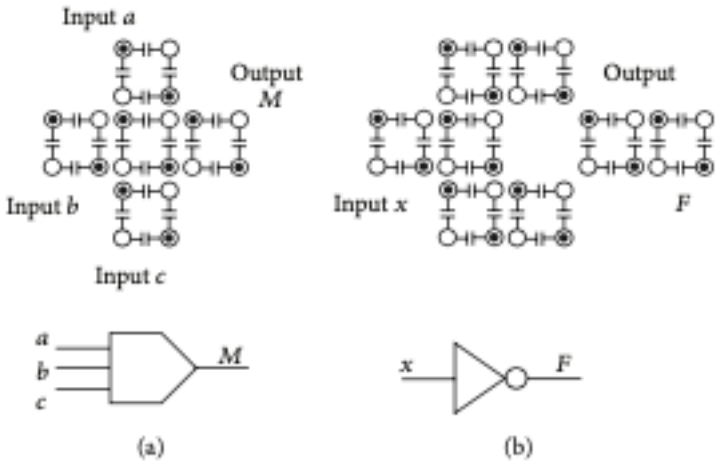
By adjacently joining QCA cells , we get a wire. This wire has a property of transferring information without current flow.

Methodology

QCA Logic Gates

All logic gates can be reproduced using two gates:

- 3-input majority gate ($M(a, b, c) = ab+bc+ac$)
- Inverters



Example:

AND Gate : AND$(a,b) = M(a,b,0) = ab$.

OR Gate : OR$(a, b) = M(a, b, 1) = ab + b \cdot 1 + a \cdot 1 = a + b$.

Analysis of the processor

QCA Clocking

For QCA Clocking we use Adiabatic switching. This switching technique reduces metastability issues and enable deep pipelines.

QCA Design Rules

• Layout Design Rules

1. Maximum number of cells in single clocking zone : 47 cells
2. Minimum number of cells in a single clocking zone : 1 cell (recommended value is 2 cells)
3. Minimum wire spacing for signal separation : space of 1 QCA cell
4. Wire crossover :
5. QCA Equivalent λ-Rule : Single cell size can be used as value of lambda.

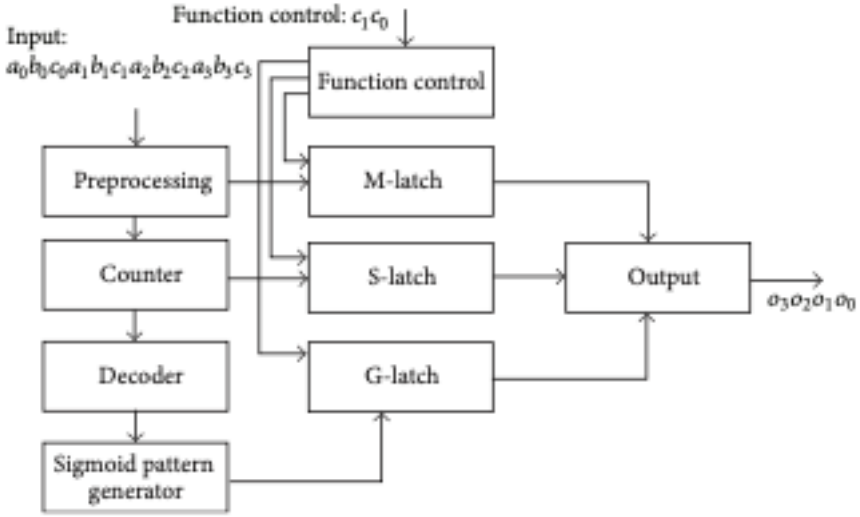
• Timing Design Rules

1. Logic Component Timing Rule : For QCA majority gate , inputs from all three input cells should reach centre cell at same time.
2. Clocking Zone Assignment Rule : cells in each clocking zone must be synchronised.

NSDP(Nano Sensor Data Processor) Architecture

Requirements from a NSDP:

A. Bridge the preprocessed data which is arriving from sensor to a high-level processor(as in modern computers)
B. Calculate the population of active majority gates.
C. Output a approximate sigmoid function which can be directly used processor designed for Artificial neural network(ANN) application.



Preprocessing

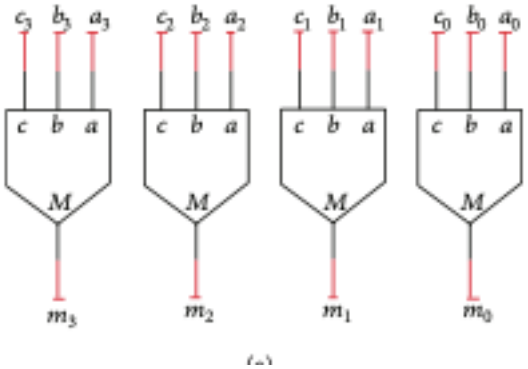
This operation is used to implement majority operation to identify which one from “0” or “1” have majority.

$m_0 = M(a_0, b_0, c_0),$

$m_1 = M(a_1, b_1, c_1),$

$m_2 = M(a_2, b_2, c_2),$

$m_3 = M(a_3, b_3, c_3)$

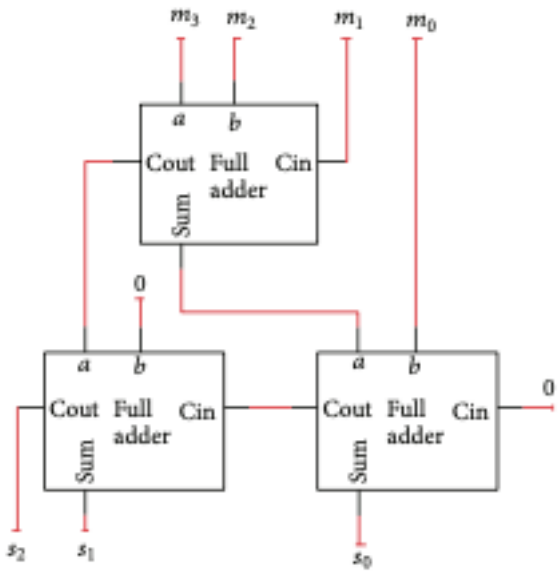


This operation takes 3/4 clock cycles to complete.

Counter

Two Output terminals from Preprocessing unit are fed to M-latch and Counter subunits.
Output of this subunit is given by the formula

$s_2 s_1 s_0 = m_3 + m_2 + m_1 + m_0$



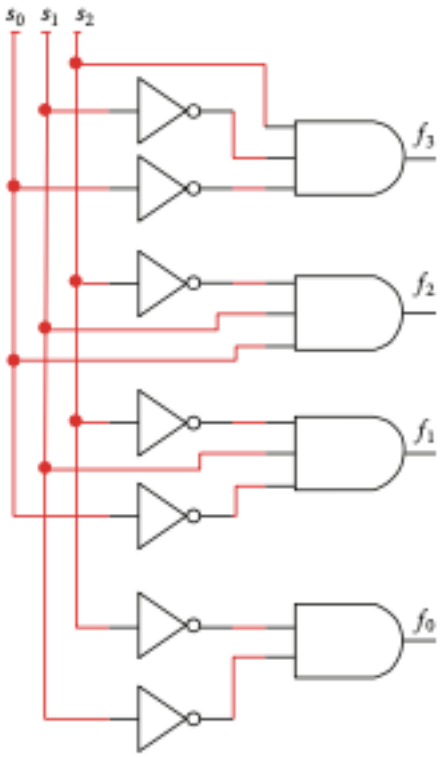
Decoder

Output of this unit is given by

$f_1 = s_2\, s_1$,

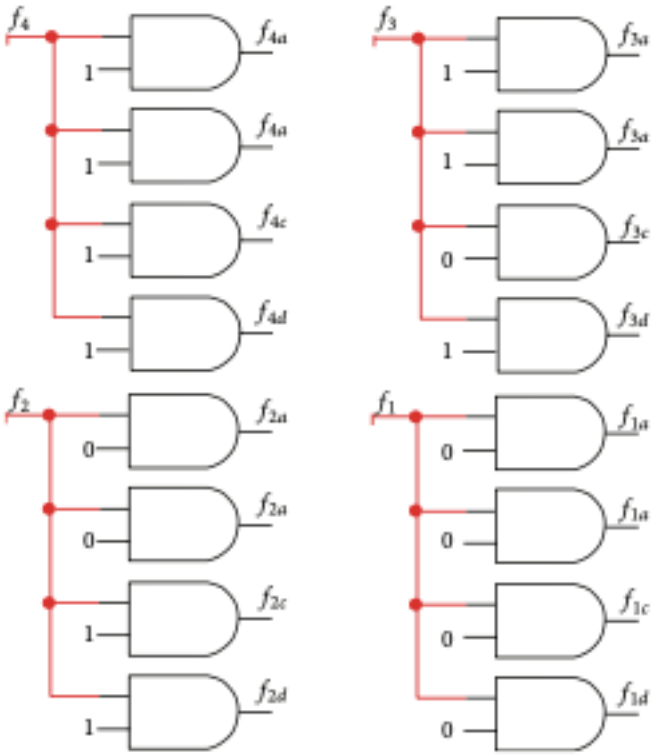
$f_2 = s_2 s_1 s_0$,

$f_3 = s_2 s_1 s_0$,



$f_4 = s_2 s_1\, s_0$

Pattern Generator

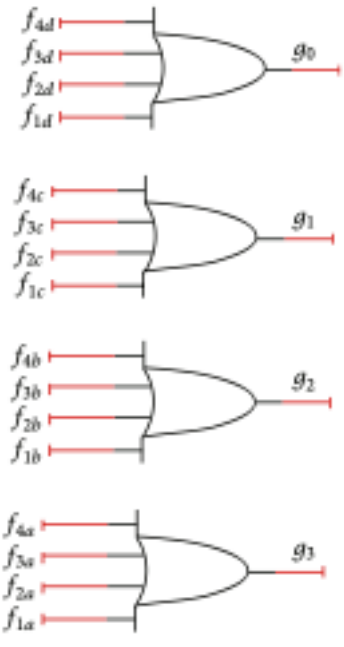


Sigmoid Function Output

$g_3 = f_{4a} + f_{3a} + f_{2a} + f_{1a}$,

$g_2 = f_{4b} + f_{3b} + f_{2b} + f_{1b}$,

$g_1 = f_{4c} + f_{3c} + f_{2c} + f_{1c}$,



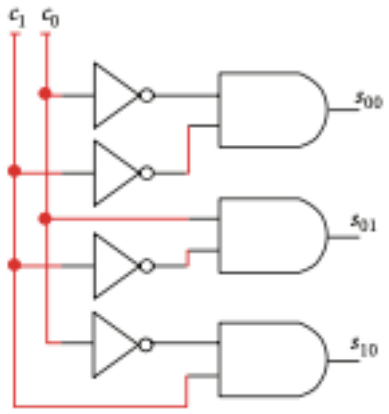
$$g_0 = f_{4d} + f_{3d} + f_{2d} + f_{1d}$$

Function Control

$s_{00} = c_1\, c_0,$

$s_{01} = c_1 c_0,$

$s_{10} = c_1 c_0.$



Output

This is decided by the appropriate control signals to control unit . This output can be either of the three subunits implemented above ,i.e,

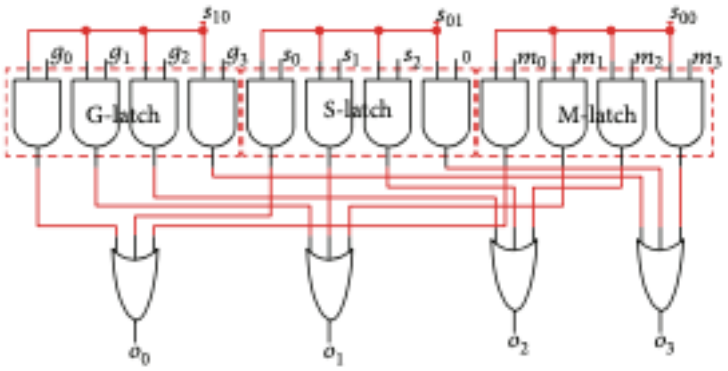
- Raw majority data
- Number of active majority gates
- Sigmoid function

$o_3 = m_3 s_{00} + 0 \cdot s_{01} + g_3 s_{10},$

$o_2 = m_2 s_{00} + s_2 \cdot s_{01} + g_2 s_{10},$

$o_1 = m_1 s_{00} + s_1 \cdot s_{01} + g_1 s_{10},$

$o_0 = m_0 s_{00} + s_0 \cdot s_{01} + g_0 s_{10}.$


s_{10}
s_{01}
s_{00}
g_0 g_1 g_2 g_3
s_0 s_1 s_2 0
m_0 m_1 m_2 m_3
G-latch
S-latch
M-latch
o_0
o_1
o_2
o_3

Applications

- Nanosensor data processing
- QCA based error detection circuit

Conclusion

- Alternative structure of classical computers building blocks was analysed.
- NSDP construction is rigorously analysed.
- Wire length and timing of the circuits using QCA vary drastically than MOSFET based classical bits.

References

- Fenghui Yao, Mohamed Saleh Zein-Sabatto, Guifeng Shao, Mohammad Bodruzzaman and Mohan Malkani , Nanosensor Data Processor in Quantum-Dot Cellular Automata , Journal of Nanotechnology , 2014 , 2