Project Phase 2 Instruction Timeline

Due Apr 8 at 11:59pmPoints 3Questions 1Time Limit None

Allowed Attempts Unlimited

Instructions

As part of Phase 2 of the project, you must create and submit a document which should explain the behavior of your processor for the perf-test-dep-ldst.asm test. You may choose to submit this electronically or as a PDF as part of your submission. This exercise is where you would do it electronically. Regardless of which mechanism you use, you will get credit.

Note: The Canvas "quiz" here assumes you are doing Phase 2 without forwarding (i.e., RF bypassing and otherwise stalling). If you added forwarding logic and your answer is correct for the version with forwarding, we will give you back points after the deadline.

See https://pages.cs.wisc.edu/~sinclair/courses/cs552/spring2023/handouts/project/cs552-spring2023-project-all.pdf

(https://pages.cs.wisc.edu/~sinclair/courses/cs552/spring2023/handouts/project/cs552-spring2023-project-all.pdf) for details about the project, including about the instruction timeline you need to submit.

Take the Quiz Again

Attempt History

	Attempt	Time	Score
KEPT	Attempt 7	5 minutes	2.79 out of 3
LATEST	Attempt 9	4 minutes	1.82 out of 3
	Attempt 8	3 minutes	1.66 out of 3
	Attempt 7	5 minutes	2.79 out of 3
	Attempt 6	5 minutes	2.04 out of 3
	Attempt 5	8 minutes	1.93 out of 3
	Attempt 4	4 minutes	1.71 out of 3
	Attempt 3	less than 1 minute	2.04 out of 3
	Attempt 2	4 minutes	1.88 out of 3

At	tempt	Time	Score
Att	tempt 1	11 minutes	1.18 out of 3

Score for this attempt: 1.82 out of 3

Submitted Apr 11 at 1:23am This attempt took 4 minutes.

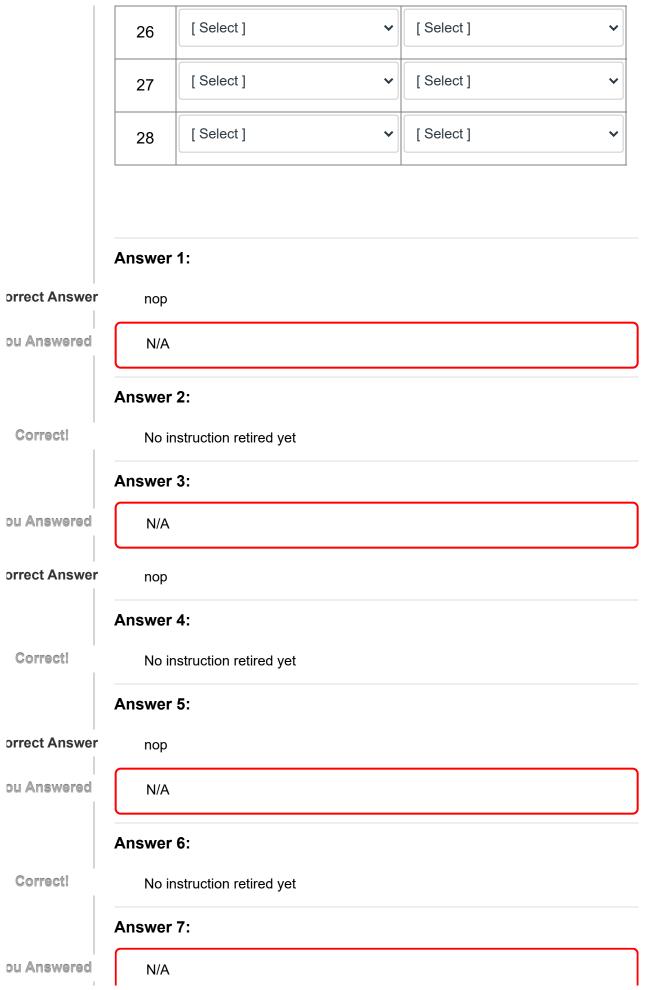
Question 1 1.82 / 3 pts

Explain the behavior of your processor for the perf-test-dep-ldst.asm test. We have provided you with more rows than are necessary. If a row is not needed, please use "N/A".

For each cycle, fill in the instruction retired (we will discuss what retired means in class, but essentially for our 5-stage in-order processor it means what is in Write Back that cycle) would either be one of the instructions from the test program or a "NOP" if dependencies necessitate any stall cycles. The reason column would explain why a stall was needed in that instance or "N/A" if no stall is needed.

Cycle	Instruction Retired	Reason
1	[Select]	[Select] v
2	[Select]	[Select] v
3	[Select]	[Select] v
4	[Select]	[Select] 🗸
5	[Select]	[Select] 🗸
6	[Select]	[Select] 🗸
7	[Select]	[Select] 🗸

8	[Select]	[Select]
9	[Select]	[Select]
10	[Select]	[Select]
11	[Select]	[Select]
12	[Select]	[Select]
13	[Select]	[Select]
14	[Select]	[Select]
15	[Select]	[Select]
16	[Select]	[Select]
17	[Select]	[Select]
18	[Select]	N/A
19	[Select]	[Select]
20	[Select]	[Select]
21	[Select]	[Select]
22	[Select]	[Select]
23	[Select]	[Select]
24	[Select]	[Select]
25	[Select]	[Select] v



orrect Answer	nop
	Answer 8:
Correct!	No instruction retired yet
	Answer 9:
Correct!	lbi r0, 0
	Answer 10:
Correct!	N/A
	Answer 11:
Correct!	lbi r5, 43
	Answer 12:
Correct!	N/A
	Answer 13:
Correct!	lbi r6, 43
	Answer 14:
Correct!	N/A
	Answer 15:
Correct!	lbi r7, 43
	Answer 16:
Correct!	N/A
	Answer 17:
Correct!	ld r1, r0, 0
	Answer 18:
Correct!	N/A

	,
	Answer 19:
Correct!	nop
	Answer 20:
Correct!	RAW hazard on r1
	Answer 21:
ou Answered	st r5, r1, 0
orrect Answer	nop
	Answer 22:
orrect Answer	RAW hazard on r1
ou Answered	N/A
	Answer 23:
ou Answered	ld r1, r0, 2
orrect Answer	st r5, r1, 0
	Answer 24:
Correct!	N/A
	Answer 25:
ou Answered	nop
orrect Answer	ld r1, r0, 2
	Answer 26:
orrect Answer	N/A
ou Answered	RAW hazard on r1
	Answer 27:

	Answer 42:
Correct!	N/A
	Answer 43:
Correct!	N/A
	Answer 44:
Correct!	N/A
	Answer 45:
Correct!	N/A
	Answer 46:
Correct!	N/A
	Answer 47:
Correct!	N/A
	Answer 48:
Correct!	N/A
	Answer 49:
Correct!	N/A
	Answer 50:
Correct!	N/A
	Answer 51:
Correct!	N/A
	Answer 52:
Correct!	N/A
	Answer 53:

4/13/23, 5:33 PM	Project	Phase 2 Instruction Timeline: COMPSCI552: Introduction to Computer Architecture (001) SP23
Correct!	N/A	
	Answer 54:	
Correct!	N/A	
	Answer 55:	
Correct!	N/A	
	Answer 56:	
Correct!	N/A	

Quiz Score: 1.82 out of 3