Operational Transconductance Amplifier (OTA) in 45nm CMOS

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Remark

1. Incompletion of Test measurements

2. Plotting works in slides are in low quality.

Outline

1. Introduction
2. Design Summary
3. Simulation and Analytical Results
4. Conclusions

[1] Introduction - 1

1. Statement of the problem

- Designing a fully differential OTA to meet the required spec

2. Main challenges

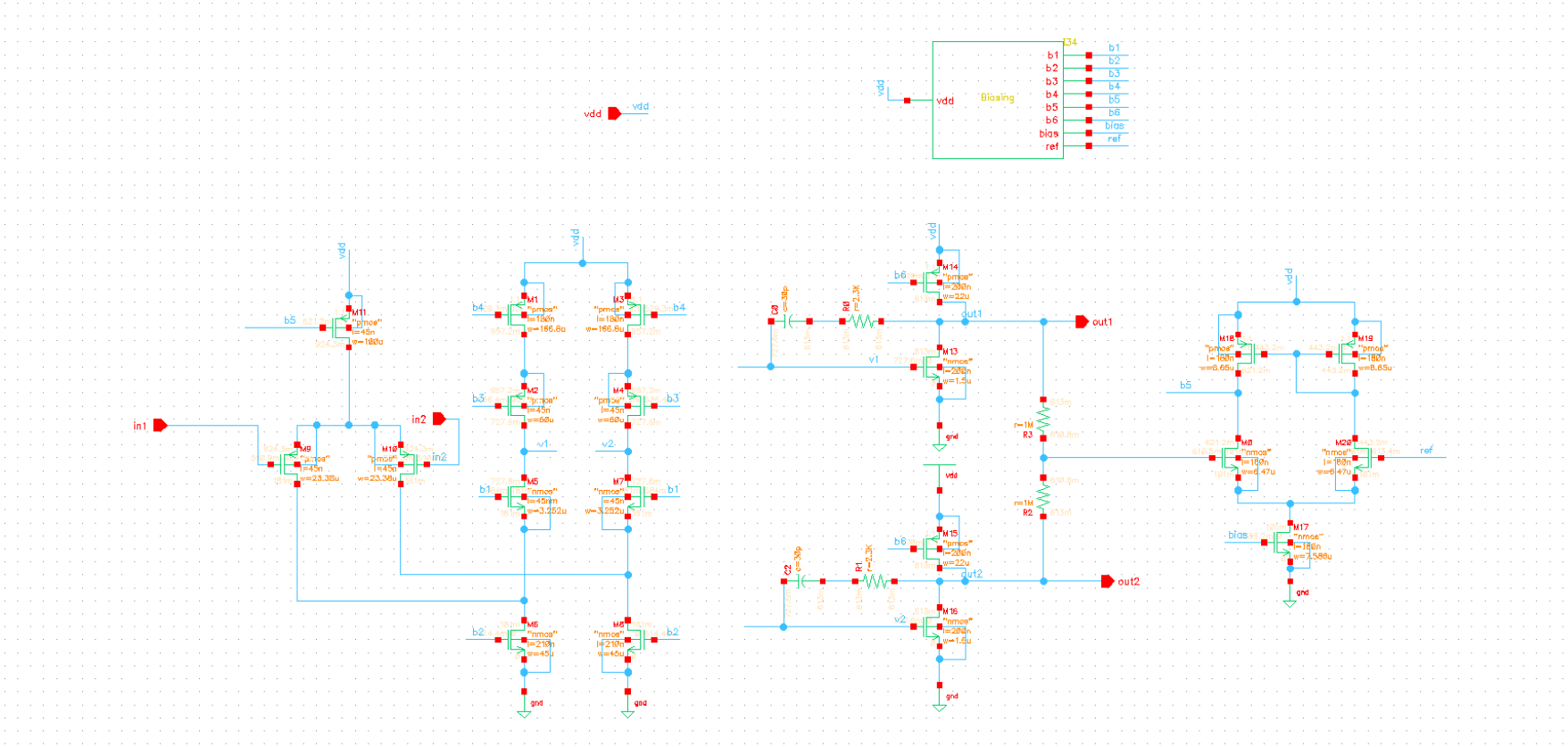
- Low Vdd : Overdrive Voltage Budget Issue
- 45nm technology : Biasing issue
- Large GBW product

[1] Introduction - 2

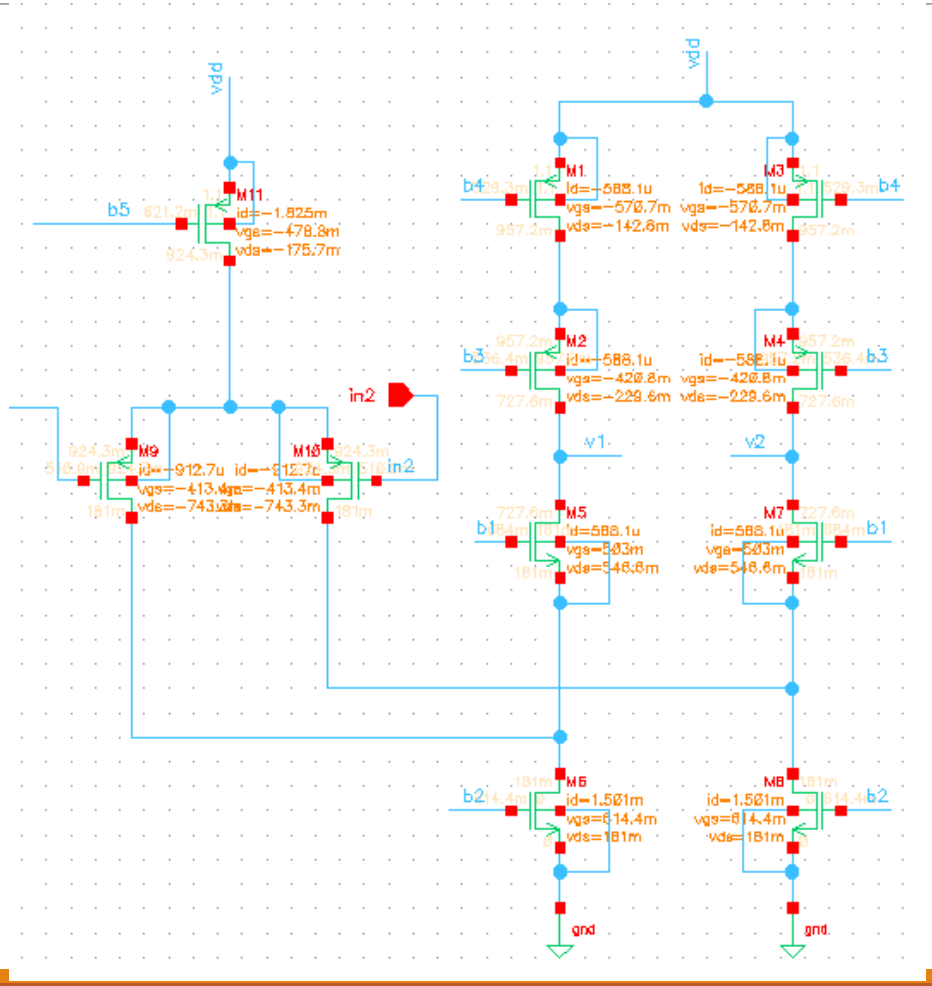
3. General approach

- Characterize the device
- Select a topology based on the required spec
- Bias and Size accordingly
- Tune the circuit for better performance

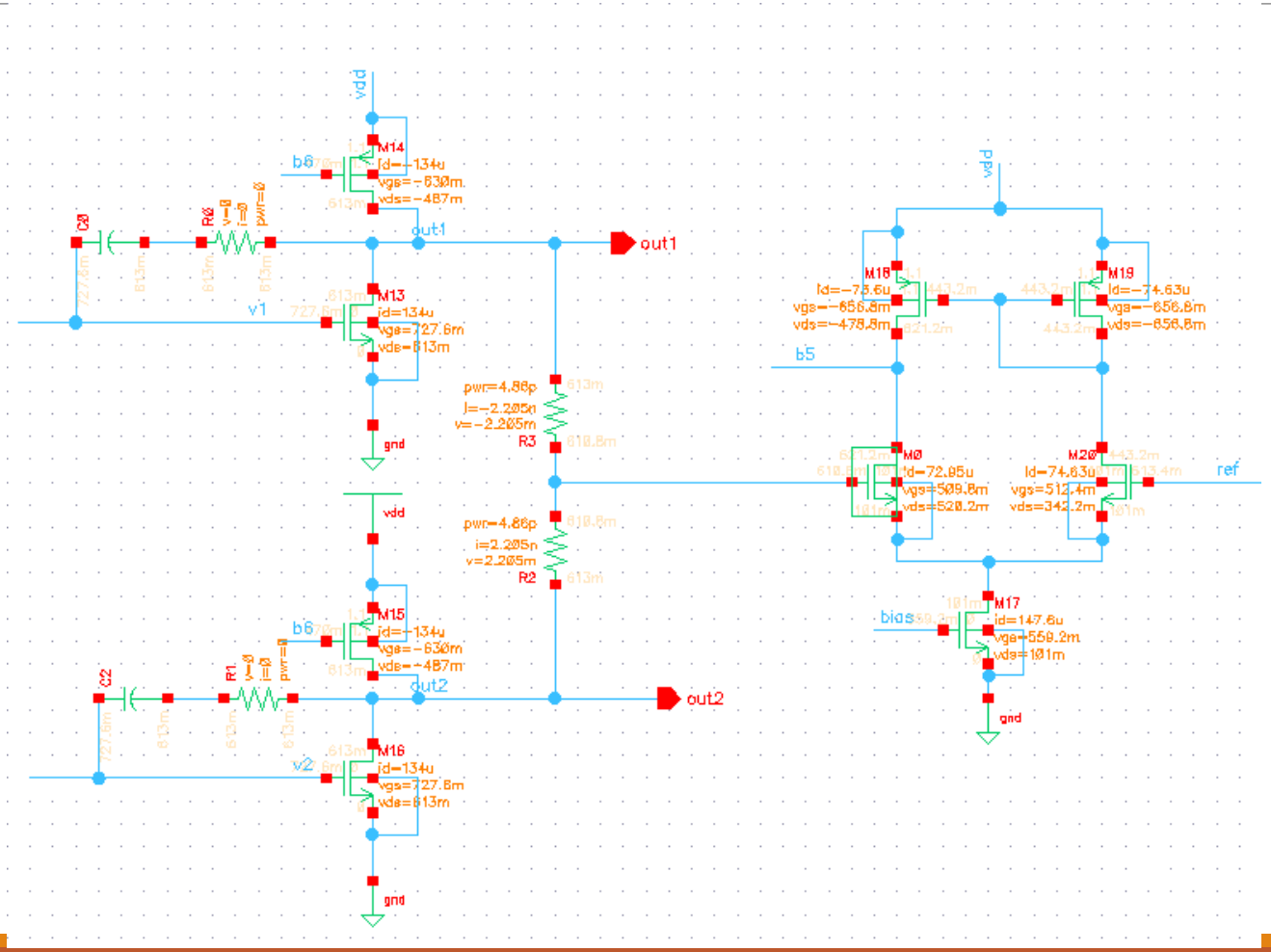
[2] Design Summary - Overview



[2] Design Summary – DC operating points(1)



[2] Design Summary – DC operating points(2)



[2] Design Summary – Device Sizing

Transistors	W/L	Transistors	W/L	Transistors	W/L
M1	166.8u/180n	M8	45u/210n	M16	1.5u/200n
M2	60u/45n	M9	23.38u/45n	M17	7.586u/180n
M3	166.8u/180n	M10	23.38u/45n	M18	8.65u/180n
M4	60u/45n	M11	100u/45n	M19	8.65u/180n
M5	3.252u/45n	M13	1.5u/200n	M20	6.47u/180n
M6	45u/210n	M14	22u/200n	M0	6.47u/180n
M7	3.252u/45n	M15	22u/200n		

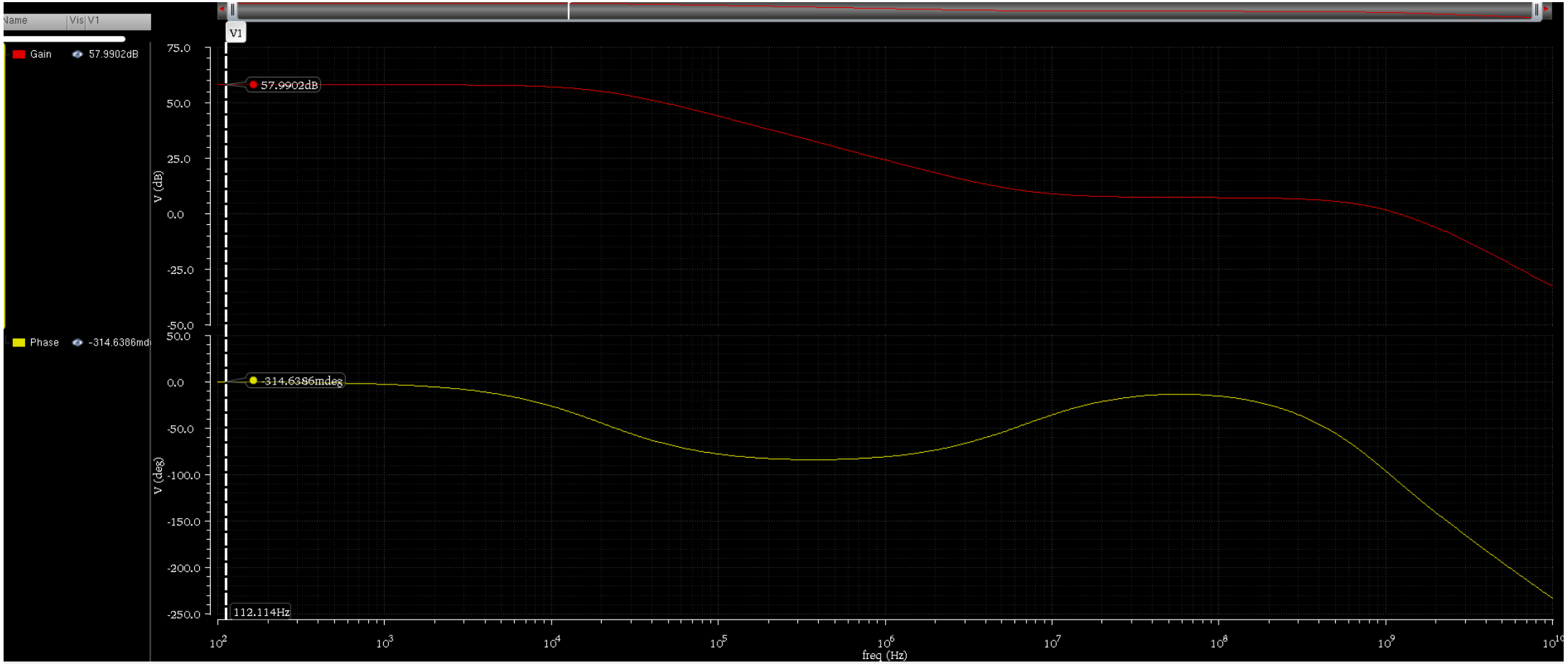
(1) Design Strategy

- Two stages Folded Cascode Structure
- Frequency Compensation
- Common Mode Feedback circuitry

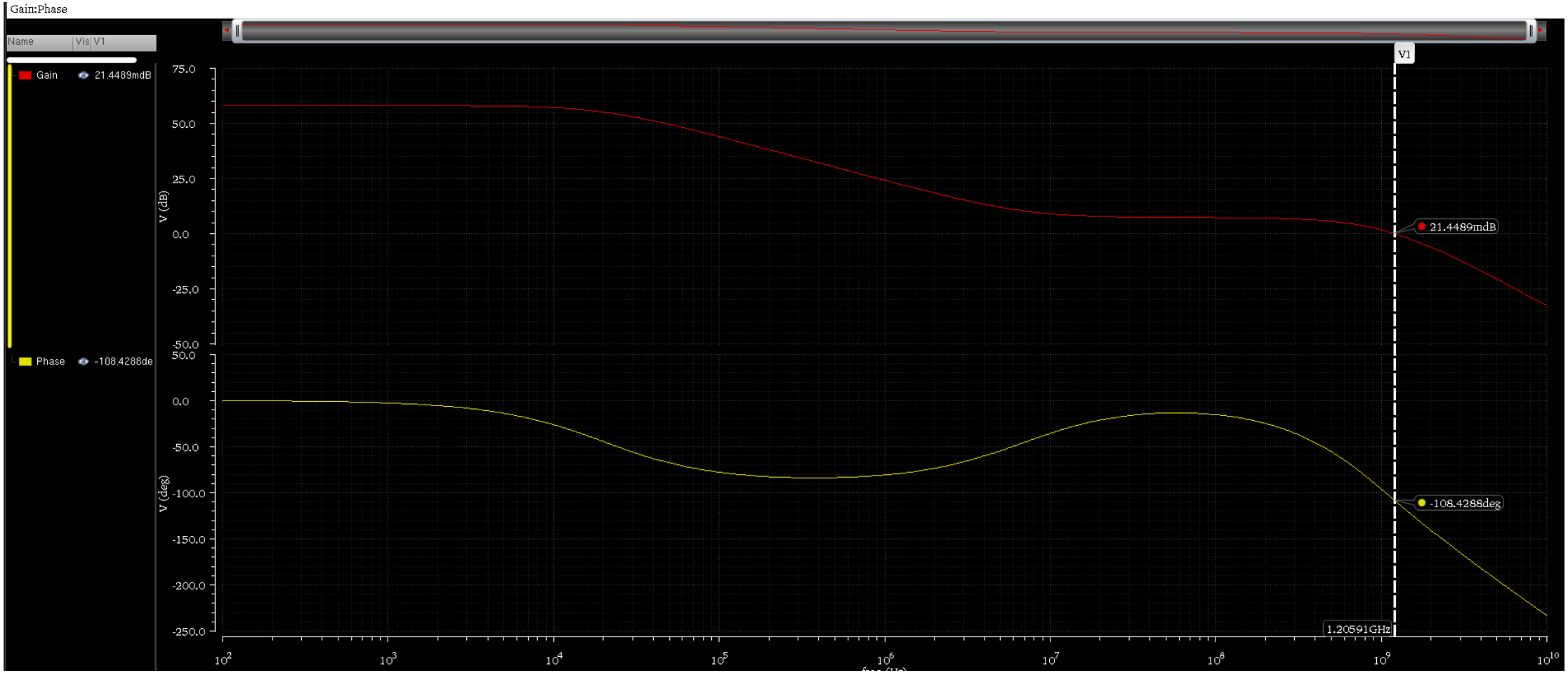
(2) Design Methdology

- Overdrive Voltage Budget Plan
- Sizing independent Biasing Method
- Gain boosting ideas

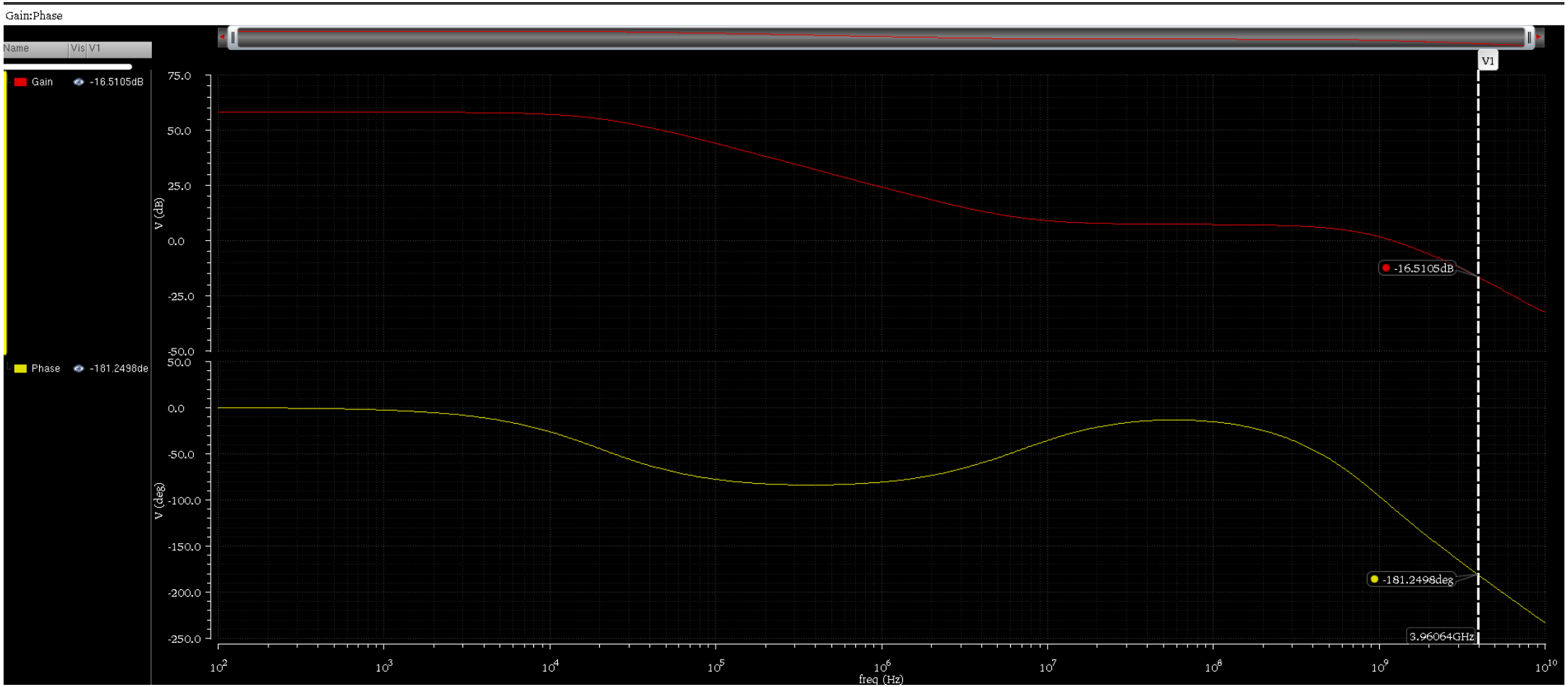
[3] Simulation Result – Closed loop gain 58 dB



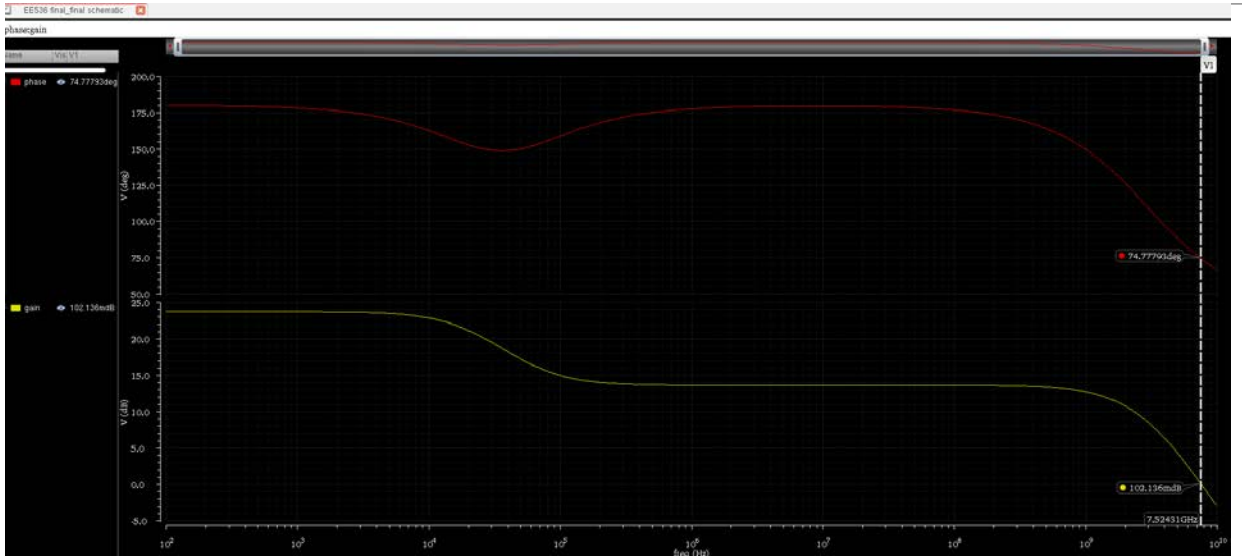
[3] Phase Margin – Closed ; 72dB

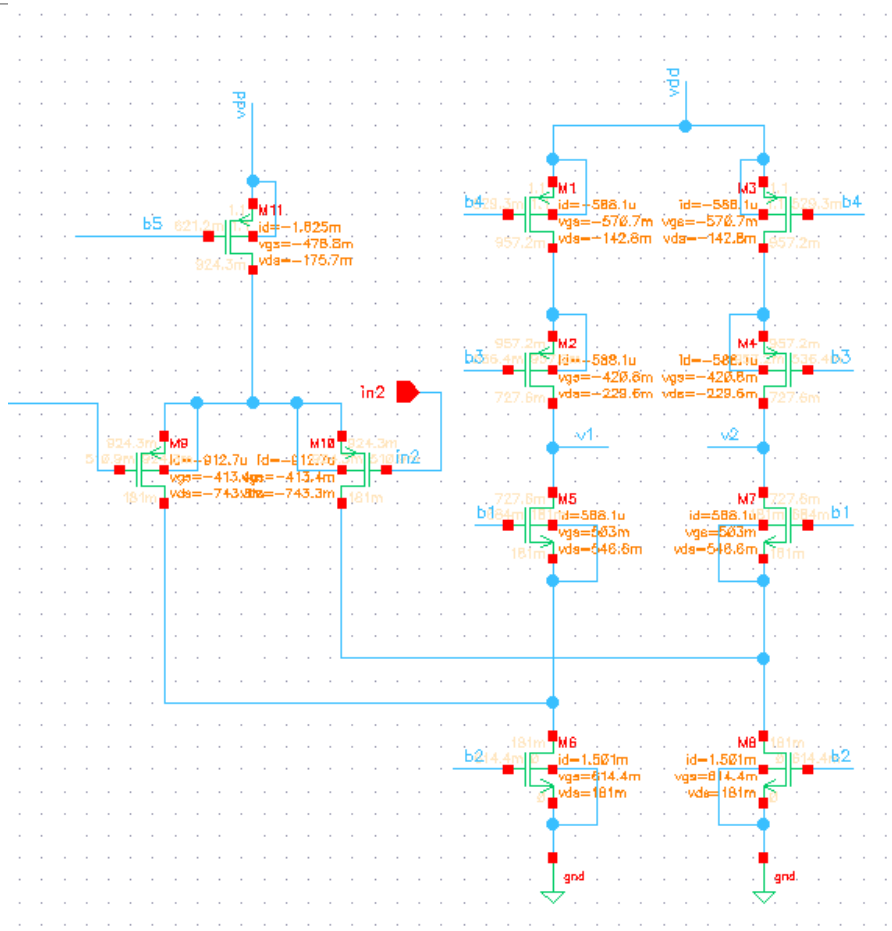


[3] Gain Margin – Closed ; 16dB

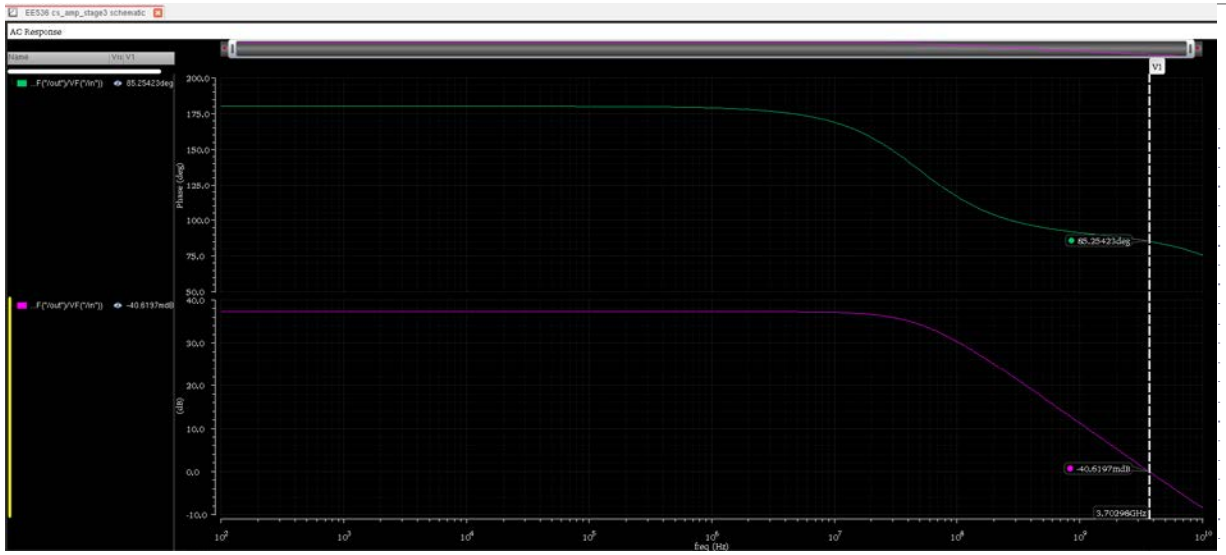


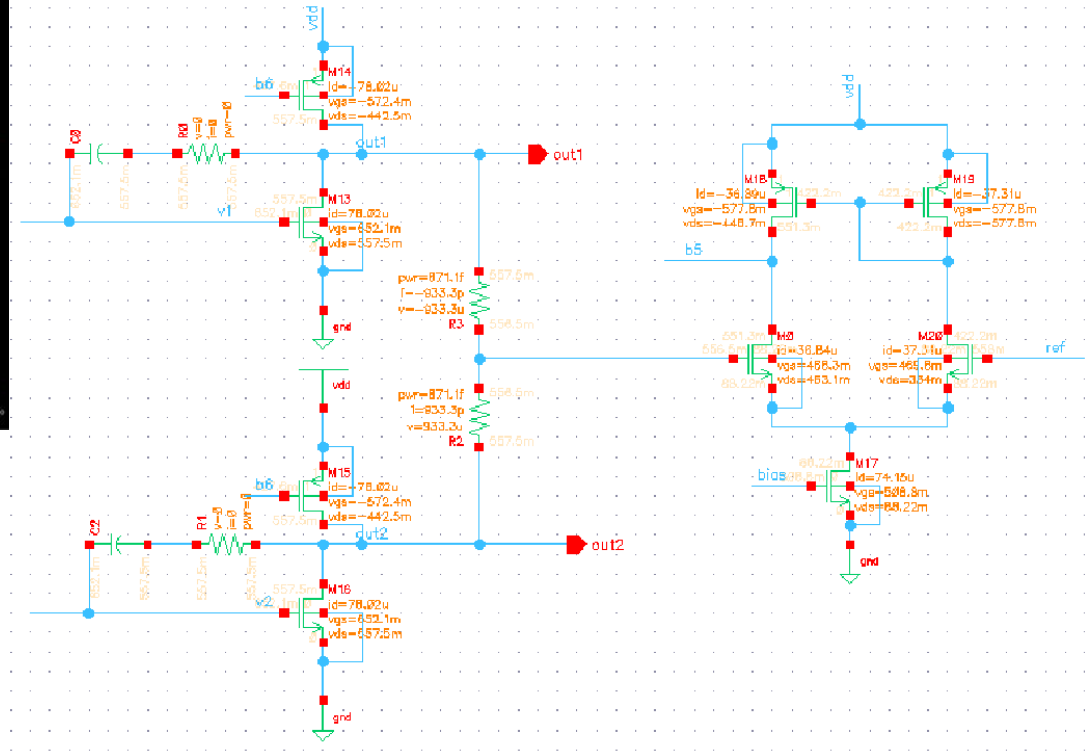
[3] First Stage : Gain 23dB, Fu=7.5GHz



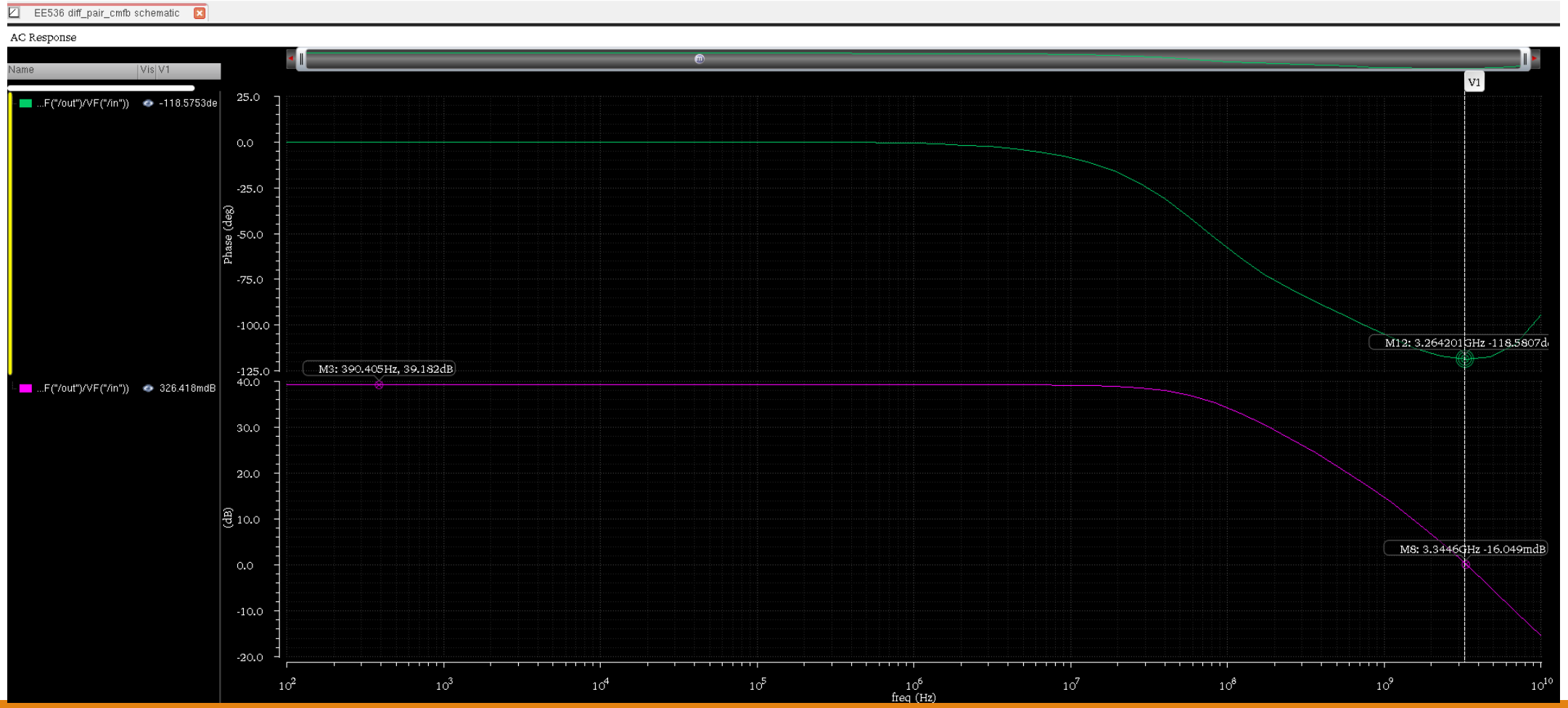


[3] Second Stage : Gain 37dB, Fu=3.6GHz





[3] CMFB Small-Signal Response



[3] Performance Summary

	Target	Simulated	Units
$\lvert A_{vd} \rvert$	> 60	58	dB
F_u	> 100	1.2	GHz
V_{dd}	1	1	V
I_{DC}	< 25	1.96	mA
C_L	100	100	fF
PM	> 60	72	Degrees
GM	> 10	16.5	dB

[4] Conclusions (1)

1. Highlights of the design

- Folded Cascoded Two stage OTA

- Good performance in gain and bandwidth product

2. Improved Suggestion

- Regulated cascodes can be utilized

[4] Conclusions (2)

3. Lessons learned

- Analog Design brings a lot of result mismatch

- Balancing all transistors whose characteristics are nonlinear requires much more efforts beyond the its relatively simple analysis

References

[1] B. Razavi, Design of Analog CMOS Integrated Circuits. McGraw-Hill, 2002.

[2] B. Ahuja, “An improved frequency compensation technique for CMOS operational amplifiers,” IEEE J. Solid- State Circuits, Vol. SC-18, pp. 629-633, Dec, 1983.

[3] F. Silveira, “A gm/Id Based Methodology for the Design of CMOS Analog Circuits and Its Application to the Synthesis of a Silicon-on-Insulator Micropower OTA, IEEE J. Solid-State, VOL 31, NO 9. Sep, 1996