Test Engineering Internship
Cypress Semiconductor Corporation

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I. INTERNSHIP SUMMARY

As a senior test engineer at Cypress Semiconductor Corporation (CY), first I was able to understand the overall procedure of producing an IC chip. The responsibility of test engineers at CY includes designing automatic test procedures to ensure that the final chip product has no manufacturing or functional defects and test holes. Test engineers correct design criterion, characterization parameters and/or test sequence to have the highest test coverage with the shortest amount of test time. During the CPT work-semester spring 2016, I was able to contribute test time reduction of 5 seconds from a single wafer test time of 27s previously. The test reduction involved test IP code optimization by which the test coverage remains same with reduced test time. Semiconductor test principle, test environment and various techniques to reduce the test time are explained throughout the report.

II. INTRODUCTION

A. Report Coverage and Internship Information

This report is written as ENGR596 course requirement under Dr. Hossein Hashemi at University of Southern California. The report summarizes my work responsibilities and its importance to the company along with what I learned during this report period. The content of this report does not violate the company's policies on Intellectual Property and/or Confidentiality. As a final semester master student, CY offered the full time position to me as a senior test engineer working in Seattle, WA.

B. About the Company

"Cypress Semiconductor Corporation is an American semiconductor design and manufacturing company founded by T.J Rodgers and others from Advanced Micro Devices. It was formed in 1982 with backing by Sevin Rosen and went public in 1986. The company initially focused on the design and development of high speed CMOS SRAMs, EEPROMs, PAL devices, and TTL logic Devices. Its headquarters are in San Jose with various divisions in the United States and its fabrication plant in Minnesota and Philippines" [1]. CY is No.1 in SRAM market share and provides embedded solution chip called PSoC product lines along with its automotive industry share.

C. What Test Engineers at CY do

I had not been told about test engineering until I work here for CY. Most classes learned in schools were analog/digital circuit design courses that cover the practical knowledge of system stability, power consumption, signal processing, semiconductor physics, logic designs, computer architecture and programming. Meanwhile, test engineering is an area of engineering that numerates semiconductor manufacturing processes so that the final product in either wafer or packaged IC chip does not have design or production defects. By providing test feedbacks to other teams and optimizing the test program coverage, test engineers at CY strive to increase yield and reduce test time. Because testing involves millions of part, the test time is directly associated with test cost and its reduction is typically of importance in both engineering and managing level. The

goal of CY is to have less than 2 defect parts per million (2ppm) by designing tests whose limits have margin of six standard deviations (six sigma) for all test functions. For large quantity, engineers use automatic test equipment (ATE) that automates semiconductor test procedures with helpful tools such as IP programming, data managing, automated test pattern and the test machine.

III. SEMICONDUCTOR TEST WORK ENVIRONMENT

The Fig. 1 is the diagram that shows the overall procedures of IC testing. It is important for test engineers to understand this structure and figure out where it needs to update once certain defects are found. The detailed explainations of what each does are shown in the following sections:

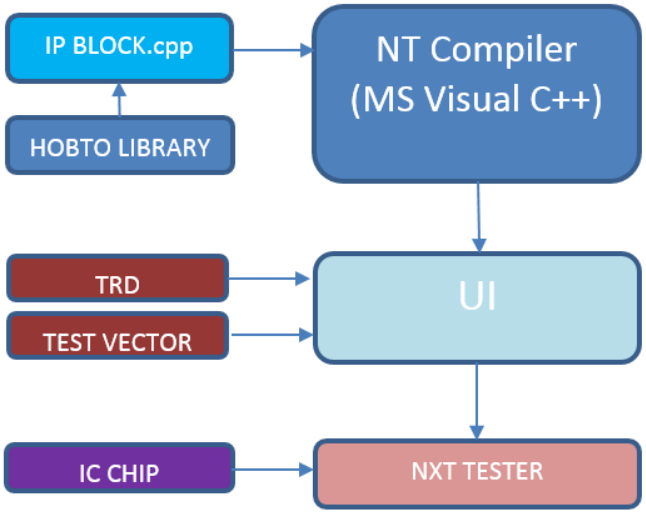

Figure 1. Test Environment Overview at CY

A. Compiler

One IP Block that is in cpp format is needed to perform one test. For example, an IP Block (possibly named IP_continuity) checks if the DUT has open/short manufacturing defects. Test engineers design the test IP blocks and make them as a group called HOBTO library. The compiler generate an executable program file that consists of groups of IP Blocks and inputs to the tester machine with other components (III-B) and (III-C) in this report sections.

B. Test Requirement Documents (TRD)

TRD is a document that defines the test sequence with customized input parameters shown in Fig. 2. It was implemented in Microsoft Excel and each row performs one test. Typically, a TRD has more than two thousand rows each with different input parameters. One IP Block has multiple test usages. For example, an IP Block (possibly called IP_powersupplycurrent) measures the power supply current which used in power leakage test and deepsleep test with different parameters in TRD [2].

				param0	param1
CRI	TN	TestName	IP_BLOCK	Label	ValLabel
X[BLE42:RF]	4401	m0s8bless_sy_bump1_def_1	IP_S8BLERF_TWEEK	BLE_BLERD_SY_BUMP1	0x0E05
X[BLE42:RF]	4403	m0s8bless_sy_bump1_def_2	IP_S8BLERF_TWEEK	BLESS_REG32_TRIM	0x0E05
X[BLE42:RF]	4405	m0s8bless_sy_bump1_def_3	IP_S8BLERF_TWEEK	SRAM_MOHR2_DATA8	0x0E05
X[BLE42:RF]	4407	m0s8bless_sy_bump2_def_1	IP_S8BLERF_TWEEK	BLE_BLERD_SY_BUMP2	0x0020
X[BLE42:RF]	4409	m0s8bless_sy_bump2_def_2	IP_S8BLERF_TWEEK	BLE_BLERD_REG_34_TRIM	0x0000
X[BLE42:RF]	4411	m0s8bless_rx_bump2_def_1	IP_S8BLERF_TWEEK	BLE_BLERD_RX_BUMP2	0x08CE
X[BLE42:RF]	4413	m0s8bless_rx_bump2_def_2	IP_S8BLERF_TWEEK	BLE_BLERD_REG_38_TRIM	0x0000
X[BLE42:RF]	4414	m0s8bless_logRemedy_init	IP_M0S8BLESS_LOG_F02FN_REMEDY	f02fn_remedy	INIT
X[BLE42:RF]	4418	m0s8bless_log_dcap_def	IP_M0S8BLESS_LOG_DCAP	m0s8bless_dcap_read_mix	SDATA
				channel	PASetting
X[BLE42:RF:!CSP]	4419	m0s8bless_TX_pwr_PA7_ch2482_LV_def	IP_M0S8BLESS_RAND_FAIL	2482	7
				sourceLabel	destinationLabels
X[BLE42:RF]	4425	m0s8bless_sy_bumpN_registerPass_def	IP_M0S8BLESS_COPY_MDUT_ActiveDut	BLE_BLERD_SY_BUMPN	BLE_BLERD_REG_34_TRIM
X[BLE42:RF]	4427	m0s8bless_rx_bumpN_registerPass_def	IP_M0S8BLESS_COPY_MDUT_ActiveDut	BLE_BLERD_RX_BUMPN	BLE_BLERD_REG_38_TRIM
				remedyContainer	INIT|SET
X[BLE42:RF:ENG_F02FN]	4423	m0s8bless_logRemedy_def	IP_M0S8BLESS_LOG_F02FN_REMEDY	f02fn_remedy	LOG

Figure 2. Screen capture of TRD

C. Test Vector

Test vectors are automatic test pattern generation (ATPG) in binary form with designed time verification and random data in memory. It assists with failure analysis and determines test quality. The test quality is defined by the amount of modeled defects that cover fault detections with good number of generated patterns. The more fault detections, the better test quality. The more patterns, the longer test time but with greater test coverage.

D. Nextest UI

This is user interface of test machine Nextest (NXT) Magnum. It loads the test program with the executable file from compiler (III-A) and TRD sequence parameters (III-B) and test vectors (III-C). Test engineers manipulate this program interface to send commands to the NXT Tester where the DUT chip is embedded.

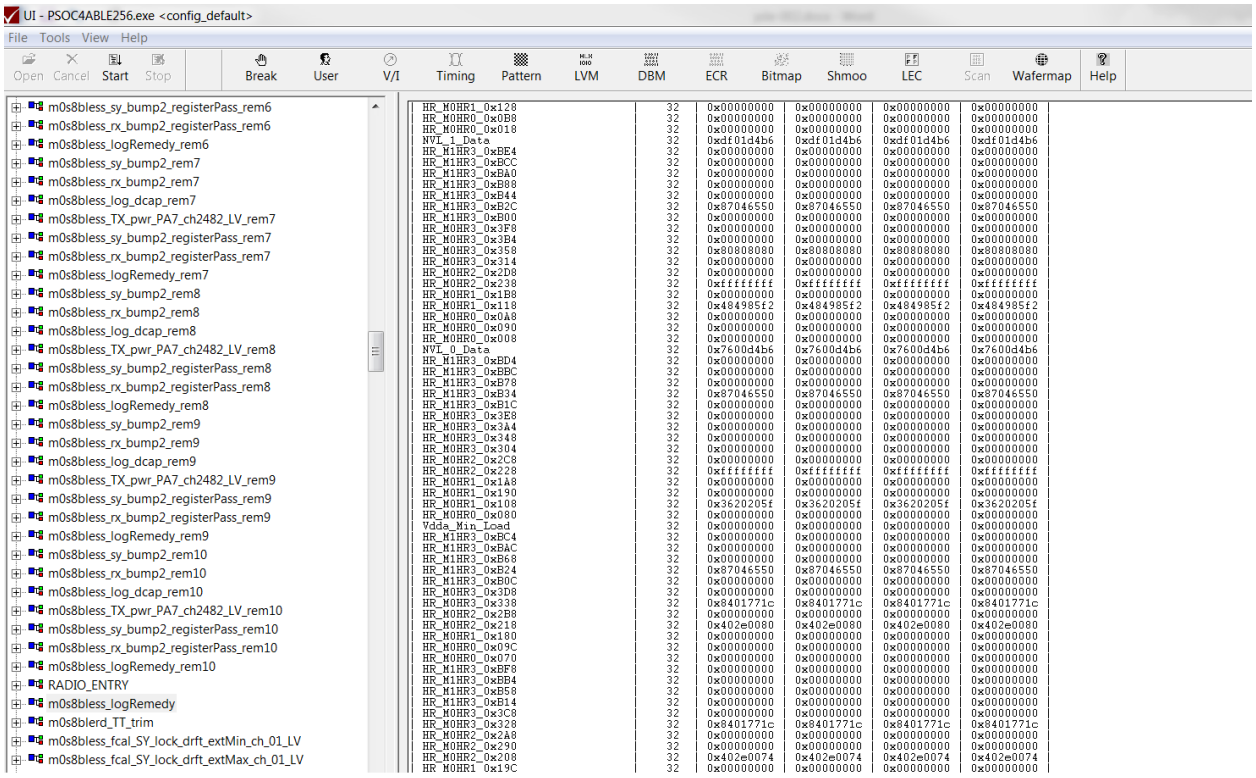

Figure 3. Nextest UI Loading Test Program and Vectors

E. Nextest Tester

This is an automatic test machine for engineers, and in production level there is another type of tester whose robots moves wafer and IC chip for numerous test volume. In NXT Tester, the tester board with IC chip is connected to the tester with pogo pins. It automatically tests desired functions [3].

IV. PSOC4A_BLE_256K

PSOC4A_BLE_256K is an internal project name for CY's programming solution product. This version of IC chip has Bluetooth low energy (BLE) with 256 KB internal flash. With test basics and structure covered as new employee training, I was involved in this project for test time reduction. The current test time for a wafer is 27s where the goal is 20.1s. Several IP Blocks are investigated for this test time reduction purpose and the followings are the IP Block codes that I worked on [4].

A. TTR6 Non-Blocking

The updated IP Block saves 0.2-0.3s for one test. The reason behind this improvement is to separate sequential RF test commands so that the next command does not necessarily wait for the previous command to finish. This is applied to non-blocking Litepoint (RF test machine) functions such that CLE and CALC commands are executed separately from FETC command. The time improvement is proved in various tool platforms with sequence and timing details. The total test time saving will be around 1.0-1.5s for five RF tests that will be updated.

B. Read_SMR MDUT

The updated version saves the test time by 2.9s (3.02s->0.12s). The main difference between versions is whether to update every registers no matter what versus to update only what's changed. The result of 0.12s is when there is no difference in memory registers between the previous and the new one. With the new DUT, it is observed to have 0.4s test time.

Old version		New version	
1st time	2nd time	1st time	2nd time
3163136 us	3072784 us	432349 us	123973 us
3045330 us	3044534 us	470466 us	123299 us

C. RXS Packet Length Option

The updated version has an option to choose short or long packets input waveforms from the TRD for the RF LitePoint test whereas the previous one is restricted to either all long packets or all short packets. The short packet length and its reduced packet interval save the test time by 0.36s (1.06s ->0.70s). For BLE4.2 testing, two RX tests of the three can use short packets, and therefore the total expected time saving is about 0.7s (2 tests of 3 run on short packet).

TestName	IP_BLOCK	Previous	Long	Short
m0s8bless_RX_mins_loCh_0_LV	IP_RXS_continuous	1060909 us	1067234 us	687136 us
m0s8bless_RX_mins_hiCh_0_HV	IP_RXS_continuous	1060620 us	1066351 us	689729 us
m0s8bless_RX_mins_loCh_impaired_LV	IP_RXS_continuous	1059824 us	1065633 us	690152 us
Possible time savings from Long to Short : 0.37s				

D. Deepsleep Current Range

This IP Block update is in progress. The product supports deepsleep mode that turns off several functions and clocks to reduce power consumption. This IP supports current measurement in DPS pins and PE channels. This IP also enables to set the measurement range, compensation capacitor value and measurements to be averaged. There are provisions to disconnect the device pins and to force the pins to VIL level during test. The ongoing work plan is to change the current range whose settling time is just about what the device needs to have within six standard deviation margins.

V. MISCELLANEOUS

During the internship period, as my first career position, I have had great lessons so far. The company culture training was conducted such as company internal work managing system along with its documentation system. I had a chance to work on CY's chip application platform, PSoC Creator. The platform organizes the system resources to one place so that users only need to write the function code and mark routing information [5]. I am starting to get involved in another project automotive backend user support. The new employee train will likely continue throughout this year.

VI. CONCLUSIONS

This report documents CPT Internship at Cypress Semiconductor Corporate. After this semester, I will continue working here as a senior test engineer. The lessons learnt during this period and school times will not be forgotten. The first half period of this internship was focused on getting used to the company culture and its test environment. And during the second half period I worked on an actual project to reduce test time. While doing so, I realized that in order to be a good test engineer understanding in circuit design and hardware architecture to understand how a test function will actually work is of great necessity.

VII. REFERENCES

[1] Wikipedia "Cypress Semiconductor" Web
[2] Status Report 3 "Test Requirement Document" Feb. 2016.
[3] Status Report 2 "NXT Tester" Feb. 2016.
[4] Status Report 5, 6 and 7 "Test Time Reduction" Mar and Apr. 2016.
[5] Status Report 4 "PSOC Creator" Mar. 2016.