Environment Building

for Windows

Github: https://github.com/verimake-team/SparkRoad-FPGA

Present by: Verimake

1 Click or Type or Sellect

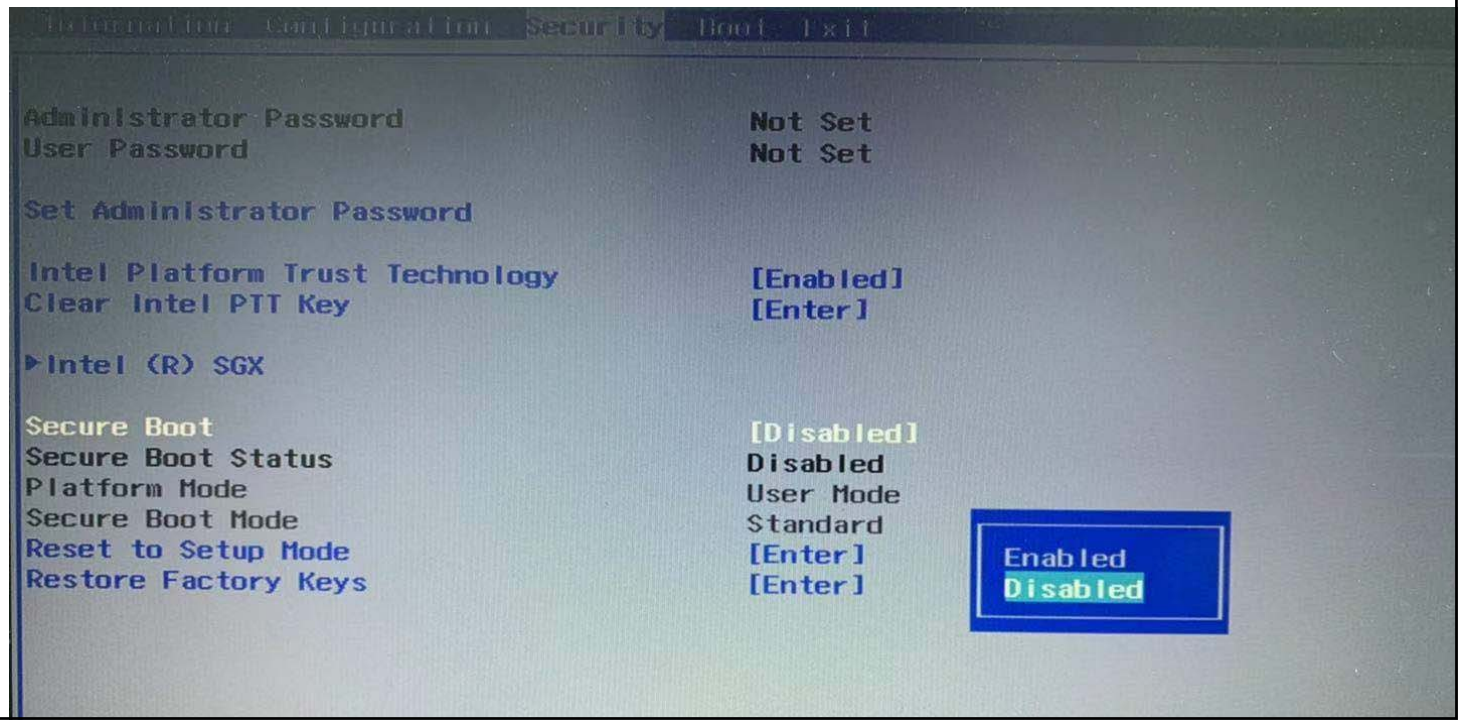
1 Click Right Button

1 Double Click

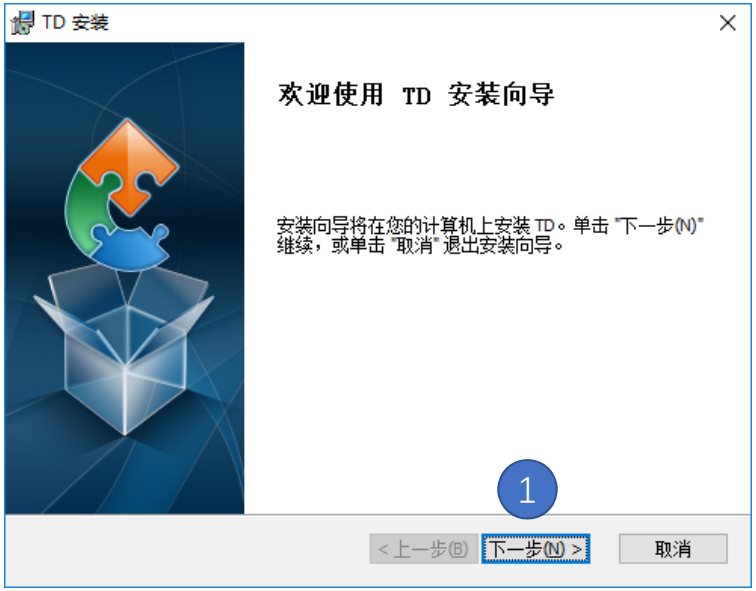
Caution

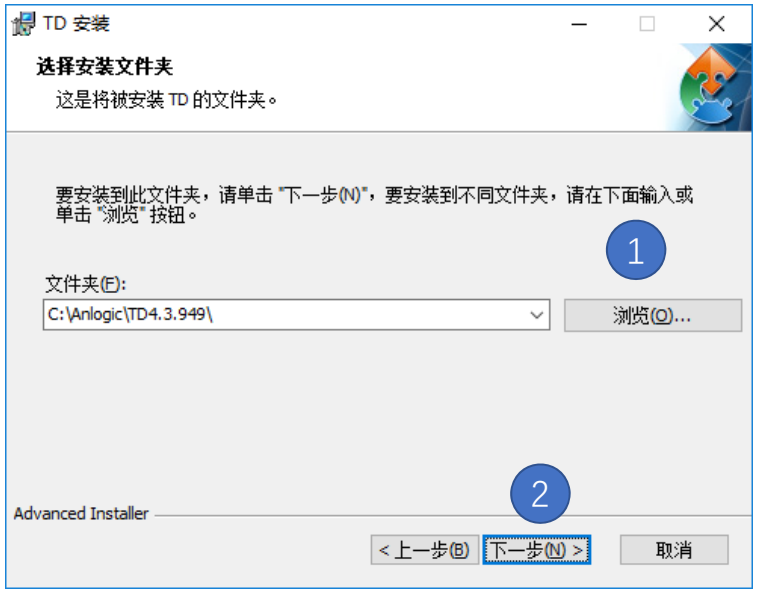
Pressing F2 or Del while your computer rebooting , entering BIOS setting

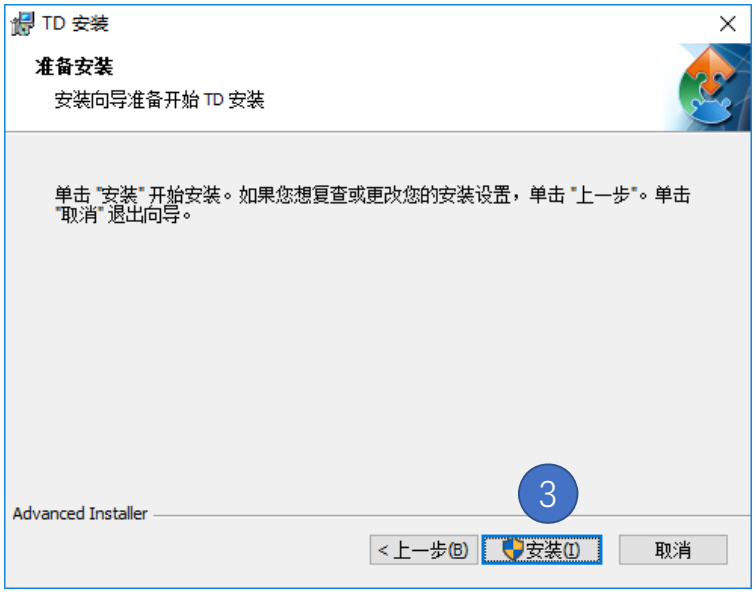
Disable “security boot”
save the bios settings
rebooting

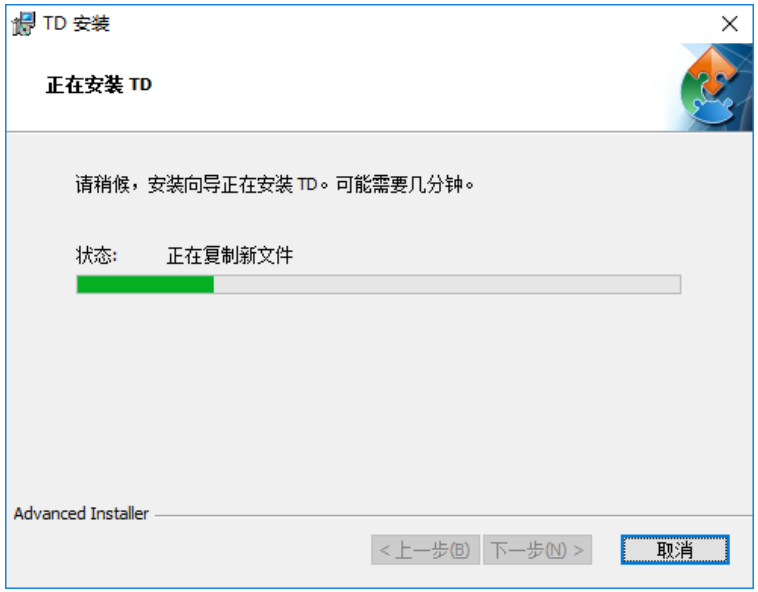


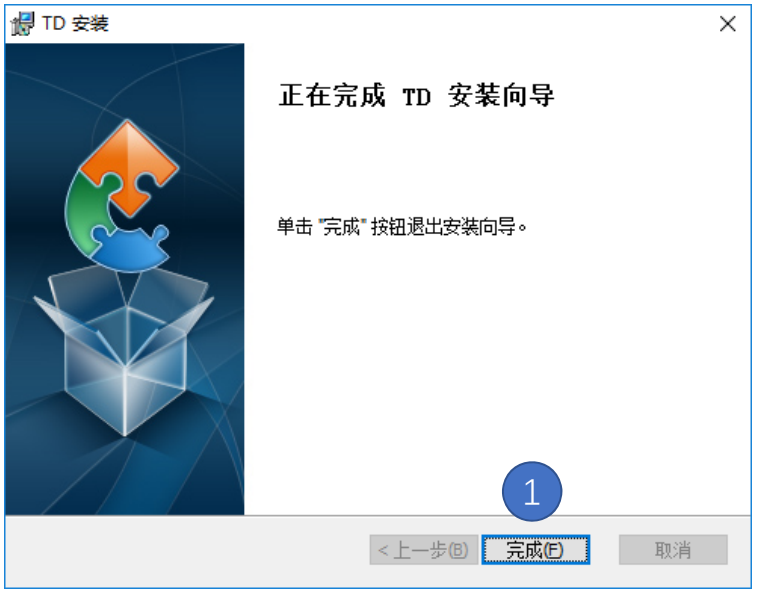
Following the GitHub, Get the latest TD
Double click the setup file




TD 安装
选择安装文件夹
这是将被安装 TD 的文件夹。
要安装到此文件夹，请单击 "下一步(N)"，要安装到不同文件夹，请在下面输入或单击 "浏览" 按钮。
1
文件夹(F):
C:\Anlogic\TD4.3.949\
浏览(O)...
2
Advanced Installer
< 上一步(B)
下一步(N) >
取消

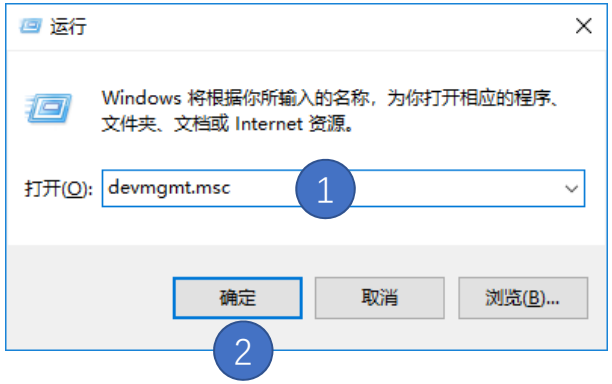

TD 安装
准备安装
安装向导准备开始 TD 安装
单击 "安装" 开始安装。如果您想复查或更改您的安装设置，单击 "上一步"。单击 "取消" 退出向导。
3
Advanced Installer
< 上一步(B)
安装(I)
取消

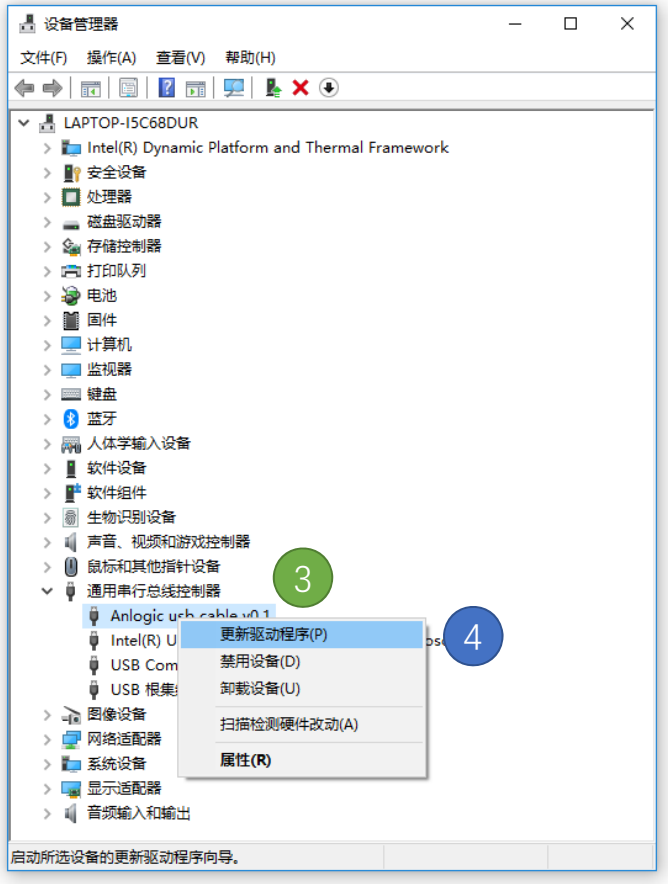

TD 安装
正在安装 TD
请稍候，安装向导正在安装 TD。可能需要几分钟。
状态:
正在复制新文件
Advanced Installer
< 上一步(B)
下一步(N) >
取消


TD 安装
正在完成 TD 安装向导
单击 "完成" 按钮退出安装向导。
1
< 上一步(B)
完成(F)
取消

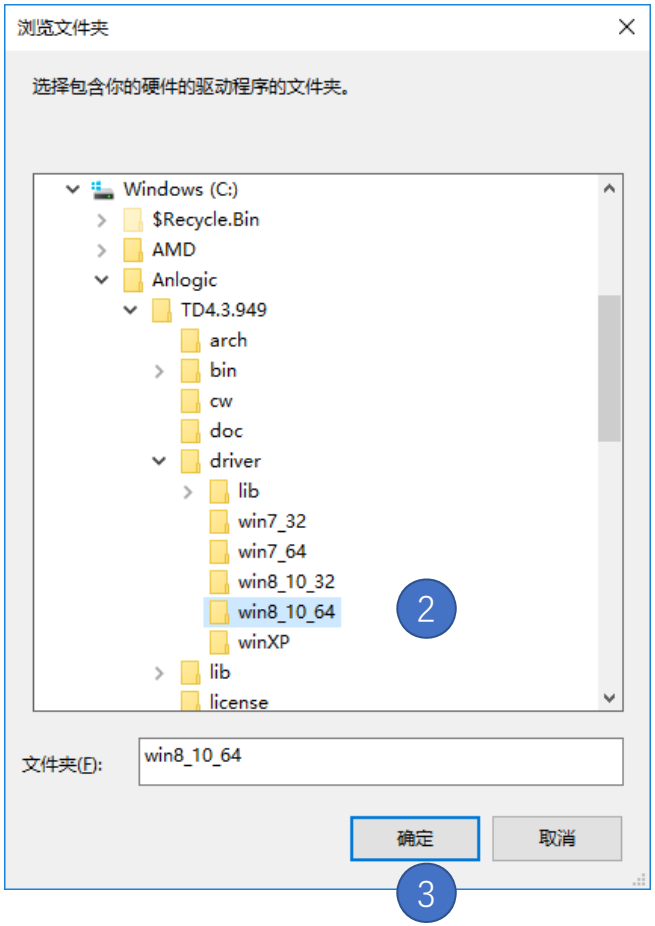
Connecting the SparkRoad and Computer via a USB-C cable

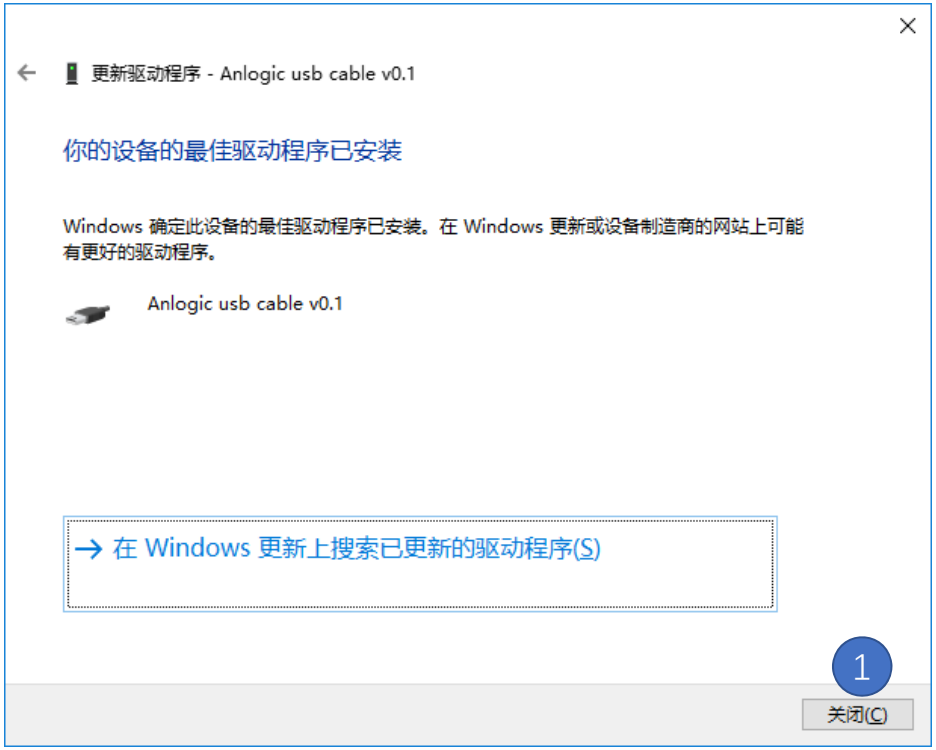
Pressing: Win + r
typing devmgmt.msc
enter



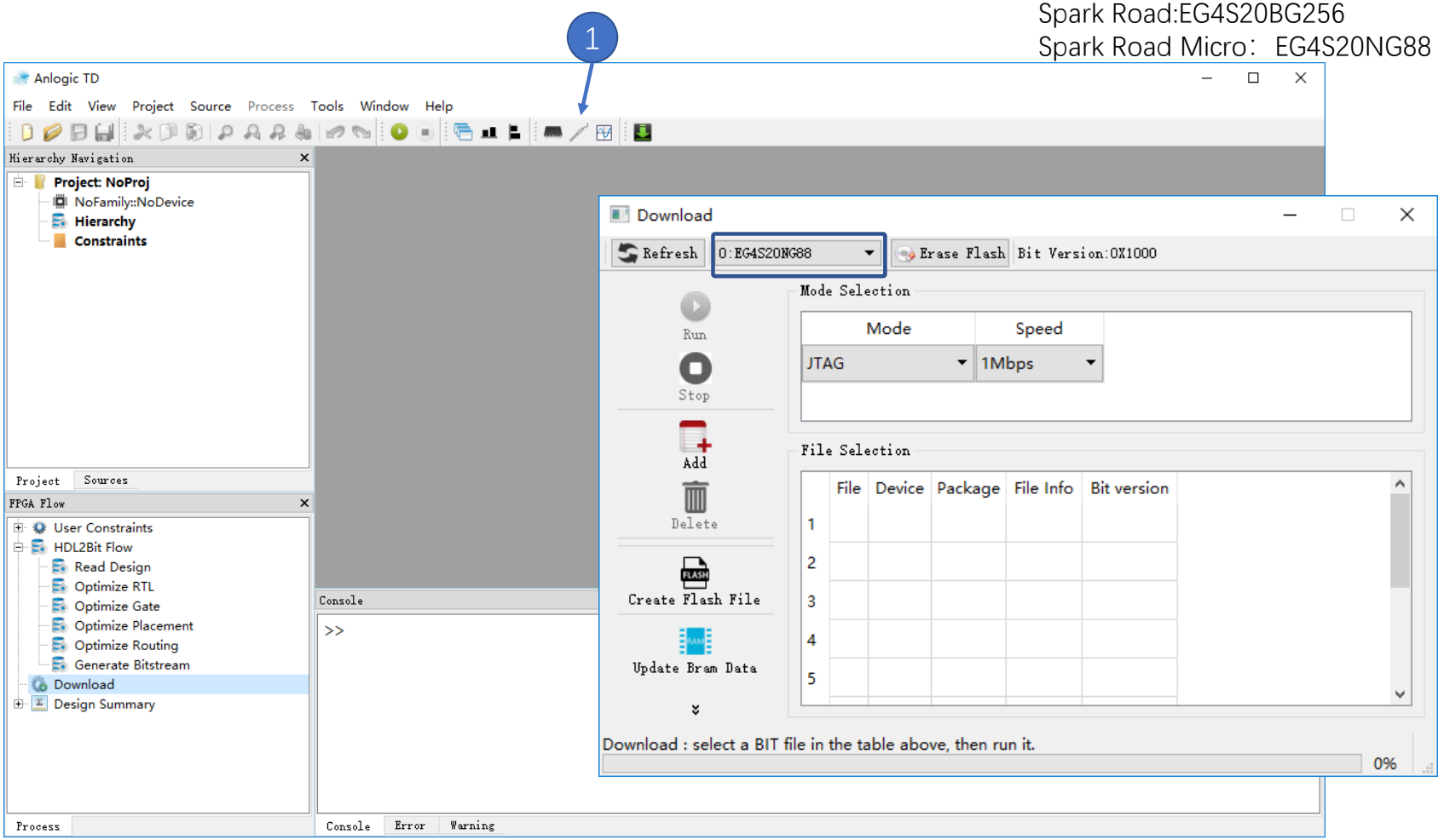



更新驱动程序 - Anlogic usb cable v0.1
你要如何搜索驱动程序?
自动搜索更新的驱动程序软件(S)
Windows 将搜索你的计算机和 Internet 以获取适合你设备的最新驱动程序软件，除非你已在设备安装设置中禁用此功能。
浏览我的计算机以查找驱动程序软件(R)
手动查找并安装驱动程序软件。
1
取消


浏览文件夹
选择包含你的硬件的驱动程序的文件夹。
Windows (C:)
$Recycle.Bin
AMD
Anlogic
TD4.3.949
arch
bin
cw
doc
driver
lib
win7_32
win7_64
win8_10_32
win8_10_64
winXP
lib
license
2
文件夹(F):
win8_10_64
确定
取消
3


更新驱动程序 - Anlogic usb cable v0.1
你的设备的最佳驱动程序已安装
Windows 确定此设备的最佳驱动程序已安装。在 Windows 更新或设备制造商的网站上可能有更好的驱动程序。
Anlogic usb cable v0.1
在 Windows 更新上搜索已更新的驱动程序(S)
1
关闭(C)

Notice:
Spark Road:EG4S20BG256
Spark Road Micro：EG4S20NG88



The End!

Enjoy Yourself!

Hello LED-SparkRoad Startup

Github: https://github.com/verimake-team/SparkRoad-FPGA

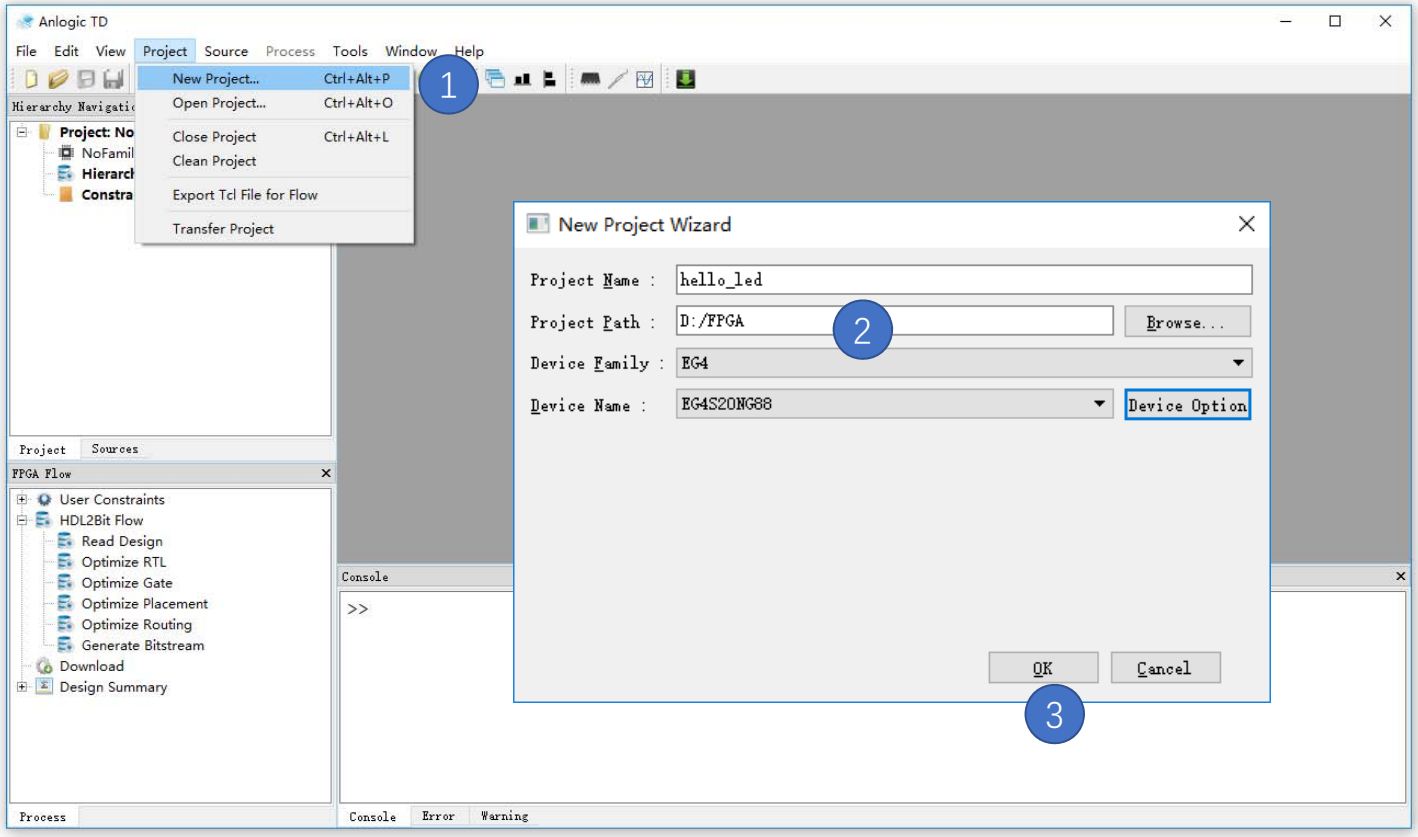
Present by: Verimake

1 Click or Type or Sellect

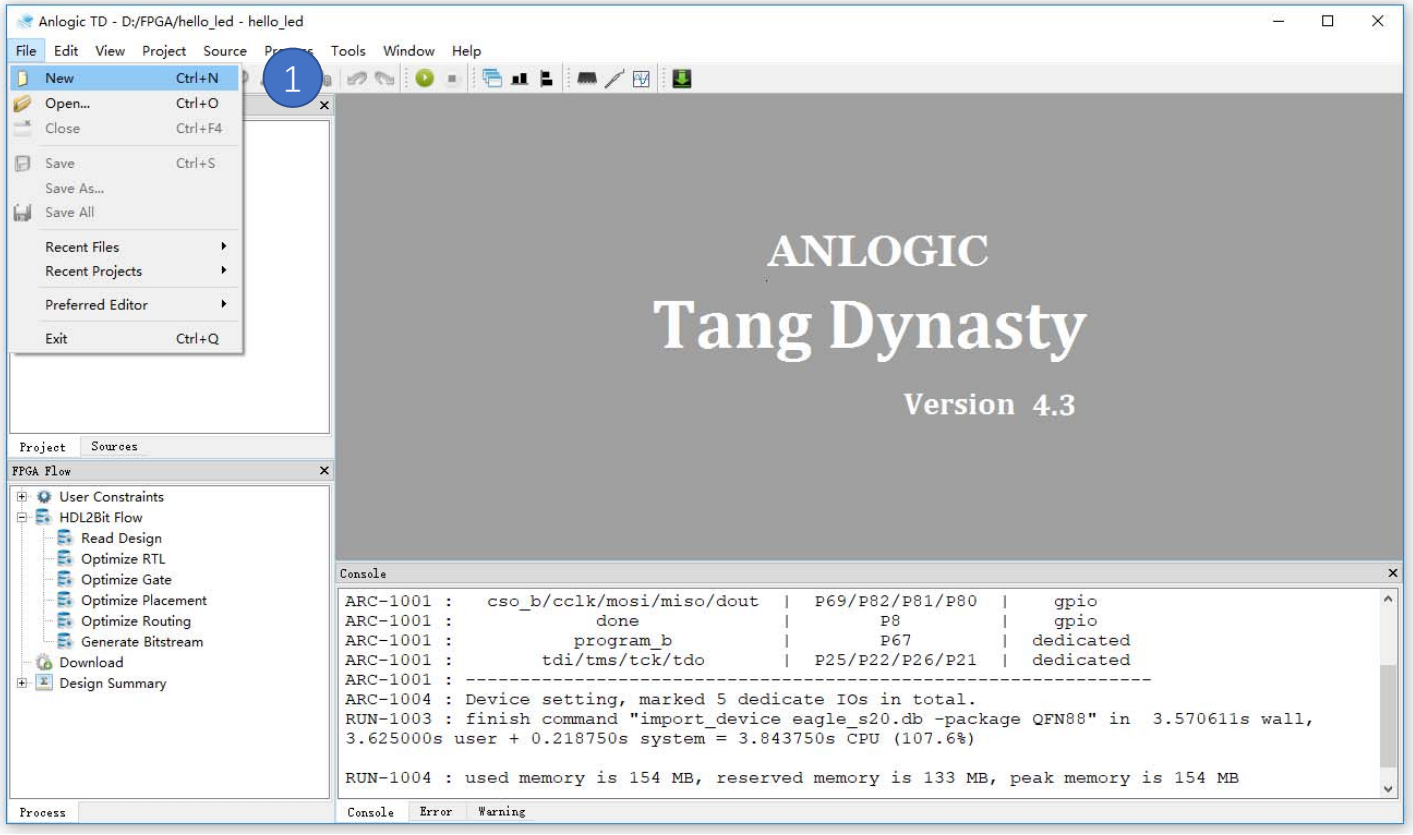
1 Click Right Button

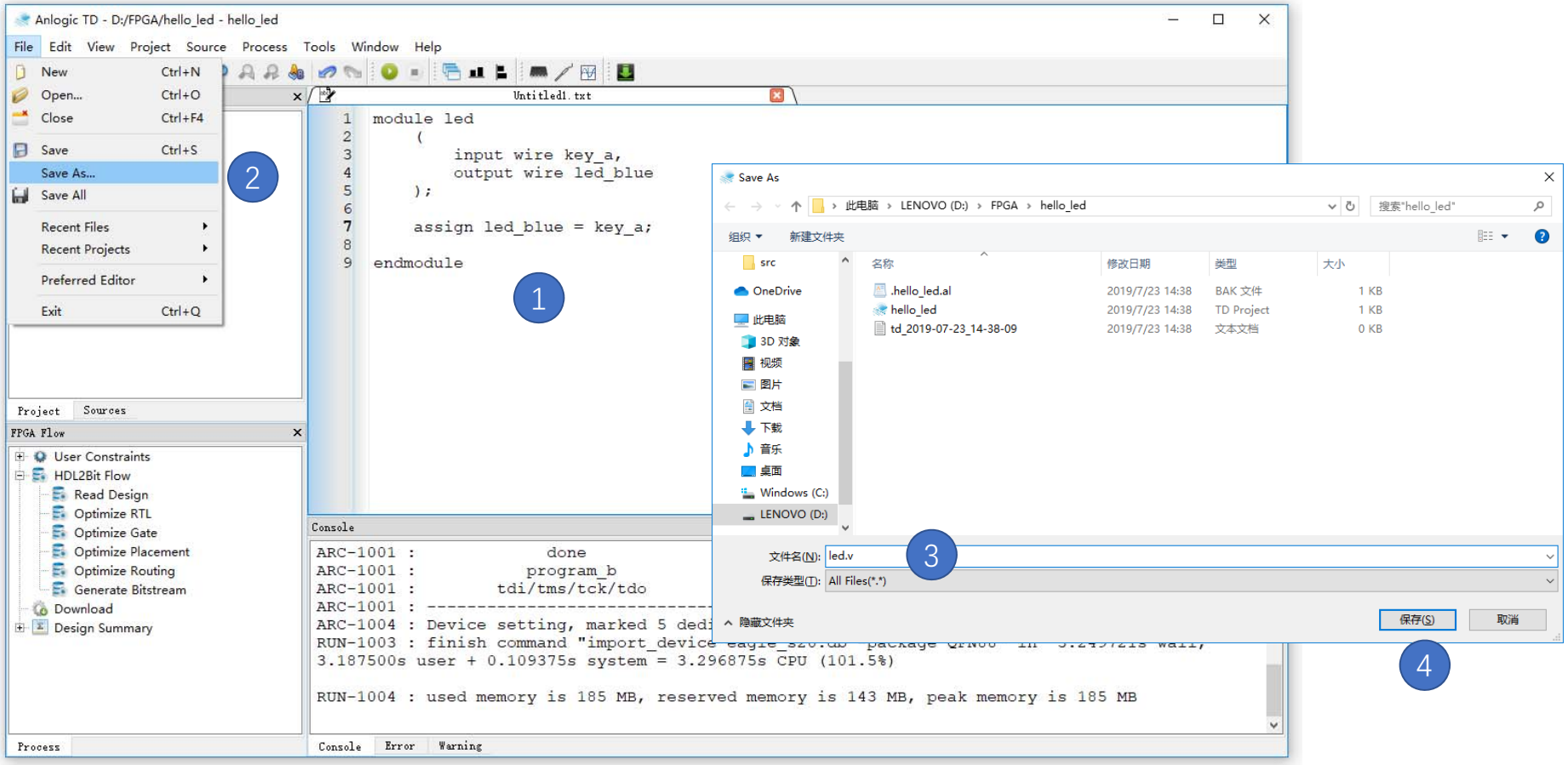
1 Double Click

Caution



Notice： Device Name
Spark Road： EG4S20BG256
Spark Road Micro： EG4S20NG88


Anlogic TD - D:/FPGA/hello_led - hello_led
File Edit View Project Source Process Tools Window Help
1
New Ctrl+N
Open... Ctrl+O
Close Ctrl+F4
Save Ctrl+S
Save As...
Save All
Recent Files
Recent Projects
Preferred Editor
Exit Ctrl+Q
Project Sources
FPGA Flow
User Constraints
HDL2Bit Flow
Read Design
Optimize RTL
Optimize Gate
Optimize Placement
Optimize Routing
Generate Bitstream
Download
Design Summary
Process
ANLOGIC
Tang Dynasty
Version 4.3
Console
ARC-1001 : cso_b/cclk/mosi/miso/dout | P69/P82/P81/P80 | gpio
ARC-1001 : done | P8 | gpio
ARC-1001 : program_b | P67 | dedicated
ARC-1001 : tdi/tms/tck/tdo | P25/P22/P26/P21 | dedicated
ARC-1001 : ----------
ARC-1004 : Device setting, marked 5 dedicate IOs in total.
RUN-1003 : finish command "import_device eagle_s20.db -package QFN88" in 3.570611s wall, 3.625000s user + 0.218750s system = 3.843750s CPU (107.6%)
RUN-1004 : used memory is 154 MB, reserved memory is 133 MB, peak memory is 154 MB
Console Error Warning

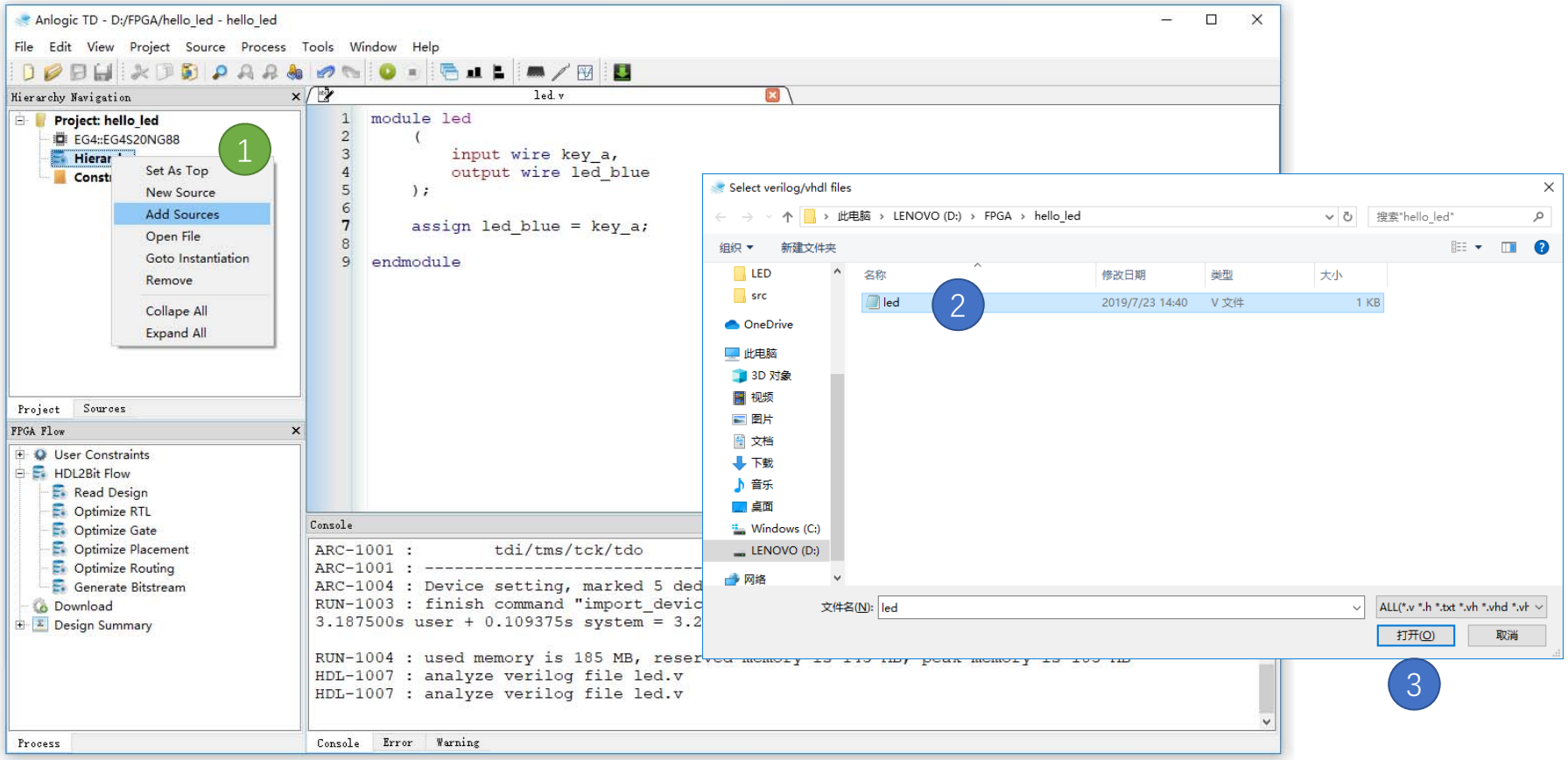

Anlogic TD - D:/FPGA/hello_led - hello_led
File Edit View Project Source Process Tools Window Help
New Ctrl+N
Open... Ctrl+O
Close Ctrl+F4
Save Ctrl+S
Save As...
Save All
Recent Files
Recent Projects
Preferred Editor
Exit Ctrl+Q
2
Untitled1.txt
1 module led
2 (
3 input wire key_a,
4 output wire led_blue
5);
6
7 assign led_blue = key_a;
8
9 endmodule
1
Project Sources
FPGA Flow
User Constraints
HDL2Bit Flow
Read Design
Optimize RTL
Optimize Gate
Optimize Placement
Optimize Routing
Generate Bitstream
Download
Design Summary
Process
Console
ARC-1001 : done
ARC-1001 : program_b
ARC-1001 : tdi/tms/tck/tdo
ARC-1001 : ----------
ARC-1004 : Device setting, marked 5 dedi
RUN-1003 : finish command "import_device
3.187500s user + 0.109375s system = 3.296875s CPU (101.5%)
RUN-1004 : used memory is 185 MB, reserved memory is 143 MB, peak memory is 185 MB
Console Error Warning
Save As
此电脑 › LENOVO (D:) › FPGA › hello_led
搜索"hello_led"
组织 新建文件夹
src
OneDrive
此电脑
3D 对象
视频
图片
文档
下载
音乐
桌面
Windows (C:)
LENOVO (D:)
名称 修改日期 类型 大小
.hello_led.al 2019/7/23 14:38 BAK 文件 1 KB
hello_led 2019/7/23 14:38 TD Project 1 KB
td_2019-07-23_14-38-09 2019/7/23 14:38 文本文档 0 KB
文件名(N): led.v
保存类型(T): All Files(*.*)
隐藏文件夹
保存(S)
取消
3
4

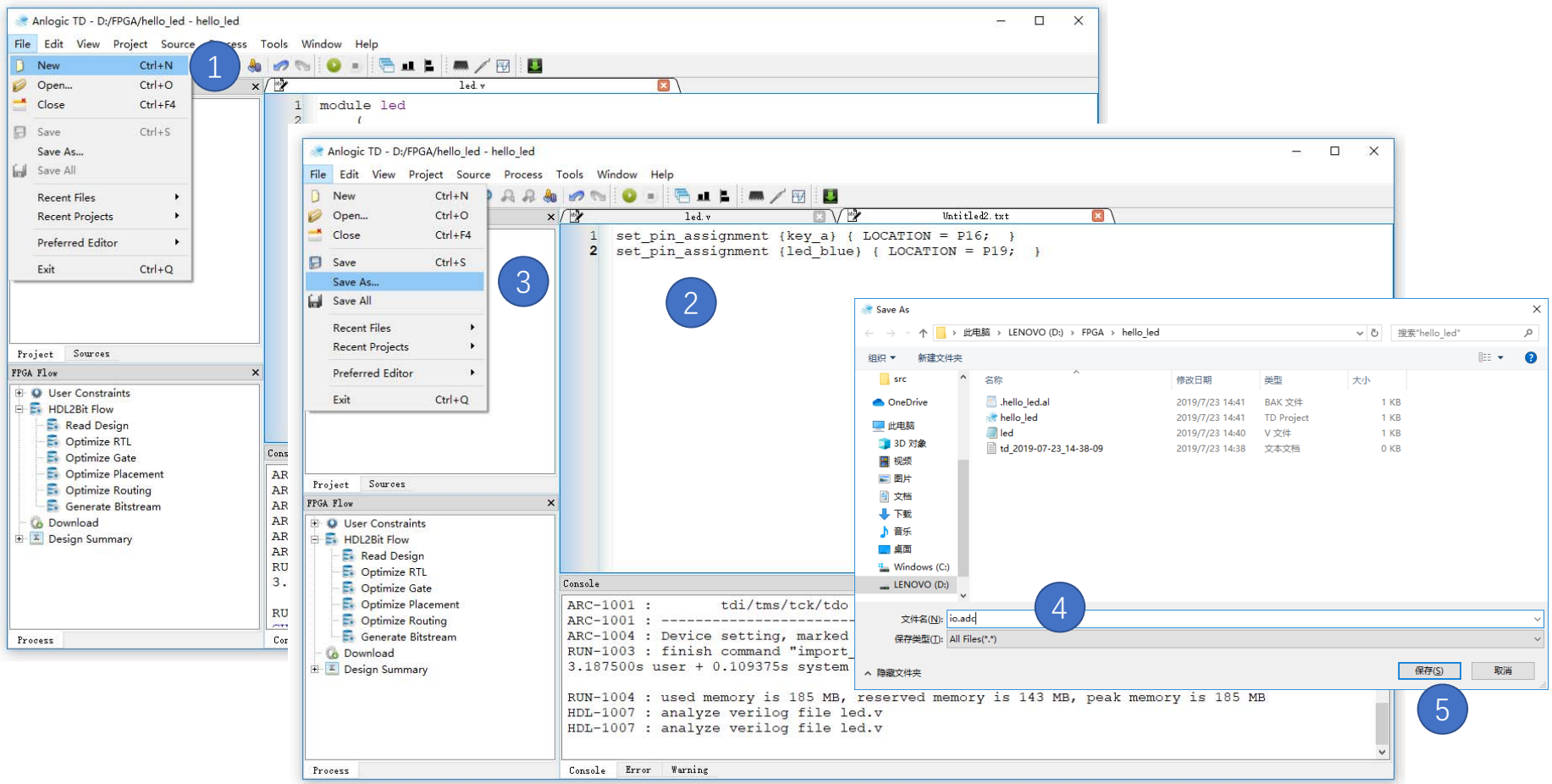
led.v

```
module led
    (
        input wire key_a,
        output wire led_blue
    );

    assign led_blue = key_a;

endmodule
```

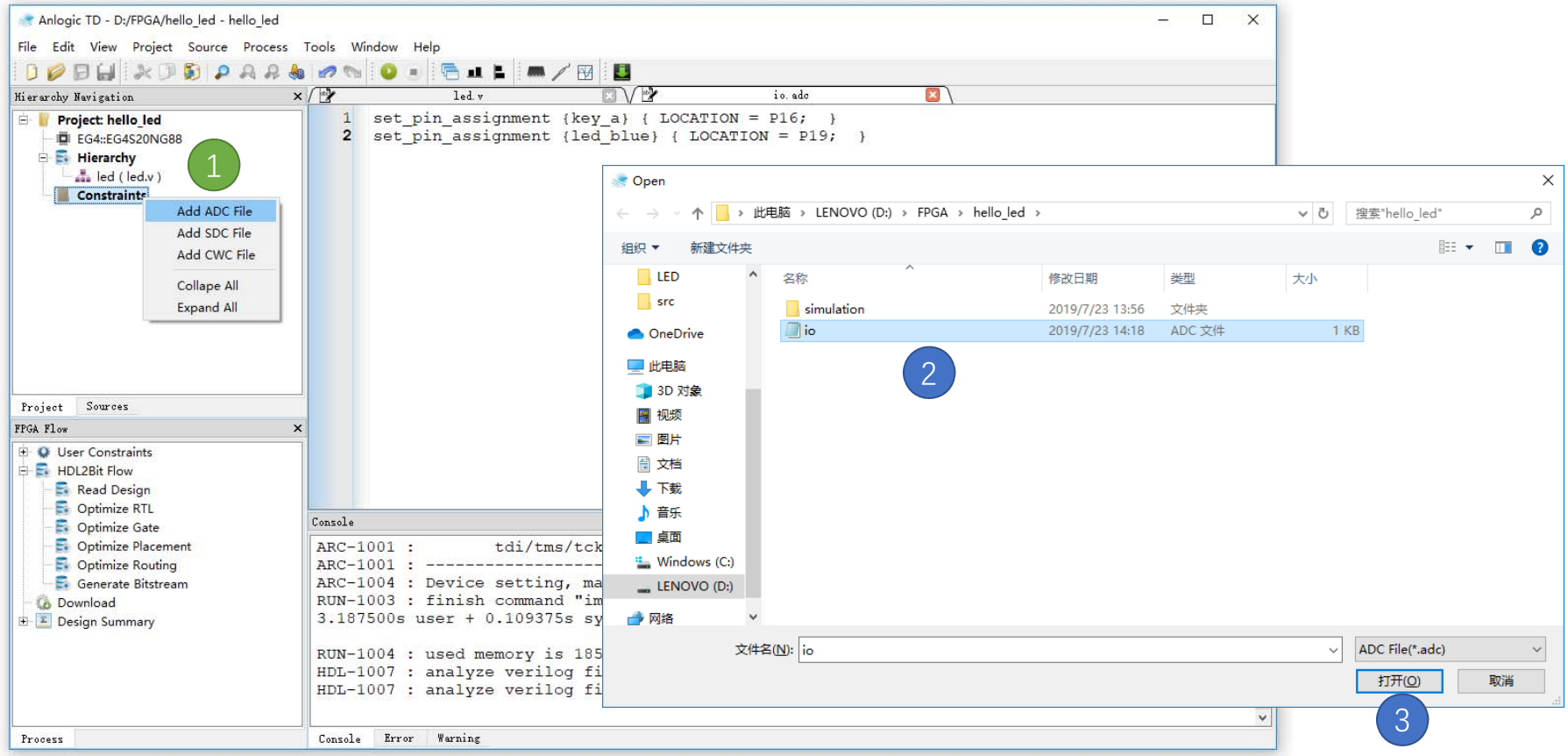

Anlogic TD - D:/FPGA/hello_led - hello_led
File Edit View Project Source Process Tools Window Help
Hierarchy Navigation
Project: hello_led
EG4::EG4S20NG88
Set As Top
New Source
Add Sources
Open File
Goto Instantiation
Remove
Collape All
Expand All
1
Project Sources
FPGA Flow
User Constraints
HDL2Bit Flow
Read Design
Optimize RTL
Optimize Gate
Optimize Placement
Optimize Routing
Generate Bitstream
Download
Design Summary
Process
led.v
module led
(
input wire key_a,
output wire led_blue
);
assign led_blue = key_a;
endmodule
Console
ARC-1001 : tdi/tms/tck/tdo
ARC-1004 : Device setting, marked 5 ded
RUN-1003 : finish command "import_devic
3.187500s user + 0.109375s system = 3.2
RUN-1004 : used memory is 185 MB,
HDL-1007 : analyze verilog file led.v
HDL-1007 : analyze verilog file led.v
Console Error Warning
Select verilog/vhdl files
此电脑 › LENOVO (D:) › FPGA › hello_led
搜索"hello_led"
组织 新建文件夹
LED
src
OneDrive
此电脑
3D 对象
视频
图片
文档
下载
音乐
桌面
Windows (C:)
LENOVO (D:)
网络
名称 修改日期 类型 大小
led 2019/7/23 14:40 V 文件 1 KB
2
文件名(N): led
ALL(*.v *.h *.txt *.vh *.vhd *.vf
打开(O)
取消
3

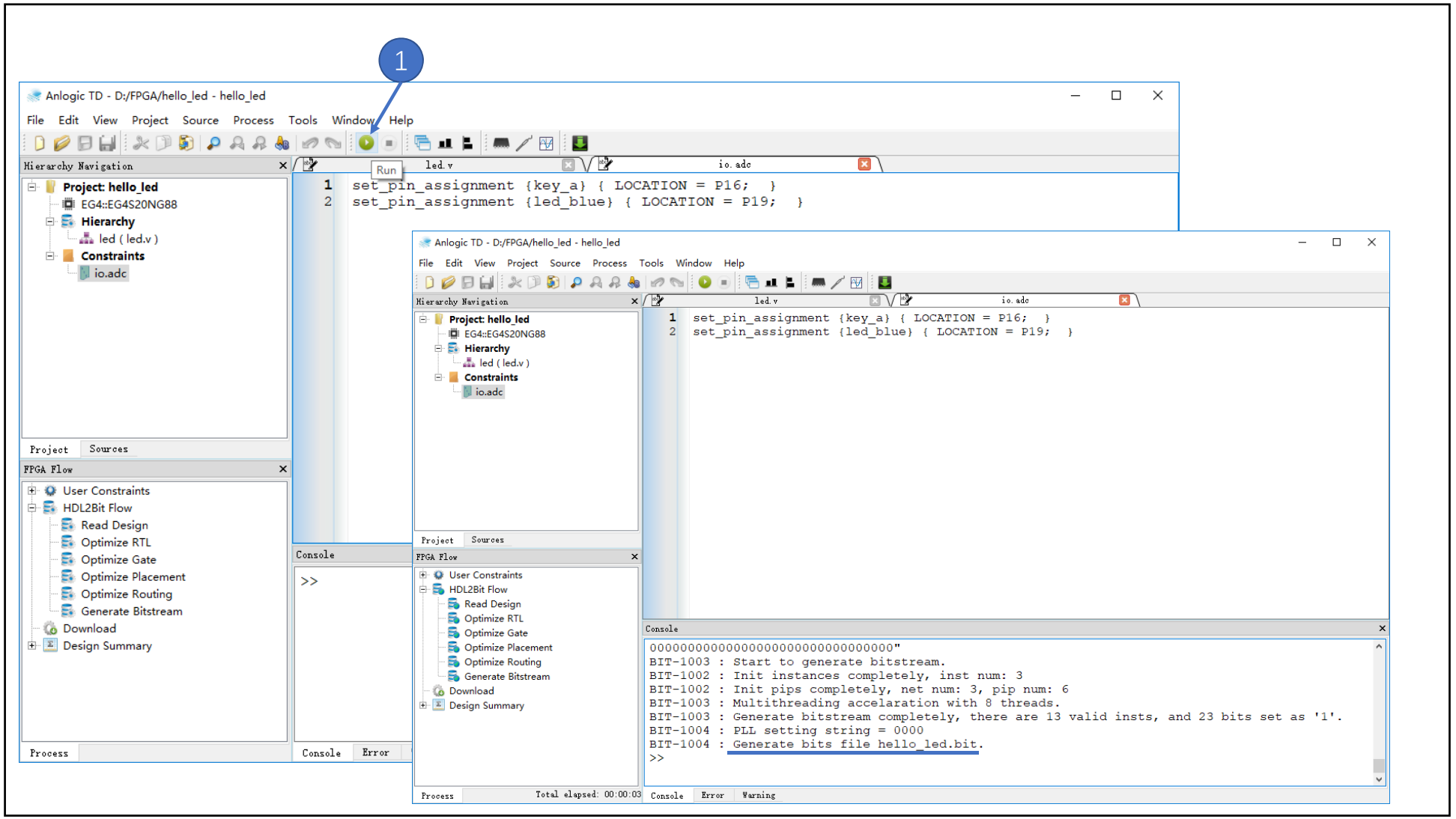

Anlogic TD - D:/FPGA/hello_led - hello_led
File Edit View Project Source Process Tools Window Help
New Ctrl+N
Open... Ctrl+O
Close Ctrl+F4
Save Ctrl+S
Save As...
Save All
Recent Files
Recent Projects
Preferred Editor
Exit Ctrl+Q
1
led.v
module led
Project Sources
FPGA Flow
User Constraints
HDL2Bit Flow
Read Design
Optimize RTL
Optimize Gate
Optimize Placement
Optimize Routing
Generate Bitstream
Download
Design Summary
Process
3
Untitled2.txt
set_pin_assignment {key_a} { LOCATION = P16; }
set_pin_assignment {led_blue} { LOCATION = P19; }
2
Save As
此电脑 › LENOVO (D:) › FPGA › hello_led
搜索"hello_led"
组织 新建文件夹
src
OneDrive
此电脑
3D 对象
视频
图片
文档
下载
音乐
桌面
Windows (C:)
LENOVO (D:)
名称 修改日期 类型 大小
.hello_led.al 2019/7/23 14:41 BAK 文件 1 KB
hello_led 2019/7/23 14:41 TD Project 1 KB
led 2019/7/23 14:40 V 文件 1 KB
td_2019-07-23_14-38-09 2019/7/23 14:38 文本文档 0 KB
4
文件名(N): io.adc
保存类型(T): All Files(*.*)
隐藏文件夹
保存(S)
取消
5
Console
ARC-1001 : tdi/tms/tck/tdo
ARC-1001 : ----------
ARC-1004 : Device setting, marked
RUN-1003 : finish command "import_
3.187500s user + 0.109375s system
RUN-1004 : used memory is 185 MB, reserved memory is 143 MB, peak memory is 185 MB
HDL-1007 : analyze verilog file led.v
HDL-1007 : analyze verilog file led.v
Console Error Warning

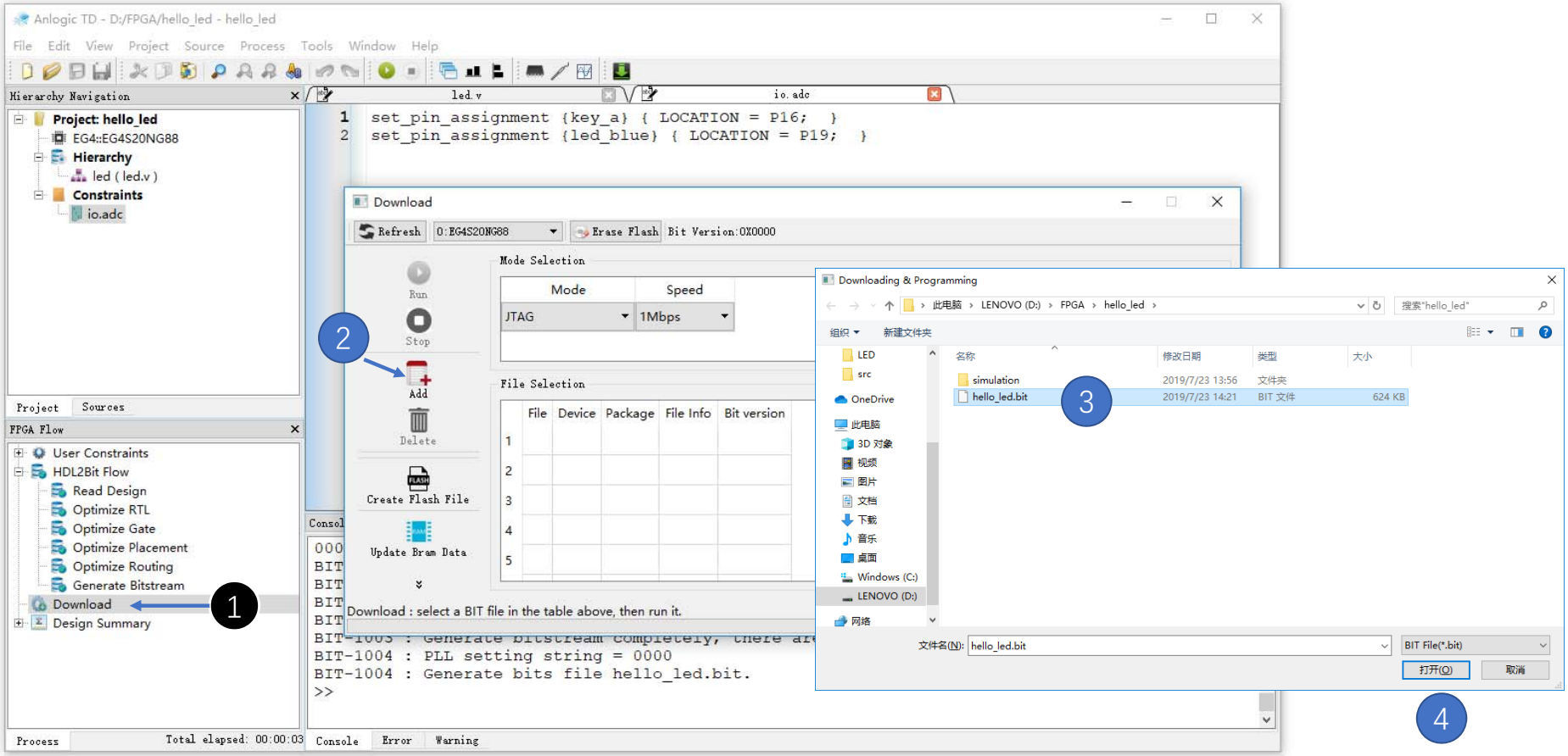
io.adc：

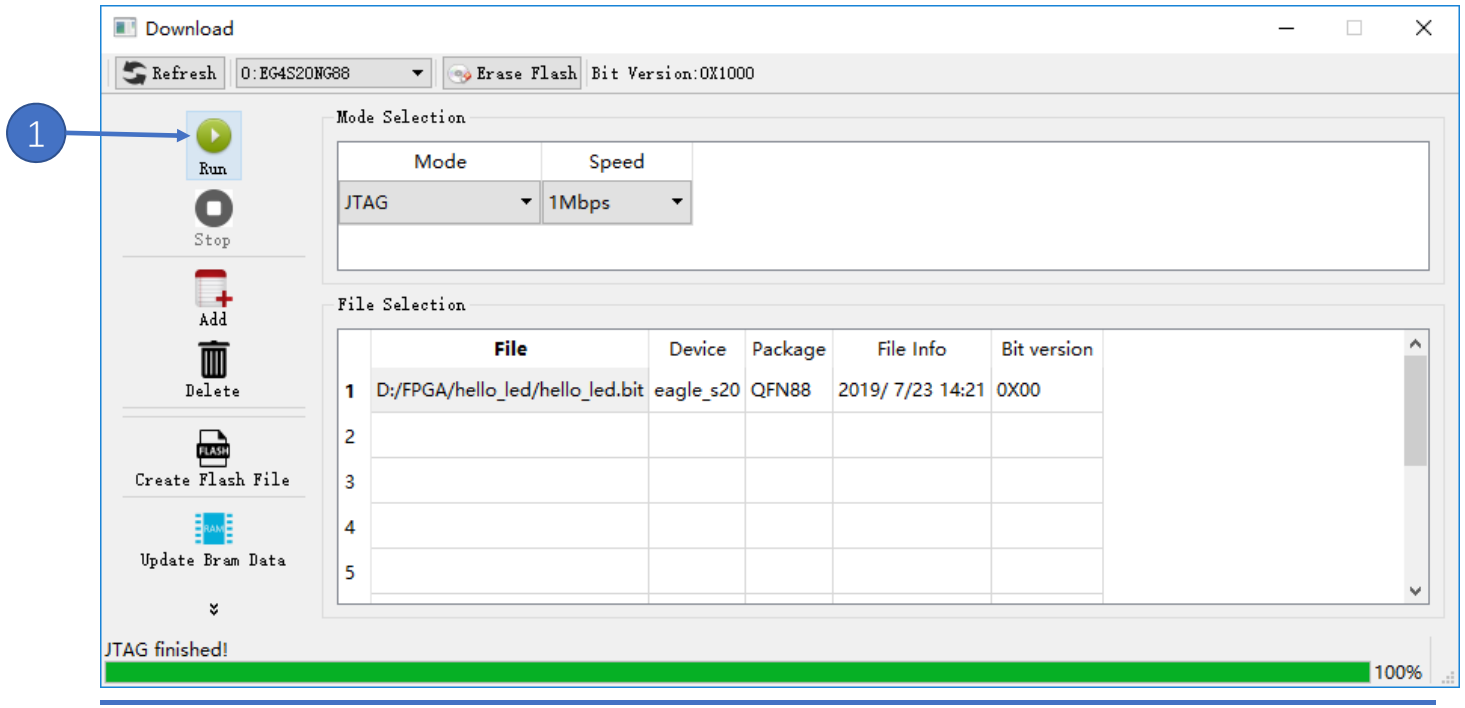
For Spark Road：
set_pin_assignment {key_a} { LOCATION = G11; }
Set_pin_assignment {led_blue} { LOCATION = N16; }

For Spark Road Micro：
set_pin_assignment {key_a} { LOCATION = P16; }
Set_pin_assignment {led_blue} { LOCATION = P19; }


Anlogic TD - D:/FPGA/hello_led - hello_led
File Edit View Project Source Process Tools Window Help
Hierarchy Navigation
Project: hello_led
EG4::EG4S20NG88
Hierarchy
led (led.v)
Constraints
Add ADC File
Add SDC File
Add CWC File
Collape All
Expand All
1
Project Sources
FPGA Flow
User Constraints
HDL2Bit Flow
Read Design
Optimize RTL
Optimize Gate
Optimize Placement
Optimize Routing
Generate Bitstream
Download
Design Summary
Process
led.v
io.adc
1 set_pin_assignment {key_a} { LOCATION = P16; }
2 set_pin_assignment {led_blue} { LOCATION = P19; }
Console
ARC-1001 : tdi/tms/tck
ARC-1001 : ----------
ARC-1004 : Device setting, ma
RUN-1003 : finish command "im
3.187500s user + 0.109375s sy
RUN-1004 : used memory is 185
HDL-1007 : analyze verilog fi
HDL-1007 : analyze verilog fi
Console Error Warning
Open
此电脑 › LENOVO (D:) › FPGA › hello_led ›
搜索"hello_led"
组织 新建文件夹
LED
src
OneDrive
此电脑
3D 对象
视频
图片
文档
下载
音乐
桌面
Windows (C:)
LENOVO (D:)
网络
名称 修改日期 类型 大小
simulation 2019/7/23 13:56 文件夹
io 2019/7/23 14:18 ADC 文件 1 KB
2
文件名(N): io
ADC File(*.adc)
打开(O)
取消
3


1
Anlogic TD - D:/FPGA/hello_led - hello_led
File Edit View Project Source Process Tools Window Help
Run
Hierarchy Navigation
Project: hello_led
EG4::EG4S20NG88
Hierarchy
led (led.v)
Constraints
io.adc
Project Sources
FPGA Flow
User Constraints
HDL2Bit Flow
Read Design
Optimize RTL
Optimize Gate
Optimize Placement
Optimize Routing
Generate Bitstream
Download
Design Summary
Process
led.v
io.adc
1 set_pin_assignment {key_a} { LOCATION = P16; }
2 set_pin_assignment {led_blue} { LOCATION = P19; }
Console
>>
Console Error
Anlogic TD - D:/FPGA/hello_led - hello_led
File Edit View Project Source Process Tools Window Help
Hierarchy Navigation
Project: hello_led
EG4::EG4S20NG88
Hierarchy
led (led.v)
Constraints
io.adc
Project Sources
FPGA Flow
User Constraints
HDL2Bit Flow
Read Design
Optimize RTL
Optimize Gate
Optimize Placement
Optimize Routing
Generate Bitstream
Download
Design Summary
Process
Total elapsed: 00:00:03
led.v
io.adc
1 set_pin_assignment {key_a} { LOCATION = P16; }
2 set_pin_assignment {led_blue} { LOCATION = P19; }
Console
00000000000000000000000000000000"
BIT-1003 : Start to generate bitstream.
BIT-1002 : Init instances completely, inst num: 3
BIT-1002 : Init pips completely, net num: 3, pip num: 6
BIT-1003 : Multithreading accelaration with 8 threads.
BIT-1003 : Generate bitstream completely, there are 13 valid insts, and 23 bits set as '1'.
BIT-1004 : PLL setting string = 0000
BIT-1004 : Generate bits file hello_led.bit.
>>
Console Error Warning


Anlogic TD - D:/FPGA/hello_led - hello_led
File Edit View Project Source Process Tools Window Help
Hierarchy Navigation
Project: hello_led
EG4::EG4S20NG88
Hierarchy
led (led.v)
Constraints
io.adc
Project Sources
FPGA Flow
User Constraints
HDL2Bit Flow
Read Design
Optimize RTL
Optimize Gate
Optimize Placement
Optimize Routing
Generate Bitstream
Download
Design Summary
Process Total elapsed: 00:00:03
led.v
io.adc
1 set_pin_assignment {key_a} { LOCATION = P16; }
2 set_pin_assignment {led_blue} { LOCATION = P19; }
Download
Refresh
0:EG4S20NG88
Erase Flash
Bit Version:0X0000
Run
Stop
Add
Delete
Create Flash File
Update Bram Data
Mode Selection
Mode
Speed
JTAG
1Mbps
File Selection
File
Device
Package
File Info
Bit version
Download : select a BIT file in the table above, then run it.
2
Downloading & Programming
此电脑 › LENOVO (D:) › FPGA › hello_led ›
搜索"hello_led"
组织
新建文件夹
LED
src
OneDrive
此电脑
3D 对象
视频
图片
文档
下载
音乐
桌面
Windows (C:)
LENOVO (D:)
网络
名称
修改日期
类型
大小
simulation
2019/7/23 13:56
文件夹
hello_led.bit
2019/7/23 14:21
BIT 文件
624 KB
3
文件名(N): hello_led.bit
BIT File(*.bit)
打开(O)
取消
4
BIT-1004 : PLL setting string = 0000
BIT-1004 : Generate bits file hello_led.bit.
>>
Console Error Warning
1


Download
Refresh
0:EG4S20NG88
Erase Flash
Bit Version:0X1000
1
Run
Stop
Add
Delete
Create Flash File
Update Bram Data
Mode Selection
Mode
Speed
JTAG
1Mbps
File Selection
File
Device
Package
File Info
Bit version
1
D:/FPGA/hello_led/hello_led.bit
eagle_s20
QFN88
2019/ 7/23 14:21
0X00
2
3
4
5
JTAG finished!
100%

Press the Key labled “A” （Spark Road Micro）
or the Central Key(Spark Road)
and see what happened!

Enjoy Yourself!

Programming Flash