Cortex®-M0 DesignStart™ Eval (AT510)

r2p0-00rel0

Release Note

Cortex-M0 DesignStart Eval Release Note

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Product status

The information in this document is for a product at Full Release status.

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Feedback

ARM limited welcomes feedback on both the product, and the documentation.

Support for Cortex-M0 DesignStart Eval

Support is not provided with Cortex-M0 DesignStart Eval. However, if you have a question you can post it on the ARM DesignStart community at https://community.arm.com/processors/designstart/.

Feedback on this document

If you have any comments about this document, please send email to errata@arm.com giving:

- The document title
- The document's number
- The page number(s) to which your comments refer
- A concise explanation of your comments

General suggestion for additions and improvements are also welcome.

ARM Internal Document Reference

PJDOC-466751330-760 1.0

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Contents

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1 PRODUCT DELIVERABLES

1.1 Product Release Status

This is a full release of ARM Cortex-M0 DesignStart Eval at revision r2p0. These deliverables are released under the terms of the agreement between ARM and each licensee (the "Agreement"). Use by recipient of the deliverables is subject to the terms and conditions of the Agreement.

1.2 About Cortex-M0 DesignStart Eval

Cortex-M0 DesignStart Eval is intended for system Verilog design and simulation of a prototype SoC based on the Cortex-M0 processor.

Cortex-M0 DesignStart Eval includes:

- An ARM Cortex-M0 processor (as obfuscated RTL)
- An example system-level design for the ARM Cortex-M0 processor, based around the ARM Cortex-M prototyping system FPGA platform.
- Reusable AMBA components for system-level development.

Cortex-M0 DesignStart Eval uses a fixed configuration of the Cortex-M0 processor, enabling low cost easy access to Cortex-M0 processor technology by offering a subset of the full product.

The processor in Cortex-M0 DesignStart Eval is delivered as a preconfigured and obfuscated, but synthesizable, Verilog version of the full Cortex-M0 processor and is intended for integration and simulation purposes. It includes debug within the obfuscated integration level and is not intended for production silicon. The other system level components and peripherals are provided in standard Verilog.

An FPGA bitstream is provided which you can load on the ARM® Versatile™ Express Cortex®-M Prototyping System (MPS2+). This FPGA platform must be purchased separately.

The RTL system integration can be modified, allowing the user to customize logic surrounding the Cortex-M0 processor. Subject to the constraints of the FPGA, a modified system can be synthesized to an MPS2+ bitstream using the Quartus Prime FPGA design tool (using the free or paid versions of this tool).

1.3 ARM Part Numbers for Cortex-M0 DesignStart Eval

The Cortex-M0 DesignStart Eval product is delivered as a single zipped tar file through ARM's IP delivery server.

The following table lists the ARM part number for the Cortex-M0 DesignStart Eval product.

Table *1.3-1*: ARM part number Cortex-M0 DesignStart Eval

Product code	Description	Version
AT510-MN-80001	Cortex-M0 DesignStart Eval Package	r2p0-00rel0

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2 INSTALLATION

2.1 Introduction

These installation instructions only cover the UNIX platform/operating system.

2.2 Installation procedure

After download, you will have a single zipped tar file:

```
AT510-MN-80001-r2p0-00rel0.tgz
```

The installation procedure is summarized below:

2.2.1 Unpacking the shipment

The following steps describe how to unpack the Cortex-M0 DesignStart Eval product deliverable.

1. **Relocate the shipment file**

Copy the tgz file to the directory where it is to be installed.

2. **Extract tar files**

   Extract the tar file contents using the UNIX GNU tar utility:

```
gtar –zxvf AT510-MN-80001-r2p0-00rel0.tgz
```

> **NOTE:** A version of GNU tar later than 1.13 should be used to untar the deliverables as some versions of tar have problems dealing with very long path names. To find the version of gtar being used type `gtar --version`.

This will extract the deliverables into a directory named the same as the deliverable number: `AT510-MN-80001-r2p0-00rel0`.

2.3 Directory Structure

Figure 2-1 shows the principal directory structure of this release created after unpacking the bundle:

```
AT510-MN-80001-r2p0-00rel0/
├── Documentation/
├── cores/
│   └── cortexm0_designstart_r2p0/
├── logical/
├── Recovery/
├── RevC/
├── smm_common/
├── software/
├── systems/
│   ├── cortex_m0_mcu/
│   └── fpga_testbench/
```

Figure 2-1: Principal directory structure after unpacking the bundle

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2.4 Documentation

The Cortex-M0 DesignStart Eval product includes the following documents which you should refer to for specific tasks:

- ARM® Cortex®-M0 DesignStart™ Eval User Guide.
  - Understand the deliverables which integrate a configuration of Cortex-M0, the Cortex-M System Design kit example system, and some basic peripherals. This includes a description of the integration tests.

- ARM® Cortex®-M0 DesignStart™ Eval FPGA User Guide.
  - Understand how to use the MPS2+ FPGA platform to evaluate software running on the Cortex-M0 DesignStart platform. This includes how to build an updated FPGA image.

2.5 License for Keil MDK

A limited term license (with no code size restrictions) for ARM Keil Microcontroller Development Kit (MDK) is available when you register to download Cortex-M0 DesignStart Eval.

3 TOOLS

3.1 Tools

This release of Cortex-M0 DesignStart Eval has been developed with the following tools:

- Mentor Questasim 10.4e_1
- Cadence Incisive 15.20.008
- Synopsys VCS 2016.06-SP2
- ARM DS5 5.06.409
- ARM Keil MDK 5.22
- GNU GCC GNU Tools for ARM Embedded Processors (ARM GCC) version 5-2016q2.
- Intel Quartus 16.1
- Perl 5 version 22

3.2 Operating Systems

This release has been developed with the following operating system:

- Linux RHE6 64-bit
- Microsoft Windows 10

3.3 ARM Keil MDK

If you use ARM Keil MDK for software development, you can install the design kit in a location that is accessible from Linux, UNIX, and Windows. Do this using one of the following procedures:

- Install the design kit on a network drive that:
  - A Linux or UNIX terminal can access.
  - Is mapped to a network drive on a Windows machine.

- Use a personal computer to do the following:
  - Install virtualization software and install a guest Operating System (OS).
  - Set up a shared folder to access the design kit through the host OS.
  - Install the design kit in the shared folder.

Then compile the software with ARM Keil MDK in the Windows environment, and run the simulations in the Linux or UNIX environment.

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3.4 Simulation

This release of Cortex-M0 DesignStart Eval supports Linux and UNIX operating systems for the simulation process.

3.5 FPGA Synthesis

FPGA synthesis can be run on Linux, UNIX or Windows operating systems without modification. When working on Windows, you should keep your working area close to the root directory of your drive since the length of paths in the design database can cause problems. This example indicates a typical location which has been confirmed to work:

`C:\designs\AT510-MN-80001-r2p0-00rel0\RevC\SMM_M0DS\synthesis`

4 KNOWN ISSUES AND LIMITATIONS

Please refer to section 1.3 of the ARM® Cortex®-M0 DesignStart™ Eval User Guide.

5 DIFFERENCES FROM PREVIOUS RELEASE

5.1 Changes since the r1p0-00rel0 release

The Cortex-M0 processor and the `CORTEXM0INTEGRATION` level of hierarchy in the design are flattened to produce an obfuscated RTL image which includes debug for simulation and FPGA synthesis.

The FPGA synthesis flow for the MPS2+ platform uses the obfuscated processor RTL and is built as a single image. This flow is supported by all versions of the Quartus tool.

The simulation testbenches and the FPGA flow are delivered in a single package.

ARM Keil and gcc toolchain support is added for the FPGA testbench.

The “ARM® Cortex®-M0 DesignStart™ FPGA Prototyping Kit" document has been replaced by the "Arm® Cortex®-M0 DesignStart™ Eval FPGA User Guide" document.

6 SUPPORT

Support is not provided with Cortex-M0 DesignStart Eval. However, if you have a question you can post it on the ARM DesignStart community at https://community.arm.com/processors/designstart/.

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