POR	RT	AF0		AF1	TIN 42	AF2	TI) 45	TD 40	AF3	1201	AF4	12.02	CDI1	AF5	CDI4	CDI2	AF6	CDIS	CDI2	AF7	LICADES	AF8	AF9	AF10	AF12	ADC		配置
-	0	SYS	TIM1	TIM2 CH1 / ETR	11M3	TIM4	CH1	11M9	TIM10 TIM11	12C1	12C2	I2C3	SPI1	SPI2	SPI4	SP13	SPI4	SPIS	SPI3	USART1	USART2 CTS	USART6	I2C2 I2C	3 OIG_FS	SDIO	ADC1_IN0	X	
	1			CH2			CH2								MOSI						RTS					ADC1_IN1	X	
	2			СН3			CH3	CH1													TX					ADC1_IN2	X	
_	3			CH4			CH4	CH2													RX					ADC1_IN3	X	KEY
	4			CIII / ETD									NSS			NSS					CK					ADC1_IN4	X	
	5		BKIN	CH1 / ETR	CH1								SCK MISO												CMD	ADC1_IN5 ADC1_IN6	X X	
	7		CH1N		CH2								MOSI												CIVID	ADC1_IN7	X	
PA	8		CH1									SCL								CK				SOF	D1	_ `	X	
	9		CH2									SMBA								TX				VBUS	D2		X	
	10		CH3															MOSI		RX				ID			X	LED_B
	11		CH4														MISO) (IGO		CTS		TX		DM			X	LED_G
	12 13	SDIO	ETR															MISO		RTS		RX		DP			X X	LED_R SWDIO
		SCLK																									X	SWCLK
		JTDI		CH1 / ETR									NSS			NSS				TX							X	CS
	0		CH2N		СНЗ													SCK								ADC1_IN8	X	
	1		CH3N		CH4													NSS								ADC1_IN9	X	
		BOOT		CITA									COL			CON				DI			an.				X	COV
		JTDO JTRST		CH2	CH1								SCK MISO			SCK MISO				RX			SDA SD	,	D0		X X	SCK SDO
	5	1131			CH2					SMBA			MOSI			MOSI							3D	-1	D3		X	SDI
	6					CH1				SCL										TX							X	TX
PB	7					CH2				SDA										RX					D0		X	RX
1.5	8					CH3			CH1	SCL								MOSI					SD	A	D4		X	IRQ
	9			CITA		CH4			CH1	SDA	COL			NSS									SDA		D5		X	RST
	10			СНЗ							SCL			SCK											D7		X	
	12		BKIN								SMBA			NSS			NSS		SCK								X	
	13		CH1N											SCK			SCK										X	
	14		CH2N											MISO											D6		X	
	15	RTC	CH3N											MOSI											CK		X	
DC.	13																										X v	EXTON WAKE
_																												WAKE
PC	14 15																										X X	