Do	ORT	AF0	AF1		AF2		AF3		AF4		AF5			AF6			AF7			AF8	AF9	AF1				配置		
1,		SYS	TIM1		TIM3	TIM4	TIM5	TIM9	TIM10 TIM11	I2C1	I2C2	I2C3	SPI1	SPI2	SPI4	SPI3	SPI4	SPI5	SPI3	USART1	USART2	USART6	I2C2 I2	C3 OTG_	FS SDI)		
	0			CH1 / ETR			CH1														CTS					ADC1_IN0		
	1			CH2			CH2								MOSI						RTS					ADC1_IN1	X	
	2 3 4 5			CH3			CH3	CH1													TX					ADC1_IN2		
				CH4			CH4	CH2					NIGG			NIGG					RX					ADC1_IN3	X	
				CHI / ETD									NSS			NSS					CK					ADC1_IN4	X	
			BKIN	CH1 / ETR	CH1								SCK												CM	ADC1_IN5		
	7		CH1N		CH1 CH2								MISO MOSI												CIVII	ADC1_IN6 ADC1_IN7		
PA	8		CH1		CHZ							SCL	MOSI							CK				SOF	D1	_	X	
	9 10 11 12 13	WICOI	CH2									SMBA								TX				VBU			X	
			CH3									SIVIDIT						MOSI		RX				ID	<i>D</i> 2		X	_
			CH4														MISO	111051		CTS		TX		DM			X	_
			ETR															MISO		RTS		RX		DP			X	
		SDIO																									X	
		SCLK																									X	
	15	JTDI		CH1 / ETR									NSS			NSS				TX							X	EXP05
	0		CH2N		СН3													SCK								ADC1_IN8	X	IMU_INTM
	1		CH3N		CH4													NSS								ADC1_IN9	X	
	3 4	BOOT																									X	
		JTDO		CH2									SCK			SCK				RX			SDA				X	
		JTRST			CH1					ar ar			MISO			MISO							SI	PΑ	D0		X	
	5				CH2	CIII				SMBA SCL			MOSI			MOSI			_	TV					D3		X	
	7					CH1 CH2				SDA										TX RX					D0		X X	_
PB	8					CH3			CH1	SCL								MOSI	_	KΛ			SI	Δ.	D4		X	_
	9 10 12 13					CH4			CH1	SDA				NSS				WOSI					SDA	71	D5		X	——————————————————————————————————————
				СН3		CIII			CIII	SDIT	SCL			SCK									SDN		D7		X	——————————————————————————————————————
			BKIN								SMBA			NSS			NSS		SCK								X	IMU_CSM
			CH1N											SCK			SCK										X	IMU_SCK
	14		CH2N											MISO											D6		X	
	15	RTC	CH3N											MOSI											CK		X	
	13																										X	_
PC	14																										X	
	15																										X	LED_B