Р	ORT	AF0		AF1		AF2			AF3		AF4			AF5			AF6			AF7		AF8	AF9			AF12	ADC		配置
		SYS		TIM2	TIM3	TIM4	TIM5	TIM9	TIM10 TIM11	I2C1	I2C2	I2C3	SPI1	SPI2	SPI4	SPI3	SPI4	SPI5	SPI3	USART1		USART6	I2C2 I	2C3 C	OTG_FS	SDIO			
	0			CH1 / ETR			CH1) (OGT						CTS						ADC1_IN0	X	
	1			CH2			CH2	CHI							MOSI						RTS						ADC1_IN1	X	
	2			CH3 CH4			CH3 CH4	CH1 CH2													TX RX						ADC1_IN2 ADC1_IN3	X	UWB_RST UWB_WAK
	3			СП 4			СП4	СП2					NSS			NSS					CK						ADC1_IN3 ADC1_IN4	X	
	5			CH1 / ETR									SCK			Nob					CK						ADC1_IN4 ADC1_IN5	X	
	6		BKIN	CIII / LIII	CH1								MISO													CMD	ADC1_IN6	X	
	7		CH1N		CH2								MOSI														ADC1_IN7	X	
P	8	MCO1	CH1									SCL								CK					SOF	D1	_	X	
	9		CH2									SMBA								TX					VBUS	D2		O	EA9
	10		CH3															MOSI		RX					ID			O	EA10
	11		CH4														MISO			CTS		TX			DM			X	USB_DM
	12		ETR															MISO		RTS		RX			DP			X	USB_DP
	13	SDIO																										O	SWDIO
	14	SCLK		CVIA / FIED) va a) Y G G												0	SWCLK
\vdash	15	JTDI		CH1 / ETR									NSS			NSS		CCV		TX				_			ADC1 INO	0	IMU_CSB
	0		CH2N CH3N		CH3 CH4													SCK NSS									ADC1_IN8 ADC1_IN9	O X	EB0 ADC_BAT
	2.	BOOT	CHISIN		CH													Noo									ADCI_IIV9	X	KEY
	3	JTDO		CH2									SCK			SCK				RX			SDA					X	IMU_SCK
	4	JTRST			CH1								MISO			MISO								DA		D0		X	
РВ	5				CH2					SMBA			MOSI			MOSI										D3		X	IMU_SDI
	6					CH1				SCL										TX								O	SWD_TX
	3 7					CH2				SDA										RX						D0		O	SWD_RX
	8					CH3			CH1	SCL								MOSI						DA		D4		O	
	9			GYYA		CH4			CH1	SDA	a a*			NSS									SDA			D5		0	
	10			CH3							SCL			SCK												D7		0	EB10
	12		BKIN								SMBA			NSS			NSS		SCK									0	EB12
	13		CH1N								SI/IB/I			SCK			SCK		Bell									O	EB13
	14		CH2N											MISO												D6		O	EB14
	15	RTC	CH3N											MOSI												CK		O	EB15
	13																											X	LED_B
PO	C 14																											X	LED_G
	15																											X	LED_R