

S U M M A R Y

H.264 Compression VHDL source code

The VHDL source code from Zexia described here consists of a number of modules released under a BSD license. These modules are intended to form a complete H.264 compliant encoder which can be customised to specific application. The design consists of a number of components to perform specific operations such as CAVLC, plus logic to tie them together.

The design has been targeted at Xilinx Spartan 3 devices, but no Xilinx specific components have been used so the design can be ported to other targets if required.

Power dissipation is low, typically 100mW, but this does not include off-chip RAM (needed to store whole images, if they are large). This corresponds to Baseline Profile Level 4 in Annex A of the standard.

The components are independently upgradeable. A choice of Intra Prediction and Inter Prediction modules are available, and customised modules may be developed to suit requirements. In particular for Inter Prediction: to do a good search over all likely pixels and sub-pixels would be either very time consuming or very large in terms of logic, so a decision must be made as to the resource to use for prediction. Typically adding additional resource does not enhance quality, for a given quantisation level, but does reduce image size, ie, video bit rate.

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