Espressif ESP8285 What we know so far

admin
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Espressif's new ESP8285 chip announced around 2 months ago and I can't wait to get it to my hands. I gathered some information about it so you can have a look below.

> *Espressif announces mass production of the ESP8285 Wi-Fi chip today, adding a new member to Espressif's Wi-Fi connectivity portfolio. This is a spinoff product of ESP8266, embedded with 1 MByte flash memory and specially designed for wearable devices, such as smartwatches, smart glasses, activity monitors and smart bracelets.*
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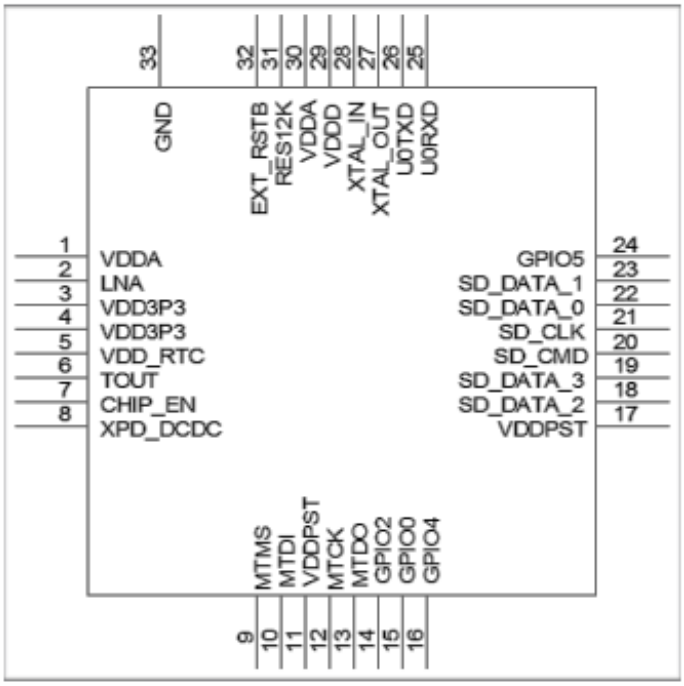
> *According to market research firm IDC, the wearables industry is expected to grow rapidly over the next few years, with unit shipments estimated to exceed 112 million by 2018. Driven by a surging need for flash memory to support the growing range of devices, Espressif has offered a more focused alternative with ESP8285 to meet the demand for smaller PCB size as required in wearable applications.*



> *The chip includes an enhanced version of Tensilica's L106 Diamond series 32-bit processor with flash memory of 1 MByte. Like its predecessor, ESP8285 is a highly integrated Wi-Fi SoC solution that will meet users' continuous demands for efficient power usage, compact design and reliable performance in the Internet of Things industry.*

Espressif's ESP8285 delivers highly integrated Wi-Fi SoC solution to meet users' continuous demands for efficient power usage, compact design and reliable performance in the Internet of Things industry. With the complete and self-contained Wi-Fi networking capabilities, ESP8285 can perform either as a standalone application or as the slave to a host MCU. When ESP8285 hosts the application, it promptly boots up from the flash.

The integrated high-speed cache helps to increase the system performance and optimize the system memory. Also, ESP8285 can be applied to any micro-controller design as a Wi-Fi adaptor through SPI / SDIO or I2C / UART interfaces. ESP8285 integrates antenna switches, RF balun, power amplifier, low noise receive amplifier, filters and power management modules. The compact design minimizes the PCB size and requires minimal external circuitries. Besides the Wi-Fi functionalities, ESP8285 also integrates an enhanced version of Tensilica's L106 Diamond series 32-bit processor and on-chip SRAM.

It can be interfaced with external sensors and other devices through the GPIOs. Software Development Kit (SDK) provides sample codes for various applications. Espressif Systems' Smart Connectivity Platform (ESCP) enables sophisticated features including fast switch between sleep and wake-up mode for energy-efficient

purpose, adaptive radio biasing for low-power operation, advance signal processing, spur cancellation and radio co-existence mechanisms for common cellular, Bluetooth, DDR, LVDS, LCD interference mitigation.

Wi-Fi Protocol

• 802.11 b/g/n/e/i support.

• Wi-Fi Direct (P2P) support.

• P2P Discovery, P2P Group Owner mode, P2P Power Management.

• Infrastructure BSS Station mode / P2P mode / softAP mode support.

• Hardware accelerators for CCMP (CBC-MAC, counter mode), TKIP (MIC, RC4), WAPI (SMS4), WEP (RC4), CRC.

• WPA/WPA2 PSK, and WPS driver.

• Additional 802.11i security features such as pre-authentication, and TSN.

• Open Interface for various upper layer authentication schemes over EAP such as TLS, PEAP, LEAP, SIM, AKA, or customer specific.

• 802.11n support (2.4 GHz).

• Supports MIMO 1×1 and 2×1, STBC, A-MPDU and A-MSDU aggregation and 0.4μs guard interval.

• WMM power save U-APSD.

• Multiple queue management to fully utilize traffic prioritization defined by 802.11e standard.

• UMA compliant and certified. • 802.1h/RFC1042 frame encapsulation.

• Scattered DMA for optimal CPU off load on Zero Copy data transfer operations.

• Antenna diversity and selection (software managed hardware).

• Clock/power gating combined with 802.11-compliant power management dynamically adapted to current connection condition providing minimal power consumption.

• Adaptive rate fallback algorithm sets the optimum transmission rate and Tx power based on actual SNR and packet loss information.

• Automatic retransmission and response on MAC to avoid packet discarding on slow host environment.

• Seamless roaming support.

• Configurable packet traffic arbitration (PTA) with dedicated slave processor based design provides flexible and exact timing Bluetooth co-existence support for a wide range of Bluetooth Chip vendors.

• Dual and single antenna Bluetooth co-existence support with optional simultaneous receive (Wi-Fi/Bluetooth) capability

CPU

ESP8285 integrates Tensilica L106 32-bit micro controller (MCU) and ultra-low-power 16- bit RSIC. The CPU clock speed is 80 MHz. It can also reach a maximum value of 160 MHz. Real Time Operation System (RTOS) is enabled. Currently, only 20% of MIPS has been occupied by the Wi-Fi stack, the rest can all be used for user application programming and development. The CPU includes the interfaces as below. • Programmable RAM/ROM interfaces (iBus), which can be connected with memory controller, and can also be used to visit flash. • Data RAM interface (dBus), which can connected with memory controller. • AHB interface which can be used to visit the register.

Memory

ESP8285 Wi-Fi SoC integrates memory controller and memory units including SRAM and ROM. MCU can access the memory units through iBus, dBus, and AHB interfaces. All memory units can be accessed upon request, while a memory arbiter will decide the running sequence according to the time when these requests are received by the processor. According to our current version of SDK, SRAM space available to users is assigned as below. RAM size < 50 kB, that is, when ESP8285 is working under the station mode and connects to the router, programmable space accessible in heap + data section is around 50 kB. • There is no programmable ROM in the SoC, therefore, user program must be stored in a SPI flash.

Flash

ESP8285 has a built-in SPI flash to store user programs. • Memory size: 1 MByte • SPI mode: Dual Out

High Frequency Clock

The high frequency clock on ESP8285 is used to drive both transmit and receive mixers. This clock is generated from internal crystal oscillator and external crystal. The crystal frequency ranges from 26 MHz to 52 MHz. The internal calibration inside the crystal oscillator ensures that a wide range of crystals can be used, nevertheless the quality of the crystal is still a factor to consider to have reasonable phase noise and good Wi-Fi sensitivity. Refer to Table 3-1 to measure the frequency offset.

Radio

ESP8285 radio consists of the following blocks. • 2.4 GHz receiver • 2.4 GHz transmitter • High speed clock generators and crystal oscillator • Real time clock • Bias and regulators • Power management