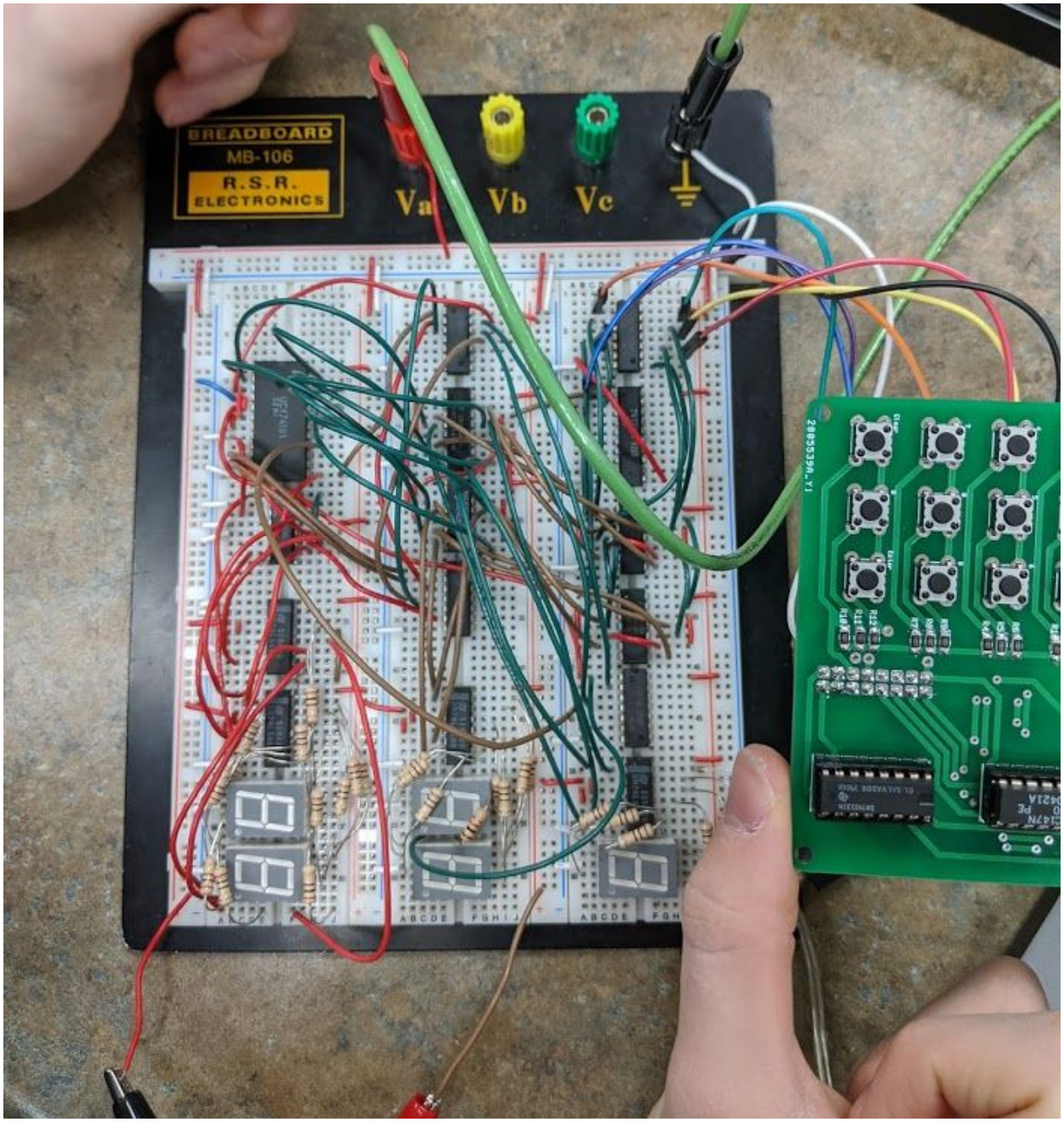
Experiment 40

ALU Adder-Subtractor



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11/25/19 - 12/11/19

Objectives:

The objective of this lab was to create a 4-bit Adder-Subtractor using an ALU (Arithmetic Logic Unit) and display the output using seven-segment displays.

Materials:

- 1 - ALU (Arithmetic Logic Unit) IC (74181) (Datasheet pages 5-7)
- 1 - 4-Bit Adder IC (7483)
- 5 - BCD to 7 Segment Decoder IC (7448)
- 5 - LED 7 Segment Displays (FND500)
- 2 - Hex Inverter Logic IC (7404)
- 1 - OR Logic IC (7432) (Datasheet page 8)
- 1 - AND Logic IC (7408) (Datasheet page 9)
- 2 - NAND Logic IC (7400) (Datasheet page 10)
- 2 - SR Latch Logic IC (74279)
- 1 - D-Type Flip-Flop Logic IC (74273)
- 1 - SPDT Linear Switch
- 29 - 200Ω Resistors
- 1 - Keypad PCB

Procedure:

1. To begin the lab a data sheet was found for the ALU chip online (shown on pages 5-7). This datasheet contains both the pin outputs for the chip along with an operating table to figure out what the selector switches' inputs must be set to so it can carry out a required operation along with what the Carry-In (C_n) and Mode control (M) inputs.

2. Using the datasheet it was found that the ALU could be switched between an adder and subtractor by toggling the SPDT switch. To get to the adder and subtractor operation the C_n input was set to a high and the M input was set to a low. This set the chip into active high operands as well as an Arithmetic mode which meant the ALU would act as a chip that could do arithmetic. To get the chip to add or subtract the following selector switch inputs were used as shown below in the ALU datasheet. The adding function is "A plus B" while the subtraction function is "A minus B minus 1" with the extra minus one because the C_n is high and the extra one gets rid of the unwanted C_n. The ALU does 2's complement in the chip for subtraction as it can't directly subtract B from A it inverts B, adds a one, and then adds the two together.

3. Once the ALU datasheet was found a circuit was designed on multisim as shown in figure 2 and tested as the inputs are both 9 and the ALU is set to adding mode and the output is shown as 18. The circuit works by taking two inputs from the keypad PCB and sending the two inputs into the ALU along with two 7448 IC's and two seven segment displays to show the two numbers being used in the ALU. The ALU is pre-set with a high on C_n and a low on M and to add or subtract the selector switches S_0-S_3 must be set to the required values shown in the gate datasheet for the 74181 chip. Once the arithmetic function is selected the output is sent to an adder IC that will correct the BCD number if it is illegal, and will not be able to be displayed on the 7 segment displays. This is achieved by adding 6 to the output of the ALU using a 4-bit Adder and a correction circuit as seen in figure 1. The output of this adder is finally sent to two 7448 ICs' which are hooked up to two 7 segment displays to show the output of the Adder-Subtractor.

4. This multisim design was built physically as shown in figure 3 and worked as expected as 9 plus 9 also equaled 18 on the physical circuit proving our design to be correct as well as accurate.

Figure 1

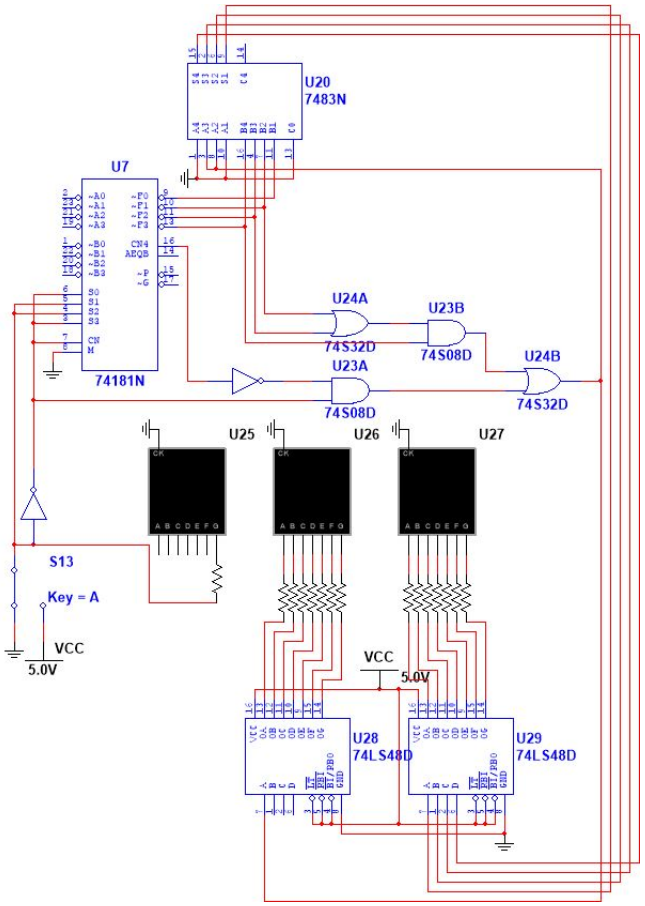


Figure 2

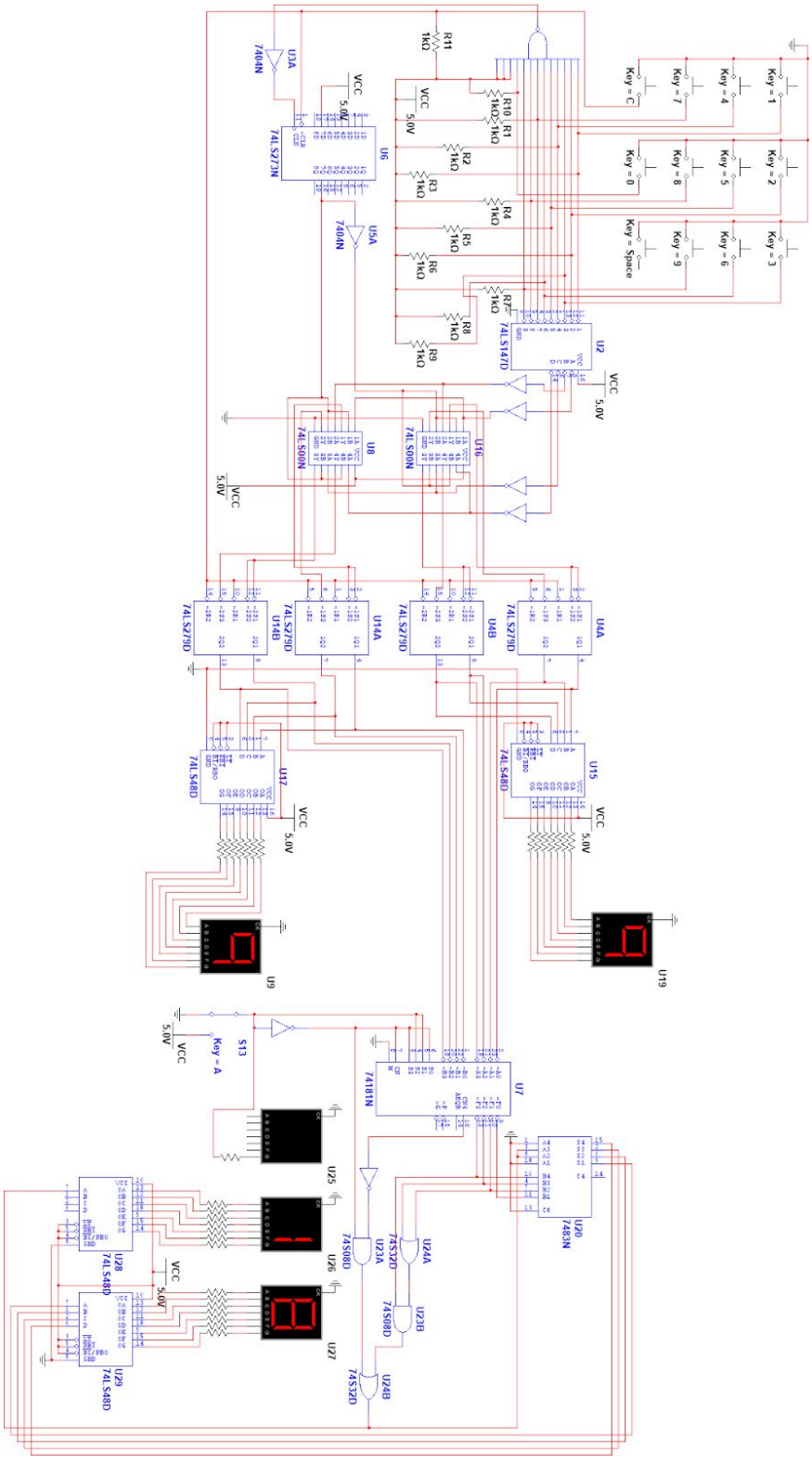
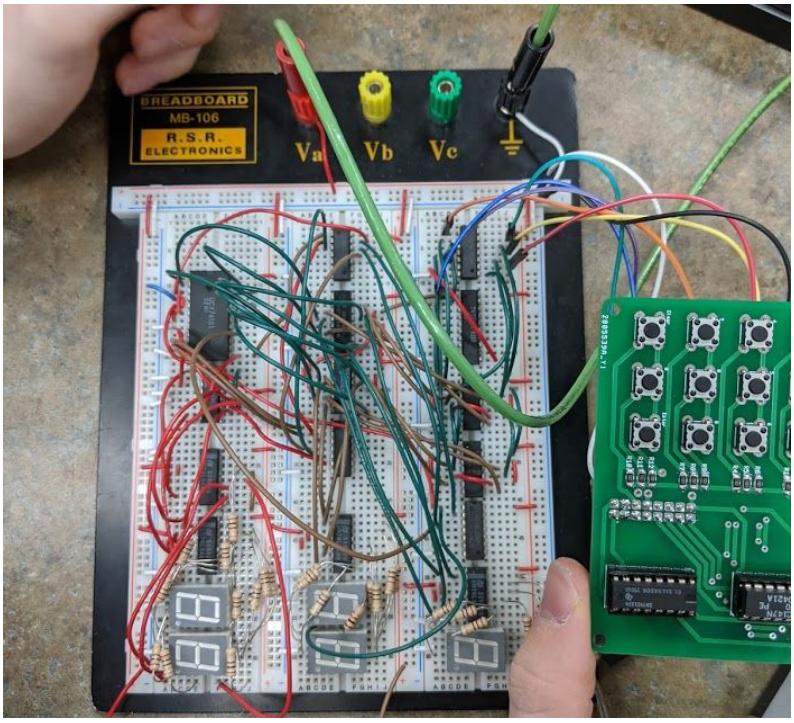

R11 1kΩ
R10 1kΩ
R1 1kΩ
R2 1kΩ
R3 1kΩ
R4 1kΩ
R5 1kΩ
R6 1kΩ
R7 1kΩ
R8 1kΩ
R9 1kΩ
VCC 5.0V
U3A 7404N
U5A 7404N
U6 74LS273N
U2 74LS147D
U8 74LS00N
U16 74LS00N
U14B 74LS279D
U14A 74LS279D
U4B 74LS279D
U4A 74LS279D
U17 74LS48D
U15 74LS48D
U9
U19
U7 74181N
U20 7483N
U25
U26
U27
U28 74LS48D
U29 74LS48D
U23A 74S32D
U24A 74S32D
U23B 74S08D
U24B 74S32D
74S08D
S13 Key = A
Key = C
Key = 7
Key = 4
Key = 1
Key = 0
Key = 8
Key = 5
Key = 2
Key = Space
Key = 9
Key = 6
Key = 3

Figure 3



Discussion:

This project was fairly easy to complete as the ALU acted similarly to the 4-bit Adder/Subtractor the week before making this circuit simple to produce along with the keypad. The keypad makes inputting numbers easier as instead of inputting a binary number only a decimal number has to be selected on the pad which is actually a binary number on the circuit board.

Conclusion:

An ALU (Arithmetic Logic Unit) chip can perform complex operations on two different inputs and can perform 16 logic or 16 arithmetic operations for a total of 32 operations. To select an operation a binary number must be inputted into the selector switches and each number designates a different function. For this lab, only "A plus B" and "A minus B minus 1" was utilized. "A plus B" was selected by inputting a high on S_0, a low on both S_1 and S_2, and a high on S_3. "A minus B minus 1" was selected by inputting a low on S_0, a high on both S_1 and S_2, and a low on S_3. "A minus B minus 1" is used instead of just "A minus B" as the C_n being high would cancel out the "minus 1" and "A minus B" isn't a selectable function on this ALU. The circuit other than the newly added ALU chip works the same as the 4-bit Adder/Subtractor with 7 segment displays used to visualize the BCD numbers in decimal and an adder after the ALU to forbid any illegal BCD outputs.

FAIRCHILD SEMICONDUCTOR TM

October 1988
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DM74LS181
4-Bit Arithmetic Logic Unit

General Description

The DM74LS181 is a 4-bit Arithmetic Logic Unit (ALU) which can perform all the possible 16 logic operations on two variables and a variety of arithmetic operations.

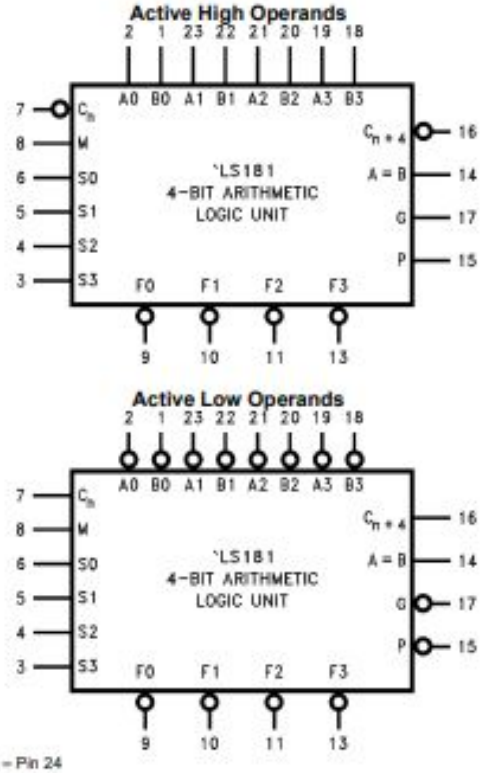
Features

- Provides 16 arithmetic operations: add, subtract, compare, double, plus twelve other arithmetic operations
- Provides all 16 logic operations of two variables: exclusive-OR, compare, AND, NAND, OR, NOR, plus ten other logic operations
- Full lookahead for high speed arithmetic operation on long words

Ordering Code:

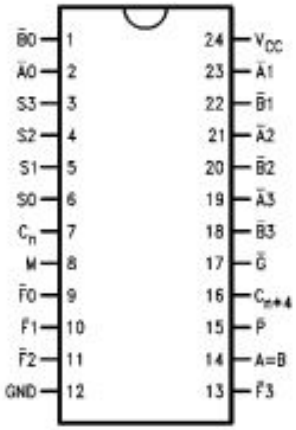
Order Number	Package Number	Package Description
DM74LS181N	N24A	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.600 Wide

Logic Symbols



V_{CC} = Pin 24
GND = Pin 12

Connection Diagram



Pin Descriptions

Pin Names	Description
$\overline{A}0$–$\overline{A}3$	Operand Inputs (Active LOW)
$\overline{B}0$–$\overline{B}3$	Operand Inputs (Active LOW)
S0–S3	Function Select Inputs
M	Mode Control Input
C_n	Carry Input
$\overline{F}0$–$\overline{F}3$	Function Outputs (Active LOW)
A = B	Comparator Output
$\overline{G}$	Carry Generate Output (Active LOW)
$\overline{P}$	Carry Propagate Output (Active LOW)
C_{n+4}	Carry Output

ALU Pin outputs

Functional Description

The DM74LS181 is a 4-bit high speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select inputs (S0–S3) and the Mode Control input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active HIGH or active LOW operands. The Function Table lists these operations

When the Mode Control input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control input is LOW, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the C_{n+4} output, or for carry lookahead between packages using the signals $\overline{P}$ (Carry Propagate) and $\overline{G}$ (Carry Generate). In the ADD mode, $\overline{P}$ indicates that $\overline{F}$ is 15 or more, while $\overline{G}$ indicates that $\overline{F}$ is 16 or more. In the SUBTRACT mode, $\overline{P}$ indicates that $\overline{F}$ is zero or less, while $\overline{G}$ indicates that $\overline{F}$ is less than zero. $\overline{P}$ and $\overline{G}$ are not affected by carry in. When speed requirements are not stringent, it can be used in a simple ripple carry mode by connecting the Carry output (C_{n+4}) signal to the Carry input (C_n) of the next unit. For high speed operation the device is used in conjunction with the 9342 or 93S42 carry lookahead circuit. One carry lookahead package is required for each group of four DM74LS181 devices. Carry lookahead can be provided at various levels and offers high speed capability over extremely long word lengths.

The A = B output from the device goes HIGH when all four $\overline{F}$ outputs are HIGH and can be used to indicate logic equivalence over four bits when the unit is in the subtract mode. The A = B output is open-collector and can be wired-AND with other A = B outputs to give a comparison for more than four bits. The A = B signal can also be used with the C_{n+4} signal to indicate A > B and A < B.

The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus a carry is generated when there is no underflow and no carry is generated when there is underflow. As indicated, this device can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

Function Table

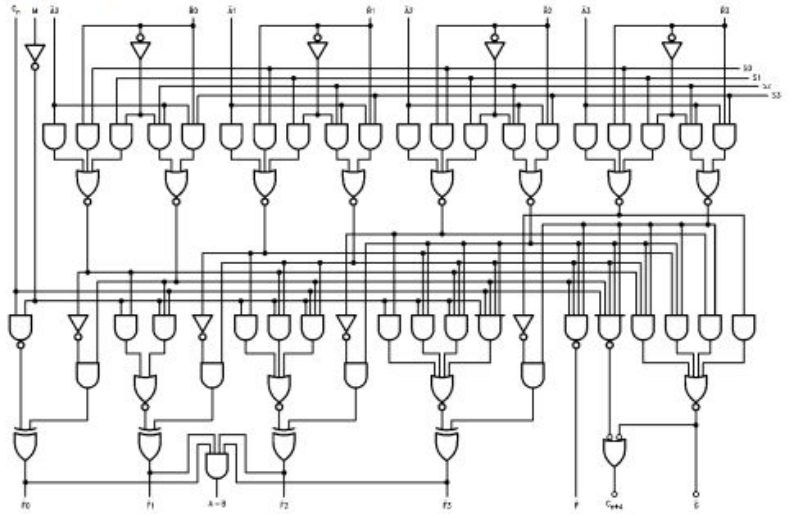
Mode Select Inputs				Active LOW Operands & F_n Outputs		Active HIGH Operands & F_n Outputs	
				Logic	Arithmetic (Note 2)	Logic	Arithmetic (Note 2)
S3	S2	S1	S0	(M = H)	(M = L) (C_n = L)	(M = H)	(M = L) (C_n = H)
L	L	L	L	$\overline{A}$	A minus 1	$\overline{A}$	A
L	L	L	H	$\overline{AB}$	AB minus 1	$\overline{A} + \overline{B}$	A + B
L	L	H	L	$\overline{A} + \overline{B}$	$A\overline{B}$ minus 1	$\overline{A}B$	$A + \overline{B}$
L	L	H	H	Logic 1	minus 1	Logic 0	minus 1
L	H	L	L	$\overline{A} + \overline{B}$	A plus $(A + \overline{B})$	$\overline{AB}$	A plus $A\overline{B}$
L	H	L	H	$\overline{B}$	AB plus $(A + \overline{B})$	$\overline{B}$	$(A + B)$ plus $A\overline{B}$
L	H	H	L	$\overline{A} \oplus \overline{B}$	A minus B minus 1	$A \oplus B$	A minus B minus 1
L	H	H	H	$A + \overline{B}$	$A + \overline{B}$	$A\overline{B}$	AB minus 1
H	L	L	L	$\overline{A}B$	A plus (A + B)	$\overline{A} + B$	A plus AB
H	L	L	H	$A \oplus B$	A plus B	$\overline{A} \oplus \overline{B}$	A plus B
H	L	H	L	B	$A\overline{B}$ plus (A + B)	B	$(A + \overline{B})$ plus AB
H	L	H	H	A + B	A + B	AB	AB minus 1
H	H	L	L	Logic 0	A plus A (Note 1)	Logic 1	A plus A (Note 1)
H	H	L	H	$A\overline{B}$	AB plus A	$A + \overline{B}$	$(A + B)$ plus A
H	H	H	L	AB	$A\overline{B}$ minus A	A + B	$(A + \overline{B})$ plus A
H	H	H	H	A	A	A	A minus 1

Note 1: Each bit is shifted to the next most significant position.

Note 2: Arithmetic operations expressed in 2s complement notation.

ALU Operations and Description of its' Functions

Logic Diagram



Absolute Maximum Ratings (Note 3)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 3: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−0.4	mA
I_{OL}	LOW Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 4)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max		2.7			V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min			0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min			0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	M input $\overline{A}_n$, $\overline{B}_n$ S_n C_n			0.1 0.3 0.4 0.5	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V	M input $\overline{A}_n$, $\overline{B}_n$ S_n C_n			20 60 80 100	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V	M input $\overline{A}_n$, $\overline{B}_n$ S_n C_n			−0.4 −1.2 −1.6 −2.0	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 5)		−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max, $\overline{B}_n$, C_n = GND S_n, M, $\overline{A}_n$ = 4.5V				37	mA

Note 4: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

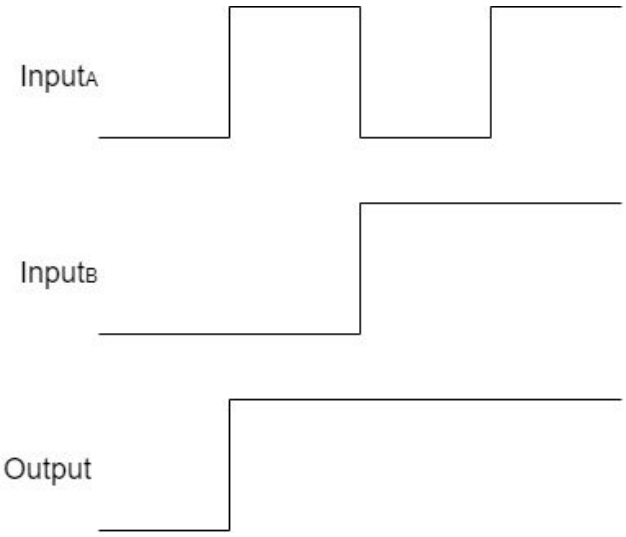
Gates in the ALU and Operating characteristics

OR Gate

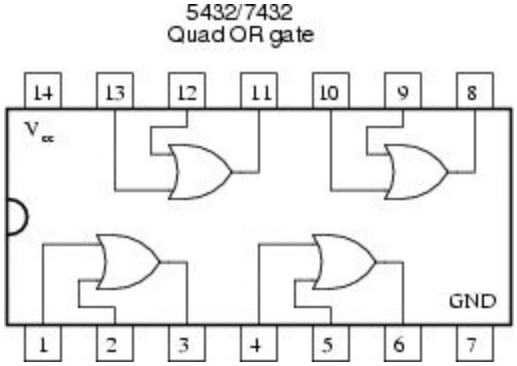
OR Gate Truth Table

Real World (5V Vcc)			Multisim		
$Input_A$	$Input_B$	Output	$Input_A$	$Input_B$	Output
0V	0V	0.1	L	L	L
5V	0V	4.3	H	L	H
0V	5V	4.3	L	H	H
5V	5V	4.3	H	H	H
Boolean equation: $A + B = X$					

OR Gate Timing



OR Gate IC Pinout



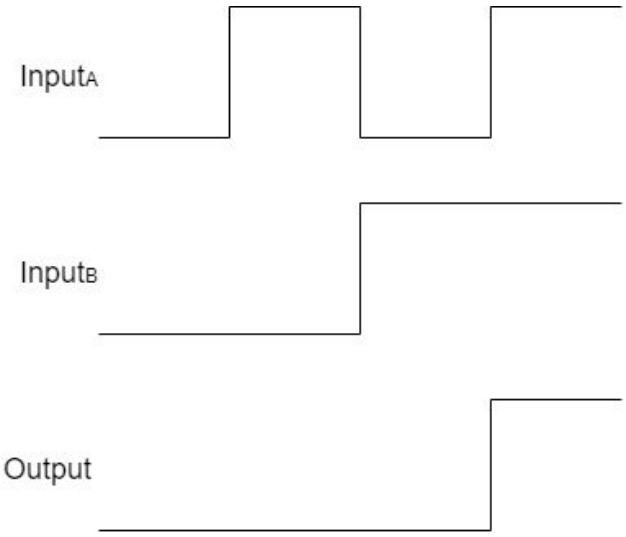
OR Gate Symbol

AND Gate

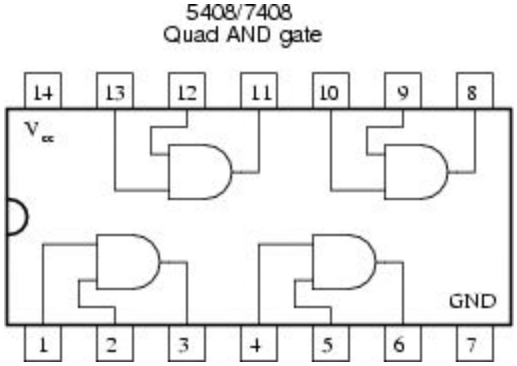
AND Gate Truth Table

Real World (5V Vcc)			Multisim		
$Input_A$	$Input_B$	Output	$Input_A$	$Input_B$	Output
0	0	0.1	L	L	L
5	0	0.1	H	L	L
0	5	0.1	L	H	L
5	5	4.3	H	H	H
Boolean equation: $A\ B = X$					

AND Gate Timing



AND Gate IC Pinout



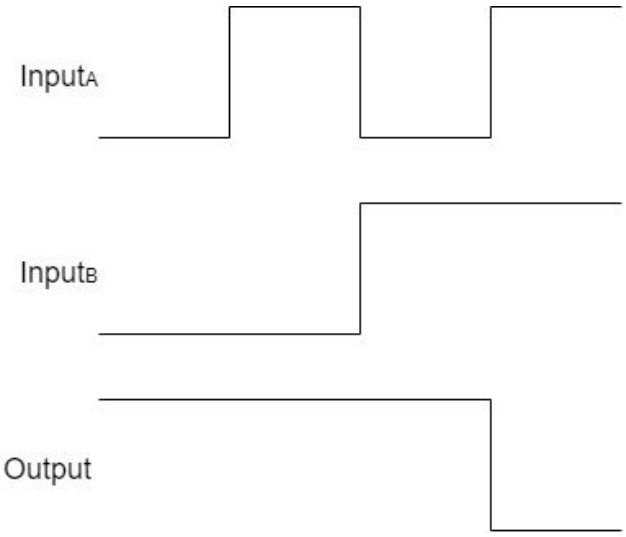
AND Gate Symbol

NAND Gate

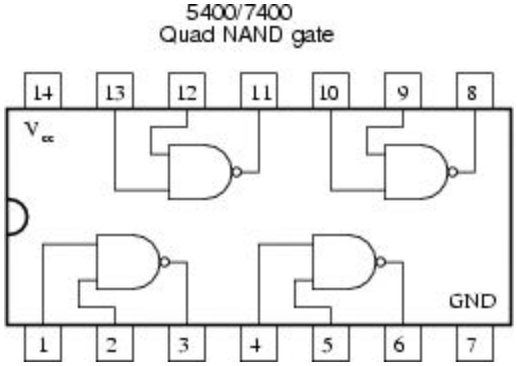
NAND Gate Truth Table

Real World (5V Vcc)			Multisim		
$Input_A$	$Input_B$	Output	$Input_A$	$Input_B$	Output
0	0	4.3	L	L	H
5	0	4.3	H	L	H
0	5	4.3	L	H	H
5	5	0.1	H	H	L
Boolean equation: $\overline{A\,B} = X$					

NAND Gate Timing



NAND Gate IC Pinout



NAND Gate Symbol