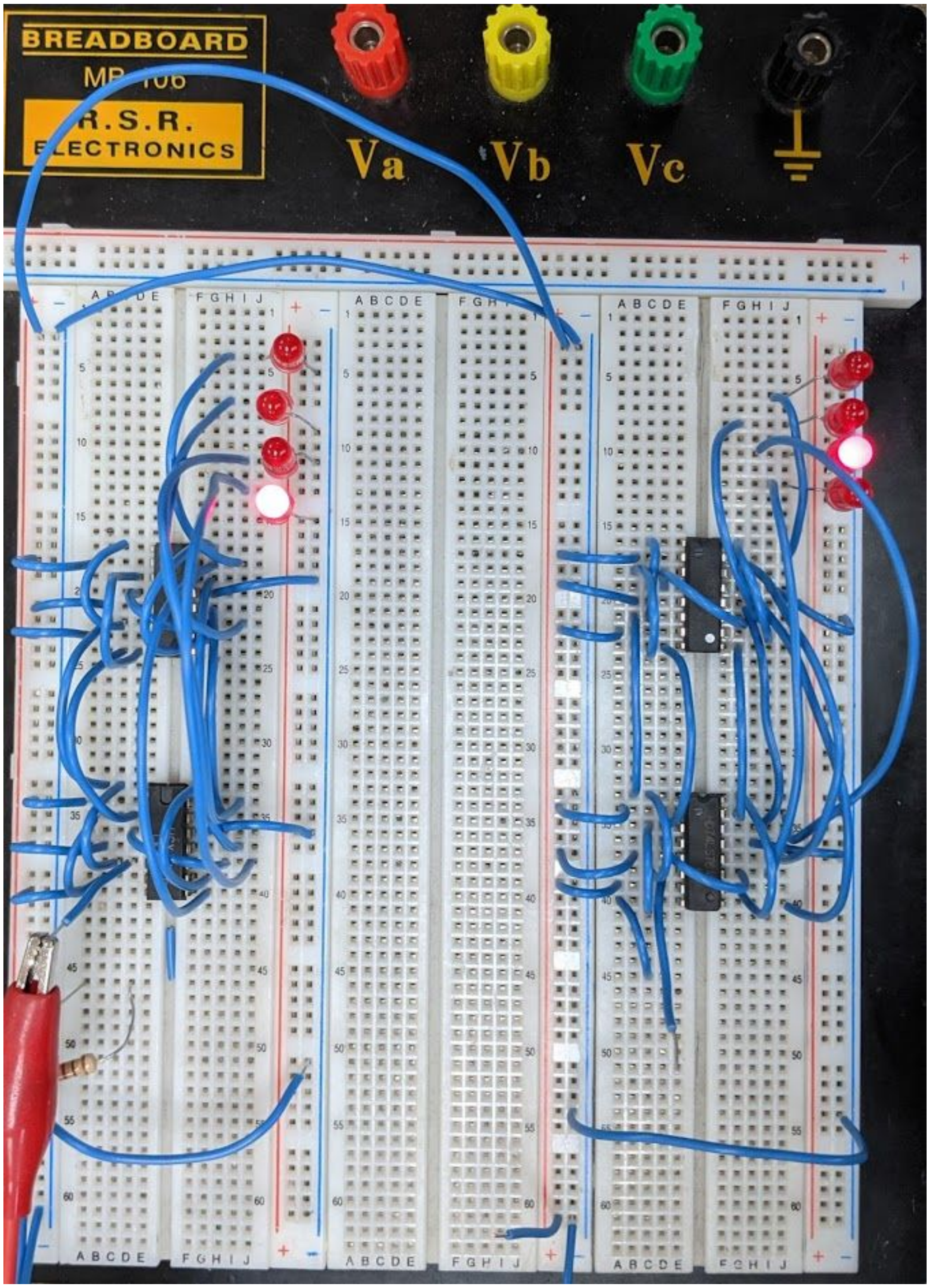
4-Bit Ring and Johnson Shift Registers



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2/24/20-2/28/10

Objective: Build a 4-bit Ring and Johnson shift register using LED's to show the output along with a multisim that shows the output of each JK Flip-Flop.

Materials:

- 4 - 7476 IC
- 8 - Red LED's
- 1 - 1.001 uF capacitor
- 1 - 1k Ω resistor
- A computer with multisim software
- Jumper Wire
- Wire Strippers & Cutters
- DC Power Supply
- AC Function Generator
- Google Docs

Procedure:

1. First, we refreshed ourselves on the basis of shift registers. We read our textbooks and took note of the schematics.

2. We constructed a ring shift register in multisim, connecting each J to the Q before it and each K to the ~Q before it. This setup resulted in a binary 1 (active LED) being shifted to the right every clock pulse and then resetting back to the first LED after reaching the final Flip-Flop. This is shown in figure 1.

3. We then built a johnson shift register by connecting the final Q to the first K, and the final ~Q to the first J. This resulted in all four of our inputs being converted, one at a time (sequentially from left to right) to a 1, and then being converted in a similar fashion to all zeroes. This circuit is shown in figure 3.

4. We tested both configurations in multisim, found them to be functional, and used an oscilloscope to plot the output of each JK Flip-Flop. The plotting of the outputs reinforced the fact that both registers were working properly.

5. On the breadboard, the circuit was able to operate as expected and each register acted like its multisim counterpart. The Johnson Registers' LED's would light up one at a time and stay lit until all four were active then they would turn off one by one until all of the LED's were not being powered. The Ring Shift Register would start with no LED's active and as each pulse occurred the light would go from one light to another until it hit all 4 LED's with only one LED being lit at a time. This can be found in figure 5.

Multisim Circuits

Figure 1: Ring Shift Register

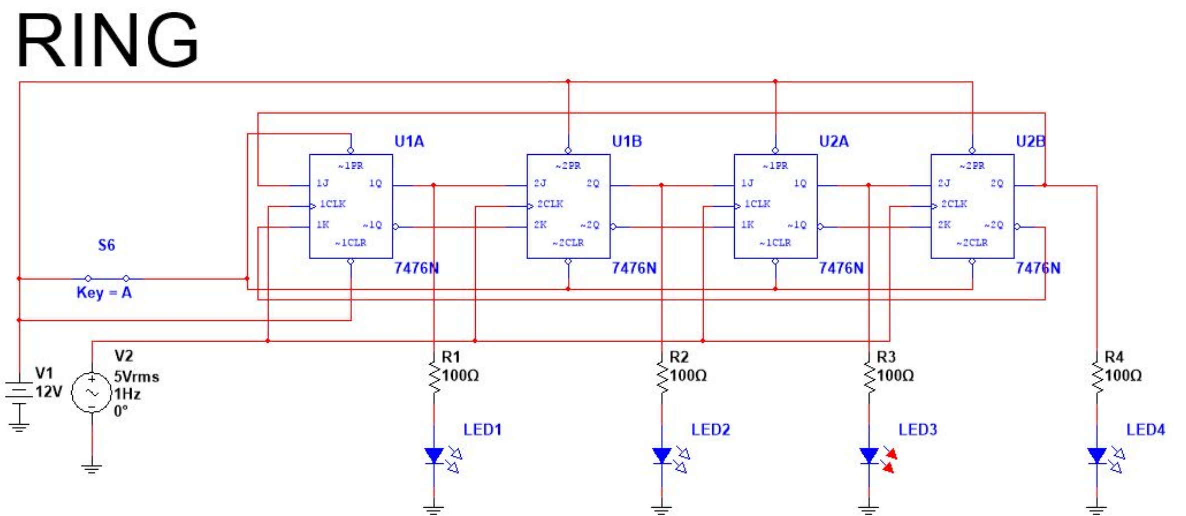


Figure 2: Digital Diagram of Ring Shift Register Outputs

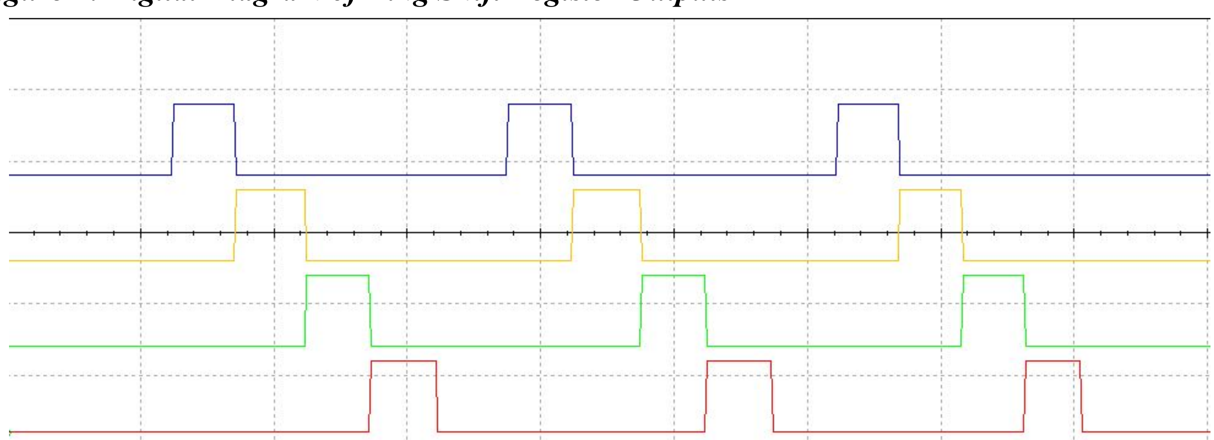


Figure 3: Johnson Register

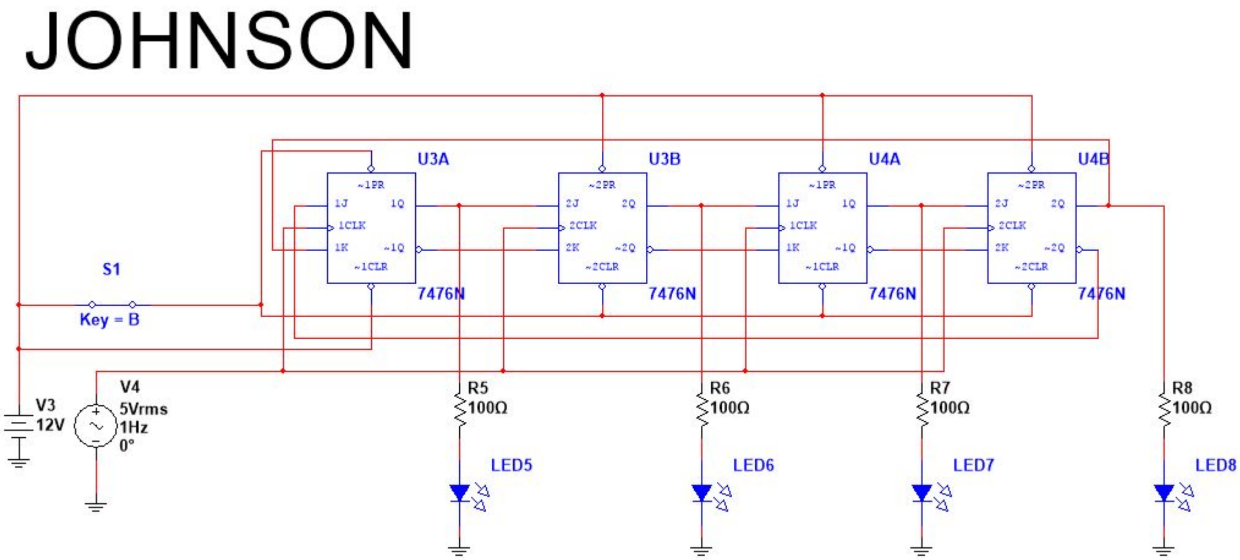


Figure 4: Digital Diagram of Johnson Register Outputs

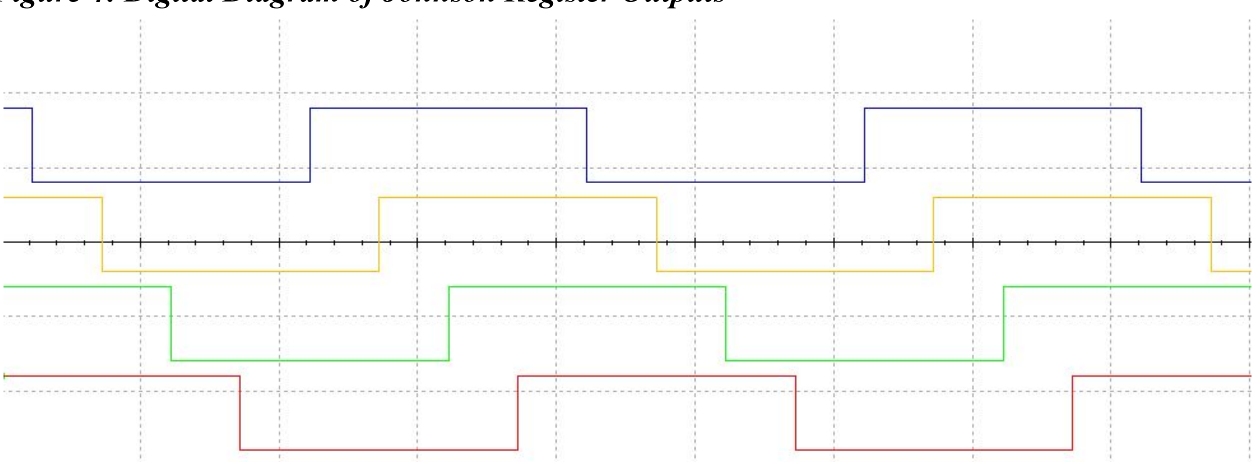
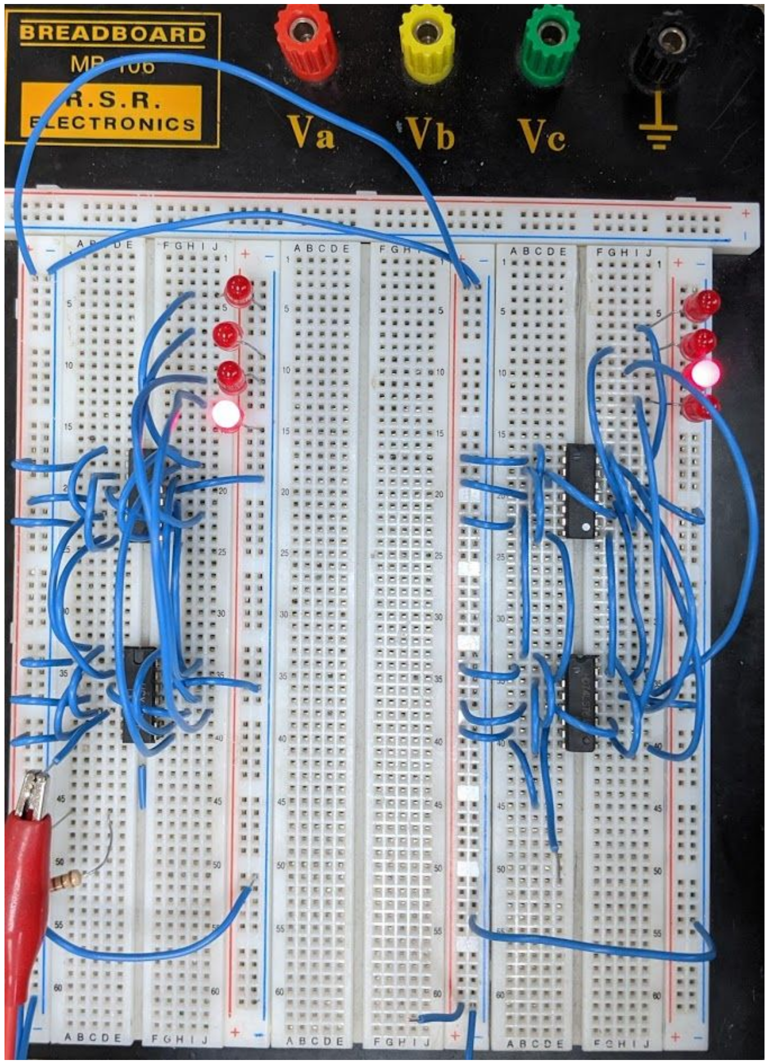


Figure 5: Physical Circuit



Discussion:

While creating the breadboard it was found that the circuit could be simplified down to only use 2 chips as the only difference between the Ring and Johnson shift registers is how the output of the final JK flip-flop is connected to the initial input of the first JK flip-flop.

Conclusion:

A Ring Shift Register is a register that shifts over a high after every clock pulse. After each clock pulse the LED's reset and continues the process. This shifts the illuminating LED to shift over each time. This can be used in applications such as an electronic roulette wheel. A Johnson Shift Register inputs a high until all of the JK's are high. Once this happens, the process repeats only outputting a low this time.

DUAL J-K FLIP-FLOPS WITH PRESET AND CLEAR

SDLS121 – DECEMBER 1983 – REVISED MARCH 1988

- **Package Options Include Plastic and Ceramic DIPs and Ceramic Flat Packages**
- **Dependable Texas Instruments Quality and Reliability**

SN5476, SN54LS76A . . . J PACKAGE
SN7476 . . . N PACKAGE
SN74LS76A . . . D OR N PACKAGE
(TOP VIEW)

1CLK	1	16	1K
1 $\overline{PRE}$	2	15	1Q
1 $\overline{CLR}$	3	14	1$\overline{Q}$
1 J	4	13	GND
V_{CC}	5	12	2K
2CLK	6	11	2Q
2 $\overline{PRE}$	7	10	2$\overline{Q}$
2 $\overline{CLR}$	8	9	2J

description

The '76 contains two independent J-K flip-flops with individual J-K, clock, preset, and clear inputs. The '76 is a positive-edge-triggered flip-flop. J-K input is loaded into the master while the clock is high and transferred to the slave on the high-to-low transition. For these devices the J and K inputs must be stable while the clock is high.

The 'LS76A contain two independent negative-edge-triggered flip-flops. The J and K inputs must be stable one setup time prior to the high-to-low clock transition for predicatble operation. The preset and clear are asynchronous active low inputs. When low they override the clock and data inputs forcing the outputs to the steady state levels as shown in the function table.

The SN5476 and the SN54LS76A are characterized for operation over the full military temperature range of −55°C to 125°C. The SN7476 and the SN74LS76A are characterized for operation from 0°C to 70°C.

**'76
FUNCTION TABLE**

INPUTS					OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	⎍	L	L	Q_0	$\overline{Q}_0$
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	TOGGLE	

**'LS76A
FUNCTION TABLE**

INPUTS					OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

† This configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.