ICM42688P eMD Driver

2.0.9

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Chapter 1

Deprecated List

Member ICM426XX_SERIAL_IF_TYPE_t

Kept for retrocompatibility. Replaced with `uint32_t` type in `struct inv_icm426xx_serif` struct.

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Chapter 5

Module Documentation

5.1 Driver

High-level API to drive the device.

Files

- file Icm426xxDriver_HL.h

Classes

- struct inv_icm426xx_sensor_event_t

  Sensor event structure definition.
- struct inv_icm426xx

  Icm426xx driver states definition.
- struct inv_icm426xx_interrupt_parameter_t

  Icm426xx set of interrupt enable flag.

Macros

- #define INV_ICM426XX_LIGHTWEIGHT_DRIVER 0

  Lighten driver logic by stripping out procedures on transitions.
- #define PLL_SCALE_FACTOR_Q24 (1UL << 24)

  Scale factor and max ODR Dependant of chip.
- #define ICM_PART_DEFAULT_OIS_MODE ICM426XX_SENSOR_CONFIG2_OIS_MODE_8KHZ
- #define ACCEL_CONFIG0_FS_SEL_MAX ICM426XX_ACCEL_CONFIG0_FS_SEL_16g

  Max FSR values for accel and gyro Dependant of chip.
- #define GYRO_CONFIG0_FS_SEL_MAX ICM426XX_GYRO_CONFIG0_FS_SEL_2000dps
- #define ACCEL_OFFUSER_MAX_MG 1000
- #define GYRO_OFFUSER_MAX_DPS 64
- #define RTC_SUPPORTED 0

  RTC Support flag Define whether the RTC mode is supported Dependant of chip.
- #define ICM426XX_FIFO_MIRRORING_SIZE 16 * 129

  Icm426xx maximum buffer size mirrored from FIFO at polling time.
- #define ICM426XX_DEFAULT_WOM_THS_MG 52 >> 2 /* = 52mg/4 */

  Default value for the WOM threshold Resolution of the threshold is ~= 4mg.
- #define ICM426XX_ACC_STARTUP_TIME_US 20000U

  Icm426xx Accelerometer start-up time before having correct data.
- #define ICM426XX_GYR_STARTUP_TIME_US 60000U

  Icm426xx Gyroscope start-up time before having correct data.

Enumerations

- enum inv_icm426xx_sensor { INV_ICM426XX_SENSOR_ACCEL , INV_ICM426XX_SENSOR_GYRO , INV_ICM426XX_SENSOR_FSYNC_EVENT , INV_ICM426XX_SENSOR_OIS , INV_ICM426XX_SENSOR_TEMPERATURE , INV_ICM426XX_SENSOR_TAP , INV_ICM426XX_SENSOR_DMP_PEDOMETER , INV_ICM426XX_SENSOR_DMP_PEDOMETER_COUNT , INV_ICM426XX_SENSOR_DMP_TILT , INV_ICM426XX_SENSOR_MAX }

  Sensor identifier for UI control and OIS function.
- enum INV_ICM426XX_FIFO_CONFIG_t { INV_ICM426XX_FIFO_DISABLED = 0 , INV_ICM426XX_FIFO_ENABLED = 1 }

  Configure Fifo usage.
- enum inv_icm426xx_interrupt_value { INV_ICM426XX_DISABLE = 0 , INV_ICM426XX_ENABLE }

Functions

- int inv_icm426xx_set_reg_bank (struct inv_icm426xx *s, uint8_t bank)

  Set register bank index.
- int inv_icm426xx_init (struct inv_icm426xx *s, struct inv_icm426xx_serif *serif, void(*sensor_event_cb)(inv_icm426xx_sensor_event_t *event))

  Initializes device.
- int inv_icm426xx_device_reset (struct inv_icm426xx *s)

  Perform a soft reset of the device.
- int inv_icm426xx_get_who_am_i (struct inv_icm426xx *s, uint8_t *who_am_i)

  return WHOAMI value
- int inv_icm426xx_force_clock_source (struct inv_icm426xx *s, ICM426XX_INTF_CONFIG1_ACCEL_LP_CLK_t clk_src)

  Configure Accel clock source.
- int inv_icm426xx_enable_accel_low_power_mode (struct inv_icm426xx *s)

  Enable accel in low power mode.
- int inv_icm426xx_enable_accel_low_noise_mode (struct inv_icm426xx *s)

  Enable accel in low noise mode.
- int inv_icm426xx_disable_accel (struct inv_icm426xx *s)

  Disable accel.
- int inv_icm426xx_enable_gyro_low_noise_mode (struct inv_icm426xx *s)

  Enable gyro in low noise mode.
- int inv_icm426xx_disable_gyro (struct inv_icm426xx *s)

  Disable gyro.
- int inv_icm426xx_enable_fsync (struct inv_icm426xx *s)

  Enable fsync tagging functionality.
- int inv_icm426xx_disable_fsync (struct inv_icm426xx *s)

  Disable fsync tagging functionality.
- int inv_icm426xx_configure_timestamp_resolution (struct inv_icm426xx *s, ICM426XX_TMST_CONFIG_RESOL_t resol)

  Configure timestamp resolution from FIFO.
- int inv_icm426xx_set_config_ibi (struct inv_icm426xx *s, inv_icm426xx_interrupt_parameter_t *interrupt_to_configure)

  Configure which interrupt source can trigger IBI interruptions.
- int inv_icm426xx_get_config_ibi (struct inv_icm426xx *s, inv_icm426xx_interrupt_parameter_t *interrupt_to_configure)

  Retrieve interrupts configuration.

- int inv_icm426xx_set_config_int1 (struct inv_icm426xx *s, inv_icm426xx_interrupt_parameter_t *interrupt_to_configure)

  Configure which interrupt source can trigger INT1.
- int inv_icm426xx_get_config_int1 (struct inv_icm426xx *s, inv_icm426xx_interrupt_parameter_t *interrupt_to_configure)

  Retrieve interrupts configuration.
- int inv_icm426xx_set_config_int2 (struct inv_icm426xx *s, inv_icm426xx_interrupt_parameter_t *interrupt_to_configure)

  Configure which interrupt source can trigger INT2.
- int inv_icm426xx_get_config_int2 (struct inv_icm426xx *s, inv_icm426xx_interrupt_parameter_t *interrupt_to_configure)

  Retrieve interrupts configuration.
- int inv_icm426xx_get_data_from_registers (struct inv_icm426xx *s)

  Read all registers containing data (temperature, accelerometer and gyroscope).
- int inv_icm426xx_get_data_from_fifo (struct inv_icm426xx *s)

  Read all available packets from the FIFO.
- uint32_t inv_icm426xx_convert_odr_bitfield_to_us (uint32_t odr_bitfield)

  Converts `ICM426XX_ACCEL_CONFIG0_ODR_t` or `ICM426XX_GYRO_CONFIG0_ODR_t` enums to period expressed in us.
- int inv_icm426xx_set_accel_frequency (struct inv_icm426xx *s, const ICM426XX_ACCEL_CONFIG0_ODR_t frequency)

  Configure accel Output Data Rate.
- int inv_icm426xx_set_gyro_frequency (struct inv_icm426xx *s, const ICM426XX_GYRO_CONFIG0_ODR_t frequency)

  Configure gyro Output Data Rate.
- int inv_icm426xx_set_accel_fsr (struct inv_icm426xx *s, ICM426XX_ACCEL_CONFIG0_FS_SEL_t accel_fsr_g)

  Set accel full scale range.
- int inv_icm426xx_get_accel_fsr (struct inv_icm426xx *s, ICM426XX_ACCEL_CONFIG0_FS_SEL_t *accel_fsr_g)

  Access accel full scale range.
- int inv_icm426xx_set_gyro_fsr (struct inv_icm426xx *s, ICM426XX_GYRO_CONFIG0_FS_SEL_t gyro_fsr_dps)

  Set gyro full scale range.
- int inv_icm426xx_get_gyro_fsr (struct inv_icm426xx *s, ICM426XX_GYRO_CONFIG0_FS_SEL_t *gyro_fsr_dps)

  Access gyro full scale range.
- int inv_icm426xx_set_accel_lp_avg (struct inv_icm426xx *s, ICM426XX_GYRO_ACCEL_CONFIG0_ACCEL_FILT_AVG_t acc_avg)

  Set accel Low-Power averaging value.
- int inv_icm426xx_set_accel_ln_bw (struct inv_icm426xx *s, ICM426XX_GYRO_ACCEL_CONFIG0_ACCEL_FILT_BW_t acc_bw)

  Set accel Low-Noise bandwidth value.
- int inv_icm426xx_set_gyro_ln_bw (struct inv_icm426xx *s, ICM426XX_GYRO_ACCEL_CONFIG0_GYRO_FILT_BW_t gyr_bw)

  Set gyro Low-Noise bandwidth value.
- int inv_icm426xx_reset_fifo (struct inv_icm426xx *s)

  reset ICM426XX fifo
- int inv_icm426xx_enable_timestamp_to_register (struct inv_icm426xx *s)

  Enable the 20bits-timestamp register access to read in a reliable way the strobed timestamp.
- int inv_icm426xx_disable_timestamp_to_register (struct inv_icm426xx *s)

  Disable the 20bits-timestamp register access.
- int inv_icm426xx_get_current_timestamp (struct inv_icm426xx *s, uint32_t *icm_time)

Get the timestamp value of icm426xx from register.

- int inv_icm426xx_enable_clkin_rtc (struct inv_icm426xx *s, uint8_t enable)

  Enable or disable CLKIN/RTC capability.
- int inv_icm426xx_get_clkin_rtc_status (struct inv_icm426xx *s)

  Get CLKIN/RTC feature status.
- int inv_icm426xx_enable_high_resolution_fifo (struct inv_icm426xx *s)

  Enable 20 bits raw acc and raw gyr data in fifo.
- int inv_icm426xx_disable_high_resolution_fifo (struct inv_icm426xx *s)

  Disable 20 bits raw acc and raw gyr data in fifo.
- int inv_icm426xx_configure_fifo (struct inv_icm426xx *s, INV_ICM426XX_FIFO_CONFIG_t fifo_config)

  Configure Fifo to select the way data are gathered.
- int inv_icm426xx_configure_fifo_wm (struct inv_icm426xx *s, uint16_t wm)

  Configure Fifo watermark (also referred to as fifo threshold).
- uint32_t inv_icm426xx_get_fifo_timestamp_resolution_us_q24 (struct inv_icm426xx *s)

  Get FIFO timestamp resolution.
- uint32_t inv_icm426xx_get_reg_timestamp_resolution_us_q24 (struct inv_icm426xx *s)

  Get register timestamp resolution.
- const char * inv_icm426xx_get_version (void)

  Return driver version x.y.z-suffix as a char array.

5.1.1 Detailed Description

High-level API to drive the device.

5.1.2 Macro Definition Documentation

5.1.2.1 ACCEL_CONFIG0_FS_SEL_MAX

```
#define ACCEL_CONFIG0_FS_SEL_MAX ICM426XX_ACCEL_CONFIG0_FS_SEL_16g
```

Max FSR values for accel and gyro Dependant of chip.

5.1.2.2 ACCEL_OFFUSER_MAX_MG

```
#define ACCEL_OFFUSER_MAX_MG 1000
```

5.1.2.3 GYRO_CONFIG0_FS_SEL_MAX

```
#define GYRO_CONFIG0_FS_SEL_MAX ICM426XX_GYRO_CONFIG0_FS_SEL_2000dps
```

5.1.2.4 GYRO_OFFUSER_MAX_DPS

```
#define GYRO_OFFUSER_MAX_DPS 64
```

5.1.2.5 ICM426XX_ACC_STARTUP_TIME_US

```
#define ICM426XX_ACC_STARTUP_TIME_US 20000U
```

Icm426xx Accelerometer start-up time before having correct data.

5.1.2.6 ICM426XX_DEFAULT_WOM_THS_MG

```
#define ICM426XX_DEFAULT_WOM_THS_MG 52 >> 2 /* = 52mg/4 */
```

Default value for the WOM threshold Resolution of the threshold is ∼= 4mg.

5.1.2.7 ICM426XX_FIFO_MIRRORING_SIZE

```
#define ICM426XX_FIFO_MIRRORING_SIZE 16 * 129
```

Icm426xx maximum buffer size mirrored from FIFO at polling time.

Warning

fifo_idx type variable must be large enough to parse the FIFO_MIRRORING_SIZE

5.1.2.8 ICM426XX_GYR_STARTUP_TIME_US

```
#define ICM426XX_GYR_STARTUP_TIME_US 60000U
```

Icm426xx Gyroscope start-up time before having correct data.

5.1.2.9 ICM_PART_DEFAULT_OIS_MODE

```
#define ICM_PART_DEFAULT_OIS_MODE ICM426XX_SENSOR_CONFIG2_OIS_MODE_8KHZ
```

5.1.2.10 INV_ICM426XX_LIGHTWEIGHT_DRIVER

```
#define INV_ICM426XX_LIGHTWEIGHT_DRIVER 0
```

Lighten driver logic by stripping out procedures on transitions.

In the nominal case, ie. when sensors are enabled and their output has settled, ICM-426XX will not need the logic to handle each transition. They are part of each API function so this code will be linked in regardless. This might not be desirable for the most size-constrained platforms and it can be avoided by setting this define to 1.

5.1.2.11 PLL_SCALE_FACTOR_Q24

```
#define PLL_SCALE_FACTOR_Q24 (1UL << 24)
```

Scale factor and max ODR Dependant of chip.

5.1.2.12 RTC_SUPPORTED

```
#define RTC_SUPPORTED 0
```

RTC Support flag Define whether the RTC mode is supported Dependant of chip.

5.1.3 Enumeration Type Documentation

5.1.3.1 INV_ICM426XX_FIFO_CONFIG_t

```
enum INV_ICM426XX_FIFO_CONFIG_t
```

Configure Fifo usage.

Enumerator

INV_ICM426XX_FIFO_DISABLED	Fifo is disabled and data source is sensors registers.
INV_ICM426XX_FIFO_ENABLED	Fifo is used as data source.

5.1.3.2 inv_icm426xx_interrupt_value

```
enum inv_icm426xx_interrupt_value
```

Enumerator

INV_ICM426XX_DISABLE	
INV_ICM426XX_ENABLE	

5.1.3.3 inv_icm426xx_sensor

```
enum inv_icm426xx_sensor
```

Sensor identifier for UI control and OIS function.

Enumerator

INV_ICM426XX_SENSOR_ACCEL	Accelerometer (UI control path)
INV_ICM426XX_SENSOR_GYRO	Gyroscope (UI control path)
INV_ICM426XX_SENSOR_FSYNC_EVENT	Used by OIS and UI control layers.
INV_ICM426XX_SENSOR_OIS	Only used by OIS layer.
INV_ICM426XX_SENSOR_TEMPERATURE	Chip temperature, enabled by default. Will be reported only if Accel and/or Gyro are also enabled. The Temperature's ODR (Output Data Rate) will match the ODR of Accel or Gyro, or the fastest if both are enabled
INV_ICM426XX_SENSOR_TAP	Tap and Double tap.
INV_ICM426XX_SENSOR_DMP_PEDOMETER_↩ EVENT	Pedometer: step is detected.
INV_ICM426XX_SENSOR_DMP_PEDOMETER_↩ COUNT	Pedometer: step counter.
INV_ICM426XX_SENSOR_DMP_TILT	Tilt.
INV_ICM426XX_SENSOR_MAX	

5.1.4 Function Documentation

5.1.4.1 inv_icm426xx_configure_fifo()

```
int inv_icm426xx_configure_fifo (
            struct inv_icm426xx * s,
            INV_ICM426XX_FIFO_CONFIG_t fifo_config )
```

Configure Fifo to select the way data are gathered.

Parameters

in	*s*	Pointer to device.
in	*fifo_config*	Fifo configuration method: If enabled data are coming from fifo and interrupt is configured on Fifo Watermark. If disabled data are coming from sensor registers and interrupt is configured on Data ready.

Returns

0 on success, negative value on error.

5.1.4.2 inv_icm426xx_configure_fifo_wm()

```
int inv_icm426xx_configure_fifo_wm (
            struct inv_icm426xx * s,
            uint16_t wm )
```

Configure Fifo watermark (also referred to as fifo threshold).

Parameters

in	*s*	Pointer to device.
in	*wm*	Watermark value.

Returns

0 on success, negative value on error.

5.1.4.3 inv_icm426xx_configure_timestamp_resolution()

```
int inv_icm426xx_configure_timestamp_resolution (
            struct inv_icm426xx * s,
            ICM426XX_TMST_CONFIG_RESOL_t resol )
```

Configure timestamp resolution from FIFO.

Parameters

in	*s*	Pointer to device.
in	*resol*	The expected resolution of the timestamp. See enum ICM426XX_TMST_CONFIG_RESOL_t.

Returns

0 on success, negative value on error.

Warning

The resolution will have no effect if RTC is enabled

5.1.4.4 inv_icm426xx_convert_odr_bitfield_to_us()

```
uint32_t inv_icm426xx_convert_odr_bitfield_to_us (
            uint32_t odr_bitfield )
```

Converts ICM426XX_ACCEL_CONFIG0_ODR_t or ICM426XX_GYRO_CONFIG0_ODR_t enums to period expressed in us.

Parameters

in	*odr_bitfield*	An ICM426XX_ACCEL_CONFIG0_ODR_t or ICM426XX_GYRO_CONFIG0_ODR_t enum

Returns

The corresponding period expressed in us

5.1.4.5 inv_icm426xx_device_reset()

```
int inv_icm426xx_device_reset (
            struct inv_icm426xx * s )
```

Perform a soft reset of the device.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

5.1.4.6 inv_icm426xx_disable_accel()

```
int inv_icm426xx_disable_accel (
            struct inv_icm426xx * s )
```

Disable accel.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

5.1.4.7 inv_icm426xx_disable_fsync()

```
int inv_icm426xx_disable_fsync (
            struct inv_icm426xx * s )
```

Disable fsync tagging functionality.

- disables fsync
- disables timestamp to registers. Once fysnc is disabled timestamp is pushed to fifo instead of fsync counter. So in order to decrease power consumption, timestamp is no more available in registers.
- disables fsync related interrupt

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

5.1.4.8 inv_icm426xx_disable_gyro()

```
int inv_icm426xx_disable_gyro (
            struct inv_icm426xx * s )
```

Disable gyro.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

5.1.4.9 inv_icm426xx_disable_high_resolution_fifo()

```
int inv_icm426xx_disable_high_resolution_fifo (
            struct inv_icm426xx * s )
```

Disable 20 bits raw acc and raw gyr data in fifo.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

5.1.4.10 inv_icm426xx_disable_timestamp_to_register()

```
int inv_icm426xx_disable_timestamp_to_register (
            struct inv_icm426xx * s )
```

Disable the 20bits-timestamp register access.

Register read always return 0's.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

5.1.4.11 inv_icm426xx_enable_accel_low_noise_mode()

```
int inv_icm426xx_enable_accel_low_noise_mode (
            struct inv_icm426xx * s )
```

Enable accel in low noise mode.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

5.1.4.12 inv_icm426xx_enable_accel_low_power_mode()

```
int inv_icm426xx_enable_accel_low_power_mode (
            struct inv_icm426xx * s )
```

Enable accel in low power mode.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

5.1.4.13 inv_icm426xx_enable_clkin_rtc()

```
int inv_icm426xx_enable_clkin_rtc (
            struct inv_icm426xx * s,
            uint8_t enable )
```

Enable or disable CLKIN/RTC capability.

Parameters

in	*s*	Pointer to device.
in	*enable*	1 if external 32kHz is provided to ICM, 0 otherwise

Returns

0 on success, negative value on error.

Warning

In case CLKIN is disabled, it is recommended to call `inv_icm426xx_configure_timestamp_resolution` just afterwards so that timestamp resolution is in line with system request.

5.1.4.14 inv_icm426xx_enable_fsync()

```
int inv_icm426xx_enable_fsync (
            struct inv_icm426xx * s )
```

Enable fsync tagging functionality.

- enables fsync
- enables timestamp to registers. Once fysnc is enabled fsync counter is pushed to fifo instead of timestamp. So timestamp is made available in registers. Note that this increase power consumption.
- enables fsync related interrupt

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

5.1.4.15 inv_icm426xx_enable_gyro_low_noise_mode()

```
int inv_icm426xx_enable_gyro_low_noise_mode (
            struct inv_icm426xx * s )
```

Enable gyro in low noise mode.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

5.1.4.16 inv_icm426xx_enable_high_resolution_fifo()

```
int inv_icm426xx_enable_high_resolution_fifo (
            struct inv_icm426xx * s )
```

Enable 20 bits raw acc and raw gyr data in fifo.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

5.1.4.17 inv_icm426xx_enable_timestamp_to_register()

```
int inv_icm426xx_enable_timestamp_to_register (
            struct inv_icm426xx * s )
```

Enable the 20bits-timestamp register access to read in a reliable way the strobed timestamp.

To do that, the fine clock is forced enabled at some power cost.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

5.1.4.18 inv_icm426xx_force_clock_source()

```
int inv_icm426xx_force_clock_source (
            struct inv_icm426xx * s,
            ICM426XX_INTF_CONFIG1_ACCEL_LP_CLK_t clk_src )
```

Configure Accel clock source.

Parameters

in	*s*	Pointer to device.
in	*clk_src*	new clock source to use

Returns

0 on success, negative value on error

Note

Transitions when enabling/disabling sensors are already handled by the driver. This function forces a specific clock source.

5.1.4.19 inv_icm426xx_get_accel_fsr()

```
int inv_icm426xx_get_accel_fsr (
            struct inv_icm426xx * s,
            ICM426XX_ACCEL_CONFIG0_FS_SEL_t * accel_fsr_g )
```

Access accel full scale range.

Parameters

in	*s*	Pointer to device.
out	*accel_fsr_g*	Current full scale range.

Returns

0 on success, negative value on error.

5.1.4.20 inv_icm426xx_get_clkin_rtc_status()

```
int inv_icm426xx_get_clkin_rtc_status (
            struct inv_icm426xx * s )
```

Get CLKIN/RTC feature status.

Parameters

in	*s*	Pointer to device.

Returns

0 if CLKIN is disabled, 1 if enabled.

Warning

In case CLKIN is disabled, it is recommended to call `inv_icm426xx_configure_timestamp_resolution` just afterwards so that timestamp resolution is in line with system request.

5.1.4.21 inv_icm426xx_get_config_ibi()

```
int inv_icm426xx_get_config_ibi (
            struct inv_icm426xx * s,
            inv_icm426xx_interrupt_parameter_t * interrupt_to_configure )
```

Retrieve interrupts configuration.

Parameters

in	*s*	Pointer to device.
in	*interrupt_to_configure*	Structure with the corresponding state to manage IBI interruptions.

Returns

0 on success, negative value on error.

5.1.4.22 inv_icm426xx_get_config_int1()

```
int inv_icm426xx_get_config_int1 (
            struct inv_icm426xx * s,
            inv_icm426xx_interrupt_parameter_t * interrupt_to_configure )
```

Retrieve interrupts configuration.

Parameters

in	*s*	Pointer to device.
in	*interrupt_to_configure*	Structure with the corresponding state to manage INT1.

Returns

0 on success, negative value on error.

5.1.4.23 inv_icm426xx_get_config_int2()

```
int inv_icm426xx_get_config_int2 (
            struct inv_icm426xx * s,
            inv_icm426xx_interrupt_parameter_t * interrupt_to_configure )
```

Retrieve interrupts configuration.

Parameters

in	*s*	Pointer to device.
in	*interrupt_to_configure*	Structure with the corresponding state to manage INT2.

Returns

0 on success, negative value on error.

5.1.4.24 inv_icm426xx_get_current_timestamp()

```
int inv_icm426xx_get_current_timestamp (
            struct inv_icm426xx * s,
            uint32_t * icm_time )
```

Get the timestamp value of icm426xx from register.

Parameters

in	*s*	Pointer to device.
in	*icm_time*	Timestamp read from register.

Returns

0 on success, negative value on error.

Warning

Timestamp register must be enabled before calling this API (see `inv_icm426xx_enable_↩ timestamp_to_register` function)

5.1.4.25 inv_icm426xx_get_data_from_fifo()

```
int inv_icm426xx_get_data_from_fifo (
            struct inv_icm426xx * s )
```

Read all available packets from the FIFO.

For each packet function builds a sensor event containing packet data and validity information. Then calls `sensor_event_cb` function for each packet.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

5.1.4.26 inv_icm426xx_get_data_from_registers()

```
int inv_icm426xx_get_data_from_registers (
            struct inv_icm426xx * s )
```

Read all registers containing data (temperature, accelerometer and gyroscope).

Then calls `sensor_event_cb` function for each packet.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

5.1.4.27 inv_icm426xx_get_fifo_timestamp_resolution_us_q24()

```
uint32_t inv_icm426xx_get_fifo_timestamp_resolution_us_q24 (
            struct inv_icm426xx * s )
```

Get FIFO timestamp resolution.

Parameters

in	*s*	Pointer to device.

Returns

The timestamp resolution in us as a q24 or 0 in case of error.

5.1.4.28 inv_icm426xx_get_gyro_fsr()

```
int inv_icm426xx_get_gyro_fsr (
            struct inv_icm426xx * s,
            ICM426XX_GYRO_CONFIG0_FS_SEL_t * gyro_fsr_dps )
```

Access gyro full scale range.

Parameters

in	*s*	Pointer to device.
out	*gyro_fsr_dps*	Current full scale range.

Returns

0 on success, negative value on error.

5.1.4.29 inv_icm426xx_get_reg_timestamp_resolution_us_q24()

```
uint32_t inv_icm426xx_get_reg_timestamp_resolution_us_q24 (
            struct inv_icm426xx * s )
```

Get register timestamp resolution.

Parameters

in	*s*	Pointer to device.

Returns

The timestamp resolution in us as a q24 or 0 in case of error.

5.1.4.30 inv_icm426xx_get_version()

```
const char* inv_icm426xx_get_version (
            void  )
```

Return driver version x.y.z-suffix as a char array.

Returns

Driver version a char array "x.y.z-suffix".

5.1.4.31 inv_icm426xx_get_who_am_i()

```
int inv_icm426xx_get_who_am_i (
            struct inv_icm426xx * s,
            uint8_t * who_am_i )
```

return WHOAMI value

Parameters

in	*s*	Pointer to device.
out	*who_am_i*	WHOAMI for device

Returns

0 on success, negative value on error

5.1.4.32 inv_icm426xx_init()

```
int inv_icm426xx_init (
            struct inv_icm426xx * s,
            struct inv_icm426xx_serif * serif,
            void(*)(inv_icm426xx_sensor_event_t *event) sensor_event_cb )
```

Initializes device.

Parameters

in	*s*	Pointer to device.
in	*serif*	Pointer on serial interface structure to be used to access icm426xx.
in	*sensor_event_cb*	Callback executed when reading data from FIFO or registers. Can be NULL if `inv_icm426xx_get_data_from_fifo` and `inv_icm426xx_get_data_from_registers` are not used by the application.

Returns

0 on success, negative value on error.

5.1.4.33 inv_icm426xx_reset_fifo()

```
int inv_icm426xx_reset_fifo (
            struct inv_icm426xx * s )
```

reset ICM426XX fifo

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

5.1.4.34 inv_icm426xx_set_accel_frequency()

```
int inv_icm426xx_set_accel_frequency (
            struct inv_icm426xx * s,
            const ICM426XX_ACCEL_CONFIG0_ODR_t frequency )
```

Configure accel Output Data Rate.

Parameters

in	*s*	Pointer to device.
in	*frequency*	The requested frequency.

Returns

0 on success, negative value on error.

5.1.4.35 inv_icm426xx_set_accel_fsr()

```
int inv_icm426xx_set_accel_fsr (
            struct inv_icm426xx * s,
            ICM426XX_ACCEL_CONFIG0_FS_SEL_t accel_fsr_g )
```

Set accel full scale range.

Parameters

in	*s*	Pointer to device.
in	*accel_fsr_g*	Requested full scale range.

Returns

0 on success, negative value on error.

5.1.4.36 inv_icm426xx_set_accel_ln_bw()

```
int inv_icm426xx_set_accel_ln_bw (
            struct inv_icm426xx * s,
            ICM426XX_GYRO_ACCEL_CONFIG0_ACCEL_FILT_BW_t acc_bw )
```

Set accel Low-Noise bandwidth value.

Parameters

in	*s*	Pointer to device.
in	*acc_bw*	Requested averaging value

Returns

0 on success, negative value on error.

5.1.4.37 inv_icm426xx_set_accel_lp_avg()

```
int inv_icm426xx_set_accel_lp_avg (
            struct inv_icm426xx * s,
            ICM426XX_GYRO_ACCEL_CONFIG0_ACCEL_FILT_AVG_t acc_avg )
```

Set accel Low-Power averaging value.

Parameters

in	*s*	Pointer to device.
in	*acc_avg*	Requested averaging value

Returns

0 on success, negative value on error.

5.1.4.38 inv_icm426xx_set_config_ibi()

```
int inv_icm426xx_set_config_ibi (
            struct inv_icm426xx * s,
            inv_icm426xx_interrupt_parameter_t * interrupt_to_configure )
```

Configure which interrupt source can trigger IBI interruptions.

Parameters

in	*s*	Pointer to device.
in	*interrupt_to_configure*	Structure with the corresponding state to manage IBI interruptions.

Returns

0 on success, negative value on error.

5.1.4.39 inv_icm426xx_set_config_int1()

```
int inv_icm426xx_set_config_int1 (
            struct inv_icm426xx * s,
            inv_icm426xx_interrupt_parameter_t * interrupt_to_configure )
```

Configure which interrupt source can trigger INT1.

Parameters

in	*s*	Pointer to device.
in	*interrupt_to_configure*	Structure with the corresponding state to manage INT1.

Returns

0 on success, negative value on error.

5.1.4.40 inv_icm426xx_set_config_int2()

```
int inv_icm426xx_set_config_int2 (
            struct inv_icm426xx * s,
            inv_icm426xx_interrupt_parameter_t * interrupt_to_configure )
```

Configure which interrupt source can trigger INT2.

Parameters

in	*s*	Pointer to device.
in	*interrupt_to_configure*	Structure with the corresponding state to INT2.

Returns

0 on success, negative value on error.

5.1.4.41 inv_icm426xx_set_gyro_frequency()

```
int inv_icm426xx_set_gyro_frequency (
            struct inv_icm426xx * s,
            const ICM426XX_GYRO_CONFIG0_ODR_t frequency )
```

Configure gyro Output Data Rate.

Parameters

in	*s*	Pointer to device.
in	*frequency*	The requested frequency.

Returns

0 on success, negative value on error.

5.1.4.42 inv_icm426xx_set_gyro_fsr()

```
int inv_icm426xx_set_gyro_fsr (
            struct inv_icm426xx * s,
            ICM426XX_GYRO_CONFIG0_FS_SEL_t gyro_fsr_dps )
```

Set gyro full scale range.

Parameters

in	*s*	Pointer to device.
in	*gyro_fsr_dps*	Requested full scale range.

Returns

0 on success, negative value on error.

5.1.4.43 inv_icm426xx_set_gyro_ln_bw()

```
int inv_icm426xx_set_gyro_ln_bw (
            struct inv_icm426xx * s,
            ICM426XX_GYRO_ACCEL_CONFIG0_GYRO_FILT_BW_t gyr_bw )
```

Set gyro Low-Noise bandwidth value.

Parameters

in	*s*	Pointer to device.
in	*gyr_bw*	Requested averaging value

Returns

0 on success, negative value on error.

5.1.4.44 inv_icm426xx_set_reg_bank()

```
int inv_icm426xx_set_reg_bank (
            struct inv_icm426xx * s,
            uint8_t bank )
```

Set register bank index.

Parameters

in	*s*	Pointer to device.
in	*bank*	New bank to be set.

Returns

0 on success, negative value on error.

5.2 APEX driver

High-level API to drive APEX-related features.

Files

- file Icm426xxDriver_HL_apex.h

Classes

- struct inv_icm426xx_tap_parameters_t

  Icm426xx TAP inputs parameters definition.
- struct inv_icm426xx_apex_parameters

  Icm426xx APEX inputs parameters definition.
- struct inv_icm426xx_apex_step_activity

  APEX pedometer outputs.
- struct inv_icm426xx_tap_data

  TAP outputs.

Typedefs

- typedef struct inv_icm426xx_apex_parameters inv_icm426xx_apex_parameters_t

  Icm426xx APEX inputs parameters definition.
- typedef struct inv_icm426xx_apex_step_activity inv_icm426xx_apex_step_activity_t

  APEX pedometer outputs.
- typedef struct inv_icm426xx_tap_data inv_icm426xx_tap_data_t

  TAP outputs.

Functions

- int inv_icm426xx_configure_smd_wom (struct inv_icm426xx ∗s, const uint8_t x_th, const uint8_t y_th, const uint8_t z_th, ICM426XX_SMD_CONFIG_WOM_INT_MODE_t wom_int, ICM426XX_SMD_CONFIG_WOM_MODE_t wom_mode)

  Configure Wake On Motion and SMD thresholds.
- int inv_icm426xx_enable_wom (struct inv_icm426xx ∗s)

  Enable Wake On Motion.
- int inv_icm426xx_disable_wom (struct inv_icm426xx ∗s)

  Disable Wake On Motion.
- int inv_icm426xx_enable_smd (struct inv_icm426xx ∗s)

  Enable Significant Motion Detection.
- int inv_icm426xx_disable_smd (struct inv_icm426xx ∗s)

  Disable Significant Motion Detection.
- int inv_icm426xx_init_tap_parameters_struct (struct inv_icm426xx ∗s, inv_icm426xx_tap_parameters_t ∗tap_inputs)

  Fill the TAP parameters structure with all the default parameters for TAP algorithm.
- int inv_icm426xx_configure_tap_parameters (struct inv_icm426xx ∗s, const inv_icm426xx_tap_parameters_t ∗tap_inputs)

  Configure TAP.
- int inv_icm426xx_get_tap_parameters (struct inv_icm426xx ∗s, inv_icm426xx_tap_parameters_t ∗tap_↩ params)

  Returns current TAP parameters.
- int inv_icm426xx_enable_tap (struct inv_icm426xx ∗s)

  Enable TAP.
- int inv_icm426xx_disable_tap (struct inv_icm426xx ∗s)

  Disable TAP.
- int inv_icm426xx_init_apex_parameters_struct (struct inv_icm426xx ∗s, inv_icm426xx_apex_parameters_t ∗apex_inputs)

  Fill the APEX parameters structure with all the default parameters for APEX algorithms (pedometer, tilt)

- int inv_icm426xx_configure_apex_parameters (struct inv_icm426xx *s, const inv_icm426xx_apex_parameters_t *apex_inputs)

  Configures DMP parameters for APEX algorithms (pedometer, tilt).
- int inv_icm426xx_get_apex_parameters (struct inv_icm426xx *s, inv_icm426xx_apex_parameters_t *apex_params)

  Returns current DMP parameters for APEX algorithms (pedometer, tilt).
- int inv_icm426xx_set_apex_frequency (struct inv_icm426xx *s, const ICM426XX_APEX_CONFIG0_DMP_ODR_t frequency)

  Configure DMP Output Data Rate for APEX algorithms (pedometer, tilt)
- int inv_icm426xx_start_dmp (struct inv_icm426xx *s)

  Start DMP for APEX algorithms.
- int inv_icm426xx_reset_dmp (struct inv_icm426xx *s)

  Reset DMP memory.
- int inv_icm426xx_enable_apex_pedometer (struct inv_icm426xx *s)

  Enable APEX algorithm Pedometer.
- int inv_icm426xx_disable_apex_pedometer (struct inv_icm426xx *s)

  Disable APEX algorithm Pedometer.
- int inv_icm426xx_enable_apex_tilt (struct inv_icm426xx *s)

  Enable APEX algorithm Tilt.
- int inv_icm426xx_disable_apex_tilt (struct inv_icm426xx *s)

  Disable APEX algorithm Tilt.
- int inv_icm426xx_get_apex_data_activity (struct inv_icm426xx *s, inv_icm426xx_apex_step_activity_t *apex_activity)

  Retrieve APEX pedometer outputs and format them.
- int inv_icm426xx_get_tap_data (struct inv_icm426xx *s, inv_icm426xx_tap_data_t *tap_data)

  Retrieve tap outputs.
- int inv_icm426xx_load_dmp_sram_code (struct inv_icm426xx *s, const uint8_t *dmp_prog, const uint32_t start_offset, const uint32_t size)

  Load custom DMP image into SRAM.

5.2.1 Detailed Description

High-level API to drive APEX-related features.

5.2.2 Typedef Documentation

5.2.2.1 inv_icm426xx_apex_parameters_t

```
typedef struct inv_icm426xx_apex_parameters inv_icm426xx_apex_parameters_t
```

Icm426xx APEX inputs parameters definition.

5.2.2.2 inv_icm426xx_apex_step_activity_t

```
typedef struct inv_icm426xx_apex_step_activity inv_icm426xx_apex_step_activity_t
```

APEX pedometer outputs.

5.2.2.3 inv_icm426xx_tap_data_t

```
typedef struct inv_icm426xx_tap_data inv_icm426xx_tap_data_t
```

TAP outputs.

5.2.3 Function Documentation

5.2.3.1 inv_icm426xx_configure_apex_parameters()

```
int inv_icm426xx_configure_apex_parameters (
            struct inv_icm426xx * s,
            const inv_icm426xx_apex_parameters_t * apex_inputs )
```

Configures DMP parameters for APEX algorithms (pedometer, tilt).

This programmable parameters will be decoded and propagate to the SRAM to be executed at DMP start.

Parameters

in	*s*	Pointer to device.
in	*apex_inputs*	The requested input parameters. See

See also

inv_icm426xx_apex_parameters_t

Warning

APEX inputs can't change on the fly, this API should be called before enabling any APEX features.

APEX configuration can't be done too frequently, but only once every 10ms. Otherwise it can create unknown behavior.

Returns

0 on success, negative value on error.

5.2.3.2 inv_icm426xx_configure_smd_wom()

```
int inv_icm426xx_configure_smd_wom (
            struct inv_icm426xx * s,
            const uint8_t x_th,
            const uint8_t y_th,
            const uint8_t z_th,
            ICM426XX_SMD_CONFIG_WOM_INT_MODE_t wom_int,
            ICM426XX_SMD_CONFIG_WOM_MODE_t wom_mode )
```

Configure Wake On Motion and SMD thresholds.

Parameters

in	*s*	Pointer to device.
in	*x_th*	Threshold value for the Wake on Motion Interrupt for X-axis accel.
in	*y_th*	Threshold value for the Wake on Motion Interrupt for Y-axis accel.
in	*z_th*	Threshold value for the Wake on Motion Interrupt for Z-axis accel.
in	*wom_int*	Select which mode between AND/OR is used to generate interrupt.
in	*wom_mode*	Select which comparison mode is used for WoM detection.

Returns

0 on success, negative value on error.

5.2.3.3 inv_icm426xx_configure_tap_parameters()

```
int inv_icm426xx_configure_tap_parameters (
            struct inv_icm426xx * s,
            const inv_icm426xx_tap_parameters_t * tap_inputs )
```

Configure TAP.

Parameters

in	*s*	Pointer to device.
in	*tap_inputs*	The requested input parameters.

Returns

0 on success, negative value on error.

5.2.3.4 inv_icm426xx_disable_apex_pedometer()

```
int inv_icm426xx_disable_apex_pedometer (
            struct inv_icm426xx * s )
```

Disable APEX algorithm Pedometer.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

5.2.3.5 inv_icm426xx_disable_apex_tilt()

```
int inv_icm426xx_disable_apex_tilt (
            struct inv_icm426xx * s )
```

Disable APEX algorithm Tilt.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

5.2.3.6 inv_icm426xx_disable_smd()

```
int inv_icm426xx_disable_smd (
            struct inv_icm426xx * s )
```

Disable Significant Motion Detection.

Disables SMD event generation and disables SMD interrupt.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

5.2.3.7 inv_icm426xx_disable_tap()

```
int inv_icm426xx_disable_tap (
            struct inv_icm426xx * s )
```

Disable TAP.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

5.2.3.8 inv_icm426xx_disable_wom()

```
int inv_icm426xx_disable_wom (
            struct inv_icm426xx * s )
```

Disable Wake On Motion.

Disables WoM event generation and reconfigures interrupt to fire on Fifo water-mark.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

5.2.3.9 inv_icm426xx_enable_apex_pedometer()

```
int inv_icm426xx_enable_apex_pedometer (
            struct inv_icm426xx * s )
```

Enable APEX algorithm Pedometer.

note : Pedometer request to have the accelerometer enabled to works with accelerometer frequency less than dmp frequency.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

Warning

Pedometer must be turned OFF to reconfigure it

5.2.3.10 inv_icm426xx_enable_apex_tilt()

```
int inv_icm426xx_enable_apex_tilt (
            struct inv_icm426xx * s )
```

Enable APEX algorithm Tilt.

note : Tilt request to have the accelerometer enabled to works with accelerometer frequency less than dmp frequency.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

5.2.3.11 inv_icm426xx_enable_smd()

```
int inv_icm426xx_enable_smd (
            struct inv_icm426xx * s )
```

Enable Significant Motion Detection.

note : SMD requests to have the accelerometer enabled to work. Enables SMD event generation and configures interrupt to fire on SMD event. WoM event will also be generated. To have good performance, it's recommended to set accelerometer ODR (Output Data Rate) to 20ms and the accelerometer in Low Power Mode.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

5.2.3.12 inv_icm426xx_enable_tap()

```
int inv_icm426xx_enable_tap (
            struct inv_icm426xx * s )
```

Enable TAP.

note : TAP requests to have the accelerometer enabled to work. To have good performance, it's recommended to set accelerometer ODR (Output Data Rate) to 1ms and the accelerometer in Low Noise Mode.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

5.2.3.13 inv_icm426xx_enable_wom()

```
int inv_icm426xx_enable_wom (
            struct inv_icm426xx * s )
```

Enable Wake On Motion.

note : WoM requests to have the accelerometer enabled to work. Enables WoM event generation and configures interrupt to fire on WoM event. As a consequence Fifo water-mark interrupt is disabled. To have good performance, it's recommended to set accelerometer ODR (Output Data Rate) to 20ms and the accelerometer in Low Power Mode.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

5.2.3.14 inv_icm426xx_get_apex_data_activity()

```
int inv_icm426xx_get_apex_data_activity (
            struct inv_icm426xx * s,
            inv_icm426xx_apex_step_activity_t * apex_activity )
```

Retrieve APEX pedometer outputs and format them.

Parameters

in	*s*	Pointer to device.
out	*apex_activity*	Apex step and activity data value.

Returns

0 on success, negative value on error.

5.2.3.15 inv_icm426xx_get_apex_parameters()

```
int inv_icm426xx_get_apex_parameters (
            struct inv_icm426xx * s,
            inv_icm426xx_apex_parameters_t * apex_params )
```

Returns current DMP parameters for APEX algorithms (pedometer, tilt).

Parameters

in	*s*	Pointer to device.
out	*apex_params*	The current parameter, fetched from registers. See

See also

inv_icm426xx_apex_parameters_t

Returns

0 on success, negative value on error.

5.2.3.16 inv_icm426xx_get_tap_data()

```
int inv_icm426xx_get_tap_data (
            struct inv_icm426xx * s,
            inv_icm426xx_tap_data_t * tap_data )
```

Retrieve tap outputs.

Parameters

in	*s*	Pointer to device.
out	*tap_data*	Tap axis, direction and type

Returns

0 on success, negative value on error.

5.2.3.17 inv_icm426xx_get_tap_parameters()

```
int inv_icm426xx_get_tap_parameters (
            struct inv_icm426xx * s,
            inv_icm426xx_tap_parameters_t * tap_params )
```

Returns current TAP parameters.

Parameters

in	*s*	Pointer to device.
out	*tap_params*	The current parameter, fetched from registers. See

See also

inv_icm426xx_tap_parameters_t

Returns

0 on success, negative value on error.

5.2.3.18 inv_icm426xx_init_apex_parameters_struct()

```
int inv_icm426xx_init_apex_parameters_struct (
            struct inv_icm426xx * s,
            inv_icm426xx_apex_parameters_t * apex_inputs )
```

Fill the APEX parameters structure with all the default parameters for APEX algorithms (pedometer, tilt)

Parameters

in	*s*	Pointer to device.
out	*apex_inputs*	Default input parameters. See

See also

inv_icm426xx_apex_parameters_t

Returns

0 on success, negative value on error.

5.2.3.19 inv_icm426xx_init_tap_parameters_struct()

```
int inv_icm426xx_init_tap_parameters_struct (
            struct inv_icm426xx * s,
            inv_icm426xx_tap_parameters_t * tap_inputs )
```

Fill the TAP parameters structure with all the default parameters for TAP algorithm.

Parameters

in	*s*	Pointer to device.
out	*tap_inputs*	Default input parameters.

Returns

0 on success, negative value on error.

5.2.3.20 inv_icm426xx_load_dmp_sram_code()

```
int inv_icm426xx_load_dmp_sram_code (
            struct inv_icm426xx * s,
            const uint8_t * dmp_prog,
            const uint32_t start_offset,
            const uint32_t size )
```

Load custom DMP image into SRAM.

Parameters

in	*s*	Pointer to device.
in	*dmp_prog*	DMP code to be loaded
in	*start_offset*	SRAM offset to which program shall be loaded (typically 16).
in	*size*	Total code size to be loaded into SRAM

Returns

0 on success, negative value on error.

Return values

INV_ERROR_SIZE	if image will not fit in 1024B SRAM
INV_ERROR	if ICM sensors are not OFF
INV_ERROR_MEM	if SRAM is not written correctly

5.2.3.21 inv_icm426xx_reset_dmp()

```
int inv_icm426xx_reset_dmp (
            struct inv_icm426xx * s )
```

Reset DMP memory.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

5.2.3.22 inv_icm426xx_set_apex_frequency()

```
int inv_icm426xx_set_apex_frequency (
            struct inv_icm426xx * s,
            const ICM426XX_APEX_CONFIG0_DMP_ODR_t frequency )
```

Configure DMP Output Data Rate for APEX algorithms (pedometer, tilt)

Parameters

in	*s*	Pointer to device.
in	*frequency*	The requested frequency.

Warning

DMP_ODR can change on the fly, and the DMP code will accommodate necessary modifications.

The user needs to take care to set Accel frequency >= DMP frequency. This is a hard constraint since HW will not handle incorrect setting.

Returns

0 on success, negative value on error.

5.2.3.23 inv_icm426xx_start_dmp()

```
int inv_icm426xx_start_dmp (
            struct inv_icm426xx * s )
```

Start DMP for APEX algorithms.

Parameters

in	*s*	Pointer to device.

Returns

0 on success, negative value on error.

5.3 External functions

External functions to be defined in application level.

Files

- file Icm426xxExtFunc.h

Functions

- void inv_icm426xx_sleep_us (uint32_t us)

  Hook for low-level high res system sleep() function to be implemented by upper layer ~100us resolution is sufficient.
- uint64_t inv_icm426xx_get_time_us (void)

  Hook for low-level high res system get_time() function to be implemented by upper layer Timer should be on 64bit with a 1 us resolution.

5.3.1 Detailed Description

External functions to be defined in application level.

5.3.2 Function Documentation

5.3.2.1 inv_icm426xx_get_time_us()

```
uint64_t inv_icm426xx_get_time_us (
            void  )
```

Hook for low-level high res system get_time() function to be implemented by upper layer Timer should be on 64bit with a 1 us resolution.

Returns

The current time in us

5.3.2.2 inv_icm426xx_sleep_us()

```
void inv_icm426xx_sleep_us (
            uint32_t us )
```

Hook for low-level high res system sleep() function to be implemented by upper layer ~100us resolution is sufficient.

Parameters

in	*us*	number of us the calling thread should sleep

5.4 Self-test

API to execute self-test procedures.

Files

- file Icm426xxSelfTest.h

Functions

- int inv_icm426xx_run_selftest (struct inv_icm426xx *s, int *result)

  Perform hardware self-test for Accel and Gyro.
- int inv_icm426xx_get_st_bias (struct inv_icm426xx *s, int st_bias[6])

  Retrieve bias collected by self-test.
- int inv_icm426xx_set_st_bias (struct inv_icm426xx *s, const int st_bias[6])

  Apply bias.

5.4.1 Detailed Description

API to execute self-test procedures.

5.4.2 Function Documentation

5.4.2.1 inv_icm426xx_get_st_bias()

```
int inv_icm426xx_get_st_bias (
            struct inv_icm426xx * s,
            int st_bias[6] )
```

Retrieve bias collected by self-test.

Parameters

in	*s*	Pointer to device.
out	*st_bias*	Bias scaled by 2^16, accel is gee and gyro is dps. The buffer will be filled as below. Gyro LN mode X,Y,Z Accel LN mode X,Y,Z

Returns

0 on success, negative value on error.

5.4.2.2 inv_icm426xx_run_selftest()

```
int inv_icm426xx_run_selftest (
            struct inv_icm426xx * s,
            int * result )
```

Perform hardware self-test for Accel and Gyro.

Parameters

in	*s*	Pointer to device.
in	*result*	Containing ACCEL_SUCCESS<<1 | GYRO_SUCCESS so 3

Returns

0 on success, negative value on error.

5.4.2.3 inv_icm426xx_set_st_bias()

```
int inv_icm426xx_set_st_bias (
            struct inv_icm426xx * s,
            const int st_bias[6] )
```

Apply bias.

Parameters

in	*s*	Pointer to device.
in	*st_bias*	Bias scaled by 2^16, accel is gee and gyro is dps. The buffer must be filled as below. Gyro LN mode X,Y,Z Accel LN mode X,Y,Z

Returns

0 on success, negative value on error.

5.5 Transport

Abstraction layer to communicate with device.

Files

- file Icm426xxTransport.h

Classes

- struct inv_icm426xx_serif
  base sensor serial interface
- struct inv_icm426xx_transport
  transport interface

Macros

- #define ICM426XX_UI_I2C 0
  identifies I2C interface.
- #define ICM426XX_UI_SPI4 1
  identifies 4-wire SPI interface.
- #define ICM426XX_UI_I3C 2
  identifies I3C interface.
- #define ICM426XX_AUX1_SPI3 3
  identifies 3-wire SPI interface for AUX1.
- #define ICM426XX_AUX2_SPI3 4
  identifies 3-wire SPI interface for AUX2.
- #define ICM426XX_AUX1_SPI4 5
  identifies 4-wire SPI interface for AUX1.

Typedefs

- typedef uint32_t ICM426XX_SERIAL_IF_TYPE_t
  Serif type definition.

Functions

- int inv_icm426xx_init_transport (struct inv_icm426xx ∗s)
  Init cache variable.
- int inv_icm426xx_read_reg (struct inv_icm426xx ∗s, uint8_t reg, uint32_t len, uint8_t ∗buf)
  Reads data from a register on Icm426xx.
- int inv_icm426xx_write_reg (struct inv_icm426xx ∗s, uint8_t reg, uint32_t len, const uint8_t ∗buf)
  Writes data to a register on Icm426xx.

5.5.1 Detailed Description

Abstraction layer to communicate with device.

5.5.2 Macro Definition Documentation

5.5.2.1 ICM426XX_AUX1_SPI3

```
#define ICM426XX_AUX1_SPI3 3
```

identifies 3-wire SPI interface for AUX1.

5.5.2.2 ICM426XX_AUX1_SPI4

```
#define ICM426XX_AUX1_SPI4 5
```

identifies 4-wire SPI interface for AUX1.

5.5.2.3 ICM426XX_AUX2_SPI3

```
#define ICM426XX_AUX2_SPI3 4
```

identifies 3-wire SPI interface for AUX2.

5.5.2.4 ICM426XX_UI_I2C

```
#define ICM426XX_UI_I2C 0
```

identifies I2C interface.

5.5.2.5 ICM426XX_UI_I3C

```
#define ICM426XX_UI_I3C 2
```

identifies I3C interface.

5.5.2.6 ICM426XX_UI_SPI4

```
#define ICM426XX_UI_SPI4 1
```

identifies 4-wire SPI interface.

5.5.3 Typedef Documentation

5.5.3.1 ICM426XX_SERIAL_IF_TYPE_t

```
typedef uint32_t ICM426XX_SERIAL_IF_TYPE_t
```

Serif type definition.

Deprecated Kept for retrocompatibility. Replaced with `uint32_t` type in `struct inv_icm426xx_serif` struct.

5.5.4 Function Documentation

5.5.4.1 inv_icm426xx_init_transport()

```
int inv_icm426xx_init_transport (
            struct inv_icm426xx * s )
```

Init cache variable.

Returns

0 in case of success, -1 for any error

5.5.4.2 inv_icm426xx_read_reg()

```
int inv_icm426xx_read_reg (
            struct inv_icm426xx * s,
            uint8_t reg,
            uint32_t len,
            uint8_t * buf )
```

Reads data from a register on Icm426xx.

Parameters

in	*s*	Pointer to device.
in	*reg*	register address to be read
in	*len*	number of byte to be read
out	*buf*	output data from the register

Returns

0 in case of success, -1 for any error

5.5.4.3 inv_icm426xx_write_reg()

```
int inv_icm426xx_write_reg (
            struct inv_icm426xx * s,
            uint8_t reg,
            uint32_t len,
            const uint8_t * buf )
```

Writes data to a register on Icm426xx.

Parameters

in	*s*	Pointer to device.
in	*reg*	register address to be written
in	*len*	number of byte to be written
in	*buf*	input data to write

Returns

0 in case of success, -1 for any error

Chapter 6

Class Documentation

6.1 fifo_header_t Union Reference

Describe the content of the FIFO header.

`#include <Icm426xxDefs.h>`

Public Attributes

- unsigned char Byte
- struct {
  unsigned char gyro_odr_different: 1
  unsigned char accel_odr_different: 1
  unsigned char fsync_bit: 1
  unsigned char timestamp_bit: 1
  unsigned char twentybits_bit: 1
  unsigned char gyro_bit: 1
  unsigned char accel_bit: 1
  unsigned char msg_bit: 1
  } bits

6.1.1 Detailed Description

Describe the content of the FIFO header.

6.1.2 Member Data Documentation

6.1.2.1 accel_bit

`unsigned char fifo_header_t::accel_bit`

6.1.2.2 accel_odr_different

```
unsigned char fifo_header_t::accel_odr_different
```

6.1.2.3

```
struct { ... } fifo_header_t::bits
```

6.1.2.4 Byte

```
unsigned char fifo_header_t::Byte
```

6.1.2.5 fsync_bit

```
unsigned char fifo_header_t::fsync_bit
```

6.1.2.6 gyro_bit

```
unsigned char fifo_header_t::gyro_bit
```

6.1.2.7 gyro_odr_different

```
unsigned char fifo_header_t::gyro_odr_different
```

6.1.2.8 msg_bit

```
unsigned char fifo_header_t::msg_bit
```

6.1.2.9 timestamp_bit

```
unsigned char fifo_header_t::timestamp_bit
```

6.1.2.10 twentybits_bit

```
unsigned char fifo_header_t::twentybits_bit
```

The documentation for this union was generated from the following file:

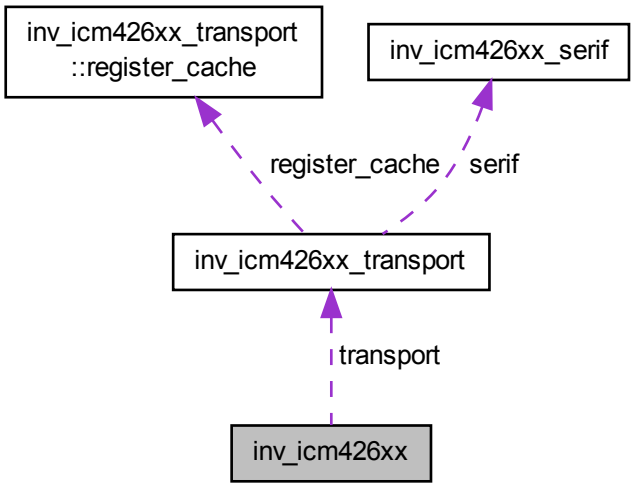
- Icm426xxDefs.h

6.2 inv_icm426xx Struct Reference

Icm426xx driver states definition.

```
#include <Icm426xxDriver_HL.h>
```

Collaboration diagram for inv_icm426xx:



Public Attributes

- struct inv_icm426xx_transport transport

  Transport structure.
- void(∗ sensor_event_cb)(inv_icm426xx_sensor_event_t ∗event)

  Callback executed when retrieving data from FIFO or registers.
- int gyro_st_bias [3]

  Gyro bias values (lsb) collected during self test.
- int accel_st_bias [3]

  Accel bias values (lsb) collected during self test.
- int st_result

  Flag to keep track if self-test has already been executed.

- uint8_t fifo_data [ICM426XX_FIFO_MIRRORING_SIZE]

  FIFO mirroring memory area.
- uint8_t tmst_to_reg_en_cnt

  Internal counter to keep track of the timestamp to register access availability.
- uint8_t dmp_is_on

  DMP started status.
- uint8_t dmp_from_sram

  DMP executes from SRAM.
- uint64_t gyro_start_time_us

  Internal state needed to discard first gyro samples.
- uint64_t accel_start_time_us

  Internal state needed to discard first accel samples.
- uint8_t endianess_data

  Internal status of data endianness mode to report correctly data.
- uint8_t fifo_highres_enabled

  Indicates if highres mode is used for FIFO.
- INV_ICM426XX_FIFO_CONFIG_t fifo_is_used

  Indicates if data are retrieved from FIFO or registers.
- uint8_t fsync_to_be_ignored

  Indicates if the next FSYNC should be ignored.
- uint32_t wu_off_acc_odr_changes

  Accel Low Power could report with wrong ODR if internal counter for ODR changed overflowed.
- uint8_t wom_smd_mask

  Keeps track if wom or smd is enabled.
- uint8_t wom_enable

  Keeps track if wom is enabled.
- struct {
  uint8_t acc_lp_avg
  Low-power averaging setting for accelerometer.
  uint8_t reserved
  reserved field
  uint8_t acc_ln_bw
  Low-noise filter bandwidth setting for accelerometer.
  uint8_t gyr_ln_bw
  Low-noise filter bandwidth setting for gyroscope.
  } avg_bw_setting

  Software mirror of BW and AVG settings in hardware.
- uint64_t gyro_power_off_tmst

  Keeps track of timestamp when gyro is power off.

6.2.1 Detailed Description

Icm426xx driver states definition.

6.2.2 Member Data Documentation

6.2.2.1 acc_ln_bw

```
uint8_t inv_icm426xx::acc_ln_bw
```

Low-noise filter bandwidth setting for accelerometer.

6.2.2.2 acc_lp_avg

```
uint8_t inv_icm426xx::acc_lp_avg
```

Low-power averaging setting for accelerometer.

6.2.2.3 accel_st_bias

```
int inv_icm426xx::accel_st_bias[3]
```

Accel bias values (lsb) collected during self test.

6.2.2.4 accel_start_time_us

```
uint64_t inv_icm426xx::accel_start_time_us
```

Internal state needed to discard first accel samples.

6.2.2.5

```
struct { ... } inv_icm426xx::avg_bw_setting
```

Software mirror of BW and AVG settings in hardware.

To be re-applied on each enabling of sensor

6.2.2.6 dmp_from_sram

```
uint8_t inv_icm426xx::dmp_from_sram
```

DMP executes from SRAM.

6.2.2.7 dmp_is_on

```
uint8_t inv_icm426xx::dmp_is_on
```

DMP started status.

6.2.2.8 endianess_data

```
uint8_t inv_icm426xx::endianess_data
```

Internal status of data endianness mode to report correctly data.

6.2.2.9 fifo_data

```
uint8_t inv_icm426xx::fifo_data[ICM426XX_FIFO_MIRRORING_SIZE]
```

FIFO mirroring memory area.

6.2.2.10 fifo_highres_enabled

```
uint8_t inv_icm426xx::fifo_highres_enabled
```

Indicates if highres mode is used for FIFO.

6.2.2.11 fifo_is_used

```
INV_ICM426XX_FIFO_CONFIG_t inv_icm426xx::fifo_is_used
```

Indicates if data are retrieved from FIFO or registers.

6.2.2.12 fsync_to_be_ignored

```
uint8_t inv_icm426xx::fsync_to_be_ignored
```

Indicates if the next FSYNC should be ignored.

When the sensors are switched off and then on again, an FSYNC tag with incorrect FSYNC value can be generated on the next first ODR. Solution: FSYNC tag and FSYNC data should be ignored on this first ODR.

6.2.2.13 gyr_ln_bw

```
uint8_t inv_icm426xx::gyr_ln_bw
```

Low-noise filter bandwidth setting for gyroscope.

6.2.2.14 gyro_power_off_tmst

```
uint64_t inv_icm426xx::gyro_power_off_tmst
```

Keeps track of timestamp when gyro is power off.

6.2.2.15 gyro_st_bias

```
int inv_icm426xx::gyro_st_bias[3]
```

Gyro bias values (lsb) collected during self test.

6.2.2.16 gyro_start_time_us

```
uint64_t inv_icm426xx::gyro_start_time_us
```

Internal state needed to discard first gyro samples.

6.2.2.17 reserved

```
uint8_t inv_icm426xx::reserved
```

reserved field

6.2.2.18 sensor_event_cb

```
void(* inv_icm426xx::sensor_event_cb) (inv_icm426xx_sensor_event_t *event)
```

Callback executed when retrieving data from FIFO or registers.

Called by `inv_icm426xx_get_data_from_fifo` for each packet in FIFO. Called by `inv_icm426xx_get_data_from_registers` when reading registers. This field may be NULL if aformentioned functions are not used by application.

6.2.2.19 st_result

```
int inv_icm426xx::st_result
```

Flag to keep track if self-test has already been executed.

6.2.2.20 tmst_to_reg_en_cnt

```
uint8_t inv_icm426xx::tmst_to_reg_en_cnt
```

Internal counter to keep track of the timestamp to register access availability.

6.2.2.21 transport

```
struct inv_icm426xx_transport inv_icm426xx::transport
```

Transport structure.

6.2.2.22 wom_enable

```
uint8_t inv_icm426xx::wom_enable
```

Keeps track if wom is enabled.

6.2.2.23 wom_smd_mask

```
uint8_t inv_icm426xx::wom_smd_mask
```

Keeps track if wom or smd is enabled.

6.2.2.24 wu_off_acc_odr_changes

```
uint32_t inv_icm426xx::wu_off_acc_odr_changes
```

Accel Low Power could report with wrong ODR if internal counter for ODR changed overflowed.

WUOSC clock domain is informed through an 3bit counter that ODR has changed in RC/PLL mode. Every 8 event, this counter overflows and goes back to 0, same as 'no ODR changes', therefore previous ALP ODR is re-used. Solution: Keep track of ODR changes when WUOSC is disabled and perform dummy ODR changes when re-enabling WU after 8∗n ODR changes.

The documentation for this struct was generated from the following file:

- Icm426xxDriver_HL.h

6.3 inv_icm426xx_apex_parameters Struct Reference

Icm426xx APEX inputs parameters definition.

`#include <Icm426xxDriver_HL_apex.h>`

Public Attributes

- ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_t pedo_amp_th

  Peak threshold value to be considered as a valid step (mg)
- uint8_t pedo_step_cnt_th

  Minimum number of steps that must be detected before the pedometer step count begins incrementing.
- uint8_t pedo_step_det_th

  Minimum number of low latency steps that must be detected before the pedometer step count begins incrementing.
- ICM426XX_APEX_CONFIG3_PEDO_SB_TIMER_TH_t pedo_sb_timer_th

  Duration of non-walk to exit the current walk mode, `pedo_step_cnt_th` number of steps must again be detected before step count starts to increase.
- ICM426XX_APEX_CONFIG3_PEDO_HI_ENRGY_TH_t pedo_hi_enrgy_th

  Threshold to improve run detection if not steps are counted while running.
- ICM426XX_APEX_CONFIG4_TILT_WAIT_TIME_t tilt_wait_time

  Number of accelerometer samples to wait before triggering tilt event.
- ICM426XX_APEX_CONFIG1_DMP_POWER_SAVE_TIME_t power_save_time
- ICM426XX_APEX_CONFIG0_DMP_POWER_SAVE_t power_save

  Power save mode for APEX algorithms.
- ICM426XX_APEX_CONFIG9_SENSITIVITY_MODE_t sensitivity_mode

  Sensitivity mode Normal(0) or Slow walk(1).
- ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_t low_energy_amp_th

  Peak threshold value to be considered as a valid step (mg) in Slow walk mode.

6.3.1 Detailed Description

Icm426xx APEX inputs parameters definition.

6.3.2 Member Data Documentation

6.3.2.1 low_energy_amp_th

`ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_t inv_icm426xx_apex_parameters::low_energy_amp_th`

Peak threshold value to be considered as a valid step (mg) in Slow walk mode.

6.3.2.2 pedo_amp_th

`ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_t inv_icm426xx_apex_parameters::pedo_amp_th`

Peak threshold value to be considered as a valid step (mg)

6.3.2.3 pedo_hi_enrgy_th

`ICM426XX_APEX_CONFIG3_PEDO_HI_ENRGY_TH_t inv_icm426xx_apex_parameters::pedo_hi_enrgy_th`

Threshold to improve run detection if not steps are counted while running.

6.3.2.4 pedo_sb_timer_th

`ICM426XX_APEX_CONFIG3_PEDO_SB_TIMER_TH_t inv_icm426xx_apex_parameters::pedo_sb_timer_th`

Duration of non-walk to exit the current walk mode, `pedo_step_cnt_th` number of steps must again be detected before step count starts to increase.

6.3.2.5 pedo_step_cnt_th

`uint8_t inv_icm426xx_apex_parameters::pedo_step_cnt_th`

Minimum number of steps that must be detected before the pedometer step count begins incrementing.

6.3.2.6 pedo_step_det_th

`uint8_t inv_icm426xx_apex_parameters::pedo_step_det_th`

Minimum number of low latency steps that must be detected before the pedometer step count begins incrementing.

6.3.2.7 power_save

`ICM426XX_APEX_CONFIG0_DMP_POWER_SAVE_t inv_icm426xx_apex_parameters::power_save`

Power save mode for APEX algorithms.

This mode will put APEX features into sleep mode, leaving only the WOM running to wake-up the DMP.

6.3.2.8 power_save_time

`ICM426XX_APEX_CONFIG1_DMP_POWER_SAVE_TIME_t inv_icm426xx_apex_parameters::power_save_time`

6.3.2.9 sensitivity_mode

`ICM426XX_APEX_CONFIG9_SENSITIVITY_MODE_t inv_icm426xx_apex_parameters::sensitivity_mode`

Sensitivity mode Normal(0) or Slow walk(1).

The Slow walk mode improve the slow walk detection (<1Hz) but in return the number of false detection might be increased.

6.3.2.10 tilt_wait_time

`ICM426XX_APEX_CONFIG4_TILT_WAIT_TIME_t inv_icm426xx_apex_parameters::tilt_wait_time`

Number of accelerometer samples to wait before triggering tilt event.

The time after which DMP goes in power save mode according to the DMP ODR configured

The documentation for this struct was generated from the following file:

- Icm426xxDriver_HL_apex.h

6.4 inv_icm426xx_apex_step_activity Struct Reference

APEX pedometer outputs.

`#include <Icm426xxDriver_HL_apex.h>`

Public Attributes

- uint16_t step_cnt
  Number of steps taken.
- uint8_t step_cadence
  Walk/run cadency in number of samples.
- uint8_t activity_class
  Detected activity unknown (0), walk (1) or run (2)

6.4.1 Detailed Description

APEX pedometer outputs.

6.4.2 Member Data Documentation

6.4.2.1 activity_class

```
uint8_t inv_icm426xx_apex_step_activity::activity_class
```

Detected activity unknown (0), walk (1) or run (2)

6.4.2.2 step_cadence

```
uint8_t inv_icm426xx_apex_step_activity::step_cadence
```

Walk/run cadency in number of samples.

Format is u6.2. E.g, At 50Hz and 2Hz walk frequency, if the cadency is 25 samples, the register will output 100.

6.4.2.3 step_cnt

```
uint16_t inv_icm426xx_apex_step_activity::step_cnt
```

Number of steps taken.

The documentation for this struct was generated from the following file:

- Icm426xxDriver_HL_apex.h

6.5 inv_icm426xx_interrupt_parameter_t Struct Reference

Icm426xx set of interrupt enable flag.

```
#include <Icm426xxDriver_HL.h>
```

Public Attributes

- inv_icm426xx_interrupt_value INV_ICM426XX_UI_FSYNC
- inv_icm426xx_interrupt_value INV_ICM426XX_UI_DRDY
- inv_icm426xx_interrupt_value INV_ICM426XX_FIFO_THS
- inv_icm426xx_interrupt_value INV_ICM426XX_FIFO_FULL
- inv_icm426xx_interrupt_value INV_ICM426XX_SMD
- inv_icm426xx_interrupt_value INV_ICM426XX_WOM_X
- inv_icm426xx_interrupt_value INV_ICM426XX_WOM_Y
- inv_icm426xx_interrupt_value INV_ICM426XX_WOM_Z
- inv_icm426xx_interrupt_value INV_ICM426XX_STEP_DET
- inv_icm426xx_interrupt_value INV_ICM426XX_STEP_CNT_OVFL
- inv_icm426xx_interrupt_value INV_ICM426XX_TILT_DET
- inv_icm426xx_interrupt_value INV_ICM426XX_TAP_DET

6.5.1 Detailed Description

Icm426xx set of interrupt enable flag.

6.5.2 Member Data Documentation

6.5.2.1 INV_ICM426XX_FIFO_FULL

```
inv_icm426xx_interrupt_value inv_icm426xx_interrupt_parameter_t::INV_ICM426XX_FIFO_FULL
```

6.5.2.2 INV_ICM426XX_FIFO_THS

```
inv_icm426xx_interrupt_value inv_icm426xx_interrupt_parameter_t::INV_ICM426XX_FIFO_THS
```

6.5.2.3 INV_ICM426XX_SMD

```
inv_icm426xx_interrupt_value inv_icm426xx_interrupt_parameter_t::INV_ICM426XX_SMD
```

6.5.2.4 INV_ICM426XX_STEP_CNT_OVFL

```
inv_icm426xx_interrupt_value inv_icm426xx_interrupt_parameter_t::INV_ICM426XX_STEP_CNT_OVFL
```

6.5.2.5 INV_ICM426XX_STEP_DET

```
inv_icm426xx_interrupt_value inv_icm426xx_interrupt_parameter_t::INV_ICM426XX_STEP_DET
```

6.5.2.6 INV_ICM426XX_TAP_DET

```
inv_icm426xx_interrupt_value inv_icm426xx_interrupt_parameter_t::INV_ICM426XX_TAP_DET
```

6.5.2.7 INV_ICM426XX_TILT_DET

inv_icm426xx_interrupt_value inv_icm426xx_interrupt_parameter_t::INV_ICM426XX_TILT_DET

6.5.2.8 INV_ICM426XX_UI_DRDY

inv_icm426xx_interrupt_value inv_icm426xx_interrupt_parameter_t::INV_ICM426XX_UI_DRDY

6.5.2.9 INV_ICM426XX_UI_FSYNC

inv_icm426xx_interrupt_value inv_icm426xx_interrupt_parameter_t::INV_ICM426XX_UI_FSYNC

6.5.2.10 INV_ICM426XX_WOM_X

inv_icm426xx_interrupt_value inv_icm426xx_interrupt_parameter_t::INV_ICM426XX_WOM_X

6.5.2.11 INV_ICM426XX_WOM_Y

inv_icm426xx_interrupt_value inv_icm426xx_interrupt_parameter_t::INV_ICM426XX_WOM_Y

6.5.2.12 INV_ICM426XX_WOM_Z

inv_icm426xx_interrupt_value inv_icm426xx_interrupt_parameter_t::INV_ICM426XX_WOM_Z

The documentation for this struct was generated from the following file:

- Icm426xxDriver_HL.h

6.6 inv_icm426xx_sensor_event_t Struct Reference

Sensor event structure definition.

```
#include <Icm426xxDriver_HL.h>
```

Public Attributes

- int sensor_mask
- uint16_t timestamp_fsync
- int16_t accel [3]
- int16_t gyro [3]
- int16_t temperature
- int8_t accel_high_res [3]
- int8_t gyro_high_res [3]

6.6.1 Detailed Description

Sensor event structure definition.

6.6.2 Member Data Documentation

6.6.2.1 accel

```
int16_t inv_icm426xx_sensor_event_t::accel[3]
```

6.6.2.2 accel_high_res

```
int8_t inv_icm426xx_sensor_event_t::accel_high_res[3]
```

6.6.2.3 gyro

```
int16_t inv_icm426xx_sensor_event_t::gyro[3]
```

6.6.2.4 gyro_high_res

```
int8_t inv_icm426xx_sensor_event_t::gyro_high_res[3]
```

6.6.2.5 sensor_mask

```
int inv_icm426xx_sensor_event_t::sensor_mask
```

6.6.2.6 temperature

```
int16_t inv_icm426xx_sensor_event_t::temperature
```

6.6.2.7 timestamp_fsync

```
uint16_t inv_icm426xx_sensor_event_t::timestamp_fsync
```

The documentation for this struct was generated from the following file:

- Icm426xxDriver_HL.h

6.7 inv_icm426xx_serif Struct Reference

base sensor serial interface

```
#include <Icm426xxTransport.h>
```

Public Attributes

- void * context
- int(* read_reg)(struct inv_icm426xx_serif *serif, uint8_t reg, uint8_t *buf, uint32_t len)
- int(* write_reg)(struct inv_icm426xx_serif *serif, uint8_t reg, const uint8_t *buf, uint32_t len)
- int(* configure)(struct inv_icm426xx_serif *serif)
- uint32_t max_read
- uint32_t max_write
- uint32_t serif_type

6.7.1 Detailed Description

base sensor serial interface

6.7.2 Member Data Documentation

6.7.2.1 configure

```
int(* inv_icm426xx_serif::configure) (struct inv_icm426xx_serif *serif)
```

6.7.2.2 context

```
void* inv_icm426xx_serif::context
```

6.7.2.3 max_read

```
uint32_t inv_icm426xx_serif::max_read
```

6.7.2.4 max_write

```
uint32_t inv_icm426xx_serif::max_write
```

6.7.2.5 read_reg

```
int(* inv_icm426xx_serif::read_reg) (struct inv_icm426xx_serif *serif, uint8_t reg, uint8_↩
t *buf, uint32_t len)
```

6.7.2.6 serif_type

```
uint32_t inv_icm426xx_serif::serif_type
```

6.7.2.7 write_reg

```
int(* inv_icm426xx_serif::write_reg) (struct inv_icm426xx_serif *serif, uint8_t reg, const
uint8_t *buf, uint32_t len)
```

The documentation for this struct was generated from the following file:

- Icm426xxTransport.h

6.8 inv_icm426xx_tap_data Struct Reference

TAP outputs.

```
#include <Icm426xxDriver_HL_apex.h>
```

Public Attributes

- ICM426XX_APEX_DATA4_TAP_NUM_t tap_num

  Detects single (1) or double (2) tap.
- ICM426XX_APEX_DATA4_TAP_AXIS_t tap_axis

  Axis along which tap has been detected.
- ICM426XX_APEX_DATA4_TAP_DIR_t tap_dir

  Direction of the tap, either +axis (1) or -axis (0)
- uint8_t double_tap_timing

  Timing between both taps of a double tap expressed in 1/16th of odr in ms (e.g At 500Hz, 2 means 64ms between each tap)

6.8.1 Detailed Description

TAP outputs.

6.8.2 Member Data Documentation

6.8.2.1 double_tap_timing

```
uint8_t inv_icm426xx_tap_data::double_tap_timing
```

Timing between both taps of a double tap expressed in 1/16th of odr in ms (e.g At 500Hz, 2 means 64ms between each tap)

6.8.2.2 tap_axis

```
ICM426XX_APEX_DATA4_TAP_AXIS_t inv_icm426xx_tap_data::tap_axis
```

Axis along which tap has been detected.

6.8.2.3 tap_dir

```
ICM426XX_APEX_DATA4_TAP_DIR_t inv_icm426xx_tap_data::tap_dir
```

Direction of the tap, either +axis (1) or -axis (0)

6.8.2.4 tap_num

```
ICM426XX_APEX_DATA4_TAP_NUM_t inv_icm426xx_tap_data::tap_num
```

Detects single (1) or double (2) tap.

The documentation for this struct was generated from the following file:

- Icm426xxDriver_HL_apex.h

6.9 inv_icm426xx_tap_parameters_t Struct Reference

Icm426xx TAP inputs parameters definition.

```
#include <Icm426xxDriver_HL_apex.h>
```

Public Attributes

- uint8_t min_jerk_thr
  Minimum Jerk Threshold.
- ICM426XX_APEX_CONFIG7_TAP_MAX_PEAK_TOL_t max_peak_tol
  Maximum peak tolerance.
- ICM426XX_APEX_CONFIG8_TAP_TMAX_t tmax
  Tap measurement window.
- ICM426XX_APEX_CONFIG8_TAP_TAVG_t tavg
  Energy measumerement window.
- ICM426XX_APEX_CONFIG8_TAP_TMIN_t tmin
  Single tap window.

6.9.1 Detailed Description

Icm426xx TAP inputs parameters definition.

6.9.2 Member Data Documentation

6.9.2.1 max_peak_tol

```
ICM426XX_APEX_CONFIG7_TAP_MAX_PEAK_TOL_t inv_icm426xx_tap_parameters_t::max_peak_tol
```

Maximum peak tolerance.

6.9.2.2 min_jerk_thr

`uint8_t inv_icm426xx_tap_parameters_t::min_jerk_thr`

Minimum Jerk Threshold.

6.9.2.3 tavg

`ICM426XX_APEX_CONFIG8_TAP_TAVG_t inv_icm426xx_tap_parameters_t::tavg`

Energy measumerement window.

6.9.2.4 tmax

`ICM426XX_APEX_CONFIG8_TAP_TMAX_t inv_icm426xx_tap_parameters_t::tmax`

Tap measurement window.

6.9.2.5 tmin

`ICM426XX_APEX_CONFIG8_TAP_TMIN_t inv_icm426xx_tap_parameters_t::tmin`

Single tap window.

The documentation for this struct was generated from the following file:

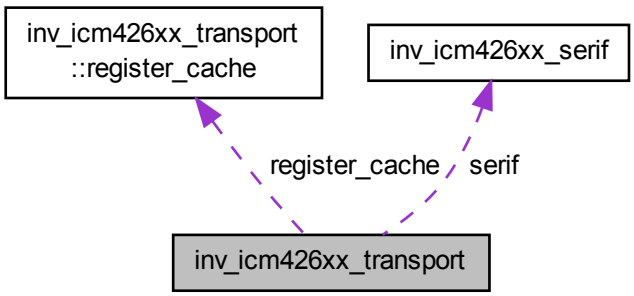
- Icm426xxDriver_HL_apex.h

6.10 inv_icm426xx_transport Struct Reference

transport interface

`#include <Icm426xxTransport.h>`

Collaboration diagram for inv_icm426xx_transport:



Classes

- struct register_cache

  Contains mirrored values of some IP registers.

Public Attributes

- struct inv_icm426xx_serif serif

  Warning : this field MUST be the first one of struct inv_icm426xx_transport.
- struct inv_icm426xx_transport::register_cache register_cache

  Store mostly used register values on SRAM.

6.10.1 Detailed Description

transport interface

6.10.2 Member Data Documentation

6.10.2.1 register_cache

```
struct inv_icm426xx_transport::register_cache inv_icm426xx_transport::register_cache
```

Store mostly used register values on SRAM.

MPUREG_OTP_SEC_STATUS_B1 and MPUREG_INT_STATUS registers are read before the cache has a chance to be initialized. Therefore, these registers shall never be added to the cache Registers from bank 1,2,3 or 4 shall never be added to the cache

6.10.2.2 serif

```
struct inv_icm426xx_serif inv_icm426xx_transport::serif
```

Warning : this field MUST be the first one of struct inv_icm426xx_transport.

The documentation for this struct was generated from the following file:

- Icm426xxTransport.h

6.11 inv_icm426xx_transport::register_cache Struct Reference

Contains mirrored values of some IP registers.

```
#include <Icm426xxTransport.h>
```

Public Attributes

- uint8_t intf_cfg_1_reg
  INTF_CONFIG1, Bank: 0, Address: 0x4D.
- uint8_t pwr_mngt_0_reg
  PWR_MGMT_0, Bank: 0, Address: 0x4E.
- uint8_t gyro_cfg_0_reg
  GYRO_CONFIG0, Bank: 0, Address: 0x4F.
- uint8_t accel_cfg_0_reg
  ACCEL_CONFIG0, Bank: 0, Address: 0x50.
- uint8_t tmst_cfg_reg
  TMST_CONFIG, Bank: 0, Address: 0x54.
- uint8_t bank_sel_reg
  MPUREG_REG_BANK_SEL, All banks, Address 0x76.

6.11.1 Detailed Description

Contains mirrored values of some IP registers.

6.11.2 Member Data Documentation

6.11.2.1 accel_cfg_0_reg

```
uint8_t inv_icm426xx_transport::register_cache::accel_cfg_0_reg
```

ACCEL_CONFIG0, Bank: 0, Address: 0x50.

6.11.2.2 bank_sel_reg

```
uint8_t inv_icm426xx_transport::register_cache::bank_sel_reg
```

MPUREG_REG_BANK_SEL, All banks, Address 0x76.

6.11.2.3 gyro_cfg_0_reg

```
uint8_t inv_icm426xx_transport::register_cache::gyro_cfg_0_reg
```

GYRO_CONFIG0, Bank: 0, Address: 0x4F.

6.11.2.4 intf_cfg_1_reg

```
uint8_t inv_icm426xx_transport::register_cache::intf_cfg_1_reg
```

INTF_CONFIG1, Bank: 0, Address: 0x4D.

6.11.2.5 pwr_mngt_0_reg

```
uint8_t inv_icm426xx_transport::register_cache::pwr_mngt_0_reg
```

PWR_MGMT_0, Bank: 0, Address: 0x4E.

6.11.2.6 tmst_cfg_reg

```
uint8_t inv_icm426xx_transport::register_cache::tmst_cfg_reg
```

TMST_CONFIG, Bank: 0, Address: 0x54.

The documentation for this struct was generated from the following file:

- Icm426xxTransport.h

Chapter 7

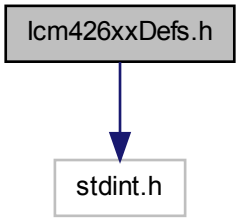
File Documentation

7.1 Icm426xxDefs.h File Reference

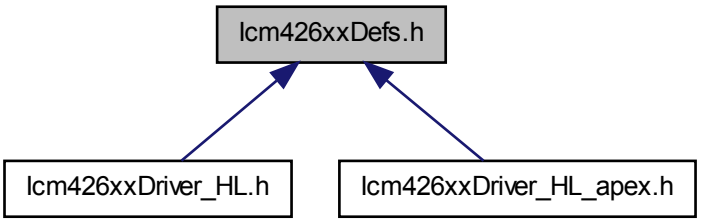
File exposing the device register map.

```
#include <stdint.h>
```

Include dependency graph for Icm426xxDefs.h:



This graph shows which files directly or indirectly include this file:



Classes

- union fifo_header_t

  Describe the content of the FIFO header.

Macros

- #define ICM40608_WHOAMI 0x39
- #define ICM42600_WHOAMI 0x40
- #define ICM42602_WHOAMI 0x41
- #define ICM42605_WHOAMI 0x42
- #define ICM42622_WHOAMI 0x46
- #define ICM42631_WHOAMI 0x5C
- #define ICM42633_WHOAMI 0x5B
- #define ICM42686P_WHOAMI 0x44
- #define ICM42688P_WHOAMI 0x47
- #define ICM42686V_WHOAMI 0xDA
- #define ICM42688V_WHOAMI 0xDB
- #define ICM42608_WHOAMI 0x48
- #define ICM_FAMILY_BPLUS

  ICM family definition Possible values are ICM_FAMILY_CPLUS or ICM_FAMILY_BPLUS.
- #define MPUREG_DEVICE_CONFIG 0x11
- #define MPUREG_CHIP_CONFIG MPUREG_DEVICE_CONFIG
- #define MPUREG_DRIVE_CONFIG 0x13
- #define MPUREG_INT_CONFIG 0x14
- #define MPUREG_FIFO_CONFIG 0x16
- #define MPUREG_TEMP_DATA0_UI 0x1D
- #define MPUREG_ACCEL_DATA_X0_UI 0x1F
- #define MPUREG_GYRO_DATA_X0_UI 0x25
- #define MPUREG_TMST_FSYNCH 0x2B
- #define MPUREG_TMST_FSYNC1 MPUREG_TMST_FSYNCH
- #define MPUREG_INT_STATUS 0x2D
- #define MPUREG_FIFO_COUNTH 0x2E
- #define MPUREG_FIFO_BYTE_COUNT1 MPUREG_FIFO_COUNTH
- #define MPUREG_FIFO_COUNTL 0x2F
- #define MPUREG_FIFO_BYTE_COUNT2 MPUREG_FIFO_COUNTL
- #define MPUREG_FIFO_DATA 0x30
- #define MPUREG_APEX_DATA0 0x31
- #define MPUREG_APEX_DATA1 0x32
- #define MPUREG_APEX_DATA2 0x33
- #define MPUREG_APEX_DATA3 0x34
- #define MPUREG_APEX_DATA4 0x35
- #define MPUREG_APEX_DATA5 0x36
- #define MPUREG_INT_STATUS2 0x37
- #define MPUREG_INT_STATUS3 0x38
- #define MPUREG_SIGNAL_PATH_RESET 0x4B
- #define MPUREG_INTF_CONFIG0 0x4C
- #define MPUREG_INTF_CONFIG1 0x4D
- #define MPUREG_PWR_MGMT_0 0x4E
- #define MPUREG_GYRO_CONFIG0 0x4F
- #define MPUREG_ACCEL_CONFIG0 0x50
- #define MPUREG_GYRO_CONFIG1 0x51
- #define MPUREG_ACCEL_GYRO_CONFIG0 0x52

- #define MPUREG_ACCEL_CONFIG1 0x53
- #define MPUREG_TMST_CONFIG 0x54
- #define MPUREG_APEX_CONFIG0 0x56
- #define MPUREG_SMD_CONFIG 0x57
- #define MPUREG_FIFO_CONFIG1 0x5F
- #define MPUREG_FIFO_CONFIG2 0x60
- #define MPUREG_FSYNC_CONFIG 0x62
- #define MPUREG_INT_CONFIG0 0x63
- #define MPUREG_INT_CONFIG1 0x64
- #define MPUREG_INT_SOURCE0 0x65
- #define MPUREG_INT_SOURCE1 0x66
- #define MPUREG_INT_SOURCE2 0x67
- #define MPUREG_INT_SOURCE3 0x68
- #define MPUREG_INT_SOURCE4 0x69
- #define MPUREG_INT_SOURCE5 0x6A
- #define MPUREG_FIFO_LOST_PKT0 0x6C
- #define MPUREG_SELF_TEST_CONFIG 0x70
- #define MPUREG_WHO_AM_I 0x75
- #define MPUREG_SCAN0 0x71
- #define MPUREG_MEM_BANK_SEL 0x72
- #define MPUREG_MEM_START_ADDR 0x73
- #define MPUREG_MEM_R_W 0x74
- #define MPUREG_REG_BANK_SEL 0x76
- #define MPUREG_SENSOR_CONFIG1_B1 0x04
- #define MPUREG_GYRO_CONFIG_STATIC2_B1 0x0B
- #define MPUREG_GYRO_CONFIG_STATIC3_B1 0x0C
- #define MPUREG_GYRO_CONFIG_STATIC4_B1 0x0D
- #define MPUREG_GYRO_CONFIG_STATIC5_B1 0x0E
- #define MPUREG_XG_ST_DATA_B1 0x5F
- #define MPUREG_YG_ST_DATA_B1 0x60
- #define MPUREG_ZG_ST_DATA_B1 0x61
- #define MPUREG_TMST_VAL0_B1 0x62
- #define MPUREG_INTF_CONFIG4_B1 0x7A
- #define MPUREG_INTF_CONFIG5_B1 0x7B
- #define MPUREG_INTF_CONFIG6_B1 0x7C
- #define MPUREG_INTF_CONFIG3_B1 0x79
- #define MPUREG_ACCEL_CONFIG_STATIC2_B2 0x03
- #define MPUREG_ACCEL_CONFIG_STATIC3_B2 0x04
- #define MPUREG_ACCEL_CONFIG_STATIC4_B2 0x05
- #define MPUREG_ACCEL_CONFIG_STATIC0_B2 0x39
- #define MPUREG_XA_ST_DATA_B2 0x3B
- #define MPUREG_YA_ST_DATA_B2 0x3C
- #define MPUREG_ZA_ST_DATA_B2 0x3D
- #define MPUREG_OIS1_CONFIG1_B2 0x44
- #define MPUREG_OIS1_CONFIG2_B2 0x45
- #define MPUREG_OIS1_CONFIG3_B2 0x46
- #define MPUREG_ACCEL_DATA_X0_OIS1_B2 0x49
- #define MPUREG_GYRO_DATA_X0_OIS1_B2 0x4F
- #define MPUREG_INT_STATUS_OIS1_B2 0x57
- #define MPUREG_OIS2_CONFIG1_B2 0x59
- #define MPUREG_OIS2_CONFIG2_B2 0x5A
- #define MPUREG_OIS2_CONFIG3_B2 0x5B
- #define MPUREG_ACCEL_DATA_X0_OIS2_B2 0x5E
- #define MPUREG_GYRO_DATA_X0_OIS2_B2 0x64
- #define MPUREG_INT_STATUS_OIS2_B2 0x6C

- #define MPUREG_TMD4_B2 0x70
- #define MPUREG_TMD5_B2 0x71
- #define MPUREG_TMD6_B2 0x72
- #define MPUREG_TMD7_B2 0x73
- #define MPUREG_PU_PD_CONFIG1_B3 0x06
- #define MPUREG_PU_PD_CONFIG2_B3 0x0E
- #define MPUREG_FDR_CONFIG_B4 0x09
- #define MPUREG_APEX_CONFIG1_B4 0x40
- #define MPUREG_APEX_CONFIG2_B4 0x41
- #define MPUREG_APEX_CONFIG3_B4 0x42
- #define MPUREG_APEX_CONFIG4_B4 0x43
- #define MPUREG_APEX_CONFIG5_B4 0x44
- #define MPUREG_APEX_CONFIG6_B4 0x45
- #define MPUREG_APEX_CONFIG7_B4 0x46
- #define MPUREG_APEX_CONFIG8_B4 0x47
- #define MPUREG_APEX_CONFIG9_B4 0x48
- #define MPUREG_APEX_CONFIG10_B4 0x49
- #define MPUREG_ACCEL_WOM_X_THR_B4 0x4A
- #define MPUREG_ACCEL_WOM_Y_THR_B4 0x4B
- #define MPUREG_ACCEL_WOM_Z_THR_B4 0x4C
- #define MPUREG_INT_SOURCE6_B4 0x4D
- #define MPUREG_INT_SOURCE7_B4 0x4E
- #define MPUREG_INT_SOURCE8_B4 0x4F
- #define MPUREG_INT_SOURCE9_B4 0x50
- #define MPUREG_INT_SOURCE10_B4 0x51
- #define MPUREG_OFFSET_USER_0_B4 0x77
- #define MPUREG_OFFSET_USER_1_B4 0x78
- #define MPUREG_OFFSET_USER_2_B4 0x79
- #define MPUREG_OFFSET_USER_3_B4 0x7A
- #define MPUREG_OFFSET_USER_4_B4 0x7B
- #define MPUREG_OFFSET_USER_5_B4 0x7C
- #define MPUREG_OFFSET_USER_6_B4 0x7D
- #define MPUREG_OFFSET_USER_7_B4 0x7E
- #define MPUREG_OFFSET_USER_8_B4 0x7F
- #define ACCEL_DATA_SIZE 6
- #define GYRO_DATA_SIZE 6
- #define TEMP_DATA_SIZE 2
- #define FIFO_HEADER_SIZE 1
- #define FIFO_ACCEL_DATA_SIZE ACCEL_DATA_SIZE
- #define FIFO_GYRO_DATA_SIZE GYRO_DATA_SIZE
- #define FIFO_TEMP_DATA_SIZE 1
- #define FIFO_TS_FSYNC_SIZE 2
- #define FIFO_TEMP_HIGH_RES_SIZE 1
- #define FIFO_ACCEL_GYRO_HIGH_RES_SIZE 3
- #define FIFO_16BYTES_PACKET_SIZE
- #define FIFO_20BYTES_PACKET_SIZE
- #define FIFO_HEADER_ODR_ACCEL 0x01
- #define FIFO_HEADER_ODR_GYRO 0x02
- #define FIFO_HEADER_FSYNC 0x04
- #define FIFO_HEADER_TMST 0x08
- #define FIFO_HEADER_HEADER_20 0x10
- #define FIFO_HEADER_GYRO 0x20
- #define FIFO_HEADER_ACC 0x40
- #define FIFO_HEADER_MSG 0x80
- #define INVALID_VALUE_FIFO ((int16_t)0x8000)

- #define INVALID_VALUE_FIFO_1B ((int8_t)0x80)
- #define I3C_IBI_PAYLOAD_ALL 0xFF
- #define I3C_IBI_PAYLOAD_TIMEC 0x80
- #define I3C_IBI_PAYLOAD_CAT_MISC 0x40
- #define I3C_IBI_PAYLOAD_CAT_ERROR 0x20
- #define I3C_IBI_PAYLOAD_CAT_APEX2 0x10
- #define I3C_IBI_PAYLOAD_CAT_APEX1 0x08
- #define I3C_IBI_PAYLOAD_CAT_OIS1_DRDY 0x04
- #define I3C_IBI_PAYLOAD_CAT_FIFO 0x02
- #define I3C_IBI_PAYLOAD_CAT_UI_DRDY 0x01
- #define BIT_DEVICE_CONFIG_SPI_MODE_POS 4
- #define BIT_DEVICE_CONFIG_SPI_MODE_MASK (0x1 << BIT_DEVICE_CONFIG_SPI_MODE_POS)
- #define BIT_CHIP_CONFIG_SPI_MODE_MASK BIT_DEVICE_CONFIG_SPI_MODE_MASK
- #define BIT_CHIP_CONFIG_SPI_MODE_POS BIT_DEVICE_CONFIG_SPI_MODE_POS
- #define BIT_DEVICE_CONFIG_RESET_POS 0
- #define BIT_DEVICE_CONFIG_RESET_MASK 0x01
- #define BIT_CHIP_CONFIG_RESET_MASK BIT_DEVICE_CONFIG_RESET_MASK
- #define BIT_CHIP_CONFIG_RESET_POS BIT_DEVICE_CONFIG_RESET_POS
- #define BIT_INT_CONFIG_INT2_DRIVE_CIRCUIT_POS 4
- #define BIT_INT_CONFIG_INT2_DRIVE_CIRCUIT_MASK (0x01 << BIT_INT_CONFIG_INT2_DRIVE_CIRCUIT_POS)
- #define BIT_INT_CONFIG_INT2_POLARITY_POS 3
- #define BIT_INT_CONFIG_INT2_POLARITY_MASK (0x01 << BIT_INT_CONFIG_INT2_POLARITY_POS)
- #define BIT_INT_CONFIG_INT1_DRIVE_CIRCUIT_POS 1
- #define BIT_INT_CONFIG_INT1_DRIVE_CIRCUIT_MASK (0x01 << BIT_INT_CONFIG_INT1_DRIVE_CIRCUIT_POS)
- #define BIT_INT_CONFIG_INT1_POLARITY_POS 0
- #define BIT_INT_CONFIG_INT1_POLARITY_MASK 0x01
- #define BIT_FIFO_CONFIG_MODE_POS 6
- #define BIT_FIFO_CONFIG_MODE_MASK (0x03 << BIT_FIFO_CONFIG_MODE_POS)
- #define ICM426XX_FIFO_CONFIG_MODE_SNAPSHOT = ICM426XX_FIFO_CONFIG_MODE_STOP_ON_FULL;
- #define BIT_INT_STATUS_UI_FSYNC 0x40
- #define BIT_INT_STATUS_PLL_RDY 0x20
- #define BIT_INT_STATUS_RESET_DONE 0x10
- #define BIT_INT_STATUS_DRDY 0x08
- #define BIT_INT_STATUS_FIFO_THS 0x04
- #define BIT_INT_STATUS_FIFO_FULL 0x02
- #define BIT_INT_STATUS_AGC_RDY 0x01
- #define BIT_APEX_DATA3_ACTIVITY_CLASS_POS 0
- #define BIT_APEX_DATA3_ACTIVITY_CLASS_MASK 0x03
- #define BIT_APEX_DATA3_DMP_IDLE_POS 2
- #define BIT_APEX_DATA3_DMP_IDLE_MASK (0x01 << BIT_APEX_DATA3_DMP_IDLE_POS)
- #define BIT_APEX_DATA4_TAP_NUM_POS 3

  TAP status flags: non-zero value - tap detected bit0 - positive or negative edge bit1 and 2 - axis detected : 0-X ; 1-Y ; 2-Z bit3 and 4 - tap type : 1-single ; 2 -double.
- #define BIT_APEX_DATA4_TAP_NUM_MASK (0x03 << BIT_APEX_DATA4_TAP_NUM_POS)
- #define BIT_APEX_DATA4_TAP_AXIS_POS 1
- #define BIT_APEX_DATA4_TAP_AXIS_MASK (0x03 << BIT_APEX_DATA4_TAP_AXIS_POS)
- #define BIT_APEX_DATA4_TAP_DIR_POS 0
- #define BIT_APEX_DATA4_TAP_DIR_MASK 0x01
- #define BIT_APEX_DATA5_DOUBLE_TAP_TIMING_POS 0
- #define BIT_APEX_DATA5_DOUBLE_TAP_TIMING_MASK (0x3F << BIT_APEX_DATA5_DOUBLE_TAP_TIMING_POS)
- #define BIT_INT_STATUS2_SMD_INT 0x08
- #define BIT_INT_STATUS2_WOM_Z_INT 0x04
- #define BIT_INT_STATUS2_WOM_Y_INT 0x02
- #define BIT_INT_STATUS2_WOM_X_INT 0x01

- #define BIT_INT_STATUS3_STEP_DET 0x20
- #define BIT_INT_STATUS3_STEP_CNT_OVFL 0x10
- #define BIT_INT_STATUS3_TILT_DET 0x08
- #define BIT_INT_STATUS3_WAKE_DET 0x04
- #define BIT_INT_STATUS3_SLEEP_DET 0x02
- #define BIT_INT_STATUS3_TAP_DET 0x01
- #define BIT_SIGNAL_PATH_RESET_DMP_INIT_POS 6
- #define BIT_SIGNAL_PATH_RESET_DMP_INIT_MASK (0x01 << BIT_SIGNAL_PATH_RESET_DMP_INIT_POS)
- #define BIT_SIGNAL_PATH_RESET_DMP_MEM_RESET_POS 5
- #define BIT_SIGNAL_PATH_RESET_DMP_MEM_RESET_MASK (0x01 << BIT_SIGNAL_PATH_RESET_DMP_MEM_RESE
- #define BIT_SIGNAL_PATH_RESET_TMST_STROBE_POS 2
- #define BIT_SIGNAL_PATH_RESET_TMST_STROBE_MASK (0x01 << BIT_SIGNAL_PATH_RESET_TMST_STROBE_POS)
- #define BIT_SIGNAL_PATH_RESET_FIFO_FLUSH_POS 1
- #define BIT_SIGNAL_PATH_RESET_FIFO_FLUSH_MASK (0x01 << BIT_SIGNAL_PATH_RESET_FIFO_FLUSH_POS)
- #define BIT_FIFO_SREG_INVALID_IND_POS 7
- #define BIT_FIFO_SREG_INVALID_IND_MASK (0x01 << BIT_FIFO_SREG_INVALID_IND_POS)
- #define BIT_FIFO_COUNT_REC_POS 6
- #define BIT_FIFO_COUNT_REC_MASK (0x01 << BIT_FIFO_COUNT_REC_POS)
- #define BIT_FIFO_COUNT_ENDIAN_POS 5
- #define BIT_FIFO_COUNT_ENDIAN_MASK (0x01 << BIT_FIFO_COUNT_ENDIAN_POS)
- #define BIT_DATA_ENDIAN_POS 4
- #define BIT_DATA_ENDIAN_MASK (0x01 << BIT_DATA_ENDIAN_POS)
- #define BIT_SPI_MODE_OIS2_POS 3
- #define BIT_SPI_MODE_OIS2_MASK (0x01 << BIT_SPI_MODE_OIS2_POS)
- #define BIT_SPI_MODE_OIS1_POS 2
- #define BIT_SPI_MODE_OIS1_MASK (0x01 << BIT_SPI_MODE_OIS1_POS)
- #define BIT_ACCEL_LP_CLK_SEL_POS 3
- #define BIT_ACCEL_LP_CLK_SEL_MASK (0x01 << BIT_ACCEL_LP_CLK_SEL_POS)
- #define BIT_RTC_MODE_POS 2
- #define BIT_RTC_MODE_MASK (0x01 << BIT_RTC_MODE_POS)
- #define BIT_PWR_MGMT_0_TEMP_POS 5
- #define BIT_PWR_MGMT_0_TEMP_MASK (0x01 << BIT_PWR_MGMT_0_TEMP_POS)
- #define BIT_PWR_MGMT_0_IDLE_POS 4
- #define BIT_PWR_MGMT_0_IDLE_MASK (0x01 << BIT_PWR_MGMT_0_IDLE_POS)
- #define BIT_PWR_MGMT_0_GYRO_MODE_POS 2
- #define BIT_PWR_MGMT_0_GYRO_MODE_MASK (0x03 << BIT_PWR_MGMT_0_GYRO_MODE_POS)
- #define BIT_PWR_MGMT_0_ACCEL_MODE_POS 0
- #define BIT_PWR_MGMT_0_ACCEL_MODE_MASK 0x03
- #define BIT_GYRO_CONFIG0_FS_SEL_POS 5
- #define BIT_GYRO_CONFIG0_FS_SEL_MASK (7 << BIT_GYRO_CONFIG0_FS_SEL_POS)
- #define BIT_GYRO_CONFIG0_ODR_POS 0
- #define BIT_GYRO_CONFIG0_ODR_MASK 0x0F
- #define BIT_ACCEL_CONFIG0_FS_SEL_POS 5
- #define BIT_ACCEL_CONFIG0_FS_SEL_MASK (0x7 << BIT_ACCEL_CONFIG0_FS_SEL_POS)
- #define BIT_ACCEL_CONFIG0_ODR_POS 0
- #define BIT_ACCEL_CONFIG0_ODR_MASK 0x0F
- #define BIT_GYRO_CONFIG1_TEMP_FILT_BW_POS 5
- #define BIT_GYRO_CONFIG1_TEMP_FILT_BW_MASK (0x7 << BIT_GYRO_CONFIG1_TEMP_FILT_BW_POS)
- #define BIT_GYRO_CONFIG1_GYRO_UI_FILT_ORD_POS 2
- #define BIT_GYRO_CONFIG1_GYRO_UI_FILT_ORD_MASK (0x3 << BIT_GYRO_CONFIG1_GYRO_UI_FILT_ORD_POS)
- #define BIT_GYRO_CONFIG1_GYRO_DEC2_M2_ORD_POS 0
- #define BIT_GYRO_CONFIG1_GYRO_DEC2_M2_ORD_MASK 0x3
- #define BIT_GYRO_ACCEL_CONFIG0_ACCEL_FILT_POS 4
- #define BIT_GYRO_ACCEL_CONFIG0_ACCEL_FILT_MASK (0xF << BIT_GYRO_ACCEL_CONFIG0_ACCEL_FILT_POS)
- #define BIT_GYRO_ACCEL_CONFIG0_GYRO_FILT_POS 0

- #define BIT_GYRO_ACCEL_CONFIG0_GYRO_FILT_MASK 0x0F
- #define BIT_ACCEL_CONFIG1_ACCEL_UI_FILT_ORD_POS 3
- #define BIT_ACCEL_CONFIG1_ACCEL_UI_FILT_ORD_MASK (0x3 << BIT_ACCEL_CONFIG1_ACCEL_UI_FILT_ORD_POS
- #define BIT_ACCEL_CONFIG1_ACCEL_DEC2_M2_ORD_POS 1
- #define BIT_ACCEL_CONFIG1_ACCEL_DEC2_M2_ORD_MASK (0x3 << BIT_ACCEL_CONFIG1_ACCEL_DEC2_M2_ORD_
- #define BIT_TMST_CONFIG_TMST_TO_REGS_EN_POS 4
- #define BIT_TMST_CONFIG_TMST_TO_REGS_EN_MASK (0x1 << BIT_TMST_CONFIG_TMST_TO_REGS_EN_POS)
- #define BIT_TMST_CONFIG_RESOL_POS 3
- #define BIT_TMST_CONFIG_RESOL_MASK (0x1 << BIT_TMST_CONFIG_RESOL_POS)
- #define BIT_TMST_CONFIG_TMST_FSYNC_POS 1
- #define BIT_TMST_CONFIG_TMST_FSYNC_MASK (0x1 << BIT_TMST_CONFIG_TMST_FSYNC_POS)
- #define BIT_TMST_CONFIG_TMST_EN_POS 0
- #define BIT_TMST_CONFIG_TMST_EN_MASK 0x1
- #define BIT_APEX_CONFIG0_DMP_POWER_SAVE_POS 7
- #define BIT_APEX_CONFIG0_DMP_POWER_SAVE_MASK (0x1 << BIT_APEX_CONFIG0_DMP_POWER_SAVE_POS)
- #define BIT_APEX_CONFIG0_TAP_ENABLE_POS 6
- #define BIT_APEX_CONFIG0_TAP_ENABLE_MASK (0x1 << BIT_APEX_CONFIG0_TAP_ENABLE_POS)
- #define BIT_APEX_CONFIG0_PEDO_EN_POS 5
- #define BIT_APEX_CONFIG0_PEDO_EN_MASK (0x1 << BIT_APEX_CONFIG0_PEDO_EN_POS)
- #define BIT_APEX_CONFIG0_R2W_EN_POS 3
- #define BIT_APEX_CONFIG0_R2W_EN_MASK (0x1 << BIT_APEX_CONFIG0_R2W_EN_POS)
- #define BIT_APEX_CONFIG0_TILT_EN_POS 4
- #define BIT_APEX_CONFIG0_TILT_EN_MASK (0x1 << BIT_APEX_CONFIG0_TILT_EN_POS)
- #define BIT_APEX_CONFIG0_DMP_ODR_POS 0
- #define BIT_APEX_CONFIG0_DMP_ODR_MASK (0x3 << BIT_APEX_CONFIG0_DMP_ODR_POS)
- #define BIT_SMD_CONFIG_WOM_INT_MODE_POS 3
- #define BIT_SMD_CONFIG_WOM_INT_MODE_MASK (0x1 << BIT_SMD_CONFIG_WOM_INT_MODE_POS)
- #define BIT_SMD_CONFIG_WOM_MODE_POS 2
- #define BIT_SMD_CONFIG_WOM_MODE_MASK (0x1 << BIT_SMD_CONFIG_WOM_MODE_POS)
- #define BIT_SMD_CONFIG_SMD_MODE_POS 0
- #define BIT_SMD_CONFIG_SMD_MODE_MASK 0x3
- #define BIT_FIFO_CONFIG1_RESUME_PARTIAL_RD_POS 6
- #define BIT_FIFO_CONFIG1_RESUME_PARTIAL_RD_MASK (0x1 << BIT_FIFO_CONFIG1_RESUME_PARTIAL_RD_POS)
- #define BIT_FIFO_CONFIG1_WM_GT_TH_POS 5
- #define BIT_FIFO_CONFIG1_WM_GT_TH_MASK (0x1 << BIT_FIFO_CONFIG1_WM_GT_TH_POS)
- #define BIT_FIFO_CONFIG1_HIRES_POS 4
- #define BIT_FIFO_CONFIG1_HIRES_MASK (0x1 << BIT_FIFO_CONFIG1_HIRES_POS)
- #define BIT_FIFO_CONFIG1_TMST_FSYNC_POS 3
- #define BIT_FIFO_CONFIG1_TMST_FSYNC_MASK (0x1 << BIT_FIFO_CONFIG1_TMST_FSYNC_POS)
- #define BIT_FIFO_CONFIG1_TEMP_POS 2
- #define BIT_FIFO_CONFIG1_TEMP_MASK (0x1 << BIT_FIFO_CONFIG1_TEMP_POS)
- #define BIT_FIFO_CONFIG1_GYRO_POS 1
- #define BIT_FIFO_CONFIG1_GYRO_MASK (0x1 << BIT_FIFO_CONFIG1_GYRO_POS)
- #define BIT_FIFO_CONFIG1_ACCEL_POS 0
- #define BIT_FIFO_CONFIG1_ACCEL_MASK 0x1
- #define BIT_FSYNC_CONFIG_UI_SEL_POS 4
- #define BIT_FSYNC_CONFIG_UI_SEL_MASK (0x7 << BIT_FSYNC_CONFIG_UI_SEL_POS)
- #define BIT_INT_TPULSE_DURATION_POS 6
- #define BIT_INT_TPULSE_DURATION_MASK (0x1 << BIT_INT_TPULSE_DURATION_POS)
- #define BIT_INT_TDEASSERT_POS 5
- #define BIT_INT_TDEASSERT_MASK (0x1 << BIT_INT_TDEASSERT_POS)
- #define BIT_INT_CONFIG1_ASY_RST_POS 4
- #define BIT_INT_CONFIG1_ASY_RST_MASK (0x1 << BIT_INT_CONFIG1_ASY_RST_POS)
- #define BIT_INT_UI_FSYNC_INT_EN_POS 6
- #define BIT_INT_PLL_RDY_INT_EN_POS 5

- #define BIT_INT_RESET_DONE_INT_EN_POS 4
- #define BIT_INT_UI_DRDY_INT_EN_POS 3
- #define BIT_INT_FIFO_THS_INT_EN_POS 2
- #define BIT_INT_FIFO_FULL_INT_EN_POS 1
- #define BIT_INT_UI_AGC_RDY_INT_EN_POS 0
- #define BIT_INT_SOURCE0_UI_FSYNC_INT1_EN 0x40
- #define BIT_INT_SOURCE0_PLL_RDY_INT1_EN 0x20
- #define BIT_INT_SOURCE0_RESET_DONE_INT1_EN 0x10
- #define BIT_INT_SOURCE0_UI_DRDY_INT1_EN 0x08
- #define BIT_INT_SOURCE0_FIFO_THS_INT1_EN 0x04
- #define BIT_INT_SOURCE0_FIFO_FULL_INT1_EN 0x02
- #define BIT_INT_SOURCE0_UI_AGC_RDY_INT1_EN 0x01
- #define BIT_INT_SMD_INT_EN_POS 3
- #define BIT_INT_WOM_Z_INT_EN_POS 2
- #define BIT_INT_WOM_Y_INT_EN_POS 1
- #define BIT_INT_WOM_X_INT_EN_POS 0
- #define BIT_INT_SOURCE1_SMD_INT1_EN 0x08
- #define BIT_INT_SOURCE1_WOM_Z_INT1_EN 0x04
- #define BIT_INT_SOURCE1_WOM_Y_INT1_EN 0x02
- #define BIT_INT_SOURCE1_WOM_X_INT1_EN 0x01
- #define BIT_INT_SOURCE2_OIS2_AGC_RDY_INT1_EN 0x20
- #define BIT_INT_SOURCE2_OIS2_FSYNC_INT1_EN 0x10
- #define BIT_INT_SOURCE2_OIS2_DRDY_INT1_EN 0x08
- #define BIT_INT_SOURCE2_OIS1_AGC_RDY_INT1_EN 0x04
- #define BIT_INT_SOURCE2_OIS1_FSYNC_INT1_EN 0x02
- #define BIT_INT_SOURCE2_OIS1_DRDY_INT1_EN 0x01
- #define BIT_INT_SOURCE3_UI_FSYNC_INT2_EN 0x40
- #define BIT_INT_SOURCE3_PLL_RDY_INT2_EN 0x20
- #define BIT_INT_SOURCE3_RESET_DONE_INT2_EN 0x10
- #define BIT_INT_SOURCE3_UI_DRDY_INT2_EN 0x08
- #define BIT_INT_SOURCE3_FIFO_THS_INT2_EN 0x04
- #define BIT_INT_SOURCE3_FIFO_FULL_INT2_EN 0x02
- #define BIT_INT_SOURCE3_UI_AGC_RDY_INT2_EN 0x01
- #define BIT_INT_SOURCE4_SMD_INT2_EN 0x08
- #define BIT_INT_SOURCE4_WOM_Z_INT2_EN 0x04
- #define BIT_INT_SOURCE4_WOM_Y_INT2_EN 0x02
- #define BIT_INT_SOURCE4_WOM_X_INT2_EN 0x01
- #define BIT_INT_SOURCE5_OIS2_AGC_RDY_INT2_EN 0x20
- #define BIT_INT_SOURCE5_OIS2_FSYNC_INT2_EN 0x10
- #define BIT_INT_SOURCE5_OIS2_DRDY_INT2_EN 0x08
- #define BIT_INT_SOURCE5_OIS1_AGC_RDY_INT2_EN 0x04
- #define BIT_INT_SOURCE5_OIS1_FSYNC_INT2_EN 0x02
- #define BIT_INT_SOURCE5_OIS1_DRDY_INT2_EN 0x01
- #define BIT_ST_REGULATOR_EN 0x40
- #define BIT_ACCEL_Z_ST_EN 0x20
- #define BIT_ACCEL_Y_ST_EN 0x10
- #define BIT_ACCEL_X_ST_EN 0x08
- #define BIT_GYRO_Z_ST_EN 0x04
- #define BIT_GYRO_Y_ST_EN 0x02
- #define BIT_GYRO_X_ST_EN 0x01
- #define BIT_DMP_MEM_ACCESS_EN 0x08
- #define BIT_MEM_OTP_ACCESS_EN 0x04
- #define BIT_FIFO_MEM_RD_SYS 0x02
- #define BIT_FIFO_MEM_WR_SER 0x01
- #define BIT_SENSOR_CONFIG2_OIS_MODE_POS 4

- #define BIT_SENSOR_CONFIG2_OIS_MODE_MASK (0x03 << BIT_SENSOR_CONFIG2_OIS_MODE_POS)
- #define BIT_GYRO_AAF_DIS_POS 1
- #define BIT_GYRO_AAF_DIS_MASK (0x01 << BIT_GYRO_AAF_DIS_POS)
- #define BIT_GYRO_NF_DIS_POS 0
- #define BIT_GYRO_NF_DIS_MASK (0x01 << BIT_GYRO_NF_DIS_POS)
- #define BIT_GYRO_AAF_DELT_POS 0
- #define BIT_GYRO_AAF_DELT_MASK (0x3F << BIT_GYRO_AAF_DELT_POS)
- #define BIT_GYRO_AAF_DELTSQR_POS_LO 0
- #define BIT_GYRO_AAF_DELTSQR_MASK_LO (0xFF << BIT_GYRO_AAF_DELTSQR_POS_LO)
- #define BIT_GYRO_AAF_DELTSQR_POS_HI 0
- #define BIT_GYRO_AAF_DELTSQR_MASK_HI (0x0F << BIT_GYRO_AAF_DELTSQR_POS_HI)
- #define BIT_GYRO_AAF_BITSHIFT_POS 4
- #define BIT_GYRO_AAF_BITSHIFT_MASK (0x0F << BIT_GYRO_AAF_BITSHIFT_POS)
- #define BIT_INTF_CONFIG4_AP_SPI_POS 1
- #define BIT_INTF_CONFIG4_AP_SPI_MASK (0x1 << BIT_INTF_CONFIG4_AP_SPI_POS)
- #define BIT_INTF_CONFIG4_AUX1_SPI_POS 2
- #define BIT_INTF_CONFIG4_AUX1_SPI_MASK (0x1 << BIT_INTF_CONFIG4_AUX1_SPI_POS)
- #define BIT_INTF_CONFIG5_GPIO_PAD_SEL_POS 1
- #define BIT_INTF_CONFIG5_GPIO_PAD_SEL_MASK (0x3 << BIT_INTF_CONFIG5_GPIO_PAD_SEL_POS)
- #define BIT_INTF_CONFIG6_I3C_DDR_EN_POS 1
- #define BIT_INTF_CONFIG6_I3C_DDR_EN_MASK (0x1 << BIT_INTF_CONFIG6_I3C_DDR_EN_POS)
- #define BIT_INTF_CONFIG6_I3C_SDR_EN_POS 0
- #define BIT_INTF_CONFIG6_I3C_SDR_EN_MASK (0x1 << BIT_INTF_CONFIG6_I3C_SDR_EN_POS)
- #define BIT_INTF_CONFIG6_I3C_IBI_BYTE_EN_POS 3
- #define BIT_INTF_CONFIG6_I3C_IBI_BYTE_EN_MASK (0x1 << BIT_INTF_CONFIG6_I3C_IBI_BYTE_EN_POS)
- #define BIT_INTF_CONFIG6_I3C_IBI_EN_POS 2
- #define BIT_INTF_CONFIG6_I3C_IBI_EN_MASK (0x1 << BIT_INTF_CONFIG6_I3C_IBI_EN_POS)
- #define BIT_ACCEL_AAF_DIS_POS 0
- #define BIT_ACCEL_AAF_DIS_MASK (0x01 << BIT_ACCEL_AAF_DIS_POS)
- #define BIT_ACCEL_AAF_DELT_POS 1
- #define BIT_ACCEL_AAF_DELT_MASK (0x3F << BIT_ACCEL_AAF_DELT_POS)
- #define BIT_ACCEL_AAF_DELTSQR_POS_LO 0
- #define BIT_ACCEL_AAF_DELTSQR_MASK_LO (0xFF << BIT_ACCEL_AAF_DELTSQR_POS_LO)
- #define BIT_ACCEL_AAF_DELTSQR_POS_HI 0
- #define BIT_ACCEL_AAF_DELTSQR_MASK_HI (0x0F << BIT_ACCEL_AAF_DELTSQR_POS_HI)
- #define BIT_ACCEL_AAF_BITSHIFT_POS 4
- #define BIT_ACCEL_AAF_BITSHIFT_MASK (0x0F << BIT_ACCEL_AAF_BITSHIFT_POS)
- #define BIT_OIS1_CONFIG1_ACCEL_LP_CLK_SEL_POS 5
- #define BIT_OIS1_CONFIG1_ACCEL_LP_CLK_SEL_MASK (0x1 << BIT_OIS1_CONFIG1_ACCEL_LP_CLK_SEL_POS)
- #define BIT_OIS1_CONFIG1_DEC_POS 2
- #define BIT_OIS1_CONFIG1_DEC_MASK (0x7 << BIT_OIS1_CONFIG1_DEC_POS)
- #define BIT_OIS1_CONFIG1_GYRO_EN_POS 1
- #define BIT_OIS1_CONFIG1_GYRO_EN_MASK (0x1 << BIT_OIS1_CONFIG1_GYRO_EN_POS)
- #define BIT_OIS1_CONFIG1_ACCEL_EN_POS 0
- #define BIT_OIS1_CONFIG1_ACCEL_EN_MASK (0x1 << BIT_OIS1_CONFIG1_ACCEL_EN_POS)
- #define BIT_OIS1_CONFIG2_GYRO_FS_SEL_POS 3
- #define BIT_OIS1_CONFIG2_GYRO_FS_SEL_MASK (0x7 << BIT_OIS1_CONFIG2_GYRO_FS_SEL_POS)
- #define BIT_OIS1_CONFIG2_ACCEL_FS_SEL_POS 0
- #define BIT_OIS1_CONFIG2_ACCEL_FS_SEL_MASK (0x7 << BIT_OIS1_CONFIG2_ACCEL_FS_SEL_POS)
- #define BIT_INT_STATUS_OIS1_FSYNC 0x04
- #define BIT_INT_STATUS_OIS1_DRDY 0x02
- #define BIT_INT_STATUS_OIS1_AGC_RDY 0x01
- #define BIT_OIS2_CONFIG1_ACCEL_LP_CLK_SEL_POS 5
- #define BIT_OIS2_CONFIG1_ACCEL_LP_CLK_SEL_MASK (0x1 << BIT_OIS2_CONFIG1_ACCEL_LP_CLK_SEL_POS)
- #define BIT_OIS2_CONFIG1_DEC_POS 2

- #define BIT_OIS2_CONFIG1_DEC_MASK (0x7 << BIT_OIS2_CONFIG1_DEC_POS)
- #define BIT_OIS2_CONFIG1_GYRO_EN_POS 1
- #define BIT_OIS2_CONFIG1_GYRO_EN_MASK (0x1 << BIT_OIS2_CONFIG1_GYRO_EN_POS)
- #define BIT_OIS2_CONFIG1_ACCEL_EN_POS 0
- #define BIT_OIS2_CONFIG1_ACCEL_EN_MASK (0x1 << BIT_OIS2_CONFIG1_ACCEL_EN_POS)
- #define BIT_OIS2_CONFIG2_GYRO_FS_SEL_POS 3
- #define BIT_OIS2_CONFIG2_GYRO_FS_SEL_MASK (0x7 << BIT_OIS2_CONFIG2_GYRO_FS_SEL_POS)
- #define BIT_OIS2_CONFIG2_ACCEL_FS_SEL_POS 0
- #define BIT_OIS2_CONFIG2_ACCEL_FS_SEL_MASK (0x7 << BIT_OIS2_CONFIG2_ACCEL_FS_SEL_POS)
- #define BIT_INT_STATUS_OIS2_FSYNC 0x04
- #define BIT_INT_STATUS_OIS2_DRDY 0x02
- #define BIT_INT_STATUS_OIS2_AGC_RDY 0x01
- #define BIT_FDR_CONFIG_FDR_SEL_POS 0
- #define BIT_FDR_CONFIG_FDR_SEL_MASK 0x7F
- #define BIT_APEX_CONFIG1_DMP_POWER_SAVE_TIME_SEL_POS 0
- #define BIT_APEX_CONFIG1_DMP_POWER_SAVE_TIME_SEL_MASK 0x0F
- #define BIT_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_POS 4
- #define BIT_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_MASK (0x0F << BIT_APEX_CONFIG1_LOW_ENERGY_AM
- #define ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_1006632MG ICM426XX_APEX_CONFIG1_LOW_ENE
- #define ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_1174405MG ICM426XX_APEX_CONFIG1_LOW_ENE
- #define ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_1342177MG ICM426XX_APEX_CONFIG1_LOW_ENE
- #define ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_1509949MG ICM426XX_APEX_CONFIG1_LOW_ENE
- #define ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_1677721MG ICM426XX_APEX_CONFIG1_LOW_ENE
- #define ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_1845493MG ICM426XX_APEX_CONFIG1_LOW_ENE
- #define ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_2013265MG ICM426XX_APEX_CONFIG1_LOW_ENE
- #define ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_2181038MG ICM426XX_APEX_CONFIG1_LOW_ENE
- #define ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_2348810MG ICM426XX_APEX_CONFIG1_LOW_ENE
- #define ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_2516582MG ICM426XX_APEX_CONFIG1_LOW_ENE
- #define ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_2684354MG ICM426XX_APEX_CONFIG1_LOW_ENE
- #define ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_2852126MG ICM426XX_APEX_CONFIG1_LOW_ENE
- #define ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_3019898MG ICM426XX_APEX_CONFIG1_LOW_ENE
- #define ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_3187671MG ICM426XX_APEX_CONFIG1_LOW_ENE
- #define ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_3355443MG ICM426XX_APEX_CONFIG1_LOW_ENE
- #define ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_3523215MG ICM426XX_APEX_CONFIG1_LOW_ENE
- #define BIT_APEX_CONFIG2_PEDO_AMP_TH_POS 4
- #define BIT_APEX_CONFIG2_PEDO_AMP_TH_MASK (0x0F << BIT_APEX_CONFIG2_PEDO_AMP_TH_POS)
- #define ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_1006632_MG ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_30MG
- #define ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_1140850_MG ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_34MG
- #define ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_1275068_MG ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_38MG
- #define ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_1409286_MG ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_42MG
- #define ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_1543503_MG ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_46MG
- #define ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_1677721_MG ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_50MG
- #define ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_1811939_MG ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_54MG
- #define ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_1946157_MG ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_58MG
- #define ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_2080374_MG ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_62MG
- #define ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_2214592_MG ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_66MG
- #define ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_2348810_MG ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_70MG
- #define ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_2483027_MG ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_74MG
- #define ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_2617245_MG ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_78MG
- #define ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_2751463_MG ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_82MG
- #define ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_2885681_MG ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_86MG
- #define ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_3019898_MG ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_90MG
- #define BIT_APEX_CONFIG2_PEDO_STEP_CNT_TH_POS 0
- #define BIT_APEX_CONFIG2_PEDO_STEP_CNT_TH_MASK 0x0F
- #define BIT_APEX_CONFIG3_PEDO_STEP_DET_TH_POS 5

- #define BIT_APEX_CONFIG3_PEDO_STEP_DET_TH_MASK (0x07 << BIT_APEX_CONFIG3_PEDO_STEP_DET_TH_POS
- #define BIT_APEX_CONFIG3_PEDO_SB_TIMER_TH_POS 2
- #define BIT_APEX_CONFIG3_PEDO_SB_TIMER_TH_MASK (0x07 << BIT_APEX_CONFIG3_PEDO_SB_TIMER_TH_POS
- #define BIT_APEX_CONFIG3_PEDO_HI_ENRGY_TH_POS 0
- #define BIT_APEX_CONFIG3_PEDO_HI_ENRGY_TH_MASK 0x03
- #define BIT_APEX_CONFIG4_TILT_WAIT_TIME_POS 6
- #define BIT_APEX_CONFIG4_TILT_WAIT_TIME_MASK (0x03 << BIT_APEX_CONFIG4_TILT_WAIT_TIME_POS)
- #define BIT_APEX_CONFIG4_R2W_SLEEP_TIME_OUT_POS 3
- #define BIT_APEX_CONFIG4_R2W_SLEEP_TIME_OUT_MASK (0x07 << BIT_APEX_CONFIG4_R2W_SLEEP_TIME_OUT
- #define BIT_APEX_CONFIG5_R2W_MOUNTING_MATRIX_POS 0
- #define BIT_APEX_CONFIG5_R2W_MOUNTING_MATRIX_MASK (0x07 << BIT_APEX_CONFIG5_R2W_MOUNTING_MAT
- #define BIT_APEX_CONFIG6_R2W_SLEEP_GEST_DELAY_POS 0
- #define BIT_APEX_CONFIG6_R2W_SLEEP_GEST_DELAY_MASK (0x07 << BIT_APEX_CONFIG6_R2W_SLEEP_GEST_D
- #define BIT_APEX_CONFIG7_TAP_MIN_JERK_THR_POS 2
- #define BIT_APEX_CONFIG7_TAP_MIN_JERK_THR_MASK (0x3F << BIT_APEX_CONFIG7_TAP_MIN_JERK_THR_POS)
- #define ICM426XX_APEX_CONFIG7_TAP_MIN_JERK_THR_281MG_DEFAULT 0x11
- #define BIT_APEX_CONFIG7_TAP_MAX_PEAK_TOL_POS 0
- #define BIT_APEX_CONFIG7_TAP_MAX_PEAK_TOL_MASK 0x3
- #define BIT_APEX_CONFIG8_TAP_TMAX_POS 5
- #define BIT_APEX_CONFIG8_TAP_TMAX_MASK (0x03 << BIT_APEX_CONFIG8_TAP_TMAX_POS)
- #define BIT_APEX_CONFIG8_TAP_TAVG_POS 3
- #define BIT_APEX_CONFIG8_TAP_TAVG_MASK (0x03 << BIT_APEX_CONFIG8_TAP_TAVG_POS)
- #define BIT_APEX_CONFIG8_TAP_TMIN_POS 0
- #define BIT_APEX_CONFIG8_TAP_TMIN_MASK 0x07
- #define BIT_APEX_CONFIG9_SENSITIVITY_MODE_POS 0
- #define BIT_APEX_CONFIG9_SENSITIVITY_MODE_MASK 0x01
- #define BIT_INT_STEP_DET_INT_EN_POS 5
- #define BIT_INT_STEP_CNT_OVFL_INT_EN_POS 4
- #define BIT_INT_TILT_DET_INT_EN_POS 3
- #define BIT_INT_WAKE_DET_INT_EN_POS 2
- #define BIT_INT_SLEEP_DET_INT_EN_POS 1
- #define BIT_INT_TAP_DET_INT_EN_POS 0
- #define BIT_INT_SOURCE6_STEP_DET_INT1_EN 0x20
- #define BIT_INT_SOURCE6_STEP_CNT_OVFL_INT1_EN 0x10
- #define BIT_INT_SOURCE6_TILT_DET_INT1_EN 0x8
- #define BIT_INT_SOURCE6_WAKE_DET_INT1_EN 0x4
- #define BIT_INT_SOURCE6_SLEEP_DET_INT1_EN 0x2
- #define BIT_INT_SOURCE6_TAP_DET_INT1_EN 0x1
- #define BIT_INT_SOURCE7_STEP_DET_INT2_EN 0x20
- #define BIT_INT_SOURCE7_STEP_CNT_OVFL_INT2_EN 0x10
- #define BIT_INT_SOURCE7_TILT_DET_INT2_EN 0x8
- #define BIT_INT_SOURCE7_WAKE_DET_INT2_EN 0x4
- #define BIT_INT_SOURCE7_SLEEP_DET_INT2_EN 0x2
- #define BIT_INT_SOURCE7_TAP_DET_INT2_EN 0x1
- #define BIT_INT_OIS1_DRDY_IBI_EN_POS 6
- #define BIT_INT_UI_FSYNC_IBI_EN_POS 5
- #define BIT_INT_PLL_RDY_IBI_EN_POS 4
- #define BIT_INT_UI_DRDY_IBI_EN_POS 3
- #define BIT_INT_FIFO_THS_IBI_EN_POS 2
- #define BIT_INT_FIFO_FULL_IBI_EN_POS 1
- #define BIT_INT_UI_AGC_RDY_IBI_EN_POS 0
- #define BIT_INT_SOURCE8_OIS1_DRDY_IBI_EN 0x40
- #define BIT_INT_SOURCE8_UI_FSYNC_IBI_EN 0x20
- #define BIT_INT_SOURCE8_PLL_RDY_IBI_EN 0x10
- #define BIT_INT_SOURCE8_UI_DRDY_IBI_EN 0x08

- #define BIT_INT_SOURCE8_FIFO_THS_IBI_EN 0x04
- #define BIT_INT_SOURCE8_FIFO_FULL_IBI_EN 0x02
- #define BIT_INT_SOURCE8_UI_AGC_RDY_IBI_EN 0x01
- #define BIT_INT_SMD_IBI_EN_POS 4
- #define BIT_INT_WOM_Z_IBI_EN_POS 3
- #define BIT_INT_WOM_Y_IBI_EN_POS 2
- #define BIT_INT_WOM_X_IBI_EN_POS 1
- #define BIT_INT_SOURCE9_SMD_IBI_EN 0x10
- #define BIT_INT_SOURCE9_WOM_Z_IBI_EN 0x08
- #define BIT_INT_SOURCE9_WOM_Y_IBI_EN 0x04
- #define BIT_INT_SOURCE9_WOM_X_IBI_EN 0x02
- #define BIT_INT_STEP_DET_IBI_EN_POS 5
- #define BIT_INT_STEP_CNT_OVFL_IBI_EN_POS 4
- #define BIT_INT_TILT_DET_IBI_EN_POS 3
- #define BIT_INT_WAKE_DET_IBI_EN_POS 2
- #define BIT_INT_SLEEP_DET_IBI_EN_POS 1
- #define BIT_INT_TAP_DET_IBI_EN_POS 0
- #define BIT_INT_SOURCE10_STEP_DET_IBI_EN 0x20
- #define BIT_INT_SOURCE10_STEP_CNT_OVFL_IBI_EN 0x10
- #define BIT_INT_SOURCE10_TILT_DET_IBI_EN 0x08
- #define BIT_INT_SOURCE10_WAKE_DET_IBI_EN 0x04
- #define BIT_INT_SOURCE10_SLEEP_DET_IBI_EN 0x02
- #define BIT_INT_SOURCE10_TAP_DET_IBI_EN 0x01
- #define BIT_GYRO_X_OFFUSER_POS_LO 0
- #define BIT_GYRO_X_OFFUSER_MASK_LO (0xFF << BIT_GYRO_X_OFFUSER_POS_LO)
- #define BIT_GYRO_X_OFFUSER_POS_HI 0
- #define BIT_GYRO_X_OFFUSER_MASK_HI (0x0F << BIT_GYRO_X_OFFUSER_POS_HI)
- #define BIT_GYRO_Y_OFFUSER_POS_HI 4
- #define BIT_GYRO_Y_OFFUSER_MASK_HI (0x0F << BIT_GYRO_Y_OFFUSER_POS_HI)
- #define BIT_GYRO_Y_OFFUSER_POS_LO 0
- #define BIT_GYRO_Y_OFFUSER_MASK_LO (0xFF << BIT_GYRO_Y_OFFUSER_POS_LO)
- #define BIT_GYRO_Z_OFFUSER_POS_LO 0
- #define BIT_GYRO_Z_OFFUSER_MASK_LO (0xFF << BIT_GYRO_Z_OFFUSER_POS_LO)
- #define BIT_GYRO_Z_OFFUSER_POS_HI 0
- #define BIT_GYRO_Z_OFFUSER_MASK_HI (0x0F << BIT_GYRO_Z_OFFUSER_POS_HI)
- #define BIT_ACCEL_X_OFFUSER_POS_HI 4
- #define BIT_ACCEL_X_OFFUSER_MASK_HI (0x0F << BIT_ACCEL_X_OFFUSER_POS_HI)
- #define BIT_ACCEL_X_OFFUSER_POS_LO 0
- #define BIT_ACCEL_X_OFFUSER_MASK_LO (0xFF << BIT_ACCEL_X_OFFUSER_POS_LO)
- #define BIT_ACCEL_Y_OFFUSER_POS_LO 0
- #define BIT_ACCEL_Y_OFFUSER_MASK_LO (0xFF << BIT_ACCEL_Y_OFFUSER_POS_LO)
- #define BIT_ACCEL_Y_OFFUSER_POS_HI 0
- #define BIT_ACCEL_Y_OFFUSER_MASK_HI (0x0F << BIT_ACCEL_Y_OFFUSER_POS_HI)
- #define BIT_ACCEL_Z_OFFUSER_POS_HI 4
- #define BIT_ACCEL_Z_OFFUSER_MASK_HI (0x0F << BIT_ACCEL_Z_OFFUSER_POS_HI)
- #define BIT_ACCEL_Z_OFFUSER_POS_LO 0
- #define BIT_ACCEL_Z_OFFUSER_MASK_LO (0xFF << BIT_ACCEL_Z_OFFUSER_POS_LO)

Enumerations

- enum ICM426XX_DEVICE_CONFIG_SPI_MODE_t { ICM426XX_DEVICE_CONFIG_SPI_MODE_1_2 = (0x1 << BIT_DEVICE_CONFIG_SPI_MODE_POS) , ICM426XX_DEVICE_CONFIG_SPI_MODE_0_3 = (0x0 << BIT_DEVICE_CONFIG_SPI_MODE_POS) }
- enum ICM426XX_CHIP_CONFIG_SPI_MODE_t { ICM426XX_CHIP_CONFIG_SPI_MODE_1_2 = (0x1 << BIT_CHIP_CONFIG_SPI_MODE_POS) , ICM426XX_CHIP_CONFIG_SPI_MODE_0_3 = (0x0 << BIT_CHIP_CONFIG_SPI_MODE_POS) }
- enum ICM426XX_DEVICE_CONFIG_RESET_t { ICM426XX_DEVICE_CONFIG_RESET_EN = 0x01 , ICM426XX_DEVICE_CONFIG_RESET_NONE = 0x00 }
- enum ICM426XX_CHIP_CONFIG_RESET_t { ICM426XX_CHIP_CONFIG_RESET_EN = 0x01 , ICM426XX_CHIP_CONFIG_R = 0x00 }
- enum ICM426XX_INT_CONFIG_INT2_DRIVE_CIRCUIT_t { ICM426XX_INT_CONFIG_INT2_DRIVE_CIRCUIT_PP = (0x01 << BIT_INT_CONFIG_INT2_DRIVE_CIRCUIT_POS) , ICM426XX_INT_CONFIG_INT2_DRIVE_CIRCUIT_OD = (0x00 << BIT_INT_CONFIG_INT2_DRIVE_CIRCUIT_POS) }
- enum ICM426XX_INT_CONFIG_INT2_POLARITY_t { ICM426XX_INT_CONFIG_INT2_POLARITY_HIGH = (0x01 << BIT_INT_CONFIG_INT2_POLARITY_POS) , ICM426XX_INT_CONFIG_INT2_POLARITY_LOW = (0x00 << BIT_INT_CONFIG_INT2_POLARITY_POS) }
- enum ICM426XX_INT_CONFIG_INT1_DRIVE_CIRCUIT_t { ICM426XX_INT_CONFIG_INT1_DRIVE_CIRCUIT_PP = (0x01 << BIT_INT_CONFIG_INT1_DRIVE_CIRCUIT_POS) , ICM426XX_INT_CONFIG_INT1_DRIVE_CIRCUIT_OD = (0x00 << BIT_INT_CONFIG_INT1_DRIVE_CIRCUIT_POS) }
- enum ICM426XX_INT_CONFIG_INT1_POLARITY_t { ICM426XX_INT_CONFIG_INT1_POLARITY_HIGH = 0x01 , ICM426XX_INT_CONFIG_INT1_POLARITY_LOW = 0x00 }
- enum ICM426XX_FIFO_CONFIG_MODE_t { ICM426XX_FIFO_CONFIG_MODE_STOP_ON_FULL = (0x02 << BIT_FIFO_CONFIG_MODE_POS) , ICM426XX_FIFO_CONFIG_MODE_STREAM = (0x01 << BIT_FIFO_CONFIG_MODE_POS) , ICM426XX_FIFO_CONFIG_MODE_BYPASS = (0x00 << BIT_FIFO_CONFIG_MODE_POS) }
- enum ICM426XX_APEX_DATA3_ACTIVITY_CLASS_t { ICM426XX_APEX_DATA3_ACTIVITY_CLASS_OTHER = 0x0 , ICM426XX_APEX_DATA3_ACTIVITY_CLASS_WALK = 0x1 , ICM426XX_APEX_DATA3_ACTIVITY_CLASS_RUN = 0x2 }
- enum ICM426XX_APEX_DATA3_DMP_IDLE_OFF_t { ICM426XX_APEX_DATA3_DMP_IDLE_ON = (0x01 << BIT_APEX_DATA3_DMP_IDLE_POS) , ICM426XX_APEX_DATA3_DMP_IDLE_OFF = (0x00 << BIT_APEX_DATA3_DMP_IDLE_POS) }
- enum ICM426XX_APEX_DATA4_TAP_NUM_t { ICM426XX_APEX_DATA4_TAP_NUM_DOUBLE = (0x02 << BIT_APEX_DATA4_TAP_NUM_POS) , ICM426XX_APEX_DATA4_TAP_NUM_SINGLE = (0x01 << BIT_APEX_DATA4_TAP_NUM_POS) }
- enum ICM426XX_APEX_DATA4_TAP_AXIS_t { ICM426XX_APEX_DATA4_TAP_AXIS_Z = (0x02 << BIT_APEX_DATA4_TAP_AXIS_POS) , ICM426XX_APEX_DATA4_TAP_AXIS_Y = (0x01 << BIT_APEX_DATA4_TAP_AXIS_POS) , ICM426XX_APEX_DATA4_TAP_AXIS_X = (0x00 << BIT_APEX_DATA4_TAP_AXIS_POS) }
- enum ICM426XX_APEX_DATA4_TAP_DIR_t { ICM426XX_APEX_DATA4_TAP_DIR_POSITIVE = (0x01 << BIT_APEX_DATA4_TAP_DIR_POS) , ICM426XX_APEX_DATA4_TAP_DIR_NEGATIVE = (0x00 << BIT_APEX_DATA4_TAP_DIR_POS) }
- enum ICM426XX_SIGNAL_PATH_RESET_DMP_INIT_t { ICM426XX_SIGNAL_PATH_RESET_DMP_INIT_EN = (0x01 << BIT_SIGNAL_PATH_RESET_DMP_INIT_POS) , ICM426XX_SIGNAL_PATH_RESET_DMP_INIT_DIS = (0x00 << BIT_SIGNAL_PATH_RESET_DMP_INIT_POS) }
- enum ICM426XX_SIGNAL_PATH_RESET_DMP_MEM_RESET_t { ICM426XX_SIGNAL_PATH_RESET_DMP_MEM_RESET_ = (0x01 << BIT_SIGNAL_PATH_RESET_DMP_MEM_RESET_POS) , ICM426XX_SIGNAL_PATH_RESET_DMP_MEM_RES }
- enum ICM426XX_SIGNAL_PATH_RESET_TMST_STROBE_t { ICM426XX_SIGNAL_PATH_RESET_TMST_STROBE_EN = (0x01 << BIT_SIGNAL_PATH_RESET_TMST_STROBE_POS) , ICM426XX_SIGNAL_PATH_RESET_TMST_STROBE_DIS = (0x00 << BIT_SIGNAL_PATH_RESET_TMST_STROBE_POS) }
- enum ICM426XX_SIGNAL_PATH_RESET_FIFO_FLUSH_t { ICM426XX_SIGNAL_PATH_RESET_FIFO_FLUSH_EN = (0x01 << BIT_SIGNAL_PATH_RESET_FIFO_FLUSH_POS) , ICM426XX_SIGNAL_PATH_RESET_FIFO_FLUSH_DIS = (0x00 << BIT_SIGNAL_PATH_RESET_FIFO_FLUSH_POS) }
- enum ICM426XX_INTF_CONFIG0_FIFO_SREG_INVALID_IND_t { ICM426XX_INTF_CONFIG0_FIFO_SREG_INVALID_IND_ = (0x01 << BIT_FIFO_SREG_INVALID_IND_POS) , ICM426XX_INTF_CONFIG0_FIFO_SREG_INVALID_IND_EN = (0x00 << BIT_FIFO_SREG_INVALID_IND_POS) }

- enum ICM426XX_INTF_CONFIG0_FIFO_COUNT_REC_t { ICM426XX_INTF_CONFIG0_FIFO_COUNT_REC_RECORD = (0x01 << BIT_FIFO_COUNT_REC_POS) , ICM426XX_INTF_CONFIG0_FIFO_COUNT_REC_BYTE = (0x00 << BIT_FIFO_COUNT_REC_POS) }
- enum ICM426XX_INTF_CONFIG0_FIFO_COUNT_ENDIAN_t { ICM426XX_INTF_CONFIG0_FIFO_COUNT_BIG_ENDIAN = (0x01 << BIT_FIFO_COUNT_ENDIAN_POS) , ICM426XX_INTF_CONFIG0_FIFO_COUNT_LITTLE_ENDIAN = (0x00 << BIT_FIFO_COUNT_ENDIAN_POS) }
- enum ICM426XX_INTF_CONFIG0_DATA_ENDIAN_t { ICM426XX_INTF_CONFIG0_DATA_BIG_ENDIAN = (0x01 << BIT_DATA_ENDIAN_POS) , ICM426XX_INTF_CONFIG0_DATA_LITTLE_ENDIAN = (0x00 << BIT_DATA_ENDIAN_POS) }
- enum ICM426XX_INTF_CONFIG0_SPI_MODE_OIS2_t { ICM426XX_INTF_CONFIG0_SPI_MODE_OIS2_1_2 = (0x01 << BIT_SPI_MODE_OIS2_POS) , ICM426XX_INTF_CONFIG0_SPI_MODE_OIS2_0_3 = (0x00 << BIT_SPI_MODE_OIS2_POS) }
- enum ICM426XX_INTF_CONFIG0_SPI_MODE_OIS1_t { ICM426XX_INTF_CONFIG0_SPI_MODE_OIS1_1_2 = (0x01 << BIT_SPI_MODE_OIS1_POS) , ICM426XX_INTF_CONFIG0_SPI_MODE_OIS1_0_3 = (0x00 << BIT_SPI_MODE_OIS1_POS) }
- enum ICM426XX_INTF_CONFIG1_ACCEL_LP_CLK_t { ICM426XX_INTF_CONFIG1_ACCEL_LP_CLK_WUOSC = (0x00 << BIT_ACCEL_LP_CLK_SEL_POS) , ICM426XX_INTF_CONFIG1_ACCEL_LP_CLK_RCOSC = (0x01 << BIT_ACCEL_LP_CLK_SEL_POS) }
- enum ICM426XX_INTF_CONFIG1_RTC_MODE_t { ICM426XX_INTF_CONFIG1_RTC_MODE_DIS = (0x00 << BIT_RTC_MODE_POS) , ICM426XX_INTF_CONFIG1_RTC_MODE_EN = (0x01 << BIT_RTC_↩ MODE_POS) }
- enum ICM426XX_PWR_MGMT_0_TEMP_t { ICM426XX_PWR_MGMT_0_TEMP_DIS = (0x01 << BIT_↩ PWR_MGMT_0_TEMP_POS) , ICM426XX_PWR_MGMT_0_TEMP_EN = (0x00 << BIT_PWR_MGMT_↩ 0_TEMP_POS) }
- enum ICM426XX_PWR_MGMT_0_IDLE_t { ICM426XX_PWR_MGMT_0_IDLE_DIS = (0x01 << BIT_↩ PWR_MGMT_0_IDLE_POS) , ICM426XX_PWR_MGMT_0_IDLE_EN = (0x00 << BIT_PWR_MGMT_0↩ _IDLE_POS) }
- enum ICM426XX_PWR_MGMT_0_GYRO_MODE_t { ICM426XX_PWR_MGMT_0_GYRO_MODE_LN = (0x03 << BIT_PWR_MGMT_0_GYRO_MODE_POS) , ICM426XX_PWR_MGMT_0_GYRO_MODE_STANDBY = (0x01 << BIT_PWR_MGMT_0_GYRO_MODE_POS) , ICM426XX_PWR_MGMT_0_GYRO_MODE_OFF = (0x00 << BIT_PWR_MGMT_0_GYRO_MODE_POS) }
- enum ICM426XX_PWR_MGMT_0_ACCEL_MODE_t { ICM426XX_PWR_MGMT_0_ACCEL_MODE_LN = 0x03 , ICM426XX_PWR_MGMT_0_ACCEL_MODE_LP = 0x02 , ICM426XX_PWR_MGMT_0_ACCEL_MODE_OFF = 0x00 }
- enum ICM426XX_GYRO_CONFIG0_FS_SEL_t { ICM426XX_GYRO_CONFIG0_FS_SEL_16dps = (7 << BIT_GYRO_CONFIG0_FS_SEL_POS) , ICM426XX_GYRO_CONFIG0_FS_SEL_31dps = (6 << BIT_GYRO_CONFIG0_FS_SEL_POS) , ICM426XX_GYRO_CONFIG0_FS_SEL_62dps = (5 << BIT_GYRO_CONFIG0_FS_SEL_POS) , ICM426XX_GYRO_CONFIG0_FS_SEL_125dps = (4 << BIT_GYRO_CONFIG0_FS_SEL_POS) , ICM426XX_GYRO_CONFIG0_FS_SEL_250dps = (3 << BIT_GYRO_CONFIG0_FS_SEL_POS) , ICM426XX_GYRO_CONFIG0_FS_SEL_500dps = (2 << BIT_GYRO_CONFIG0_FS_SEL_POS) , ICM426XX_GYRO_CONFIG0_FS_SEL_1000dps = (1 << BIT_GYRO_CONFIG0_FS_SEL_POS) , ICM426XX_GYRO_CONFIG0_FS_SEL_2000dps = (0 << BIT_GYRO_CONFIG0_FS_SEL_POS) }

  Gyroscope FSR selection.
- enum ICM426XX_GYRO_CONFIG0_ODR_t { ICM426XX_GYRO_CONFIG0_ODR_500_HZ = 0x0F , ICM426XX_GYRO_CONFIG0_ODR_12_5_HZ = 0x0B , ICM426XX_GYRO_CONFIG0_ODR_25_HZ = 0x0A , ICM426XX_GYRO_CONFIG0_ODR_50_HZ = 0x09 , ICM426XX_GYRO_CONFIG0_ODR_100_HZ = 0x08 , ICM426XX_GYRO_CONFIG0_ODR_200_HZ = 0x07 , ICM426XX_GYRO_CONFIG0_ODR_1_KHZ = 0x06 , ICM426XX_GYRO_CONFIG0_ODR_2_KHZ = 0x05 , ICM426XX_GYRO_CONFIG0_ODR_4_KHZ = 0x04 , ICM426XX_GYRO_CONFIG0_ODR_8_KHZ = 0x03 , ICM426XX_GYRO_CONFIG0_ODR_16_KHZ = 0x02 , ICM426XX_GYRO_CONFIG0_ODR_32_KHZ = 0x01 }

  Gyroscope ODR selection.

- enum ICM426XX_ACCEL_CONFIG0_FS_SEL_t { ICM426XX_ACCEL_CONFIG0_FS_SEL_RESERVED = (0x4 << BIT_ACCEL_CONFIG0_FS_SEL_POS) , ICM426XX_ACCEL_CONFIG0_FS_SEL_2g = (0x3 << BIT_ACCEL_CONFIG0_FS_SEL_POS) , ICM426XX_ACCEL_CONFIG0_FS_SEL_4g = (0x2 << BIT_ACCEL_CONFIG0_FS_SEL_POS) , ICM426XX_ACCEL_CONFIG0_FS_SEL_8g = (0x1 << BIT_ACCEL_CONFIG0_FS_SEL_POS) , ICM426XX_ACCEL_CONFIG0_FS_SEL_16g = (0x0 << BIT_ACCEL_CONFIG0_FS_SEL_POS) }

  Accelerometer FSR selection.
- enum ICM426XX_ACCEL_CONFIG0_ODR_t { ICM426XX_ACCEL_CONFIG0_ODR_500_HZ = 0xF , ICM426XX_ACCEL_CONFIG0_ODR_1_5625_HZ = 0xE , ICM426XX_ACCEL_CONFIG0_ODR_3_125_HZ = 0xD , ICM426XX_ACCEL_CONFIG0_ODR_6_25_HZ = 0xC , ICM426XX_ACCEL_CONFIG0_ODR_12_5_HZ = 0xB , ICM426XX_ACCEL_CONFIG0_ODR_25_HZ = 0xA , ICM426XX_ACCEL_CONFIG0_ODR_50_HZ = 0x9 , ICM426XX_ACCEL_CONFIG0_ODR_100_HZ = 0x8 , ICM426XX_ACCEL_CONFIG0_ODR_200_HZ = 0x7 , ICM426XX_ACCEL_CONFIG0_ODR_1_KHZ = 0x6 , ICM426XX_ACCEL_CONFIG0_ODR_2_KHZ = 0x5 , ICM426XX_ACCEL_CONFIG0_ODR_4_KHZ = 0x4 , ICM426XX_ACCEL_CONFIG0_ODR_8_KHZ = 0x3 , ICM426XX_ACCEL_CONFIG0_ODR_16_KHZ = 0x2 , ICM426XX_ACCEL_CONFIG0_ODR_32_KHZ = 0x1 }

  Accelerometer ODR selection.
- enum ICM426XX_GYRO_CONFIG_GYRO_UI_FILT_ORD_t { ICM426XX_GYRO_CONFIG_GYRO_UI_FILT_ORD_1ST_ORD , ICM426XX_GYRO_CONFIG_GYRO_UI_FILT_ORD_2ND_ORDER , ICM426XX_GYRO_CONFIG_GYRO_UI_FILT_ORD_3F }
- enum ICM426XX_GYRO_ACCEL_CONFIG0_ACCEL_FILT_BW_t { ICM426XX_GYRO_ACCEL_CONFIG0_ACCEL_FILT_BW_40 = (0x7 << BIT_GYRO_ACCEL_CONFIG0_ACCEL_FILT_POS) , ICM426XX_GYRO_ACCEL_CONFIG0_ACCEL_FILT_BW_20 = (0x6 << BIT_GYRO_ACCEL_CONFIG0_ACCEL_FILT_POS) , ICM426XX_GYRO_ACCEL_CONFIG0_ACCEL_FILT_BW_16 = (0x5 << BIT_GYRO_ACCEL_CONFIG0_ACCEL_FILT_POS) , ICM426XX_GYRO_ACCEL_CONFIG0_ACCEL_FILT_BW_1 = (0x4 << BIT_GYRO_ACCEL_CONFIG0_ACCEL_FILT_POS) , ICM426XX_GYRO_ACCEL_CONFIG0_ACCEL_FILT_BW_8 = (0x3 << BIT_GYRO_ACCEL_CONFIG0_ACCEL_FILT_POS) , ICM426XX_GYRO_ACCEL_CONFIG0_ACCEL_FILT_BW_5 = (0x2 << BIT_GYRO_ACCEL_CONFIG0_ACCEL_FILT_POS) , ICM426XX_GYRO_ACCEL_CONFIG0_ACCEL_FILT_BW_4 = (0x1 << BIT_GYRO_ACCEL_CONFIG0_ACCEL_FILT_POS) , ICM426XX_GYRO_ACCEL_CONFIG0_ACCEL_FILT_BW_2 = (0x0 << BIT_GYRO_ACCEL_CONFIG0_ACCEL_FILT_POS) }
- enum ICM426XX_GYRO_ACCEL_CONFIG0_ACCEL_FILT_AVG_t { ICM426XX_GYRO_ACCEL_CONFIG0_ACCEL_FILT_AV = (0x6 << BIT_GYRO_ACCEL_CONFIG0_ACCEL_FILT_POS) , ICM426XX_GYRO_ACCEL_CONFIG0_ACCEL_FILT_AVG_ = (0x1 << BIT_GYRO_ACCEL_CONFIG0_ACCEL_FILT_POS) }
- enum ICM426XX_GYRO_ACCEL_CONFIG0_GYRO_FILT_BW_t { ICM426XX_GYRO_ACCEL_CONFIG0_GYRO_FILT_BW_40 = 0x07 , ICM426XX_GYRO_ACCEL_CONFIG0_GYRO_FILT_BW = 0x06 , ICM426XX_GYRO_ACCEL_CONFIG0_GYRO_FILT_BW_16 = 0x05 , ICM426XX_GYRO_ACCEL_CONFIG0_GYRO_ = 0x04 , ICM426XX_GYRO_ACCEL_CONFIG0_GYRO_FILT_BW_8 = 0x03 , ICM426XX_GYRO_ACCEL_CONFIG0_GYRO_FILT_BW = 0x02 , ICM426XX_GYRO_ACCEL_CONFIG0_GYRO_FILT_BW_4 = 0x01 , ICM426XX_GYRO_ACCEL_CONFIG0_GYRO_F = 0x00 }
- enum ICM426XX_ACCEL_CONFIG_ACCEL_UI_FILT_ORD_t { ICM426XX_ACCEL_CONFIG_ACCEL_UI_FILT_ORD_1ST_O , ICM426XX_ACCEL_CONFIG_ACCEL_UI_FILT_ORD_2ND_ORDER , ICM426XX_ACCEL_CONFIG_ACCEL_UI_FILT_ORD_ }
- enum ICM426XX_TMST_CONFIG_TMST_TO_REGS_EN_t { ICM426XX_TMST_CONFIG_TMST_TO_REGS_EN = (0x1 << BIT_TMST_CONFIG_TMST_TO_REGS_EN_POS) , ICM426XX_TMST_CONFIG_TMST_TO_REGS_DIS = (0x0 << BIT_TMST_CONFIG_TMST_TO_REGS_EN_POS) }
- enum ICM426XX_TMST_CONFIG_RESOL_t { ICM426XX_TMST_CONFIG_RESOL_16us = (0x01 << BIT_TMST_CONFIG_RESOL_POS) , ICM426XX_TMST_CONFIG_RESOL_1us = (0x00 << BIT_TMST_CONFIG_RESOL_POS) }
- enum ICM426XX_TMST_CONFIG_TMST_FSYNC_EN_t { ICM426XX_TMST_CONFIG_TMST_FSYNC_EN = (0x01 << BIT_TMST_CONFIG_TMST_FSYNC_POS) , ICM426XX_TMST_CONFIG_TMST_FSYNC_DIS = (0x00 << BIT_TMST_CONFIG_TMST_FSYNC_POS) }
- enum ICM426XX_TMST_CONFIG_TMST_EN_t { ICM426XX_TMST_CONFIG_TMST_EN = 0x01 , ICM426XX_TMST_CONFIG_TMST_DIS = 0x00 }

- enum ICM426XX_APEX_CONFIG0_DMP_POWER_SAVE_t { ICM426XX_APEX_CONFIG0_DMP_POWER_SAVE_EN = (0x1 << BIT_APEX_CONFIG0_DMP_POWER_SAVE_POS) , ICM426XX_APEX_CONFIG0_DMP_POWER_SAVE_DIS = (0x0 << BIT_APEX_CONFIG0_DMP_POWER_SAVE_POS) }
- enum ICM426XX_APEX_CONFIG0_TAP_ENABLE_t { ICM426XX_APEX_CONFIG0_TAP_ENABLE_EN = (0x1 << BIT_APEX_CONFIG0_TAP_ENABLE_POS) , ICM426XX_APEX_CONFIG0_TAP_ENABLE_DIS = (0x0 << BIT_APEX_CONFIG0_TAP_ENABLE_POS) }
- enum ICM426XX_APEX_CONFIG0_PEDO_EN_t { ICM426XX_APEX_CONFIG0_PEDO_EN_EN = (0x1 << BIT_APEX_CONFIG0_PEDO_EN_POS) , ICM426XX_APEX_CONFIG0_PEDO_EN_DIS = (0x0 << BIT_APEX_CONFIG0_PEDO_EN_POS) }
- enum ICM426XX_APEX_CONFIG0_R2W_EN_t { ICM426XX_APEX_CONFIG0_R2W_EN_EN = (0x1 << BIT_APEX_CONFIG0_R2W_EN_POS) , ICM426XX_APEX_CONFIG0_R2W_EN_DIS = (0x0 << BIT_↩ APEX_CONFIG0_R2W_EN_POS) }
- enum ICM426XX_APEX_CONFIG0_TILT_EN_t { ICM426XX_APEX_CONFIG0_TILT_EN_EN = (0x1 << BIT_APEX_CONFIG0_TILT_EN_POS) , ICM426XX_APEX_CONFIG0_TILT_EN_DIS = (0x0 << BIT_↩ APEX_CONFIG0_TILT_EN_POS) }
- enum ICM426XX_APEX_CONFIG0_DMP_ODR_t { ICM426XX_APEX_CONFIG0_DMP_ODR_25Hz = (0x0 << BIT_APEX_CONFIG0_DMP_ODR_POS) , ICM426XX_APEX_CONFIG0_DMP_ODR_50Hz = (0x2 << BIT_APEX_CONFIG0_DMP_ODR_POS) , ICM426XX_APEX_CONFIG0_DMP_ODR_100Hz , ICM426XX_APEX_CONFIG0_DMP_ODR_500Hz }

  DMP ODR selection.
- enum ICM426XX_SMD_CONFIG_WOM_INT_MODE_t { ICM426XX_SMD_CONFIG_WOM_INT_MODE_ANDED = (0x01 << BIT_SMD_CONFIG_WOM_INT_MODE_POS) , ICM426XX_SMD_CONFIG_WOM_INT_MODE_ORED = (0x00 << BIT_SMD_CONFIG_WOM_INT_MODE_POS) }
- enum ICM426XX_SMD_CONFIG_WOM_MODE_t { ICM426XX_SMD_CONFIG_WOM_MODE_CMP_PREV = (0x01 << BIT_SMD_CONFIG_WOM_MODE_POS) , ICM426XX_SMD_CONFIG_WOM_MODE_CMP_INIT = (0x00 << BIT_SMD_CONFIG_WOM_MODE_POS) }
- enum ICM426XX_SMD_CONFIG_SMD_MODE_t { ICM426XX_SMD_CONFIG_SMD_MODE_LONG = 0x03 , ICM426XX_SMD_CONFIG_SMD_MODE_SHORT = 0x02 , ICM426XX_SMD_CONFIG_SMD_MODE_WOM = 0x01 , ICM426XX_SMD_CONFIG_SMD_MODE_DISABLED = 0x00 }
- enum ICM426XX_FIFO_CONFIG1_WM_GT_t { ICM426XX_FIFO_CONFIG1_WM_GT_TH_EN = (0x1 << BIT_FIFO_CONFIG1_WM_GT_TH_POS) , ICM426XX_FIFO_CONFIG1_WM_GT_TH_DIS = (0x0 << BIT_FIFO_CONFIG1_WM_GT_TH_POS) }
- enum ICM426XX_FIFO_CONFIG1_HIRES_t { ICM426XX_FIFO_CONFIG1_HIRES_EN = (0x1 << BIT↩ _FIFO_CONFIG1_HIRES_POS) , ICM426XX_FIFO_CONFIG1_HIRES_DIS = (0x0 << BIT_FIFO_↩ CONFIG1_HIRES_POS) }
- enum ICM426XX_FIFO_CONFIG1_TMST_FSYNC_t { ICM426XX_FIFO_CONFIG1_TMST_FSYNC_EN = (0x1 << BIT_FIFO_CONFIG1_TMST_FSYNC_POS) , ICM426XX_FIFO_CONFIG1_TMST_FSYNC_DIS = (0x0 << BIT_FIFO_CONFIG1_TMST_FSYNC_POS) }
- enum ICM426XX_FIFO_CONFIG1_TEMP_t { ICM426XX_FIFO_CONFIG1_TEMP_EN = (0x1 << BIT↩ _FIFO_CONFIG1_TEMP_POS) , ICM426XX_FIFO_CONFIG1_TEMP_DIS = (0x0 << BIT_FIFO_↩ CONFIG1_TEMP_POS) }
- enum ICM426XX_FIFO_CONFIG1_GYRO_t { ICM426XX_FIFO_CONFIG1_GYRO_EN = (0x1 << BIT↩ _FIFO_CONFIG1_GYRO_POS) , ICM426XX_FIFO_CONFIG1_GYRO_DIS = (0x0 << BIT_FIFO_↩ CONFIG1_GYRO_POS) }
- enum ICM426XX_FIFO_CONFIG1_ACCEL_t { ICM426XX_FIFO_CONFIG1_ACCEL_EN = 0x01 , ICM426XX_FIFO_CONFIG1_ACCEL_DIS = 0x00 }
- enum ICM426XX_FSYNC_CONFIG_UI_SEL_t { ICM426XX_FSYNC_CONFIG_UI_SEL_NO = (0x0 << BIT_FSYNC_CONFIG_UI_SEL_POS) , ICM426XX_FSYNC_CONFIG_ = (0x1 << BIT_FSYNC_CONFIG_UI_SEL_POS) , ICM426XX_FSYNC_CONFIG_UI_SEL_GYRO_X = (0x2 << BIT_FSYNC_CONFIG_UI_SEL_POS) , ICM426XX_FSYNC_CONFIG_UI_SEL_GYRO_Y = (0x3 << BIT_FSYNC_CONFIG_UI_SEL_POS) , ICM426XX_FSYNC_CONFIG_UI_SEL_GYRO_Z = (0x4 << BIT_FSYNC_CONFIG_UI_SEL_POS) , ICM426XX_FSYNC_CONFIG_UI_SEL_ACCEL_X = (0x5 << BIT_FSYNC_CONFIG_UI_SEL_POS) , ICM426XX_FSYNC_CONFIG_UI_SEL_ACCEL_Y = (0x6 << BIT_FSYNC_CONFIG_UI_SEL_POS) , ICM426XX_FSYNC_CONFIG_UI_SEL_ACCEL_Z = (0x7 << BIT_FSYNC_CONFIG_UI_SEL_POS) }
- enum ICM426XX_INT_TPULSE_DURATION_t { ICM426XX_INT_TPULSE_DURATION_8_US = (0x1 << BIT_INT_TPULSE_DURATION_POS) , ICM426XX_INT_TPULSE_DURATION_100_US = (0x0 << BIT_↩ INT_TPULSE_DURATION_POS) }

- enum ICM426XX_INT_TDEASSERT_t { ICM426XX_INT_TDEASSERT_DISABLED = (0x1 << BIT_INT_TDEASSERT_POS) , ICM426XX_INT_TDEASSERT_ENABLED = (0x0 << BIT_INT_TDEASSERT_POS) }
- enum ICM426XX_INT_CONFIG1_ASY_RST_t { ICM426XX_INT_CONFIG1_ASY_RST_DISABLED = (0x1 << BIT_INT_CONFIG1_ASY_RST_POS) , ICM426XX_INT_CONFIG1_ASY_RST_ENABLED = (0x0 << BIT_INT_CONFIG1_ASY_RST_POS) }
- enum ICM426XX_SENSOR_CONFIG2_OIS_MODE_t { ICM426XX_SENSOR_CONFIG2_OIS_MODE_32KHZ = (0x2 << BIT_SENSOR_CONFIG2_OIS_MODE_POS) , ICM426XX_SENSOR_CONFIG2_OIS_MODE_8KHZ = (0x1 << BIT_SENSOR_CONFIG2_OIS_MODE_POS) , ICM426XX_SENSOR_CONFIG2_OIS_MODE_DIS = (0x0 << BIT_SENSOR_CONFIG2_OIS_MODE_POS) }
- enum ICM426XX_GYRO_AAF_DIS_t { ICM426XX_GYRO_AAF_EN = (0x0 << BIT_GYRO_AAF_DIS_POS) , ICM426XX_GYRO_AAF_DIS = (0x1 << BIT_GYRO_AAF_DIS_POS) }
- enum ICM426XX_GYRO_NF_DIS_t { ICM426XX_GYRO_NF_EN = (0x0 << BIT_GYRO_NF_DIS_POS) , ICM426XX_GYRO_NF_DIS = (0x1 << BIT_GYRO_NF_DIS_POS) }
- enum ICM426XX_INTF_CONFIG4_AP_SPI_t { ICM426XX_INTF_CONFIG4_AP_SPI4W = (0x1 << BIT_INTF_CONFIG4_AP_SPI_POS) , ICM426XX_INTF_CONFIG4_AP_SPI3W = (0x0 << BIT_INTF_CONFIG4_AP_SPI_POS) }
- enum ICM426XX_INTF_CONFIG4_AUX1_SPI_t { ICM426XX_INTF_CONFIG4_AUX1_SPI4W = (0x1 << BIT_INTF_CONFIG4_AUX1_SPI_POS) , ICM426XX_INTF_CONFIG4_AUX1_SPI3W = (0x0 << BIT_INTF_CONFIG4_AUX1_SPI_POS) }
- enum ICM426XX_ACCEL_AAF_DIS_t { ICM426XX_ACCEL_AAF_EN = (0x0 << BIT_ACCEL_AAF_DIS_POS) , ICM426XX_ACCEL_AAF_DIS = (0x1 << BIT_ACCEL_AAF_DIS_POS) }
- enum ICM426XX_OIS1_CONFIG1_ACCEL_LP_CLK_SEL_t { ICM426XX_OIS1_CONFIG1_ACCEL_LP_CLK_SEL_WUOSC = (0x0 << BIT_OIS1_CONFIG1_ACCEL_LP_CLK_SEL_POS) , ICM426XX_OIS1_CONFIG1_ACCEL_LP_CLK_SEL_RCOSC = (0x1 << BIT_OIS1_CONFIG1_ACCEL_LP_CLK_SEL_POS) }
- enum ICM426XX_OIS1_CONFIG1_DEC_t { ICM426XX_OIS1_CONFIG1_DEC_1 = (0x0 << BIT_OIS1_CONFIG1_DEC_POS) , ICM426XX_OIS1_CONFIG1_DEC_2 = (0x1 << BIT_OIS1_CONFIG1_DEC_POS) , ICM426XX_OIS1_CONFIG1_DEC_4 = (0x2 << BIT_OIS1_CONFIG1_DEC_POS) , ICM426XX_OIS1_CONFIG1_DEC_8 = (0x3 << BIT_OIS1_CONFIG1_DEC_POS) , ICM426XX_OIS1_CONFIG1_DEC_16 = (0x4 << BIT_OIS1_CONFIG1_DEC_POS) , ICM426XX_OIS1_CONFIG1_DEC_32 = (0x5 << BIT_OIS1_CONFIG1_DEC_POS) }

  OIS1 rate selection (base clock fixed by OTP divided by decimator value)
- enum ICM426XX_OIS1_CONFIG1_GYRO_EN_t { ICM426XX_OIS1_CONFIG1_GYRO_EN = (0x1 << BIT_OIS1_CONFIG1_GYRO_EN_POS) , ICM426XX_OIS1_CONFIG1_GYRO_DIS = (0x0 << BIT_OIS1_CONFIG1_GYRO_EN_POS) }
- enum ICM426XX_OIS1_CONFIG1_ACCEL_EN_t { ICM426XX_OIS1_CONFIG1_ACCEL_EN = (0x1 << BIT_OIS1_CONFIG1_ACCEL_EN_POS) , ICM426XX_OIS1_CONFIG1_ACCEL_DIS = (0x0 << BIT_OIS1_CONFIG1_ACCEL_EN_POS) }
- enum ICM426XX_OIS1_CONFIG2_GYRO_FS_SEL_t { ICM426XX_OIS1_CONFIG2_GYRO_FS_SEL_16dps , ICM426XX_OIS1_CONFIG2_GYRO_FS_SEL_31dps , ICM426XX_OIS1_CONFIG2_GYRO_FS_SEL_62dps , ICM426XX_OIS1_CONFIG2_GYRO_FS_SEL_125dps , ICM426XX_OIS1_CONFIG2_GYRO_FS_SEL_250dps , ICM426XX_OIS1_CONFIG2_GYRO_FS_SEL_500dps , ICM426XX_OIS1_CONFIG2_GYRO_FS_SEL_1000dps , ICM426XX_OIS1_CONFIG2_GYRO_FS_SEL_2000dps }

  OIS1 gyroscope FSR selection.
- enum ICM426XX_OIS1_CONFIG2_ACCEL_FS_SEL_t { ICM426XX_OIS1_CONFIG2_ACCEL_FS_SEL_RESERVED = (0x4 << BIT_OIS1_CONFIG2_ACCEL_FS_SEL_POS) , ICM426XX_OIS1_CONFIG2_ACCEL_FS_SEL_2g = (0x3 << BIT_OIS1_CONFIG2_ACCEL_FS_SEL_POS) , ICM426XX_OIS1_CONFIG2_ACCEL_FS_SEL_4g = (0x2 << BIT_OIS1_CONFIG2_ACCEL_FS_SEL_POS) , ICM426XX_OIS1_CONFIG2_ACCEL_FS_SEL_8g = (0x1 << BIT_OIS1_CONFIG2_ACCEL_FS_SEL_POS) , ICM426XX_OIS1_CONFIG2_ACCEL_FS_SEL_16g = (0x0 << BIT_OIS1_CONFIG2_ACCEL_FS_SEL_POS) }

  OIS1 accelerometer FSR selection.

- enum ICM426XX_OIS2_CONFIG1_ACCEL_LP_CLK_SEL_t { ICM426XX_OIS2_CONFIG1_ACCEL_LP_CLK_SEL_WUOSC = (0x0 << BIT_OIS2_CONFIG1_ACCEL_LP_CLK_SEL_POS) , ICM426XX_OIS2_CONFIG1_ACCEL_LP_CLK_SEL_RCOSC = (0x1 << BIT_OIS2_CONFIG1_ACCEL_LP_CLK_SEL_POS) }
- enum ICM426XX_OIS2_CONFIG1_DEC_t { ICM426XX_OIS2_CONFIG1_DEC_1 = (0x0 << BIT_OIS2_CONFIG1_DEC_POS) , ICM426XX_OIS2_CONFIG1_DEC_2 = (0x1 << BIT_OIS2_CONFIG1_DEC_POS) , ICM426XX_OIS2_CONFIG1_DEC_4 = (0x2 << BIT_OIS2_CONFIG1_DEC_POS) , ICM426XX_OIS2_CONFIG1_DEC_8 = (0x3 << BIT_OIS2_CONFIG1_DEC_POS) , ICM426XX_OIS2_CONFIG1_DEC_16 = (0x4 << BIT_OIS2_CONFIG1_DEC_POS) , ICM426XX_OIS2_CONFIG1_DEC_32 = (0x5 << BIT_OIS2_CONFIG1_DEC_POS) }

  OIS2 rate selection (base clock fixed by OTP divided by decimator value)
- enum ICM426XX_OIS2_CONFIG1_GYRO_EN_t { ICM426XX_OIS2_CONFIG1_GYRO_EN = (0x1 << BIT_OIS2_CONFIG1_GYRO_EN_POS) , ICM426XX_OIS2_CONFIG1_GYRO_DIS = (0x0 << BIT_OIS2_CONFIG1_GYRO_EN_POS) }
- enum ICM426XX_OIS2_CONFIG1_ACCEL_EN_t { ICM426XX_OIS2_CONFIG1_ACCEL_EN = (0x1 << BIT_OIS2_CONFIG1_ACCEL_EN_POS) , ICM426XX_OIS2_CONFIG1_ACCEL_DIS = (0x0 << BIT_OIS2_CONFIG1_ACCEL_EN_POS) }
- enum ICM426XX_OIS2_CONFIG2_GYRO_FS_SEL_t { ICM426XX_OIS2_CONFIG2_GYRO_FS_SEL_16dps , ICM426XX_OIS2_CONFIG2_GYRO_FS_SEL_31dps , ICM426XX_OIS2_CONFIG2_GYRO_FS_SEL_62dps , ICM426XX_OIS2_CONFIG2_GYRO_FS_SEL_125dps , ICM426XX_OIS2_CONFIG2_GYRO_FS_SEL_250dps , ICM426XX_OIS2_CONFIG2_GYRO_FS_SEL_500dps , ICM426XX_OIS2_CONFIG2_GYRO_FS_SEL_1000dps , ICM426XX_OIS2_CONFIG2_GYRO_FS_SEL_2000dps }

  OIS2 gyroscope FSR selection.
- enum ICM426XX_OIS2_CONFIG2_ACCEL_FS_SEL_t { ICM426XX_OIS2_CONFIG2_ACCEL_FS_SEL_RESERVED = (0x4 << BIT_OIS2_CONFIG2_ACCEL_FS_SEL_POS) , ICM426XX_OIS2_CONFIG2_ACCEL_FS_SEL_2g = (0x3 << BIT_OIS2_CONFIG2_ACCEL_FS_SEL_POS) , ICM426XX_OIS2_CONFIG2_ACCEL_FS_SEL_4g = (0x2 << BIT_OIS2_CONFIG2_ACCEL_FS_SEL_POS) , ICM426XX_OIS2_CONFIG2_ACCEL_FS_SEL_8g = (0x1 << BIT_OIS2_CONFIG2_ACCEL_FS_SEL_POS) , ICM426XX_OIS2_CONFIG2_ACCEL_FS_SEL_16g = (0x0 << BIT_OIS2_CONFIG2_ACCEL_FS_SEL_POS) }

  OIS2 accelerometer FSR selection.
- enum ICM426XX_APEX_CONFIG1_DMP_POWER_SAVE_TIME_t { ICM426XX_APEX_CONFIG1_DMP_POWER_SAVE_TIME_SEL_0S = 0x0 , ICM426XX_APEX_CONFIG1_DMP_POWER_SA = 0x1 , ICM426XX_APEX_CONFIG1_DMP_POWER_SAVE_TIME_SEL_8S = 0x2 , ICM426XX_APEX_CONFIG1_DMP_POW = 0x3 , ICM426XX_APEX_CONFIG1_DMP_POWER_SAVE_TIME_SEL_16S = 0x4 , ICM426XX_APEX_CONFIG1_DMP_POWER_S = 0x5 , ICM426XX_APEX_CONFIG1_DMP_POWER_SAVE_TIME_SEL_24S = 0x6 , ICM426XX_APEX_CONFIG1_DMP_POW = 0x7 , ICM426XX_APEX_CONFIG1_DMP_POWER_SAVE_TIME_SEL_32S = 0x8 , ICM426XX_APEX_CONFIG1_DMP_POWER_S = 0x9 , ICM426XX_APEX_CONFIG1_DMP_POWER_SAVE_TIME_SEL_40S = 0xA , ICM426XX_APEX_CONFIG1_DMP_POW = 0xB , ICM426XX_APEX_CONFIG1_DMP_POWER_SAVE_TIME_SEL_48S = 0xC , ICM426XX_APEX_CONFIG1_DMP_POWER_S = 0xD , ICM426XX_APEX_CONFIG1_DMP_POWER_SAVE_TIME_SEL_56S = 0xE , ICM426XX_APEX_CONFIG1_DMP_POW = 0xF }
- enum ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_t { ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_30MG , ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_ , ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_40MG , ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP , ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_50MG , ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_ , ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_60MG , ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP , ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_70MG , ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_ , ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_80MG , ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP ,

ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_90MG , ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_T
, ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_100MG , ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP
}

- enum ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_t {
ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_30MG = (0 << BIT_APEX_CONFIG2_PEDO_AMP_TH↩
_POS) , ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_34MG = (1 << BIT_APEX_CONFIG2_PEDO_↩
AMP_TH_POS) , ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_38MG = (2 << BIT_APEX_CONFIG2↩
_PEDO_AMP_TH_POS) , ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_42MG = (3 << BIT_APEX_↩
CONFIG2_PEDO_AMP_TH_POS) ,
ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_46MG = (4 << BIT_APEX_CONFIG2_PEDO_AMP_TH↩
_POS) , ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_50MG = (5 << BIT_APEX_CONFIG2_PEDO_↩
AMP_TH_POS) , ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_54MG = (6 << BIT_APEX_CONFIG2↩
_PEDO_AMP_TH_POS) , ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_58MG = (7 << BIT_APEX_↩
CONFIG2_PEDO_AMP_TH_POS) ,
ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_62MG = (8 << BIT_APEX_CONFIG2_PEDO_AMP_TH↩
_POS) , ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_66MG = (9 << BIT_APEX_CONFIG2_PEDO_↩
AMP_TH_POS) , ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_70MG = (10 << BIT_APEX_CONFIG2↩
_PEDO_AMP_TH_POS) , ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_74MG = (11 << BIT_APEX_↩
CONFIG2_PEDO_AMP_TH_POS) ,
ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_78MG = (12 << BIT_APEX_CONFIG2_PEDO_AMP_TH↩
_POS) , ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_82MG = (13 << BIT_APEX_CONFIG2_PEDO_↩
AMP_TH_POS) , ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_86MG = (14 << BIT_APEX_CONFIG2↩
_PEDO_AMP_TH_POS) , ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_90MG = (15 << BIT_APEX_↩
CONFIG2_PEDO_AMP_TH_POS) }
- enum ICM426XX_APEX_CONFIG3_PEDO_SB_TIMER_TH_t {
ICM426XX_APEX_CONFIG3_PEDO_SB_TIMER_TH_50_SAMPLES , ICM426XX_APEX_CONFIG3_PEDO_SB_TIMER_TH_
, ICM426XX_APEX_CONFIG3_PEDO_SB_TIMER_TH_100_SAMPLES , ICM426XX_APEX_CONFIG3_PEDO_SB_TIMER_T
,
ICM426XX_APEX_CONFIG3_PEDO_SB_TIMER_TH_150_SAMPLES , ICM426XX_APEX_CONFIG3_PEDO_SB_TIMER_TH
, ICM426XX_APEX_CONFIG3_PEDO_SB_TIMER_TH_200_SAMPLES , ICM426XX_APEX_CONFIG3_PEDO_SB_TIMER_T
}
- enum ICM426XX_APEX_CONFIG3_PEDO_HI_ENRGY_TH_t { ICM426XX_APEX_CONFIG3_PEDO_HI_ENRGY_TH_90
= 0x0 , ICM426XX_APEX_CONFIG3_PEDO_HI_ENRGY_TH_107 = 0x1 , ICM426XX_APEX_CONFIG3_PEDO_HI_ENRGY_T
= 0x2 , ICM426XX_APEX_CONFIG3_PEDO_HI_ENRGY_TH_159 = 0x3 }
- enum ICM426XX_APEX_CONFIG4_TILT_WAIT_TIME_t { ICM426XX_APEX_CONFIG4_TILT_WAIT_TIME_0S
= (0 << BIT_APEX_CONFIG4_TILT_WAIT_TIME_POS) , ICM426XX_APEX_CONFIG4_TILT_WAIT_TIME_2S
= (1 << BIT_APEX_CONFIG4_TILT_WAIT_TIME_POS) , ICM426XX_APEX_CONFIG4_TILT_WAIT_TIME_4S
= (2 << BIT_APEX_CONFIG4_TILT_WAIT_TIME_POS) , ICM426XX_APEX_CONFIG4_TILT_WAIT_TIME_6S
= (3 << BIT_APEX_CONFIG4_TILT_WAIT_TIME_POS) }
- enum ICM426XX_APEX_CONFIG4_R2W_SLEEP_TIME_OUT_t {
ICM426XX_APEX_CONFIG4_R2W_SLEEP_TIME_OUT_1_28S = (0 << BIT_APEX_CONFIG4_R2↩
W_SLEEP_TIME_OUT_POS) , ICM426XX_APEX_CONFIG4_R2W_SLEEP_TIME_OUT_2_56S = (1 <<
BIT_APEX_CONFIG4_R2W_SLEEP_TIME_OUT_POS) , ICM426XX_APEX_CONFIG4_R2W_SLEEP_TIME_OUT_3_84S
= (2 << BIT_APEX_CONFIG4_R2W_SLEEP_TIME_OUT_POS) , ICM426XX_APEX_CONFIG4_R2W_SLEEP_TIME_OUT_5
= (3 << BIT_APEX_CONFIG4_R2W_SLEEP_TIME_OUT_POS) ,
ICM426XX_APEX_CONFIG4_R2W_SLEEP_TIME_OUT_6_4S = (4 << BIT_APEX_CONFIG4_R2W↩
_SLEEP_TIME_OUT_POS) , ICM426XX_APEX_CONFIG4_R2W_SLEEP_TIME_OUT_7_68S = (5 <<
BIT_APEX_CONFIG4_R2W_SLEEP_TIME_OUT_POS) , ICM426XX_APEX_CONFIG4_R2W_SLEEP_TIME_OUT_8_96S
= (6 << BIT_APEX_CONFIG4_R2W_SLEEP_TIME_OUT_POS) , ICM426XX_APEX_CONFIG4_R2W_SLEEP_TIME_OUT_1
= (7 << BIT_APEX_CONFIG4_R2W_SLEEP_TIME_OUT_POS) }
- enum ICM426XX_APEX_CONFIG5_R2W_MOUNTING_MATRIX_t {
ICM426XX_APEX_CONFIG5_R2W_MOUNTING_MATRIX_0 = (0 << BIT_APEX_CONFIG5_R2W_↩
MOUNTING_MATRIX_POS) , ICM426XX_APEX_CONFIG5_R2W_MOUNTING_MATRIX_1 = (1 << BIT_↩
APEX_CONFIG5_R2W_MOUNTING_MATRIX_POS) , ICM426XX_APEX_CONFIG5_R2W_MOUNTING_MATRIX_2
= (2 << BIT_APEX_CONFIG5_R2W_MOUNTING_MATRIX_POS) , ICM426XX_APEX_CONFIG5_R2W_MOUNTING_MATRI
= (3 << BIT_APEX_CONFIG5_R2W_MOUNTING_MATRIX_POS) ,
ICM426XX_APEX_CONFIG5_R2W_MOUNTING_MATRIX_4 = (4 << BIT_APEX_CONFIG5_R2W_↩
MOUNTING_MATRIX_POS) , ICM426XX_APEX_CONFIG5_R2W_MOUNTING_MATRIX_5 = (5 << BIT_↩

APEX_CONFIG5_R2W_MOUNTING_MATRIX_POS) , ICM426XX_APEX_CONFIG5_R2W_MOUNTING_MATRIX_6 = (6 << BIT_APEX_CONFIG5_R2W_MOUNTING_MATRIX_POS) , ICM426XX_APEX_CONFIG5_R2W_MOUNTING_MATRI = (7 << BIT_APEX_CONFIG5_R2W_MOUNTING_MATRIX_POS) }

- enum ICM426XX_APEX_CONFIG6_R2W_SLEEP_GEST_DELAY_t { ICM426XX_APEX_CONFIG6_R2W_SLEEP_GEST_DELAY_0_32S , ICM426XX_APEX_CONFIG6_R2W_SLEEP_GEST_DE , ICM426XX_APEX_CONFIG6_R2W_SLEEP_GEST_DELAY_0_96S , ICM426XX_APEX_CONFIG6_R2W_SLEEP_GEST_DE , ICM426XX_APEX_CONFIG6_R2W_SLEEP_GEST_DELAY_1_6S , ICM426XX_APEX_CONFIG6_R2W_SLEEP_GEST_DEL , ICM426XX_APEX_CONFIG6_R2W_SLEEP_GEST_DELAY_2_24S , ICM426XX_APEX_CONFIG6_R2W_SLEEP_GEST_DE }
- enum ICM426XX_APEX_CONFIG7_TAP_MAX_PEAK_TOL_t { ICM426XX_APEX_CONFIG7_TAP_MAX_PEAK_TOL_12 = 0x0 , ICM426XX_APEX_CONFIG7_TAP_MAX_PEAK_TOL_25 = 0x1 , ICM426XX_APEX_CONFIG7_TAP_MAX_PEAK_TOL = 0x2 , ICM426XX_APEX_CONFIG7_TAP_MAX_PEAK_TOL_50 = 0x3 }
- enum ICM426XX_APEX_CONFIG8_TAP_TMAX_t { ICM426XX_APEX_CONFIG8_TAP_TMAX_250MS = (0 << BIT_APEX_CONFIG8_TAP_TMAX_POS) , ICM426XX_APEX_CONFIG8_TAP_TMAX_375MS = (1 << BIT_APEX_CONFIG8_TAP_TMAX_POS) , ICM426XX_APEX_CONFIG8_TAP_TMAX_500MS = (2 << BIT_APEX_CONFIG8_TAP_TMAX_POS) , ICM426XX_APEX_CONFIG8_TAP_TMAX_625MS = (3 << BIT_APEX_CONFIG8_TAP_TMAX_POS) }
- enum ICM426XX_APEX_CONFIG8_TAP_TAVG_t { ICM426XX_APEX_CONFIG8_TAP_TAVG_1SAMPLE = (0 << BIT_APEX_CONFIG8_TAP_TAVG_POS) , ICM426XX_APEX_CONFIG8_TAP_TAVG_2SAMPLE = (1 << BIT_APEX_CONFIG8_TAP_TAVG_POS) , ICM426XX_APEX_CONFIG8_TAP_TAVG_4SAMPLE = (2 << BIT_APEX_CONFIG8_TAP_TAVG_POS) , ICM426XX_APEX_CONFIG8_TAP_TAVG_8SAMPLE = (3 << BIT_APEX_CONFIG8_TAP_TAVG_POS) }
- enum ICM426XX_APEX_CONFIG8_TAP_TMIN_t { ICM426XX_APEX_CONFIG8_TAP_TMIN_125MS = 0x0 , ICM426XX_APEX_CONFIG8_TAP_TMIN_140MS = 0x1 , ICM426XX_APEX_CONFIG8_TAP_TMIN_156MS = 0x2 , ICM426XX_APEX_CONFIG8_TAP_TMIN_171MS = 0x3 , ICM426XX_APEX_CONFIG8_TAP_TMIN_187MS = 0x4 , ICM426XX_APEX_CONFIG8_TAP_TMIN_203MS = 0x5 , ICM426XX_APEX_CONFIG8_TAP_TMIN_218MS = 0x6 , ICM426XX_APEX_CONFIG8_TAP_TMIN_234MS = 0x7 }
- enum ICM426XX_APEX_CONFIG9_SENSITIVITY_MODE_t { ICM426XX_APEX_CONFIG9_SENSITIVITY_MODE_NORMAL = 0x00 , ICM426XX_APEX_CONFIG9_SENSITIVITY_MODE_RESERVED = 0x01 }

7.1.1 Detailed Description

File exposing the device register map.

7.1.2 Macro Definition Documentation

7.1.2.1 ACCEL_DATA_SIZE

```
#define ACCEL_DATA_SIZE 6
```

7.1.2.2 BIT_ACCEL_AAF_BITSHIFT_MASK

```
#define BIT_ACCEL_AAF_BITSHIFT_MASK (0x0F << BIT_ACCEL_AAF_BITSHIFT_POS)
```

7.1.2.3 BIT_ACCEL_AAF_BITSHIFT_POS

```
#define BIT_ACCEL_AAF_BITSHIFT_POS 4
```

7.1.2.4 BIT_ACCEL_AAF_DELT_MASK

```
#define BIT_ACCEL_AAF_DELT_MASK (0x3F << BIT_ACCEL_AAF_DELT_POS)
```

7.1.2.5 BIT_ACCEL_AAF_DELT_POS

```
#define BIT_ACCEL_AAF_DELT_POS 1
```

7.1.2.6 BIT_ACCEL_AAF_DELTSQR_MASK_HI

```
#define BIT_ACCEL_AAF_DELTSQR_MASK_HI (0x0F << BIT_ACCEL_AAF_DELTSQR_POS_HI)
```

7.1.2.7 BIT_ACCEL_AAF_DELTSQR_MASK_LO

```
#define BIT_ACCEL_AAF_DELTSQR_MASK_LO (0xFF << BIT_ACCEL_AAF_DELTSQR_POS_LO)
```

7.1.2.8 BIT_ACCEL_AAF_DELTSQR_POS_HI

```
#define BIT_ACCEL_AAF_DELTSQR_POS_HI 0
```

7.1.2.9 BIT_ACCEL_AAF_DELTSQR_POS_LO

```
#define BIT_ACCEL_AAF_DELTSQR_POS_LO 0
```

7.1.2.10 BIT_ACCEL_AAF_DIS_MASK

```
#define BIT_ACCEL_AAF_DIS_MASK (0x01 << BIT_ACCEL_AAF_DIS_POS)
```

7.1.2.11 BIT_ACCEL_AAF_DIS_POS

```
#define BIT_ACCEL_AAF_DIS_POS 0
```

7.1.2.12 BIT_ACCEL_CONFIG0_FS_SEL_MASK

```
#define BIT_ACCEL_CONFIG0_FS_SEL_MASK (0x7 << BIT_ACCEL_CONFIG0_FS_SEL_POS)
```

7.1.2.13 BIT_ACCEL_CONFIG0_FS_SEL_POS

```
#define BIT_ACCEL_CONFIG0_FS_SEL_POS 5
```

7.1.2.14 BIT_ACCEL_CONFIG0_ODR_MASK

```
#define BIT_ACCEL_CONFIG0_ODR_MASK 0x0F
```

7.1.2.15 BIT_ACCEL_CONFIG0_ODR_POS

```
#define BIT_ACCEL_CONFIG0_ODR_POS 0
```

7.1.2.16 BIT_ACCEL_CONFIG1_ACCEL_DEC2_M2_ORD_MASK

```
#define BIT_ACCEL_CONFIG1_ACCEL_DEC2_M2_ORD_MASK (0x3 << BIT_ACCEL_CONFIG1_ACCEL_DEC2_M2_ORD_POS)
```

7.1.2.17 BIT_ACCEL_CONFIG1_ACCEL_DEC2_M2_ORD_POS

```
#define BIT_ACCEL_CONFIG1_ACCEL_DEC2_M2_ORD_POS 1
```

7.1.2.18 BIT_ACCEL_CONFIG1_ACCEL_UI_FILT_ORD_MASK

```
#define BIT_ACCEL_CONFIG1_ACCEL_UI_FILT_ORD_MASK (0x3 << BIT_ACCEL_CONFIG1_ACCEL_UI_FILT_ORD_POS)
```

7.1.2.19 BIT_ACCEL_CONFIG1_ACCEL_UI_FILT_ORD_POS

```
#define BIT_ACCEL_CONFIG1_ACCEL_UI_FILT_ORD_POS 3
```

7.1.2.20 BIT_ACCEL_LP_CLK_SEL_MASK

```
#define BIT_ACCEL_LP_CLK_SEL_MASK (0x01 << BIT_ACCEL_LP_CLK_SEL_POS)
```

7.1.2.21 BIT_ACCEL_LP_CLK_SEL_POS

```
#define BIT_ACCEL_LP_CLK_SEL_POS 3
```

7.1.2.22 BIT_ACCEL_X_OFFUSER_MASK_HI

```
#define BIT_ACCEL_X_OFFUSER_MASK_HI (0x0F << BIT_ACCEL_X_OFFUSER_POS_HI)
```

7.1.2.23 BIT_ACCEL_X_OFFUSER_MASK_LO

```
#define BIT_ACCEL_X_OFFUSER_MASK_LO (0xFF << BIT_ACCEL_X_OFFUSER_POS_LO)
```

7.1.2.24 BIT_ACCEL_X_OFFUSER_POS_HI

```
#define BIT_ACCEL_X_OFFUSER_POS_HI 4
```

7.1.2.25 BIT_ACCEL_X_OFFUSER_POS_LO

```
#define BIT_ACCEL_X_OFFUSER_POS_LO 0
```

7.1.2.26 BIT_ACCEL_X_ST_EN

```
#define BIT_ACCEL_X_ST_EN 0x08
```

7.1.2.27 BIT_ACCEL_Y_OFFUSER_MASK_HI

```
#define BIT_ACCEL_Y_OFFUSER_MASK_HI (0x0F << BIT_ACCEL_Y_OFFUSER_POS_HI)
```

7.1.2.28 BIT_ACCEL_Y_OFFUSER_MASK_LO

```
#define BIT_ACCEL_Y_OFFUSER_MASK_LO (0xFF << BIT_ACCEL_Y_OFFUSER_POS_LO)
```

7.1.2.29 BIT_ACCEL_Y_OFFUSER_POS_HI

```
#define BIT_ACCEL_Y_OFFUSER_POS_HI 0
```

7.1.2.30 BIT_ACCEL_Y_OFFUSER_POS_LO

```
#define BIT_ACCEL_Y_OFFUSER_POS_LO 0
```

7.1.2.31 BIT_ACCEL_Y_ST_EN

```
#define BIT_ACCEL_Y_ST_EN 0x10
```

7.1.2.32 BIT_ACCEL_Z_OFFUSER_MASK_HI

```
#define BIT_ACCEL_Z_OFFUSER_MASK_HI (0x0F << BIT_ACCEL_Z_OFFUSER_POS_HI)
```

7.1.2.33 BIT_ACCEL_Z_OFFUSER_MASK_LO

```
#define BIT_ACCEL_Z_OFFUSER_MASK_LO (0xFF << BIT_ACCEL_Z_OFFUSER_POS_LO)
```

7.1.2.34 BIT_ACCEL_Z_OFFUSER_POS_HI

```
#define BIT_ACCEL_Z_OFFUSER_POS_HI 4
```

7.1.2.35 BIT_ACCEL_Z_OFFUSER_POS_LO

```
#define BIT_ACCEL_Z_OFFUSER_POS_LO 0
```

7.1.2.36 BIT_ACCEL_Z_ST_EN

```
#define BIT_ACCEL_Z_ST_EN 0x20
```

7.1.2.37 BIT_APEX_CONFIG0_DMP_ODR_MASK

```
#define BIT_APEX_CONFIG0_DMP_ODR_MASK (0x3 << BIT_APEX_CONFIG0_DMP_ODR_POS)
```

7.1.2.38 BIT_APEX_CONFIG0_DMP_ODR_POS

```
#define BIT_APEX_CONFIG0_DMP_ODR_POS 0
```

7.1.2.39 BIT_APEX_CONFIG0_DMP_POWER_SAVE_MASK

```
#define BIT_APEX_CONFIG0_DMP_POWER_SAVE_MASK (0x1 << BIT_APEX_CONFIG0_DMP_POWER_SAVE_POS)
```

7.1.2.40 BIT_APEX_CONFIG0_DMP_POWER_SAVE_POS

```
#define BIT_APEX_CONFIG0_DMP_POWER_SAVE_POS 7
```

7.1.2.41 BIT_APEX_CONFIG0_PEDO_EN_MASK

```
#define BIT_APEX_CONFIG0_PEDO_EN_MASK (0x1 << BIT_APEX_CONFIG0_PEDO_EN_POS)
```

7.1.2.42 BIT_APEX_CONFIG0_PEDO_EN_POS

```
#define BIT_APEX_CONFIG0_PEDO_EN_POS 5
```

7.1.2.43 BIT_APEX_CONFIG0_R2W_EN_MASK

```
#define BIT_APEX_CONFIG0_R2W_EN_MASK (0x1 << BIT_APEX_CONFIG0_R2W_EN_POS)
```

7.1.2.44 BIT_APEX_CONFIG0_R2W_EN_POS

```
#define BIT_APEX_CONFIG0_R2W_EN_POS 3
```

7.1.2.45 BIT_APEX_CONFIG0_TAP_ENABLE_MASK

```
#define BIT_APEX_CONFIG0_TAP_ENABLE_MASK (0x1 << BIT_APEX_CONFIG0_TAP_ENABLE_POS)
```

7.1.2.46 BIT_APEX_CONFIG0_TAP_ENABLE_POS

```
#define BIT_APEX_CONFIG0_TAP_ENABLE_POS 6
```

7.1.2.47 BIT_APEX_CONFIG0_TILT_EN_MASK

```
#define BIT_APEX_CONFIG0_TILT_EN_MASK (0x1 << BIT_APEX_CONFIG0_TILT_EN_POS)
```

7.1.2.48 BIT_APEX_CONFIG0_TILT_EN_POS

```
#define BIT_APEX_CONFIG0_TILT_EN_POS 4
```

7.1.2.49 BIT_APEX_CONFIG1_DMP_POWER_SAVE_TIME_SEL_MASK

```
#define BIT_APEX_CONFIG1_DMP_POWER_SAVE_TIME_SEL_MASK 0x0F
```

7.1.2.50 BIT_APEX_CONFIG1_DMP_POWER_SAVE_TIME_SEL_POS

```
#define BIT_APEX_CONFIG1_DMP_POWER_SAVE_TIME_SEL_POS 0
```

7.1.2.51 BIT_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_MASK

```
#define BIT_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_MASK  (0x0F << BIT_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_POS)
```

7.1.2.52 BIT_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_POS

```
#define BIT_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_POS 4
```

7.1.2.53 BIT_APEX_CONFIG2_PEDO_AMP_TH_MASK

```
#define BIT_APEX_CONFIG2_PEDO_AMP_TH_MASK (0x0F << BIT_APEX_CONFIG2_PEDO_AMP_TH_POS)
```

7.1.2.54 BIT_APEX_CONFIG2_PEDO_AMP_TH_POS

```
#define BIT_APEX_CONFIG2_PEDO_AMP_TH_POS 4
```

7.1.2.55 BIT_APEX_CONFIG2_PEDO_STEP_CNT_TH_MASK

```
#define BIT_APEX_CONFIG2_PEDO_STEP_CNT_TH_MASK 0x0F
```

7.1.2.56 BIT_APEX_CONFIG2_PEDO_STEP_CNT_TH_POS

```
#define BIT_APEX_CONFIG2_PEDO_STEP_CNT_TH_POS 0
```

7.1.2.57 BIT_APEX_CONFIG3_PEDO_HI_ENRGY_TH_MASK

```
#define BIT_APEX_CONFIG3_PEDO_HI_ENRGY_TH_MASK 0x03
```

7.1.2.58 BIT_APEX_CONFIG3_PEDO_HI_ENRGY_TH_POS

```
#define BIT_APEX_CONFIG3_PEDO_HI_ENRGY_TH_POS 0
```

7.1.2.59 BIT_APEX_CONFIG3_PEDO_SB_TIMER_TH_MASK

```
#define BIT_APEX_CONFIG3_PEDO_SB_TIMER_TH_MASK (0x07 << BIT_APEX_CONFIG3_PEDO_SB_TIMER_TH_POS)
```

7.1.2.60 BIT_APEX_CONFIG3_PEDO_SB_TIMER_TH_POS

```
#define BIT_APEX_CONFIG3_PEDO_SB_TIMER_TH_POS 2
```

7.1.2.61 BIT_APEX_CONFIG3_PEDO_STEP_DET_TH_MASK

```
#define BIT_APEX_CONFIG3_PEDO_STEP_DET_TH_MASK (0x07 << BIT_APEX_CONFIG3_PEDO_STEP_DET_TH_POS)
```

7.1.2.62 BIT_APEX_CONFIG3_PEDO_STEP_DET_TH_POS

```
#define BIT_APEX_CONFIG3_PEDO_STEP_DET_TH_POS 5
```

7.1.2.63 BIT_APEX_CONFIG4_R2W_SLEEP_TIME_OUT_MASK

```
#define BIT_APEX_CONFIG4_R2W_SLEEP_TIME_OUT_MASK (0x07 << BIT_APEX_CONFIG4_R2W_SLEEP_TIME_OUT_POS)
```

7.1.2.64 BIT_APEX_CONFIG4_R2W_SLEEP_TIME_OUT_POS

```
#define BIT_APEX_CONFIG4_R2W_SLEEP_TIME_OUT_POS 3
```

7.1.2.65 BIT_APEX_CONFIG4_TILT_WAIT_TIME_MASK

```
#define BIT_APEX_CONFIG4_TILT_WAIT_TIME_MASK (0x03 << BIT_APEX_CONFIG4_TILT_WAIT_TIME_POS)
```

7.1.2.66 BIT_APEX_CONFIG4_TILT_WAIT_TIME_POS

```
#define BIT_APEX_CONFIG4_TILT_WAIT_TIME_POS 6
```

7.1.2.67 BIT_APEX_CONFIG5_R2W_MOUNTING_MATRIX_MASK

```
#define BIT_APEX_CONFIG5_R2W_MOUNTING_MATRIX_MASK (0x07 << BIT_APEX_CONFIG5_R2W_MOUNTING_MATRIX_POS)
```

7.1.2.68 BIT_APEX_CONFIG5_R2W_MOUNTING_MATRIX_POS

```
#define BIT_APEX_CONFIG5_R2W_MOUNTING_MATRIX_POS 0
```

7.1.2.69 BIT_APEX_CONFIG6_R2W_SLEEP_GEST_DELAY_MASK

```
#define BIT_APEX_CONFIG6_R2W_SLEEP_GEST_DELAY_MASK  (0x07 << BIT_APEX_CONFIG6_R2W_SLEEP_GEST_DELAY_POS)
```

7.1.2.70 BIT_APEX_CONFIG6_R2W_SLEEP_GEST_DELAY_POS

```
#define BIT_APEX_CONFIG6_R2W_SLEEP_GEST_DELAY_POS 0
```

7.1.2.71 BIT_APEX_CONFIG7_TAP_MAX_PEAK_TOL_MASK

```
#define BIT_APEX_CONFIG7_TAP_MAX_PEAK_TOL_MASK 0x3
```

7.1.2.72 BIT_APEX_CONFIG7_TAP_MAX_PEAK_TOL_POS

```
#define BIT_APEX_CONFIG7_TAP_MAX_PEAK_TOL_POS 0
```

7.1.2.73 BIT_APEX_CONFIG7_TAP_MIN_JERK_THR_MASK

```
#define BIT_APEX_CONFIG7_TAP_MIN_JERK_THR_MASK (0x3F << BIT_APEX_CONFIG7_TAP_MIN_JERK_THR_POS)
```

7.1.2.74 BIT_APEX_CONFIG7_TAP_MIN_JERK_THR_POS

```
#define BIT_APEX_CONFIG7_TAP_MIN_JERK_THR_POS 2
```

7.1.2.75 BIT_APEX_CONFIG8_TAP_TAVG_MASK

```
#define BIT_APEX_CONFIG8_TAP_TAVG_MASK (0x03 << BIT_APEX_CONFIG8_TAP_TAVG_POS)
```

7.1.2.76 BIT_APEX_CONFIG8_TAP_TAVG_POS

```
#define BIT_APEX_CONFIG8_TAP_TAVG_POS 3
```

7.1.2.77 BIT_APEX_CONFIG8_TAP_TMAX_MASK

```
#define BIT_APEX_CONFIG8_TAP_TMAX_MASK (0x03 << BIT_APEX_CONFIG8_TAP_TMAX_POS)
```

7.1.2.78 BIT_APEX_CONFIG8_TAP_TMAX_POS

```
#define BIT_APEX_CONFIG8_TAP_TMAX_POS 5
```

7.1.2.79 BIT_APEX_CONFIG8_TAP_TMIN_MASK

```
#define BIT_APEX_CONFIG8_TAP_TMIN_MASK 0x07
```

7.1.2.80 BIT_APEX_CONFIG8_TAP_TMIN_POS

```
#define BIT_APEX_CONFIG8_TAP_TMIN_POS 0
```

7.1.2.81 BIT_APEX_CONFIG9_SENSITIVITY_MODE_MASK

```
#define BIT_APEX_CONFIG9_SENSITIVITY_MODE_MASK 0x01
```

7.1.2.82 BIT_APEX_CONFIG9_SENSITIVITY_MODE_POS

```
#define BIT_APEX_CONFIG9_SENSITIVITY_MODE_POS 0
```

7.1.2.83 BIT_APEX_DATA3_ACTIVITY_CLASS_MASK

```
#define BIT_APEX_DATA3_ACTIVITY_CLASS_MASK 0x03
```

7.1.2.84 BIT_APEX_DATA3_ACTIVITY_CLASS_POS

```
#define BIT_APEX_DATA3_ACTIVITY_CLASS_POS 0
```

7.1.2.85 BIT_APEX_DATA3_DMP_IDLE_MASK

```
#define BIT_APEX_DATA3_DMP_IDLE_MASK (0x01 << BIT_APEX_DATA3_DMP_IDLE_POS)
```

7.1.2.86 BIT_APEX_DATA3_DMP_IDLE_POS

```
#define BIT_APEX_DATA3_DMP_IDLE_POS 2
```

7.1.2.87 BIT_APEX_DATA4_TAP_AXIS_MASK

```
#define BIT_APEX_DATA4_TAP_AXIS_MASK (0x03 << BIT_APEX_DATA4_TAP_AXIS_POS)
```

7.1.2.88 BIT_APEX_DATA4_TAP_AXIS_POS

```
#define BIT_APEX_DATA4_TAP_AXIS_POS 1
```

7.1.2.89 BIT_APEX_DATA4_TAP_DIR_MASK

```
#define BIT_APEX_DATA4_TAP_DIR_MASK 0x01
```

7.1.2.90 BIT_APEX_DATA4_TAP_DIR_POS

```
#define BIT_APEX_DATA4_TAP_DIR_POS 0
```

7.1.2.91 BIT_APEX_DATA4_TAP_NUM_MASK

```
#define BIT_APEX_DATA4_TAP_NUM_MASK (0x03 << BIT_APEX_DATA4_TAP_NUM_POS)
```

7.1.2.92 BIT_APEX_DATA4_TAP_NUM_POS

```
#define BIT_APEX_DATA4_TAP_NUM_POS 3
```

TAP status flags: non-zero value - tap detected bit0 - positive or negative edge bit1 and 2 - axis detected : 0-X ; 1-Y ; 2-Z bit3 and 4 - tap type : 1-single ; 2 -double.

7.1.2.93 BIT_APEX_DATA5_DOUBLE_TAP_TIMING_MASK

```
#define BIT_APEX_DATA5_DOUBLE_TAP_TIMING_MASK (0x3F << BIT_APEX_DATA5_DOUBLE_TAP_TIMING_POS)
```

7.1.2.94 BIT_APEX_DATA5_DOUBLE_TAP_TIMING_POS

```
#define BIT_APEX_DATA5_DOUBLE_TAP_TIMING_POS 0
```

7.1.2.95 BIT_CHIP_CONFIG_RESET_MASK

```
#define BIT_CHIP_CONFIG_RESET_MASK BIT_DEVICE_CONFIG_RESET_MASK
```

7.1.2.96 BIT_CHIP_CONFIG_RESET_POS

```
#define BIT_CHIP_CONFIG_RESET_POS BIT_DEVICE_CONFIG_RESET_POS
```

7.1.2.97 BIT_CHIP_CONFIG_SPI_MODE_MASK

```
#define BIT_CHIP_CONFIG_SPI_MODE_MASK BIT_DEVICE_CONFIG_SPI_MODE_MASK
```

7.1.2.98 BIT_CHIP_CONFIG_SPI_MODE_POS

```
#define BIT_CHIP_CONFIG_SPI_MODE_POS BIT_DEVICE_CONFIG_SPI_MODE_POS
```

7.1.2.99 BIT_DATA_ENDIAN_MASK

```
#define BIT_DATA_ENDIAN_MASK (0x01 << BIT_DATA_ENDIAN_POS)
```

7.1.2.100 BIT_DATA_ENDIAN_POS

```
#define BIT_DATA_ENDIAN_POS 4
```

7.1.2.101 BIT_DEVICE_CONFIG_RESET_MASK

```
#define BIT_DEVICE_CONFIG_RESET_MASK 0x01
```

7.1.2.102 BIT_DEVICE_CONFIG_RESET_POS

```
#define BIT_DEVICE_CONFIG_RESET_POS 0
```

7.1.2.103 BIT_DEVICE_CONFIG_SPI_MODE_MASK

```
#define BIT_DEVICE_CONFIG_SPI_MODE_MASK (0x1 << BIT_DEVICE_CONFIG_SPI_MODE_POS)
```

7.1.2.104 BIT_DEVICE_CONFIG_SPI_MODE_POS

```
#define BIT_DEVICE_CONFIG_SPI_MODE_POS 4
```

7.1.2.105 BIT_DMP_MEM_ACCESS_EN

```
#define BIT_DMP_MEM_ACCESS_EN 0x08
```

7.1.2.106 BIT_FDR_CONFIG_FDR_SEL_MASK

```
#define BIT_FDR_CONFIG_FDR_SEL_MASK 0x7F
```

7.1.2.107 BIT_FDR_CONFIG_FDR_SEL_POS

```
#define BIT_FDR_CONFIG_FDR_SEL_POS 0
```

7.1.2.108 BIT_FIFO_CONFIG1_ACCEL_MASK

```
#define BIT_FIFO_CONFIG1_ACCEL_MASK 0x1
```

7.1.2.109 BIT_FIFO_CONFIG1_ACCEL_POS

```
#define BIT_FIFO_CONFIG1_ACCEL_POS 0
```

7.1.2.110 BIT_FIFO_CONFIG1_GYRO_MASK

```
#define BIT_FIFO_CONFIG1_GYRO_MASK (0x1 << BIT_FIFO_CONFIG1_GYRO_POS)
```

7.1.2.111 BIT_FIFO_CONFIG1_GYRO_POS

```
#define BIT_FIFO_CONFIG1_GYRO_POS 1
```

7.1.2.112 BIT_FIFO_CONFIG1_HIRES_MASK

```
#define BIT_FIFO_CONFIG1_HIRES_MASK (0x1 << BIT_FIFO_CONFIG1_HIRES_POS)
```

7.1.2.113 BIT_FIFO_CONFIG1_HIRES_POS

```
#define BIT_FIFO_CONFIG1_HIRES_POS 4
```

7.1.2.114 BIT_FIFO_CONFIG1_RESUME_PARTIAL_RD_MASK

```
#define BIT_FIFO_CONFIG1_RESUME_PARTIAL_RD_MASK (0x1 << BIT_FIFO_CONFIG1_RESUME_PARTIAL_RD_POS)
```

7.1.2.115 BIT_FIFO_CONFIG1_RESUME_PARTIAL_RD_POS

```
#define BIT_FIFO_CONFIG1_RESUME_PARTIAL_RD_POS 6
```

7.1.2.116 BIT_FIFO_CONFIG1_TEMP_MASK

```
#define BIT_FIFO_CONFIG1_TEMP_MASK (0x1 << BIT_FIFO_CONFIG1_TEMP_POS)
```

7.1.2.117 BIT_FIFO_CONFIG1_TEMP_POS

```
#define BIT_FIFO_CONFIG1_TEMP_POS 2
```

7.1.2.118 BIT_FIFO_CONFIG1_TMST_FSYNC_MASK

```
#define BIT_FIFO_CONFIG1_TMST_FSYNC_MASK (0x1 << BIT_FIFO_CONFIG1_TMST_FSYNC_POS)
```

7.1.2.119 BIT_FIFO_CONFIG1_TMST_FSYNC_POS

```
#define BIT_FIFO_CONFIG1_TMST_FSYNC_POS 3
```

7.1.2.120 BIT_FIFO_CONFIG1_WM_GT_TH_MASK

```
#define BIT_FIFO_CONFIG1_WM_GT_TH_MASK (0x1 << BIT_FIFO_CONFIG1_WM_GT_TH_POS)
```

7.1.2.121 BIT_FIFO_CONFIG1_WM_GT_TH_POS

```
#define BIT_FIFO_CONFIG1_WM_GT_TH_POS 5
```

7.1.2.122 BIT_FIFO_CONFIG_MODE_MASK

```
#define BIT_FIFO_CONFIG_MODE_MASK (0x03 << BIT_FIFO_CONFIG_MODE_POS)
```

7.1.2.123 BIT_FIFO_CONFIG_MODE_POS

```
#define BIT_FIFO_CONFIG_MODE_POS 6
```

7.1.2.124 BIT_FIFO_COUNT_ENDIAN_MASK

```
#define BIT_FIFO_COUNT_ENDIAN_MASK (0x01 << BIT_FIFO_COUNT_ENDIAN_POS)
```

7.1.2.125 BIT_FIFO_COUNT_ENDIAN_POS

```
#define BIT_FIFO_COUNT_ENDIAN_POS 5
```

7.1.2.126 BIT_FIFO_COUNT_REC_MASK

```
#define BIT_FIFO_COUNT_REC_MASK (0x01 << BIT_FIFO_COUNT_REC_POS)
```

7.1.2.127 BIT_FIFO_COUNT_REC_POS

```
#define BIT_FIFO_COUNT_REC_POS 6
```

7.1.2.128 BIT_FIFO_MEM_RD_SYS

```
#define BIT_FIFO_MEM_RD_SYS 0x02
```

7.1.2.129 BIT_FIFO_MEM_WR_SER

```
#define BIT_FIFO_MEM_WR_SER 0x01
```

7.1.2.130 BIT_FIFO_SREG_INVALID_IND_MASK

```
#define BIT_FIFO_SREG_INVALID_IND_MASK (0x01 << BIT_FIFO_SREG_INVALID_IND_POS)
```

7.1.2.131 BIT_FIFO_SREG_INVALID_IND_POS

```
#define BIT_FIFO_SREG_INVALID_IND_POS 7
```

7.1.2.132 BIT_FSYNC_CONFIG_UI_SEL_MASK

```
#define BIT_FSYNC_CONFIG_UI_SEL_MASK (0x7 << BIT_FSYNC_CONFIG_UI_SEL_POS)
```

7.1.2.133 BIT_FSYNC_CONFIG_UI_SEL_POS

```
#define BIT_FSYNC_CONFIG_UI_SEL_POS 4
```

7.1.2.134 BIT_GYRO_AAF_BITSHIFT_MASK

```
#define BIT_GYRO_AAF_BITSHIFT_MASK (0x0F << BIT_GYRO_AAF_BITSHIFT_POS)
```

7.1.2.135 BIT_GYRO_AAF_BITSHIFT_POS

```
#define BIT_GYRO_AAF_BITSHIFT_POS 4
```

7.1.2.136 BIT_GYRO_AAF_DELT_MASK

```
#define BIT_GYRO_AAF_DELT_MASK (0x3F << BIT_GYRO_AAF_DELT_POS)
```

7.1.2.137 BIT_GYRO_AAF_DELT_POS

```
#define BIT_GYRO_AAF_DELT_POS 0
```

7.1.2.138 BIT_GYRO_AAF_DELTSQR_MASK_HI

```
#define BIT_GYRO_AAF_DELTSQR_MASK_HI (0x0F << BIT_GYRO_AAF_DELTSQR_POS_HI)
```

7.1.2.139 BIT_GYRO_AAF_DELTSQR_MASK_LO

```
#define BIT_GYRO_AAF_DELTSQR_MASK_LO (0xFF << BIT_GYRO_AAF_DELTSQR_POS_LO)
```

7.1.2.140 BIT_GYRO_AAF_DELTSQR_POS_HI

```
#define BIT_GYRO_AAF_DELTSQR_POS_HI 0
```

7.1.2.141 BIT_GYRO_AAF_DELTSQR_POS_LO

```
#define BIT_GYRO_AAF_DELTSQR_POS_LO 0
```

7.1.2.142 BIT_GYRO_AAF_DIS_MASK

```
#define BIT_GYRO_AAF_DIS_MASK (0x01 << BIT_GYRO_AAF_DIS_POS)
```

7.1.2.143 BIT_GYRO_AAF_DIS_POS

```
#define BIT_GYRO_AAF_DIS_POS 1
```

7.1.2.144 BIT_GYRO_ACCEL_CONFIG0_ACCEL_FILT_MASK

```
#define BIT_GYRO_ACCEL_CONFIG0_ACCEL_FILT_MASK (0xF << BIT_GYRO_ACCEL_CONFIG0_ACCEL_FILT_POS)
```

7.1.2.145 BIT_GYRO_ACCEL_CONFIG0_ACCEL_FILT_POS

```
#define BIT_GYRO_ACCEL_CONFIG0_ACCEL_FILT_POS 4
```

7.1.2.146 BIT_GYRO_ACCEL_CONFIG0_GYRO_FILT_MASK

```
#define BIT_GYRO_ACCEL_CONFIG0_GYRO_FILT_MASK 0x0F
```

7.1.2.147 BIT_GYRO_ACCEL_CONFIG0_GYRO_FILT_POS

```
#define BIT_GYRO_ACCEL_CONFIG0_GYRO_FILT_POS 0
```

7.1.2.148 BIT_GYRO_CONFIG0_FS_SEL_MASK

```
#define BIT_GYRO_CONFIG0_FS_SEL_MASK (7 << BIT_GYRO_CONFIG0_FS_SEL_POS)
```

7.1.2.149 BIT_GYRO_CONFIG0_FS_SEL_POS

```
#define BIT_GYRO_CONFIG0_FS_SEL_POS 5
```

7.1.2.150 BIT_GYRO_CONFIG0_ODR_MASK

```
#define BIT_GYRO_CONFIG0_ODR_MASK 0x0F
```

7.1.2.151 BIT_GYRO_CONFIG0_ODR_POS

```
#define BIT_GYRO_CONFIG0_ODR_POS 0
```

7.1.2.152 BIT_GYRO_CONFIG1_GYRO_DEC2_M2_ORD_MASK

```
#define BIT_GYRO_CONFIG1_GYRO_DEC2_M2_ORD_MASK 0x3
```

7.1.2.153 BIT_GYRO_CONFIG1_GYRO_DEC2_M2_ORD_POS

```
#define BIT_GYRO_CONFIG1_GYRO_DEC2_M2_ORD_POS 0
```

7.1.2.154 BIT_GYRO_CONFIG1_GYRO_UI_FILT_ORD_MASK

```
#define BIT_GYRO_CONFIG1_GYRO_UI_FILT_ORD_MASK (0x3 << BIT_GYRO_CONFIG1_GYRO_UI_FILT_ORD_POS)
```

7.1.2.155 BIT_GYRO_CONFIG1_GYRO_UI_FILT_ORD_POS

```
#define BIT_GYRO_CONFIG1_GYRO_UI_FILT_ORD_POS 2
```

7.1.2.156 BIT_GYRO_CONFIG1_TEMP_FILT_BW_MASK

```
#define BIT_GYRO_CONFIG1_TEMP_FILT_BW_MASK (0x7 << BIT_GYRO_CONFIG1_TEMP_FILT_BW_POS)
```

7.1.2.157 BIT_GYRO_CONFIG1_TEMP_FILT_BW_POS

```
#define BIT_GYRO_CONFIG1_TEMP_FILT_BW_POS 5
```

7.1.2.158 BIT_GYRO_NF_DIS_MASK

```
#define BIT_GYRO_NF_DIS_MASK (0x01 << BIT_GYRO_NF_DIS_POS)
```

7.1.2.159 BIT_GYRO_NF_DIS_POS

```
#define BIT_GYRO_NF_DIS_POS 0
```

7.1.2.160 BIT_GYRO_X_OFFUSER_MASK_HI

```
#define BIT_GYRO_X_OFFUSER_MASK_HI (0x0F << BIT_GYRO_X_OFFUSER_POS_HI)
```

7.1.2.161 BIT_GYRO_X_OFFUSER_MASK_LO

```
#define BIT_GYRO_X_OFFUSER_MASK_LO (0xFF << BIT_GYRO_X_OFFUSER_POS_LO)
```

7.1.2.162 BIT_GYRO_X_OFFUSER_POS_HI

```
#define BIT_GYRO_X_OFFUSER_POS_HI 0
```

7.1.2.163 BIT_GYRO_X_OFFUSER_POS_LO

```
#define BIT_GYRO_X_OFFUSER_POS_LO 0
```

7.1.2.164 BIT_GYRO_X_ST_EN

```
#define BIT_GYRO_X_ST_EN 0x01
```

7.1.2.165 BIT_GYRO_Y_OFFUSER_MASK_HI

```
#define BIT_GYRO_Y_OFFUSER_MASK_HI (0x0F << BIT_GYRO_Y_OFFUSER_POS_HI)
```

7.1.2.166 BIT_GYRO_Y_OFFUSER_MASK_LO

```
#define BIT_GYRO_Y_OFFUSER_MASK_LO (0xFF << BIT_GYRO_Y_OFFUSER_POS_LO)
```

7.1.2.167 BIT_GYRO_Y_OFFUSER_POS_HI

```
#define BIT_GYRO_Y_OFFUSER_POS_HI 4
```

7.1.2.168 BIT_GYRO_Y_OFFUSER_POS_LO

```
#define BIT_GYRO_Y_OFFUSER_POS_LO 0
```

7.1.2.169 BIT_GYRO_Y_ST_EN

```
#define BIT_GYRO_Y_ST_EN 0x02
```

7.1.2.170 BIT_GYRO_Z_OFFUSER_MASK_HI

```
#define BIT_GYRO_Z_OFFUSER_MASK_HI (0x0F << BIT_GYRO_Z_OFFUSER_POS_HI)
```

7.1.2.171 BIT_GYRO_Z_OFFUSER_MASK_LO

```
#define BIT_GYRO_Z_OFFUSER_MASK_LO (0xFF << BIT_GYRO_Z_OFFUSER_POS_LO)
```

7.1.2.172 BIT_GYRO_Z_OFFUSER_POS_HI

```
#define BIT_GYRO_Z_OFFUSER_POS_HI 0
```

7.1.2.173 BIT_GYRO_Z_OFFUSER_POS_LO

```
#define BIT_GYRO_Z_OFFUSER_POS_LO 0
```

7.1.2.174 BIT_GYRO_Z_ST_EN

```
#define BIT_GYRO_Z_ST_EN 0x04
```

7.1.2.175 BIT_INT_CONFIG1_ASY_RST_MASK

```
#define BIT_INT_CONFIG1_ASY_RST_MASK (0x1 << BIT_INT_CONFIG1_ASY_RST_POS)
```

7.1.2.176 BIT_INT_CONFIG1_ASY_RST_POS

```
#define BIT_INT_CONFIG1_ASY_RST_POS 4
```

7.1.2.177 BIT_INT_CONFIG_INT1_DRIVE_CIRCUIT_MASK

```
#define BIT_INT_CONFIG_INT1_DRIVE_CIRCUIT_MASK (0x01 << BIT_INT_CONFIG_INT1_DRIVE_CIRCUIT_POS)
```

7.1.2.178 BIT_INT_CONFIG_INT1_DRIVE_CIRCUIT_POS

```
#define BIT_INT_CONFIG_INT1_DRIVE_CIRCUIT_POS 1
```

7.1.2.179 BIT_INT_CONFIG_INT1_POLARITY_MASK

```
#define BIT_INT_CONFIG_INT1_POLARITY_MASK 0x01
```

7.1.2.180 BIT_INT_CONFIG_INT1_POLARITY_POS

```
#define BIT_INT_CONFIG_INT1_POLARITY_POS 0
```

7.1.2.181 BIT_INT_CONFIG_INT2_DRIVE_CIRCUIT_MASK

```
#define BIT_INT_CONFIG_INT2_DRIVE_CIRCUIT_MASK (0x01 << BIT_INT_CONFIG_INT2_DRIVE_CIRCUIT_POS)
```

7.1.2.182 BIT_INT_CONFIG_INT2_DRIVE_CIRCUIT_POS

```
#define BIT_INT_CONFIG_INT2_DRIVE_CIRCUIT_POS 4
```

7.1.2.183 BIT_INT_CONFIG_INT2_POLARITY_MASK

```
#define BIT_INT_CONFIG_INT2_POLARITY_MASK (0x01 << BIT_INT_CONFIG_INT2_POLARITY_POS)
```

7.1.2.184 BIT_INT_CONFIG_INT2_POLARITY_POS

```
#define BIT_INT_CONFIG_INT2_POLARITY_POS 3
```

7.1.2.185 BIT_INT_FIFO_FULL_IBI_EN_POS

```
#define BIT_INT_FIFO_FULL_IBI_EN_POS 1
```

7.1.2.186 BIT_INT_FIFO_FULL_INT_EN_POS

```
#define BIT_INT_FIFO_FULL_INT_EN_POS 1
```

7.1.2.187 BIT_INT_FIFO_THS_IBI_EN_POS

```
#define BIT_INT_FIFO_THS_IBI_EN_POS 2
```

7.1.2.188 BIT_INT_FIFO_THS_INT_EN_POS

```
#define BIT_INT_FIFO_THS_INT_EN_POS 2
```

7.1.2.189 BIT_INT_OIS1_DRDY_IBI_EN_POS

```
#define BIT_INT_OIS1_DRDY_IBI_EN_POS 6
```

7.1.2.190 BIT_INT_PLL_RDY_IBI_EN_POS

```
#define BIT_INT_PLL_RDY_IBI_EN_POS 4
```

7.1.2.191 BIT_INT_PLL_RDY_INT_EN_POS

```
#define BIT_INT_PLL_RDY_INT_EN_POS 5
```

7.1.2.192 BIT_INT_RESET_DONE_INT_EN_POS

```
#define BIT_INT_RESET_DONE_INT_EN_POS 4
```

7.1.2.193 BIT_INT_SLEEP_DET_IBI_EN_POS

```
#define BIT_INT_SLEEP_DET_IBI_EN_POS 1
```

7.1.2.194 BIT_INT_SLEEP_DET_INT_EN_POS

```
#define BIT_INT_SLEEP_DET_INT_EN_POS 1
```

7.1.2.195 BIT_INT_SMD_IBI_EN_POS

```
#define BIT_INT_SMD_IBI_EN_POS 4
```

7.1.2.196 BIT_INT_SMD_INT_EN_POS

```
#define BIT_INT_SMD_INT_EN_POS 3
```

7.1.2.197 BIT_INT_SOURCE0_FIFO_FULL_INT1_EN

```
#define BIT_INT_SOURCE0_FIFO_FULL_INT1_EN 0x02
```

7.1.2.198 BIT_INT_SOURCE0_FIFO_THS_INT1_EN

```
#define BIT_INT_SOURCE0_FIFO_THS_INT1_EN 0x04
```

7.1.2.199 BIT_INT_SOURCE0_PLL_RDY_INT1_EN

```
#define BIT_INT_SOURCE0_PLL_RDY_INT1_EN 0x20
```

7.1.2.200 BIT_INT_SOURCE0_RESET_DONE_INT1_EN

```
#define BIT_INT_SOURCE0_RESET_DONE_INT1_EN 0x10
```

7.1.2.201 BIT_INT_SOURCE0_UI_AGC_RDY_INT1_EN

```
#define BIT_INT_SOURCE0_UI_AGC_RDY_INT1_EN 0x01
```

7.1.2.202 BIT_INT_SOURCE0_UI_DRDY_INT1_EN

```
#define BIT_INT_SOURCE0_UI_DRDY_INT1_EN 0x08
```

7.1.2.203 BIT_INT_SOURCE0_UI_FSYNC_INT1_EN

```
#define BIT_INT_SOURCE0_UI_FSYNC_INT1_EN 0x40
```

7.1.2.204 BIT_INT_SOURCE10_SLEEP_DET_IBI_EN

```
#define BIT_INT_SOURCE10_SLEEP_DET_IBI_EN 0x02
```

7.1.2.205 BIT_INT_SOURCE10_STEP_CNT_OVFL_IBI_EN

```
#define BIT_INT_SOURCE10_STEP_CNT_OVFL_IBI_EN 0x10
```

7.1.2.206 BIT_INT_SOURCE10_STEP_DET_IBI_EN

```
#define BIT_INT_SOURCE10_STEP_DET_IBI_EN 0x20
```

7.1.2.207 BIT_INT_SOURCE10_TAP_DET_IBI_EN

```
#define BIT_INT_SOURCE10_TAP_DET_IBI_EN 0x01
```

7.1.2.208 BIT_INT_SOURCE10_TILT_DET_IBI_EN

```
#define BIT_INT_SOURCE10_TILT_DET_IBI_EN 0x08
```

7.1.2.209 BIT_INT_SOURCE10_WAKE_DET_IBI_EN

```
#define BIT_INT_SOURCE10_WAKE_DET_IBI_EN 0x04
```

7.1.2.210 BIT_INT_SOURCE1_SMD_INT1_EN

```
#define BIT_INT_SOURCE1_SMD_INT1_EN 0x08
```

7.1.2.211 BIT_INT_SOURCE1_WOM_X_INT1_EN

```
#define BIT_INT_SOURCE1_WOM_X_INT1_EN 0x01
```

7.1.2.212 BIT_INT_SOURCE1_WOM_Y_INT1_EN

```
#define BIT_INT_SOURCE1_WOM_Y_INT1_EN 0x02
```

7.1.2.213 BIT_INT_SOURCE1_WOM_Z_INT1_EN

```
#define BIT_INT_SOURCE1_WOM_Z_INT1_EN 0x04
```

7.1.2.214 BIT_INT_SOURCE2_OIS1_AGC_RDY_INT1_EN

```
#define BIT_INT_SOURCE2_OIS1_AGC_RDY_INT1_EN 0x04
```

7.1.2.215 BIT_INT_SOURCE2_OIS1_DRDY_INT1_EN

```
#define BIT_INT_SOURCE2_OIS1_DRDY_INT1_EN 0x01
```

7.1.2.216 BIT_INT_SOURCE2_OIS1_FSYNC_INT1_EN

```
#define BIT_INT_SOURCE2_OIS1_FSYNC_INT1_EN 0x02
```

7.1.2.217 BIT_INT_SOURCE2_OIS2_AGC_RDY_INT1_EN

```
#define BIT_INT_SOURCE2_OIS2_AGC_RDY_INT1_EN 0x20
```

7.1.2.218 BIT_INT_SOURCE2_OIS2_DRDY_INT1_EN

```
#define BIT_INT_SOURCE2_OIS2_DRDY_INT1_EN 0x08
```

7.1.2.219 BIT_INT_SOURCE2_OIS2_FSYNC_INT1_EN

```
#define BIT_INT_SOURCE2_OIS2_FSYNC_INT1_EN 0x10
```

7.1.2.220 BIT_INT_SOURCE3_FIFO_FULL_INT2_EN

```
#define BIT_INT_SOURCE3_FIFO_FULL_INT2_EN 0x02
```

7.1.2.221 BIT_INT_SOURCE3_FIFO_THS_INT2_EN

```
#define BIT_INT_SOURCE3_FIFO_THS_INT2_EN 0x04
```

7.1.2.222 BIT_INT_SOURCE3_PLL_RDY_INT2_EN

```
#define BIT_INT_SOURCE3_PLL_RDY_INT2_EN 0x20
```

7.1.2.223 BIT_INT_SOURCE3_RESET_DONE_INT2_EN

```
#define BIT_INT_SOURCE3_RESET_DONE_INT2_EN 0x10
```

7.1.2.224 BIT_INT_SOURCE3_UI_AGC_RDY_INT2_EN

```
#define BIT_INT_SOURCE3_UI_AGC_RDY_INT2_EN 0x01
```

7.1.2.225 BIT_INT_SOURCE3_UI_DRDY_INT2_EN

```
#define BIT_INT_SOURCE3_UI_DRDY_INT2_EN 0x08
```

7.1.2.226 BIT_INT_SOURCE3_UI_FSYNC_INT2_EN

```
#define BIT_INT_SOURCE3_UI_FSYNC_INT2_EN 0x40
```

7.1.2.227 BIT_INT_SOURCE4_SMD_INT2_EN

```
#define BIT_INT_SOURCE4_SMD_INT2_EN 0x08
```

7.1.2.228 BIT_INT_SOURCE4_WOM_X_INT2_EN

```
#define BIT_INT_SOURCE4_WOM_X_INT2_EN 0x01
```

7.1.2.229 BIT_INT_SOURCE4_WOM_Y_INT2_EN

```
#define BIT_INT_SOURCE4_WOM_Y_INT2_EN 0x02
```

7.1.2.230 BIT_INT_SOURCE4_WOM_Z_INT2_EN

```
#define BIT_INT_SOURCE4_WOM_Z_INT2_EN 0x04
```

7.1.2.231 BIT_INT_SOURCE5_OIS1_AGC_RDY_INT2_EN

```
#define BIT_INT_SOURCE5_OIS1_AGC_RDY_INT2_EN 0x04
```

7.1.2.232 BIT_INT_SOURCE5_OIS1_DRDY_INT2_EN

```
#define BIT_INT_SOURCE5_OIS1_DRDY_INT2_EN 0x01
```

7.1.2.233 BIT_INT_SOURCE5_OIS1_FSYNC_INT2_EN

```
#define BIT_INT_SOURCE5_OIS1_FSYNC_INT2_EN 0x02
```

7.1.2.234 BIT_INT_SOURCE5_OIS2_AGC_RDY_INT2_EN

```
#define BIT_INT_SOURCE5_OIS2_AGC_RDY_INT2_EN 0x20
```

7.1.2.235 BIT_INT_SOURCE5_OIS2_DRDY_INT2_EN

```
#define BIT_INT_SOURCE5_OIS2_DRDY_INT2_EN 0x08
```

7.1.2.236 BIT_INT_SOURCE5_OIS2_FSYNC_INT2_EN

```
#define BIT_INT_SOURCE5_OIS2_FSYNC_INT2_EN 0x10
```

7.1.2.237 BIT_INT_SOURCE6_SLEEP_DET_INT1_EN

```
#define BIT_INT_SOURCE6_SLEEP_DET_INT1_EN 0x2
```

7.1.2.238 BIT_INT_SOURCE6_STEP_CNT_OVFL_INT1_EN

```
#define BIT_INT_SOURCE6_STEP_CNT_OVFL_INT1_EN 0x10
```

7.1.2.239 BIT_INT_SOURCE6_STEP_DET_INT1_EN

```
#define BIT_INT_SOURCE6_STEP_DET_INT1_EN 0x20
```

7.1.2.240 BIT_INT_SOURCE6_TAP_DET_INT1_EN

```
#define BIT_INT_SOURCE6_TAP_DET_INT1_EN 0x1
```

7.1.2.241 BIT_INT_SOURCE6_TILT_DET_INT1_EN

```
#define BIT_INT_SOURCE6_TILT_DET_INT1_EN 0x8
```

7.1.2.242 BIT_INT_SOURCE6_WAKE_DET_INT1_EN

```
#define BIT_INT_SOURCE6_WAKE_DET_INT1_EN 0x4
```

7.1.2.243 BIT_INT_SOURCE7_SLEEP_DET_INT2_EN

```
#define BIT_INT_SOURCE7_SLEEP_DET_INT2_EN 0x2
```

7.1.2.244 BIT_INT_SOURCE7_STEP_CNT_OVFL_INT2_EN

```
#define BIT_INT_SOURCE7_STEP_CNT_OVFL_INT2_EN 0x10
```

7.1.2.245 BIT_INT_SOURCE7_STEP_DET_INT2_EN

```
#define BIT_INT_SOURCE7_STEP_DET_INT2_EN 0x20
```

7.1.2.246 BIT_INT_SOURCE7_TAP_DET_INT2_EN

```
#define BIT_INT_SOURCE7_TAP_DET_INT2_EN 0x1
```

7.1.2.247 BIT_INT_SOURCE7_TILT_DET_INT2_EN

```
#define BIT_INT_SOURCE7_TILT_DET_INT2_EN 0x8
```

7.1.2.248 BIT_INT_SOURCE7_WAKE_DET_INT2_EN

```
#define BIT_INT_SOURCE7_WAKE_DET_INT2_EN 0x4
```

7.1.2.249 BIT_INT_SOURCE8_FIFO_FULL_IBI_EN

```
#define BIT_INT_SOURCE8_FIFO_FULL_IBI_EN 0x02
```

7.1.2.250 BIT_INT_SOURCE8_FIFO_THS_IBI_EN

```
#define BIT_INT_SOURCE8_FIFO_THS_IBI_EN 0x04
```

7.1.2.251 BIT_INT_SOURCE8_OIS1_DRDY_IBI_EN

```
#define BIT_INT_SOURCE8_OIS1_DRDY_IBI_EN 0x40
```

7.1.2.252 BIT_INT_SOURCE8_PLL_RDY_IBI_EN

```
#define BIT_INT_SOURCE8_PLL_RDY_IBI_EN 0x10
```

7.1.2.253 BIT_INT_SOURCE8_UI_AGC_RDY_IBI_EN

```
#define BIT_INT_SOURCE8_UI_AGC_RDY_IBI_EN 0x01
```

7.1.2.254 BIT_INT_SOURCE8_UI_DRDY_IBI_EN

```
#define BIT_INT_SOURCE8_UI_DRDY_IBI_EN 0x08
```

7.1.2.255 BIT_INT_SOURCE8_UI_FSYNC_IBI_EN

```
#define BIT_INT_SOURCE8_UI_FSYNC_IBI_EN 0x20
```

7.1.2.256 BIT_INT_SOURCE9_SMD_IBI_EN

```
#define BIT_INT_SOURCE9_SMD_IBI_EN 0x10
```

7.1.2.257 BIT_INT_SOURCE9_WOM_X_IBI_EN

```
#define BIT_INT_SOURCE9_WOM_X_IBI_EN 0x02
```

7.1.2.258 BIT_INT_SOURCE9_WOM_Y_IBI_EN

```
#define BIT_INT_SOURCE9_WOM_Y_IBI_EN 0x04
```

7.1.2.259 BIT_INT_SOURCE9_WOM_Z_IBI_EN

```
#define BIT_INT_SOURCE9_WOM_Z_IBI_EN 0x08
```

7.1.2.260 BIT_INT_STATUS2_SMD_INT

```
#define BIT_INT_STATUS2_SMD_INT 0x08
```

7.1.2.261 BIT_INT_STATUS2_WOM_X_INT

```
#define BIT_INT_STATUS2_WOM_X_INT 0x01
```

7.1.2.262 BIT_INT_STATUS2_WOM_Y_INT

```
#define BIT_INT_STATUS2_WOM_Y_INT 0x02
```

7.1.2.263 BIT_INT_STATUS2_WOM_Z_INT

```
#define BIT_INT_STATUS2_WOM_Z_INT 0x04
```

7.1.2.264 BIT_INT_STATUS3_SLEEP_DET

```
#define BIT_INT_STATUS3_SLEEP_DET 0x02
```

7.1.2.265 BIT_INT_STATUS3_STEP_CNT_OVFL

```
#define BIT_INT_STATUS3_STEP_CNT_OVFL 0x10
```

7.1.2.266 BIT_INT_STATUS3_STEP_DET

```
#define BIT_INT_STATUS3_STEP_DET 0x20
```

7.1.2.267 BIT_INT_STATUS3_TAP_DET

```
#define BIT_INT_STATUS3_TAP_DET 0x01
```

7.1.2.268 BIT_INT_STATUS3_TILT_DET

```
#define BIT_INT_STATUS3_TILT_DET 0x08
```

7.1.2.269 BIT_INT_STATUS3_WAKE_DET

```
#define BIT_INT_STATUS3_WAKE_DET 0x04
```

7.1.2.270 BIT_INT_STATUS_AGC_RDY

```
#define BIT_INT_STATUS_AGC_RDY 0x01
```

7.1.2.271 BIT_INT_STATUS_DRDY

```
#define BIT_INT_STATUS_DRDY 0x08
```

7.1.2.272 BIT_INT_STATUS_FIFO_FULL

```
#define BIT_INT_STATUS_FIFO_FULL 0x02
```

7.1.2.273 BIT_INT_STATUS_FIFO_THS

```
#define BIT_INT_STATUS_FIFO_THS 0x04
```

7.1.2.274 BIT_INT_STATUS_OIS1_AGC_RDY

```
#define BIT_INT_STATUS_OIS1_AGC_RDY 0x01
```

7.1.2.275 BIT_INT_STATUS_OIS1_DRDY

```
#define BIT_INT_STATUS_OIS1_DRDY 0x02
```

7.1.2.276 BIT_INT_STATUS_OIS1_FSYNC

```
#define BIT_INT_STATUS_OIS1_FSYNC 0x04
```

7.1.2.277 BIT_INT_STATUS_OIS2_AGC_RDY

```
#define BIT_INT_STATUS_OIS2_AGC_RDY 0x01
```

7.1.2.278 BIT_INT_STATUS_OIS2_DRDY

```
#define BIT_INT_STATUS_OIS2_DRDY 0x02
```

7.1.2.279 BIT_INT_STATUS_OIS2_FSYNC

```
#define BIT_INT_STATUS_OIS2_FSYNC 0x04
```

7.1.2.280 BIT_INT_STATUS_PLL_RDY

```
#define BIT_INT_STATUS_PLL_RDY 0x20
```

7.1.2.281 BIT_INT_STATUS_RESET_DONE

```
#define BIT_INT_STATUS_RESET_DONE 0x10
```

7.1.2.282 BIT_INT_STATUS_UI_FSYNC

```
#define BIT_INT_STATUS_UI_FSYNC 0x40
```

7.1.2.283 BIT_INT_STEP_CNT_OVFL_IBI_EN_POS

```
#define BIT_INT_STEP_CNT_OVFL_IBI_EN_POS 4
```

7.1.2.284 BIT_INT_STEP_CNT_OVFL_INT_EN_POS

```
#define BIT_INT_STEP_CNT_OVFL_INT_EN_POS 4
```

7.1.2.285 BIT_INT_STEP_DET_IBI_EN_POS

```
#define BIT_INT_STEP_DET_IBI_EN_POS 5
```

7.1.2.286 BIT_INT_STEP_DET_INT_EN_POS

```
#define BIT_INT_STEP_DET_INT_EN_POS 5
```

7.1.2.287 BIT_INT_TAP_DET_IBI_EN_POS

```
#define BIT_INT_TAP_DET_IBI_EN_POS 0
```

7.1.2.288 BIT_INT_TAP_DET_INT_EN_POS

```
#define BIT_INT_TAP_DET_INT_EN_POS 0
```

7.1.2.289 BIT_INT_TDEASSERT_MASK

```
#define BIT_INT_TDEASSERT_MASK (0x1 << BIT_INT_TDEASSERT_POS)
```

7.1.2.290 BIT_INT_TDEASSERT_POS

```
#define BIT_INT_TDEASSERT_POS 5
```

7.1.2.291 BIT_INT_TILT_DET_IBI_EN_POS

```
#define BIT_INT_TILT_DET_IBI_EN_POS 3
```

7.1.2.292 BIT_INT_TILT_DET_INT_EN_POS

```
#define BIT_INT_TILT_DET_INT_EN_POS 3
```

7.1.2.293 BIT_INT_TPULSE_DURATION_MASK

```
#define BIT_INT_TPULSE_DURATION_MASK (0x1 << BIT_INT_TPULSE_DURATION_POS)
```

7.1.2.294 BIT_INT_TPULSE_DURATION_POS

```
#define BIT_INT_TPULSE_DURATION_POS 6
```

7.1.2.295 BIT_INT_UI_AGC_RDY_IBI_EN_POS

```
#define BIT_INT_UI_AGC_RDY_IBI_EN_POS 0
```

7.1.2.296 BIT_INT_UI_AGC_RDY_INT_EN_POS

```
#define BIT_INT_UI_AGC_RDY_INT_EN_POS 0
```

7.1.2.297 BIT_INT_UI_DRDY_IBI_EN_POS

```
#define BIT_INT_UI_DRDY_IBI_EN_POS 3
```

7.1.2.298 BIT_INT_UI_DRDY_INT_EN_POS

```
#define BIT_INT_UI_DRDY_INT_EN_POS 3
```

7.1.2.299 BIT_INT_UI_FSYNC_IBI_EN_POS

```
#define BIT_INT_UI_FSYNC_IBI_EN_POS 5
```

7.1.2.300 BIT_INT_UI_FSYNC_INT_EN_POS

```
#define BIT_INT_UI_FSYNC_INT_EN_POS 6
```

7.1.2.301 BIT_INT_WAKE_DET_IBI_EN_POS

```
#define BIT_INT_WAKE_DET_IBI_EN_POS 2
```

7.1.2.302 BIT_INT_WAKE_DET_INT_EN_POS

```
#define BIT_INT_WAKE_DET_INT_EN_POS 2
```

7.1.2.303 BIT_INT_WOM_X_IBI_EN_POS

```
#define BIT_INT_WOM_X_IBI_EN_POS 1
```

7.1.2.304 BIT_INT_WOM_X_INT_EN_POS

```
#define BIT_INT_WOM_X_INT_EN_POS 0
```

7.1.2.305 BIT_INT_WOM_Y_IBI_EN_POS

```
#define BIT_INT_WOM_Y_IBI_EN_POS 2
```

7.1.2.306 BIT_INT_WOM_Y_INT_EN_POS

```
#define BIT_INT_WOM_Y_INT_EN_POS 1
```

7.1.2.307 BIT_INT_WOM_Z_IBI_EN_POS

```
#define BIT_INT_WOM_Z_IBI_EN_POS 3
```

7.1.2.308 BIT_INT_WOM_Z_INT_EN_POS

```
#define BIT_INT_WOM_Z_INT_EN_POS 2
```

7.1.2.309 BIT_INTF_CONFIG4_AP_SPI_MASK

```
#define BIT_INTF_CONFIG4_AP_SPI_MASK (0x1 << BIT_INTF_CONFIG4_AP_SPI_POS)
```

7.1.2.310 BIT_INTF_CONFIG4_AP_SPI_POS

```
#define BIT_INTF_CONFIG4_AP_SPI_POS 1
```

7.1.2.311 BIT_INTF_CONFIG4_AUX1_SPI_MASK

```
#define BIT_INTF_CONFIG4_AUX1_SPI_MASK (0x1 << BIT_INTF_CONFIG4_AUX1_SPI_POS)
```

7.1.2.312 BIT_INTF_CONFIG4_AUX1_SPI_POS

```
#define BIT_INTF_CONFIG4_AUX1_SPI_POS 2
```

7.1.2.313 BIT_INTF_CONFIG5_GPIO_PAD_SEL_MASK

```
#define BIT_INTF_CONFIG5_GPIO_PAD_SEL_MASK (0x3 << BIT_INTF_CONFIG5_GPIO_PAD_SEL_POS)
```

7.1.2.314 BIT_INTF_CONFIG5_GPIO_PAD_SEL_POS

```
#define BIT_INTF_CONFIG5_GPIO_PAD_SEL_POS 1
```

7.1.2.315 BIT_INTF_CONFIG6_I3C_DDR_EN_MASK

```
#define BIT_INTF_CONFIG6_I3C_DDR_EN_MASK (0x1 << BIT_INTF_CONFIG6_I3C_DDR_EN_POS)
```

7.1.2.316 BIT_INTF_CONFIG6_I3C_DDR_EN_POS

```
#define BIT_INTF_CONFIG6_I3C_DDR_EN_POS 1
```

7.1.2.317 BIT_INTF_CONFIG6_I3C_IBI_BYTE_EN_MASK

```
#define BIT_INTF_CONFIG6_I3C_IBI_BYTE_EN_MASK (0x1 << BIT_INTF_CONFIG6_I3C_IBI_BYTE_EN_POS)
```

7.1.2.318 BIT_INTF_CONFIG6_I3C_IBI_BYTE_EN_POS

```
#define BIT_INTF_CONFIG6_I3C_IBI_BYTE_EN_POS 3
```

7.1.2.319 BIT_INTF_CONFIG6_I3C_IBI_EN_MASK

```
#define BIT_INTF_CONFIG6_I3C_IBI_EN_MASK (0x1 << BIT_INTF_CONFIG6_I3C_IBI_EN_POS)
```

7.1.2.320 BIT_INTF_CONFIG6_I3C_IBI_EN_POS

```
#define BIT_INTF_CONFIG6_I3C_IBI_EN_POS 2
```

7.1.2.321 BIT_INTF_CONFIG6_I3C_SDR_EN_MASK

```
#define BIT_INTF_CONFIG6_I3C_SDR_EN_MASK (0x1 << BIT_INTF_CONFIG6_I3C_SDR_EN_POS)
```

7.1.2.322 BIT_INTF_CONFIG6_I3C_SDR_EN_POS

```
#define BIT_INTF_CONFIG6_I3C_SDR_EN_POS 0
```

7.1.2.323 BIT_MEM_OTP_ACCESS_EN

```
#define BIT_MEM_OTP_ACCESS_EN 0x04
```

7.1.2.324 BIT_OIS1_CONFIG1_ACCEL_EN_MASK

```
#define BIT_OIS1_CONFIG1_ACCEL_EN_MASK (0x1 << BIT_OIS1_CONFIG1_ACCEL_EN_POS)
```

7.1.2.325 BIT_OIS1_CONFIG1_ACCEL_EN_POS

```
#define BIT_OIS1_CONFIG1_ACCEL_EN_POS 0
```

7.1.2.326 BIT_OIS1_CONFIG1_ACCEL_LP_CLK_SEL_MASK

```
#define BIT_OIS1_CONFIG1_ACCEL_LP_CLK_SEL_MASK (0x1 << BIT_OIS1_CONFIG1_ACCEL_LP_CLK_SEL_POS)
```

7.1.2.327 BIT_OIS1_CONFIG1_ACCEL_LP_CLK_SEL_POS

```
#define BIT_OIS1_CONFIG1_ACCEL_LP_CLK_SEL_POS 5
```

7.1.2.328 BIT_OIS1_CONFIG1_DEC_MASK

```
#define BIT_OIS1_CONFIG1_DEC_MASK (0x7 << BIT_OIS1_CONFIG1_DEC_POS)
```

7.1.2.329 BIT_OIS1_CONFIG1_DEC_POS

```
#define BIT_OIS1_CONFIG1_DEC_POS 2
```

7.1.2.330 BIT_OIS1_CONFIG1_GYRO_EN_MASK

```
#define BIT_OIS1_CONFIG1_GYRO_EN_MASK (0x1 << BIT_OIS1_CONFIG1_GYRO_EN_POS)
```

7.1.2.331 BIT_OIS1_CONFIG1_GYRO_EN_POS

```
#define BIT_OIS1_CONFIG1_GYRO_EN_POS 1
```

7.1.2.332 BIT_OIS1_CONFIG2_ACCEL_FS_SEL_MASK

```
#define BIT_OIS1_CONFIG2_ACCEL_FS_SEL_MASK (0x7 << BIT_OIS1_CONFIG2_ACCEL_FS_SEL_POS)
```

7.1.2.333 BIT_OIS1_CONFIG2_ACCEL_FS_SEL_POS

```
#define BIT_OIS1_CONFIG2_ACCEL_FS_SEL_POS 0
```

7.1.2.334 BIT_OIS1_CONFIG2_GYRO_FS_SEL_MASK

```
#define BIT_OIS1_CONFIG2_GYRO_FS_SEL_MASK (0x7 << BIT_OIS1_CONFIG2_GYRO_FS_SEL_POS)
```

7.1.2.335 BIT_OIS1_CONFIG2_GYRO_FS_SEL_POS

```
#define BIT_OIS1_CONFIG2_GYRO_FS_SEL_POS 3
```

7.1.2.336 BIT_OIS2_CONFIG1_ACCEL_EN_MASK

```
#define BIT_OIS2_CONFIG1_ACCEL_EN_MASK (0x1 << BIT_OIS2_CONFIG1_ACCEL_EN_POS)
```

7.1.2.337 BIT_OIS2_CONFIG1_ACCEL_EN_POS

```
#define BIT_OIS2_CONFIG1_ACCEL_EN_POS 0
```

7.1.2.338 BIT_OIS2_CONFIG1_ACCEL_LP_CLK_SEL_MASK

```
#define BIT_OIS2_CONFIG1_ACCEL_LP_CLK_SEL_MASK (0x1 << BIT_OIS2_CONFIG1_ACCEL_LP_CLK_SEL_POS)
```

7.1.2.339 BIT_OIS2_CONFIG1_ACCEL_LP_CLK_SEL_POS

```
#define BIT_OIS2_CONFIG1_ACCEL_LP_CLK_SEL_POS 5
```

7.1.2.340 BIT_OIS2_CONFIG1_DEC_MASK

```
#define BIT_OIS2_CONFIG1_DEC_MASK (0x7 << BIT_OIS2_CONFIG1_DEC_POS)
```

7.1.2.341 BIT_OIS2_CONFIG1_DEC_POS

```
#define BIT_OIS2_CONFIG1_DEC_POS 2
```

7.1.2.342 BIT_OIS2_CONFIG1_GYRO_EN_MASK

```
#define BIT_OIS2_CONFIG1_GYRO_EN_MASK (0x1 << BIT_OIS2_CONFIG1_GYRO_EN_POS)
```

7.1.2.343 BIT_OIS2_CONFIG1_GYRO_EN_POS

```
#define BIT_OIS2_CONFIG1_GYRO_EN_POS 1
```

7.1.2.344 BIT_OIS2_CONFIG2_ACCEL_FS_SEL_MASK

```
#define BIT_OIS2_CONFIG2_ACCEL_FS_SEL_MASK (0x7 << BIT_OIS2_CONFIG2_ACCEL_FS_SEL_POS)
```

7.1.2.345 BIT_OIS2_CONFIG2_ACCEL_FS_SEL_POS

```
#define BIT_OIS2_CONFIG2_ACCEL_FS_SEL_POS 0
```

7.1.2.346 BIT_OIS2_CONFIG2_GYRO_FS_SEL_MASK

```
#define BIT_OIS2_CONFIG2_GYRO_FS_SEL_MASK (0x7 << BIT_OIS2_CONFIG2_GYRO_FS_SEL_POS)
```

7.1.2.347 BIT_OIS2_CONFIG2_GYRO_FS_SEL_POS

```
#define BIT_OIS2_CONFIG2_GYRO_FS_SEL_POS 3
```

7.1.2.348 BIT_PWR_MGMT_0_ACCEL_MODE_MASK

```
#define BIT_PWR_MGMT_0_ACCEL_MODE_MASK 0x03
```

7.1.2.349 BIT_PWR_MGMT_0_ACCEL_MODE_POS

```
#define BIT_PWR_MGMT_0_ACCEL_MODE_POS 0
```

7.1.2.350 BIT_PWR_MGMT_0_GYRO_MODE_MASK

```
#define BIT_PWR_MGMT_0_GYRO_MODE_MASK (0x03 << BIT_PWR_MGMT_0_GYRO_MODE_POS)
```

7.1.2.351 BIT_PWR_MGMT_0_GYRO_MODE_POS

```
#define BIT_PWR_MGMT_0_GYRO_MODE_POS 2
```

7.1.2.352 BIT_PWR_MGMT_0_IDLE_MASK

```
#define BIT_PWR_MGMT_0_IDLE_MASK (0x01 << BIT_PWR_MGMT_0_IDLE_POS)
```

7.1.2.353 BIT_PWR_MGMT_0_IDLE_POS

```
#define BIT_PWR_MGMT_0_IDLE_POS 4
```

7.1.2.354 BIT_PWR_MGMT_0_TEMP_MASK

```
#define BIT_PWR_MGMT_0_TEMP_MASK (0x01 << BIT_PWR_MGMT_0_TEMP_POS)
```

7.1.2.355 BIT_PWR_MGMT_0_TEMP_POS

```
#define BIT_PWR_MGMT_0_TEMP_POS 5
```

7.1.2.356 BIT_RTC_MODE_MASK

```
#define BIT_RTC_MODE_MASK (0x01 << BIT_RTC_MODE_POS)
```

7.1.2.357 BIT_RTC_MODE_POS

```
#define BIT_RTC_MODE_POS 2
```

7.1.2.358 BIT_SENSOR_CONFIG2_OIS_MODE_MASK

```
#define BIT_SENSOR_CONFIG2_OIS_MODE_MASK (0x03 << BIT_SENSOR_CONFIG2_OIS_MODE_POS)
```

7.1.2.359 BIT_SENSOR_CONFIG2_OIS_MODE_POS

```
#define BIT_SENSOR_CONFIG2_OIS_MODE_POS 4
```

7.1.2.360 BIT_SIGNAL_PATH_RESET_DMP_INIT_MASK

```
#define BIT_SIGNAL_PATH_RESET_DMP_INIT_MASK (0x01 << BIT_SIGNAL_PATH_RESET_DMP_INIT_POS)
```

7.1.2.361 BIT_SIGNAL_PATH_RESET_DMP_INIT_POS

```
#define BIT_SIGNAL_PATH_RESET_DMP_INIT_POS 6
```

7.1.2.362 BIT_SIGNAL_PATH_RESET_DMP_MEM_RESET_MASK

```
#define BIT_SIGNAL_PATH_RESET_DMP_MEM_RESET_MASK (0x01 << BIT_SIGNAL_PATH_RESET_DMP_MEM_RESET_POS)
```

7.1.2.363 BIT_SIGNAL_PATH_RESET_DMP_MEM_RESET_POS

```
#define BIT_SIGNAL_PATH_RESET_DMP_MEM_RESET_POS 5
```

7.1.2.364 BIT_SIGNAL_PATH_RESET_FIFO_FLUSH_MASK

```
#define BIT_SIGNAL_PATH_RESET_FIFO_FLUSH_MASK (0x01 << BIT_SIGNAL_PATH_RESET_FIFO_FLUSH_POS)
```

7.1.2.365 BIT_SIGNAL_PATH_RESET_FIFO_FLUSH_POS

```
#define BIT_SIGNAL_PATH_RESET_FIFO_FLUSH_POS 1
```

7.1.2.366 BIT_SIGNAL_PATH_RESET_TMST_STROBE_MASK

```
#define BIT_SIGNAL_PATH_RESET_TMST_STROBE_MASK (0x01 << BIT_SIGNAL_PATH_RESET_TMST_STROBE_POS)
```

7.1.2.367 BIT_SIGNAL_PATH_RESET_TMST_STROBE_POS

```
#define BIT_SIGNAL_PATH_RESET_TMST_STROBE_POS 2
```

7.1.2.368 BIT_SMD_CONFIG_SMD_MODE_MASK

```
#define BIT_SMD_CONFIG_SMD_MODE_MASK 0x3
```

7.1.2.369 BIT_SMD_CONFIG_SMD_MODE_POS

```
#define BIT_SMD_CONFIG_SMD_MODE_POS 0
```

7.1.2.370 BIT_SMD_CONFIG_WOM_INT_MODE_MASK

```
#define BIT_SMD_CONFIG_WOM_INT_MODE_MASK (0x1 << BIT_SMD_CONFIG_WOM_INT_MODE_POS)
```

7.1.2.371 BIT_SMD_CONFIG_WOM_INT_MODE_POS

```
#define BIT_SMD_CONFIG_WOM_INT_MODE_POS 3
```

7.1.2.372 BIT_SMD_CONFIG_WOM_MODE_MASK

```
#define BIT_SMD_CONFIG_WOM_MODE_MASK (0x1 << BIT_SMD_CONFIG_WOM_MODE_POS)
```

7.1.2.373 BIT_SMD_CONFIG_WOM_MODE_POS

```
#define BIT_SMD_CONFIG_WOM_MODE_POS 2
```

7.1.2.374 BIT_SPI_MODE_OIS1_MASK

```
#define BIT_SPI_MODE_OIS1_MASK (0x01 << BIT_SPI_MODE_OIS1_POS)
```

7.1.2.375 BIT_SPI_MODE_OIS1_POS

```
#define BIT_SPI_MODE_OIS1_POS 2
```

7.1.2.376 BIT_SPI_MODE_OIS2_MASK

```
#define BIT_SPI_MODE_OIS2_MASK (0x01 << BIT_SPI_MODE_OIS2_POS)
```

7.1.2.377 BIT_SPI_MODE_OIS2_POS

```
#define BIT_SPI_MODE_OIS2_POS 3
```

7.1.2.378 BIT_ST_REGULATOR_EN

```
#define BIT_ST_REGULATOR_EN 0x40
```

7.1.2.379 BIT_TMST_CONFIG_RESOL_MASK

```
#define BIT_TMST_CONFIG_RESOL_MASK (0x1 << BIT_TMST_CONFIG_RESOL_POS)
```

7.1.2.380 BIT_TMST_CONFIG_RESOL_POS

```
#define BIT_TMST_CONFIG_RESOL_POS 3
```

7.1.2.381 BIT_TMST_CONFIG_TMST_EN_MASK

```
#define BIT_TMST_CONFIG_TMST_EN_MASK 0x1
```

7.1.2.382 BIT_TMST_CONFIG_TMST_EN_POS

```
#define BIT_TMST_CONFIG_TMST_EN_POS 0
```

7.1.2.383 BIT_TMST_CONFIG_TMST_FSYNC_MASK

```
#define BIT_TMST_CONFIG_TMST_FSYNC_MASK (0x1 << BIT_TMST_CONFIG_TMST_FSYNC_POS)
```

7.1.2.384 BIT_TMST_CONFIG_TMST_FSYNC_POS

```
#define BIT_TMST_CONFIG_TMST_FSYNC_POS 1
```

7.1.2.385 BIT_TMST_CONFIG_TMST_TO_REGS_EN_MASK

```
#define BIT_TMST_CONFIG_TMST_TO_REGS_EN_MASK (0x1 << BIT_TMST_CONFIG_TMST_TO_REGS_EN_POS)
```

7.1.2.386 BIT_TMST_CONFIG_TMST_TO_REGS_EN_POS

```
#define BIT_TMST_CONFIG_TMST_TO_REGS_EN_POS 4
```

7.1.2.387 FIFO_16BYTES_PACKET_SIZE

```
#define FIFO_16BYTES_PACKET_SIZE
```

Value:

```
(FIFO_HEADER_SIZE + FIFO_ACCEL_DATA_SIZE + FIFO_GYRO_DATA_SIZE + FIFO_TEMP_DATA_SIZE +          \
 FIFO_TS_FSYNC_SIZE)
```

7.1.2.388 FIFO_20BYTES_PACKET_SIZE

```
#define FIFO_20BYTES_PACKET_SIZE
```

Value:

```
(FIFO_HEADER_SIZE + FIFO_ACCEL_DATA_SIZE + FIFO_GYRO_DATA_SIZE + FIFO_TEMP_DATA_SIZE +          \
 FIFO_TS_FSYNC_SIZE + FIFO_TEMP_HIGH_RES_SIZE + FIFO_ACCEL_GYRO_HIGH_RES_SIZE)
```

7.1.2.389 FIFO_ACCEL_DATA_SIZE

```
#define FIFO_ACCEL_DATA_SIZE ACCEL_DATA_SIZE
```

7.1.2.390 FIFO_ACCEL_GYRO_HIGH_RES_SIZE

```
#define FIFO_ACCEL_GYRO_HIGH_RES_SIZE 3
```

7.1.2.391 FIFO_GYRO_DATA_SIZE

```
#define FIFO_GYRO_DATA_SIZE GYRO_DATA_SIZE
```

7.1.2.392 FIFO_HEADER_ACC

```
#define FIFO_HEADER_ACC 0x40
```

7.1.2.393 FIFO_HEADER_FSYNC

```
#define FIFO_HEADER_FSYNC 0x04
```

7.1.2.394 FIFO_HEADER_GYRO

```
#define FIFO_HEADER_GYRO 0x20
```

7.1.2.395 FIFO_HEADER_HEADER_20

```
#define FIFO_HEADER_HEADER_20 0x10
```

7.1.2.396 FIFO_HEADER_MSG

```
#define FIFO_HEADER_MSG 0x80
```

7.1.2.397 FIFO_HEADER_ODR_ACCEL

```
#define FIFO_HEADER_ODR_ACCEL 0x01
```

7.1.2.398 FIFO_HEADER_ODR_GYRO

```
#define FIFO_HEADER_ODR_GYRO 0x02
```

7.1.2.399 FIFO_HEADER_SIZE

```
#define FIFO_HEADER_SIZE 1
```

7.1.2.400 FIFO_HEADER_TMST

```
#define FIFO_HEADER_TMST 0x08
```

7.1.2.401 FIFO_TEMP_DATA_SIZE

```
#define FIFO_TEMP_DATA_SIZE 1
```

7.1.2.402 FIFO_TEMP_HIGH_RES_SIZE

```
#define FIFO_TEMP_HIGH_RES_SIZE 1
```

7.1.2.403 FIFO_TS_FSYNC_SIZE

```
#define FIFO_TS_FSYNC_SIZE 2
```

7.1.2.404 GYRO_DATA_SIZE

```
#define GYRO_DATA_SIZE 6
```

7.1.2.405 I3C_IBI_PAYLOAD_ALL

```
#define I3C_IBI_PAYLOAD_ALL 0xFF
```

7.1.2.406 I3C_IBI_PAYLOAD_CAT_APEX1

```
#define I3C_IBI_PAYLOAD_CAT_APEX1 0x08
```

7.1.2.407 I3C_IBI_PAYLOAD_CAT_APEX2

```
#define I3C_IBI_PAYLOAD_CAT_APEX2 0x10
```

7.1.2.408 I3C_IBI_PAYLOAD_CAT_ERROR

```
#define I3C_IBI_PAYLOAD_CAT_ERROR 0x20
```

7.1.2.409 I3C_IBI_PAYLOAD_CAT_FIFO

```
#define I3C_IBI_PAYLOAD_CAT_FIFO 0x02
```

7.1.2.410 I3C_IBI_PAYLOAD_CAT_MISC

```
#define I3C_IBI_PAYLOAD_CAT_MISC 0x40
```

7.1.2.411 I3C_IBI_PAYLOAD_CAT_OIS1_DRDY

```
#define I3C_IBI_PAYLOAD_CAT_OIS1_DRDY 0x04
```

7.1.2.412 I3C_IBI_PAYLOAD_CAT_UI_DRDY

```
#define I3C_IBI_PAYLOAD_CAT_UI_DRDY 0x01
```

7.1.2.413 I3C_IBI_PAYLOAD_TIMEC

```
#define I3C_IBI_PAYLOAD_TIMEC 0x80
```

7.1.2.414 ICM40608_WHOAMI

```
#define ICM40608_WHOAMI 0x39
```

7.1.2.415 ICM42600_WHOAMI

```
#define ICM42600_WHOAMI 0x40
```

7.1.2.416 ICM42602_WHOAMI

```
#define ICM42602_WHOAMI 0x41
```

7.1.2.417 ICM42605_WHOAMI

```
#define ICM42605_WHOAMI 0x42
```

7.1.2.418 ICM42608_WHOAMI

```
#define ICM42608_WHOAMI 0x48
```

7.1.2.419 ICM42622_WHOAMI

```
#define ICM42622_WHOAMI 0x46
```

7.1.2.420 ICM42631_WHOAMI

```
#define ICM42631_WHOAMI 0x5C
```

7.1.2.421 ICM42633_WHOAMI

```
#define ICM42633_WHOAMI 0x5B
```

7.1.2.422 ICM42686P_WHOAMI

```
#define ICM42686P_WHOAMI 0x44
```

7.1.2.423 ICM42686V_WHOAMI

```
#define ICM42686V_WHOAMI 0xDA
```

7.1.2.424 ICM42688P_WHOAMI

```
#define ICM42688P_WHOAMI 0x47
```

7.1.2.425 ICM42688V_WHOAMI

```
#define ICM42688V_WHOAMI 0xDB
```

7.1.2.426 ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_1006632MG

```
#define ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_1006632MG  ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_30M
```

7.1.2.427 ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_1174405MG

```
#define ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_1174405MG  ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_35M
```

7.1.2.428 ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_1342177MG

```
#define ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_1342177MG  ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_40M
```

7.1.2.429 ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_1509949MG

```
#define ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_1509949MG  ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_45M
```

7.1.2.430 ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_1677721MG

```
#define ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_1677721MG  ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_50M
```

7.1.2.431 ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_1845493MG

```
#define ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_1845493MG  ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_55M
```

7.1.2.432 ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_2013265MG

```
#define ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_2013265MG  ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_60M
```

7.1.2.433 ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_2181038MG

```
#define ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_2181038MG  ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_65M
```

7.1.2.434 ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_2348810MG

```
#define ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_2348810MG  ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_70M
```

7.1.2.435 ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_2516582MG

```
#define ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_2516582MG  ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_75M
```

7.1.2.436 ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_2684354MG

```
#define ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_2684354MG  ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_80M
```

7.1.2.437 ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_2852126MG

```
#define ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_2852126MG  ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_85M
```

7.1.2.438 ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_3019898MG

```
#define ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_3019898MG  ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_90M
```

7.1.2.439 ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_3187671MG

```
#define ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_3187671MG  ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_95M
```

7.1.2.440 ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_3355443MG

```
#define ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_3355443MG  ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_100
```

7.1.2.441 ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_3523215MG

```
#define ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_3523215MG  ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_105
```

7.1.2.442 ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_1006632_MG

```
#define ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_1006632_MG ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_30MG
```

7.1.2.443 ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_1140850_MG

```
#define ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_1140850_MG ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_34MG
```

7.1.2.444 ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_1275068_MG

```
#define ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_1275068_MG ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_38MG
```

7.1.2.445 ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_1409286_MG

```
#define ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_1409286_MG ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_42MG
```

7.1.2.446 ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_1543503_MG

```
#define ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_1543503_MG ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_46MG
```

7.1.2.447 ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_1677721_MG

```
#define ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_1677721_MG ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_50MG
```

7.1.2.448 ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_1811939_MG

```
#define ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_1811939_MG ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_54MG
```

7.1.2.449 ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_1946157_MG

```
#define ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_1946157_MG ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_58MG
```

7.1.2.450 ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_2080374_MG

```
#define ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_2080374_MG ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_62MG
```

7.1.2.451 ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_2214592_MG

```
#define ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_2214592_MG ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_66MG
```

7.1.2.452 ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_2348810_MG

```
#define ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_2348810_MG ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_70MG
```

7.1.2.453 ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_2483027_MG

```
#define ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_2483027_MG ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_74MG
```

7.1.2.454 ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_2617245_MG

```
#define ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_2617245_MG ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_78MG
```

7.1.2.455 ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_2751463_MG

```
#define ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_2751463_MG ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_82MG
```

7.1.2.456 ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_2885681_MG

```
#define ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_2885681_MG ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_86MG
```

7.1.2.457 ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_3019898_MG

```
#define ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_3019898_MG ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_90MG
```

7.1.2.458 ICM426XX_APEX_CONFIG7_TAP_MIN_JERK_THR_281MG_DEFAULT

```
#define ICM426XX_APEX_CONFIG7_TAP_MIN_JERK_THR_281MG_DEFAULT 0x11
```

7.1.2.459 ICM426XX_FIFO_CONFIG_MODE_SNAPSHOT

```
#define ICM426XX_FIFO_CONFIG_MODE_SNAPSHOT  = ICM426XX_FIFO_CONFIG_MODE_STOP_ON_FULL;
```

7.1.2.460 ICM_FAMILY_BPLUS

```
#define ICM_FAMILY_BPLUS
```

ICM family definition Possible values are ICM_FAMILY_CPLUS or ICM_FAMILY_BPLUS.

7.1.2.461 INVALID_VALUE_FIFO

```
#define INVALID_VALUE_FIFO ((int16_t)0x8000)
```

7.1.2.462 INVALID_VALUE_FIFO_1B

```
#define INVALID_VALUE_FIFO_1B ((int8_t)0x80)
```

7.1.2.463 MPUREG_ACCEL_CONFIG0

```
#define MPUREG_ACCEL_CONFIG0 0x50
```

7.1.2.464 MPUREG_ACCEL_CONFIG1

```
#define MPUREG_ACCEL_CONFIG1 0x53
```

7.1.2.465 MPUREG_ACCEL_CONFIG_STATIC0_B2

```
#define MPUREG_ACCEL_CONFIG_STATIC0_B2 0x39
```

7.1.2.466 MPUREG_ACCEL_CONFIG_STATIC2_B2

```
#define MPUREG_ACCEL_CONFIG_STATIC2_B2 0x03
```

7.1.2.467 MPUREG_ACCEL_CONFIG_STATIC3_B2

```
#define MPUREG_ACCEL_CONFIG_STATIC3_B2 0x04
```

7.1.2.468 MPUREG_ACCEL_CONFIG_STATIC4_B2

```
#define MPUREG_ACCEL_CONFIG_STATIC4_B2 0x05
```

7.1.2.469 MPUREG_ACCEL_DATA_X0_OIS1_B2

```
#define MPUREG_ACCEL_DATA_X0_OIS1_B2 0x49
```

7.1.2.470 MPUREG_ACCEL_DATA_X0_OIS2_B2

```
#define MPUREG_ACCEL_DATA_X0_OIS2_B2 0x5E
```

7.1.2.471 MPUREG_ACCEL_DATA_X0_UI

```
#define MPUREG_ACCEL_DATA_X0_UI 0x1F
```

7.1.2.472 MPUREG_ACCEL_GYRO_CONFIG0

```
#define MPUREG_ACCEL_GYRO_CONFIG0 0x52
```

7.1.2.473 MPUREG_ACCEL_WOM_X_THR_B4

```
#define MPUREG_ACCEL_WOM_X_THR_B4 0x4A
```

7.1.2.474 MPUREG_ACCEL_WOM_Y_THR_B4

```
#define MPUREG_ACCEL_WOM_Y_THR_B4 0x4B
```

7.1.2.475 MPUREG_ACCEL_WOM_Z_THR_B4

```
#define MPUREG_ACCEL_WOM_Z_THR_B4 0x4C
```

7.1.2.476 MPUREG_APEX_CONFIG0

```
#define MPUREG_APEX_CONFIG0 0x56
```

7.1.2.477 MPUREG_APEX_CONFIG10_B4

```
#define MPUREG_APEX_CONFIG10_B4 0x49
```

7.1.2.478 MPUREG_APEX_CONFIG1_B4

```
#define MPUREG_APEX_CONFIG1_B4 0x40
```

7.1.2.479 MPUREG_APEX_CONFIG2_B4

```
#define MPUREG_APEX_CONFIG2_B4 0x41
```

7.1.2.480 MPUREG_APEX_CONFIG3_B4

```
#define MPUREG_APEX_CONFIG3_B4 0x42
```

7.1.2.481 MPUREG_APEX_CONFIG4_B4

```
#define MPUREG_APEX_CONFIG4_B4 0x43
```

7.1.2.482 MPUREG_APEX_CONFIG5_B4

```
#define MPUREG_APEX_CONFIG5_B4 0x44
```

7.1.2.483 MPUREG_APEX_CONFIG6_B4

```
#define MPUREG_APEX_CONFIG6_B4 0x45
```

7.1.2.484 MPUREG_APEX_CONFIG7_B4

```
#define MPUREG_APEX_CONFIG7_B4 0x46
```

7.1.2.485 MPUREG_APEX_CONFIG8_B4

```
#define MPUREG_APEX_CONFIG8_B4 0x47
```

7.1.2.486 MPUREG_APEX_CONFIG9_B4

```
#define MPUREG_APEX_CONFIG9_B4 0x48
```

7.1.2.487 MPUREG_APEX_DATA0

```
#define MPUREG_APEX_DATA0 0x31
```

7.1.2.488 MPUREG_APEX_DATA1

```
#define MPUREG_APEX_DATA1 0x32
```

7.1.2.489 MPUREG_APEX_DATA2

```
#define MPUREG_APEX_DATA2 0x33
```

7.1.2.490 MPUREG_APEX_DATA3

```
#define MPUREG_APEX_DATA3 0x34
```

7.1.2.491 MPUREG_APEX_DATA4

```
#define MPUREG_APEX_DATA4 0x35
```

7.1.2.492 MPUREG_APEX_DATA5

```
#define MPUREG_APEX_DATA5 0x36
```

7.1.2.493 MPUREG_CHIP_CONFIG

```
#define MPUREG_CHIP_CONFIG MPUREG_DEVICE_CONFIG
```

7.1.2.494 MPUREG_DEVICE_CONFIG

```
#define MPUREG_DEVICE_CONFIG 0x11
```

7.1.2.495 MPUREG_DRIVE_CONFIG

```
#define MPUREG_DRIVE_CONFIG 0x13
```

7.1.2.496 MPUREG_FDR_CONFIG_B4

```
#define MPUREG_FDR_CONFIG_B4 0x09
```

7.1.2.497 MPUREG_FIFO_BYTE_COUNT1

```
#define MPUREG_FIFO_BYTE_COUNT1 MPUREG_FIFO_COUNTH
```

7.1.2.498 MPUREG_FIFO_BYTE_COUNT2

```
#define MPUREG_FIFO_BYTE_COUNT2 MPUREG_FIFO_COUNTL
```

7.1.2.499 MPUREG_FIFO_CONFIG

```
#define MPUREG_FIFO_CONFIG 0x16
```

7.1.2.500 MPUREG_FIFO_CONFIG1

```
#define MPUREG_FIFO_CONFIG1 0x5F
```

7.1.2.501 MPUREG_FIFO_CONFIG2

```
#define MPUREG_FIFO_CONFIG2 0x60
```

7.1.2.502 MPUREG_FIFO_COUNTH

```
#define MPUREG_FIFO_COUNTH 0x2E
```

7.1.2.503 MPUREG_FIFO_COUNTL

```
#define MPUREG_FIFO_COUNTL 0x2F
```

7.1.2.504 MPUREG_FIFO_DATA

```
#define MPUREG_FIFO_DATA 0x30
```

7.1.2.505 MPUREG_FIFO_LOST_PKT0

```
#define MPUREG_FIFO_LOST_PKT0 0x6C
```

7.1.2.506 MPUREG_FSYNC_CONFIG

```
#define MPUREG_FSYNC_CONFIG 0x62
```

7.1.2.507 MPUREG_GYRO_CONFIG0

```
#define MPUREG_GYRO_CONFIG0 0x4F
```

7.1.2.508 MPUREG_GYRO_CONFIG1

```
#define MPUREG_GYRO_CONFIG1 0x51
```

7.1.2.509 MPUREG_GYRO_CONFIG_STATIC2_B1

```
#define MPUREG_GYRO_CONFIG_STATIC2_B1 0x0B
```

7.1.2.510 MPUREG_GYRO_CONFIG_STATIC3_B1

```
#define MPUREG_GYRO_CONFIG_STATIC3_B1 0x0C
```

7.1.2.511 MPUREG_GYRO_CONFIG_STATIC4_B1

```
#define MPUREG_GYRO_CONFIG_STATIC4_B1 0x0D
```

7.1.2.512 MPUREG_GYRO_CONFIG_STATIC5_B1

```
#define MPUREG_GYRO_CONFIG_STATIC5_B1 0x0E
```

7.1.2.513 MPUREG_GYRO_DATA_X0_OIS1_B2

```
#define MPUREG_GYRO_DATA_X0_OIS1_B2 0x4F
```

7.1.2.514 MPUREG_GYRO_DATA_X0_OIS2_B2

```
#define MPUREG_GYRO_DATA_X0_OIS2_B2 0x64
```

7.1.2.515 MPUREG_GYRO_DATA_X0_UI

```
#define MPUREG_GYRO_DATA_X0_UI 0x25
```

7.1.2.516 MPUREG_INT_CONFIG

```
#define MPUREG_INT_CONFIG 0x14
```

7.1.2.517 MPUREG_INT_CONFIG0

```
#define MPUREG_INT_CONFIG0 0x63
```

7.1.2.518 MPUREG_INT_CONFIG1

```
#define MPUREG_INT_CONFIG1 0x64
```

7.1.2.519 MPUREG_INT_SOURCE0

```
#define MPUREG_INT_SOURCE0 0x65
```

7.1.2.520 MPUREG_INT_SOURCE1

```
#define MPUREG_INT_SOURCE1 0x66
```

7.1.2.521 MPUREG_INT_SOURCE10_B4

```
#define MPUREG_INT_SOURCE10_B4 0x51
```

7.1.2.522 MPUREG_INT_SOURCE2

```
#define MPUREG_INT_SOURCE2 0x67
```

7.1.2.523 MPUREG_INT_SOURCE3

```
#define MPUREG_INT_SOURCE3 0x68
```

7.1.2.524 MPUREG_INT_SOURCE4

```
#define MPUREG_INT_SOURCE4 0x69
```

7.1.2.525 MPUREG_INT_SOURCE5

```
#define MPUREG_INT_SOURCE5 0x6A
```

7.1.2.526 MPUREG_INT_SOURCE6_B4

```
#define MPUREG_INT_SOURCE6_B4 0x4D
```

7.1.2.527 MPUREG_INT_SOURCE7_B4

```
#define MPUREG_INT_SOURCE7_B4 0x4E
```

7.1.2.528 MPUREG_INT_SOURCE8_B4

```
#define MPUREG_INT_SOURCE8_B4 0x4F
```

7.1.2.529 MPUREG_INT_SOURCE9_B4

```
#define MPUREG_INT_SOURCE9_B4 0x50
```

7.1.2.530 MPUREG_INT_STATUS

```
#define MPUREG_INT_STATUS 0x2D
```

7.1.2.531 MPUREG_INT_STATUS2

```
#define MPUREG_INT_STATUS2 0x37
```

7.1.2.532 MPUREG_INT_STATUS3

```
#define MPUREG_INT_STATUS3 0x38
```

7.1.2.533 MPUREG_INT_STATUS_OIS1_B2

```
#define MPUREG_INT_STATUS_OIS1_B2 0x57
```

7.1.2.534 MPUREG_INT_STATUS_OIS2_B2

```
#define MPUREG_INT_STATUS_OIS2_B2 0x6C
```

7.1.2.535 MPUREG_INTF_CONFIG0

```
#define MPUREG_INTF_CONFIG0 0x4C
```

7.1.2.536 MPUREG_INTF_CONFIG1

```
#define MPUREG_INTF_CONFIG1 0x4D
```

7.1.2.537 MPUREG_INTF_CONFIG3_B1

```
#define MPUREG_INTF_CONFIG3_B1 0x79
```

7.1.2.538 MPUREG_INTF_CONFIG4_B1

```
#define MPUREG_INTF_CONFIG4_B1 0x7A
```

7.1.2.539 MPUREG_INTF_CONFIG5_B1

```
#define MPUREG_INTF_CONFIG5_B1 0x7B
```

7.1.2.540 MPUREG_INTF_CONFIG6_B1

```
#define MPUREG_INTF_CONFIG6_B1 0x7C
```

7.1.2.541 MPUREG_MEM_BANK_SEL

```
#define MPUREG_MEM_BANK_SEL 0x72
```

7.1.2.542 MPUREG_MEM_R_W

```
#define MPUREG_MEM_R_W 0x74
```

7.1.2.543 MPUREG_MEM_START_ADDR

```
#define MPUREG_MEM_START_ADDR 0x73
```

7.1.2.544 MPUREG_OFFSET_USER_0_B4

```
#define MPUREG_OFFSET_USER_0_B4 0x77
```

7.1.2.545 MPUREG_OFFSET_USER_1_B4

```
#define MPUREG_OFFSET_USER_1_B4 0x78
```

7.1.2.546 MPUREG_OFFSET_USER_2_B4

```
#define MPUREG_OFFSET_USER_2_B4 0x79
```

7.1.2.547 MPUREG_OFFSET_USER_3_B4

```
#define MPUREG_OFFSET_USER_3_B4 0x7A
```

7.1.2.548 MPUREG_OFFSET_USER_4_B4

```
#define MPUREG_OFFSET_USER_4_B4 0x7B
```

7.1.2.549 MPUREG_OFFSET_USER_5_B4

```
#define MPUREG_OFFSET_USER_5_B4 0x7C
```

7.1.2.550 MPUREG_OFFSET_USER_6_B4

```
#define MPUREG_OFFSET_USER_6_B4 0x7D
```

7.1.2.551 MPUREG_OFFSET_USER_7_B4

```
#define MPUREG_OFFSET_USER_7_B4 0x7E
```

7.1.2.552 MPUREG_OFFSET_USER_8_B4

```
#define MPUREG_OFFSET_USER_8_B4 0x7F
```

7.1.2.553 MPUREG_OIS1_CONFIG1_B2

```
#define MPUREG_OIS1_CONFIG1_B2 0x44
```

7.1.2.554 MPUREG_OIS1_CONFIG2_B2

```
#define MPUREG_OIS1_CONFIG2_B2 0x45
```

7.1.2.555 MPUREG_OIS1_CONFIG3_B2

```
#define MPUREG_OIS1_CONFIG3_B2 0x46
```

7.1.2.556 MPUREG_OIS2_CONFIG1_B2

```
#define MPUREG_OIS2_CONFIG1_B2 0x59
```

7.1.2.557 MPUREG_OIS2_CONFIG2_B2

```
#define MPUREG_OIS2_CONFIG2_B2 0x5A
```

7.1.2.558 MPUREG_OIS2_CONFIG3_B2

```
#define MPUREG_OIS2_CONFIG3_B2 0x5B
```

7.1.2.559 MPUREG_PU_PD_CONFIG1_B3

```
#define MPUREG_PU_PD_CONFIG1_B3 0x06
```

7.1.2.560 MPUREG_PU_PD_CONFIG2_B3

```
#define MPUREG_PU_PD_CONFIG2_B3 0x0E
```

7.1.2.561 MPUREG_PWR_MGMT_0

```
#define MPUREG_PWR_MGMT_0 0x4E
```

7.1.2.562 MPUREG_REG_BANK_SEL

```
#define MPUREG_REG_BANK_SEL 0x76
```

7.1.2.563 MPUREG_SCAN0

```
#define MPUREG_SCAN0 0x71
```

7.1.2.564 MPUREG_SELF_TEST_CONFIG

```
#define MPUREG_SELF_TEST_CONFIG 0x70
```

7.1.2.565 MPUREG_SENSOR_CONFIG1_B1

```
#define MPUREG_SENSOR_CONFIG1_B1 0x04
```

7.1.2.566 MPUREG_SIGNAL_PATH_RESET

```
#define MPUREG_SIGNAL_PATH_RESET 0x4B
```

7.1.2.567 MPUREG_SMD_CONFIG

```
#define MPUREG_SMD_CONFIG 0x57
```

7.1.2.568 MPUREG_TEMP_DATA0_UI

```
#define MPUREG_TEMP_DATA0_UI 0x1D
```

7.1.2.569 MPUREG_TMD4_B2

```
#define MPUREG_TMD4_B2 0x70
```

7.1.2.570 MPUREG_TMD5_B2

```
#define MPUREG_TMD5_B2 0x71
```

7.1.2.571 MPUREG_TMD6_B2

```
#define MPUREG_TMD6_B2 0x72
```

7.1.2.572 MPUREG_TMD7_B2

```
#define MPUREG_TMD7_B2 0x73
```

7.1.2.573 MPUREG_TMST_CONFIG

```
#define MPUREG_TMST_CONFIG 0x54
```

7.1.2.574 MPUREG_TMST_FSYNC1

```
#define MPUREG_TMST_FSYNC1 MPUREG_TMST_FSYNCH
```

7.1.2.575 MPUREG_TMST_FSYNCH

```
#define MPUREG_TMST_FSYNCH 0x2B
```

7.1.2.576 MPUREG_TMST_VAL0_B1

```
#define MPUREG_TMST_VAL0_B1 0x62
```

7.1.2.577 MPUREG_WHO_AM_I

```
#define MPUREG_WHO_AM_I 0x75
```

7.1.2.578 MPUREG_XA_ST_DATA_B2

```
#define MPUREG_XA_ST_DATA_B2 0x3B
```

7.1.2.579 MPUREG_XG_ST_DATA_B1

```
#define MPUREG_XG_ST_DATA_B1 0x5F
```

7.1.2.580 MPUREG_YA_ST_DATA_B2

```
#define MPUREG_YA_ST_DATA_B2 0x3C
```

7.1.2.581 MPUREG_YG_ST_DATA_B1

```
#define MPUREG_YG_ST_DATA_B1 0x60
```

7.1.2.582 MPUREG_ZA_ST_DATA_B2

```
#define MPUREG_ZA_ST_DATA_B2 0x3D
```

7.1.2.583 MPUREG_ZG_ST_DATA_B1

```
#define MPUREG_ZG_ST_DATA_B1 0x61
```

7.1.2.584 TEMP_DATA_SIZE

```
#define TEMP_DATA_SIZE 2
```

7.1.3 Enumeration Type Documentation

7.1.3.1 ICM426XX_ACCEL_AAF_DIS_t

```
enum ICM426XX_ACCEL_AAF_DIS_t
```

Enumerator

ICM426XX_ACCEL_AAF_EN	
ICM426XX_ACCEL_AAF_DIS	

7.1.3.2 ICM426XX_ACCEL_CONFIG0_FS_SEL_t

```
enum ICM426XX_ACCEL_CONFIG0_FS_SEL_t
```

Accelerometer FSR selection.

Enumerator

ICM426XX_ACCEL_CONFIG0_FS_SEL_RESERVED	
ICM426XX_ACCEL_CONFIG0_FS_SEL_2g	2g
ICM426XX_ACCEL_CONFIG0_FS_SEL_4g	4g
ICM426XX_ACCEL_CONFIG0_FS_SEL_8g	8g
ICM426XX_ACCEL_CONFIG0_FS_SEL_16g	16g

7.1.3.3 ICM426XX_ACCEL_CONFIG0_ODR_t

```
enum ICM426XX_ACCEL_CONFIG0_ODR_t
```

Accelerometer ODR selection.

Enumerator

ICM426XX_ACCEL_CONFIG0_ODR_500_HZ	500 Hz (2 ms)
ICM426XX_ACCEL_CONFIG0_ODR_1_5625_HZ	1.5625 Hz (640 ms)
ICM426XX_ACCEL_CONFIG0_ODR_3_125_HZ	3.125 Hz (320 ms)

Enumerator

ICM426XX_ACCEL_CONFIG0_ODR_6_25_HZ	6.25 Hz (160 ms)
ICM426XX_ACCEL_CONFIG0_ODR_12_5_HZ	12.5 Hz (80 ms)
ICM426XX_ACCEL_CONFIG0_ODR_25_HZ	25 Hz (40 ms)
ICM426XX_ACCEL_CONFIG0_ODR_50_HZ	50 Hz (20 ms)
ICM426XX_ACCEL_CONFIG0_ODR_100_HZ	100 Hz (10 ms)
ICM426XX_ACCEL_CONFIG0_ODR_200_HZ	200 Hz (5 ms)
ICM426XX_ACCEL_CONFIG0_ODR_1_KHZ	1 KHz (1 ms)
ICM426XX_ACCEL_CONFIG0_ODR_2_KHZ	2 KHz (500 us)
ICM426XX_ACCEL_CONFIG0_ODR_4_KHZ	4 KHz (250 us)
ICM426XX_ACCEL_CONFIG0_ODR_8_KHZ	8 KHz (125 us)
ICM426XX_ACCEL_CONFIG0_ODR_16_KHZ	16 KHz (62.5 us)
ICM426XX_ACCEL_CONFIG0_ODR_32_KHZ	32 KHz (31.25 us)

7.1.3.4 ICM426XX_ACCEL_CONFIG_ACCEL_UI_FILT_ORD_t

`enum ICM426XX_ACCEL_CONFIG_ACCEL_UI_FILT_ORD_t`

Enumerator

ICM426XX_ACCEL_CONFIG_ACCEL_UI_FILT_ORD_1ST_ORDER	
ICM426XX_ACCEL_CONFIG_ACCEL_UI_FILT_ORD_2ND_ORDER	
ICM426XX_ACCEL_CONFIG_ACCEL_UI_FILT_ORD_3RD_ORDER	

7.1.3.5 ICM426XX_APEX_CONFIG0_DMP_ODR_t

`enum ICM426XX_APEX_CONFIG0_DMP_ODR_t`

DMP ODR selection.

Enumerator

ICM426XX_APEX_CONFIG0_DMP_ODR_25Hz	25Hz (40ms)
ICM426XX_APEX_CONFIG0_DMP_ODR_50Hz	50Hz (20ms)
ICM426XX_APEX_CONFIG0_DMP_ODR_100Hz	100Hz (10ms)
ICM426XX_APEX_CONFIG0_DMP_ODR_500Hz	500Hz (40ms)

7.1.3.6 ICM426XX_APEX_CONFIG0_DMP_POWER_SAVE_t

`enum ICM426XX_APEX_CONFIG0_DMP_POWER_SAVE_t`

Enumerator

ICM426XX_APEX_CONFIG0_DMP_POWER_SAVE_EN	
ICM426XX_APEX_CONFIG0_DMP_POWER_SAVE_DIS	

7.1.3.7 ICM426XX_APEX_CONFIG0_PEDO_EN_t

`enum ICM426XX_APEX_CONFIG0_PEDO_EN_t`

Enumerator

ICM426XX_APEX_CONFIG0_PEDO_EN_EN	
ICM426XX_APEX_CONFIG0_PEDO_EN_DIS	

7.1.3.8 ICM426XX_APEX_CONFIG0_R2W_EN_t

`enum ICM426XX_APEX_CONFIG0_R2W_EN_t`

Enumerator

ICM426XX_APEX_CONFIG0_R2W_EN_EN	
ICM426XX_APEX_CONFIG0_R2W_EN_DIS	

7.1.3.9 ICM426XX_APEX_CONFIG0_TAP_ENABLE_t

`enum ICM426XX_APEX_CONFIG0_TAP_ENABLE_t`

Enumerator

ICM426XX_APEX_CONFIG0_TAP_ENABLE_EN	
ICM426XX_APEX_CONFIG0_TAP_ENABLE_DIS	

7.1.3.10 ICM426XX_APEX_CONFIG0_TILT_EN_t

`enum ICM426XX_APEX_CONFIG0_TILT_EN_t`

Enumerator

ICM426XX_APEX_CONFIG0_TILT_EN_EN	
ICM426XX_APEX_CONFIG0_TILT_EN_DIS	

7.1.3.11 ICM426XX_APEX_CONFIG1_DMP_POWER_SAVE_TIME_t

`enum ICM426XX_APEX_CONFIG1_DMP_POWER_SAVE_TIME_t`

Enumerator

ICM426XX_APEX_CONFIG1_DMP_POWER_SAVE_TIME_SEL_0S	
ICM426XX_APEX_CONFIG1_DMP_POWER_SAVE_TIME_SEL_4S	
ICM426XX_APEX_CONFIG1_DMP_POWER_SAVE_TIME_SEL_8S	
ICM426XX_APEX_CONFIG1_DMP_POWER_SAVE_TIME_SEL_12S	
ICM426XX_APEX_CONFIG1_DMP_POWER_SAVE_TIME_SEL_16S	
ICM426XX_APEX_CONFIG1_DMP_POWER_SAVE_TIME_SEL_20S	
ICM426XX_APEX_CONFIG1_DMP_POWER_SAVE_TIME_SEL_24S	
ICM426XX_APEX_CONFIG1_DMP_POWER_SAVE_TIME_SEL_28S	
ICM426XX_APEX_CONFIG1_DMP_POWER_SAVE_TIME_SEL_32S	
ICM426XX_APEX_CONFIG1_DMP_POWER_SAVE_TIME_SEL_36S	
ICM426XX_APEX_CONFIG1_DMP_POWER_SAVE_TIME_SEL_40S	
ICM426XX_APEX_CONFIG1_DMP_POWER_SAVE_TIME_SEL_44S	
ICM426XX_APEX_CONFIG1_DMP_POWER_SAVE_TIME_SEL_48S	
ICM426XX_APEX_CONFIG1_DMP_POWER_SAVE_TIME_SEL_52S	
ICM426XX_APEX_CONFIG1_DMP_POWER_SAVE_TIME_SEL_56S	
ICM426XX_APEX_CONFIG1_DMP_POWER_SAVE_TIME_SEL_60S	

7.1.3.12 ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_t

`enum ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_t`

Enumerator

ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_30MG	
ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_35MG	
ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_40MG	
ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_45MG	
ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_50MG	
ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_55MG	
ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_60MG	
ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_65MG	
ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_70MG	
ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_75MG	

Enumerator

ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_80MG	
ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_85MG	
ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_90MG	
ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_95MG	
ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_100MG	
ICM426XX_APEX_CONFIG1_LOW_ENERGY_AMP_TH_SEL_105MG	

7.1.3.13 ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_t

`enum ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_t`

Enumerator

ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_30MG	
ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_34MG	
ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_38MG	
ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_42MG	
ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_46MG	
ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_50MG	
ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_54MG	
ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_58MG	
ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_62MG	
ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_66MG	
ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_70MG	
ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_74MG	
ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_78MG	
ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_82MG	
ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_86MG	
ICM426XX_APEX_CONFIG2_PEDO_AMP_TH_90MG	

7.1.3.14 ICM426XX_APEX_CONFIG3_PEDO_HI_ENRGY_TH_t

`enum ICM426XX_APEX_CONFIG3_PEDO_HI_ENRGY_TH_t`

Enumerator

ICM426XX_APEX_CONFIG3_PEDO_HI_ENRGY_TH_90	
ICM426XX_APEX_CONFIG3_PEDO_HI_ENRGY_TH_107	
ICM426XX_APEX_CONFIG3_PEDO_HI_ENRGY_TH_136	
ICM426XX_APEX_CONFIG3_PEDO_HI_ENRGY_TH_159	

7.1.3.15 ICM426XX_APEX_CONFIG3_PEDO_SB_TIMER_TH_t

enum ICM426XX_APEX_CONFIG3_PEDO_SB_TIMER_TH_t

Enumerator

ICM426XX_APEX_CONFIG3_PEDO_SB_TIMER_TH_50_SAMPLES	
ICM426XX_APEX_CONFIG3_PEDO_SB_TIMER_TH_75_SAMPLES	
ICM426XX_APEX_CONFIG3_PEDO_SB_TIMER_TH_100_SAMPLES	
ICM426XX_APEX_CONFIG3_PEDO_SB_TIMER_TH_125_SAMPLES	
ICM426XX_APEX_CONFIG3_PEDO_SB_TIMER_TH_150_SAMPLES	
ICM426XX_APEX_CONFIG3_PEDO_SB_TIMER_TH_175_SAMPLES	
ICM426XX_APEX_CONFIG3_PEDO_SB_TIMER_TH_200_SAMPLES	
ICM426XX_APEX_CONFIG3_PEDO_SB_TIMER_TH_225_SAMPLES	

7.1.3.16 ICM426XX_APEX_CONFIG4_R2W_SLEEP_TIME_OUT_t

enum ICM426XX_APEX_CONFIG4_R2W_SLEEP_TIME_OUT_t

Enumerator

ICM426XX_APEX_CONFIG4_R2W_SLEEP_TIME_OUT_1_28S	
ICM426XX_APEX_CONFIG4_R2W_SLEEP_TIME_OUT_2_56S	
ICM426XX_APEX_CONFIG4_R2W_SLEEP_TIME_OUT_3_84S	
ICM426XX_APEX_CONFIG4_R2W_SLEEP_TIME_OUT_5_12S	
ICM426XX_APEX_CONFIG4_R2W_SLEEP_TIME_OUT_6_4S	
ICM426XX_APEX_CONFIG4_R2W_SLEEP_TIME_OUT_7_68S	
ICM426XX_APEX_CONFIG4_R2W_SLEEP_TIME_OUT_8_96S	
ICM426XX_APEX_CONFIG4_R2W_SLEEP_TIME_OUT_10_24S	

7.1.3.17 ICM426XX_APEX_CONFIG4_TILT_WAIT_TIME_t

enum ICM426XX_APEX_CONFIG4_TILT_WAIT_TIME_t

Enumerator

ICM426XX_APEX_CONFIG4_TILT_WAIT_TIME_0S	
ICM426XX_APEX_CONFIG4_TILT_WAIT_TIME_2S	
ICM426XX_APEX_CONFIG4_TILT_WAIT_TIME_4S	
ICM426XX_APEX_CONFIG4_TILT_WAIT_TIME_6S	

7.1.3.18 ICM426XX_APEX_CONFIG5_R2W_MOUNTING_MATRIX_t

enum ICM426XX_APEX_CONFIG5_R2W_MOUNTING_MATRIX_t

Enumerator

ICM426XX_APEX_CONFIG5_R2W_MOUNTING_MATRIX_0	
ICM426XX_APEX_CONFIG5_R2W_MOUNTING_MATRIX_1	
ICM426XX_APEX_CONFIG5_R2W_MOUNTING_MATRIX_2	
ICM426XX_APEX_CONFIG5_R2W_MOUNTING_MATRIX_3	
ICM426XX_APEX_CONFIG5_R2W_MOUNTING_MATRIX_4	
ICM426XX_APEX_CONFIG5_R2W_MOUNTING_MATRIX_5	
ICM426XX_APEX_CONFIG5_R2W_MOUNTING_MATRIX_6	
ICM426XX_APEX_CONFIG5_R2W_MOUNTING_MATRIX_7	

7.1.3.19 ICM426XX_APEX_CONFIG6_R2W_SLEEP_GEST_DELAY_t

enum ICM426XX_APEX_CONFIG6_R2W_SLEEP_GEST_DELAY_t

Enumerator

ICM426XX_APEX_CONFIG6_R2W_SLEEP_GEST_DELAY_0_32S	
ICM426XX_APEX_CONFIG6_R2W_SLEEP_GEST_DELAY_0_64S	
ICM426XX_APEX_CONFIG6_R2W_SLEEP_GEST_DELAY_0_96S	
ICM426XX_APEX_CONFIG6_R2W_SLEEP_GEST_DELAY_1_28S	
ICM426XX_APEX_CONFIG6_R2W_SLEEP_GEST_DELAY_1_6S	
ICM426XX_APEX_CONFIG6_R2W_SLEEP_GEST_DELAY_1_92S	
ICM426XX_APEX_CONFIG6_R2W_SLEEP_GEST_DELAY_2_24S	
ICM426XX_APEX_CONFIG6_R2W_SLEEP_GEST_DELAY_2_56S	

7.1.3.20 ICM426XX_APEX_CONFIG7_TAP_MAX_PEAK_TOL_t

enum ICM426XX_APEX_CONFIG7_TAP_MAX_PEAK_TOL_t

Enumerator

ICM426XX_APEX_CONFIG7_TAP_MAX_PEAK_TOL_12	
ICM426XX_APEX_CONFIG7_TAP_MAX_PEAK_TOL_25	
ICM426XX_APEX_CONFIG7_TAP_MAX_PEAK_TOL_37	
ICM426XX_APEX_CONFIG7_TAP_MAX_PEAK_TOL_50	

7.1.3.21 ICM426XX_APEX_CONFIG8_TAP_TAVG_t

enum ICM426XX_APEX_CONFIG8_TAP_TAVG_t

Enumerator

ICM426XX_APEX_CONFIG8_TAP_TAVG_1SAMPLE	
ICM426XX_APEX_CONFIG8_TAP_TAVG_2SAMPLE	
ICM426XX_APEX_CONFIG8_TAP_TAVG_4SAMPLE	
ICM426XX_APEX_CONFIG8_TAP_TAVG_8SAMPLE	

7.1.3.22 ICM426XX_APEX_CONFIG8_TAP_TMAX_t

enum ICM426XX_APEX_CONFIG8_TAP_TMAX_t

Enumerator

ICM426XX_APEX_CONFIG8_TAP_TMAX_250MS	
ICM426XX_APEX_CONFIG8_TAP_TMAX_375MS	
ICM426XX_APEX_CONFIG8_TAP_TMAX_500MS	
ICM426XX_APEX_CONFIG8_TAP_TMAX_625MS	

7.1.3.23 ICM426XX_APEX_CONFIG8_TAP_TMIN_t

enum ICM426XX_APEX_CONFIG8_TAP_TMIN_t

Enumerator

ICM426XX_APEX_CONFIG8_TAP_TMIN_125MS	
ICM426XX_APEX_CONFIG8_TAP_TMIN_140MS	
ICM426XX_APEX_CONFIG8_TAP_TMIN_156MS	
ICM426XX_APEX_CONFIG8_TAP_TMIN_171MS	
ICM426XX_APEX_CONFIG8_TAP_TMIN_187MS	
ICM426XX_APEX_CONFIG8_TAP_TMIN_203MS	
ICM426XX_APEX_CONFIG8_TAP_TMIN_218MS	
ICM426XX_APEX_CONFIG8_TAP_TMIN_234MS	

7.1.3.24 ICM426XX_APEX_CONFIG9_SENSITIVITY_MODE_t

enum ICM426XX_APEX_CONFIG9_SENSITIVITY_MODE_t

Enumerator

ICM426XX_APEX_CONFIG9_SENSITIVITY_MODE_NORMAL	
ICM426XX_APEX_CONFIG9_SENSITIVITY_MODE_RESERVED	

7.1.3.25 ICM426XX_APEX_DATA3_ACTIVITY_CLASS_t

enum ICM426XX_APEX_DATA3_ACTIVITY_CLASS_t

Enumerator

ICM426XX_APEX_DATA3_ACTIVITY_CLASS_OTHER	
ICM426XX_APEX_DATA3_ACTIVITY_CLASS_WALK	
ICM426XX_APEX_DATA3_ACTIVITY_CLASS_RUN	

7.1.3.26 ICM426XX_APEX_DATA3_DMP_IDLE_OFF_t

enum ICM426XX_APEX_DATA3_DMP_IDLE_OFF_t

Enumerator

ICM426XX_APEX_DATA3_DMP_IDLE_ON	
ICM426XX_APEX_DATA3_DMP_IDLE_OFF	

7.1.3.27 ICM426XX_APEX_DATA4_TAP_AXIS_t

enum ICM426XX_APEX_DATA4_TAP_AXIS_t

Enumerator

ICM426XX_APEX_DATA4_TAP_AXIS↩ _Z	
ICM426XX_APEX_DATA4_TAP_AXIS↩ _Y	
ICM426XX_APEX_DATA4_TAP_AXIS↩ _X	

7.1.3.28 ICM426XX_APEX_DATA4_TAP_DIR_t

enum ICM426XX_APEX_DATA4_TAP_DIR_t

Enumerator

ICM426XX_APEX_DATA4_TAP_DIR_POSITIVE	
ICM426XX_APEX_DATA4_TAP_DIR_NEGATIVE	

7.1.3.29 ICM426XX_APEX_DATA4_TAP_NUM_t

enum ICM426XX_APEX_DATA4_TAP_NUM_t

Enumerator

ICM426XX_APEX_DATA4_TAP_NUM_DOUBLE	
ICM426XX_APEX_DATA4_TAP_NUM_SINGLE	

7.1.3.30 ICM426XX_CHIP_CONFIG_RESET_t

enum ICM426XX_CHIP_CONFIG_RESET_t

Enumerator

ICM426XX_CHIP_CONFIG_RESET_EN	
ICM426XX_CHIP_CONFIG_RESET_NONE	

7.1.3.31 ICM426XX_CHIP_CONFIG_SPI_MODE_t

enum ICM426XX_CHIP_CONFIG_SPI_MODE_t

Enumerator

ICM426XX_CHIP_CONFIG_SPI_MODE_1↩ _2	
ICM426XX_CHIP_CONFIG_SPI_MODE_0↩ _3	

7.1.3.32 ICM426XX_DEVICE_CONFIG_RESET_t

enum ICM426XX_DEVICE_CONFIG_RESET_t

Enumerator

ICM426XX_DEVICE_CONFIG_RESET_EN	
ICM426XX_DEVICE_CONFIG_RESET_NONE	

7.1.3.33 ICM426XX_DEVICE_CONFIG_SPI_MODE_t

enum ICM426XX_DEVICE_CONFIG_SPI_MODE_t

Enumerator

ICM426XX_DEVICE_CONFIG_SPI_MODE_1↩_2	
ICM426XX_DEVICE_CONFIG_SPI_MODE_0↩_3	

7.1.3.34 ICM426XX_FIFO_CONFIG1_ACCEL_t

enum ICM426XX_FIFO_CONFIG1_ACCEL_t

Enumerator

ICM426XX_FIFO_CONFIG1_ACCEL_EN	
ICM426XX_FIFO_CONFIG1_ACCEL_DIS	

7.1.3.35 ICM426XX_FIFO_CONFIG1_GYRO_t

enum ICM426XX_FIFO_CONFIG1_GYRO_t

Enumerator

ICM426XX_FIFO_CONFIG1_GYRO_EN	
ICM426XX_FIFO_CONFIG1_GYRO_DIS	

7.1.3.36 ICM426XX_FIFO_CONFIG1_HIRES_t

enum ICM426XX_FIFO_CONFIG1_HIRES_t

Enumerator

ICM426XX_FIFO_CONFIG1_HIRES_EN	
ICM426XX_FIFO_CONFIG1_HIRES_DIS	

7.1.3.37 ICM426XX_FIFO_CONFIG1_TEMP_t

enum ICM426XX_FIFO_CONFIG1_TEMP_t

Enumerator

ICM426XX_FIFO_CONFIG1_TEMP_EN	
ICM426XX_FIFO_CONFIG1_TEMP_DIS	

7.1.3.38 ICM426XX_FIFO_CONFIG1_TMST_FSYNC_t

enum ICM426XX_FIFO_CONFIG1_TMST_FSYNC_t

Enumerator

ICM426XX_FIFO_CONFIG1_TMST_FSYNC_EN	
ICM426XX_FIFO_CONFIG1_TMST_FSYNC_DIS	

7.1.3.39 ICM426XX_FIFO_CONFIG1_WM_GT_t

enum ICM426XX_FIFO_CONFIG1_WM_GT_t

Enumerator

ICM426XX_FIFO_CONFIG1_WM_GT_TH_EN	
ICM426XX_FIFO_CONFIG1_WM_GT_TH_DIS	

7.1.3.40 ICM426XX_FIFO_CONFIG_MODE_t

enum ICM426XX_FIFO_CONFIG_MODE_t

Enumerator

ICM426XX_FIFO_CONFIG_MODE_STOP_ON_FULL	
ICM426XX_FIFO_CONFIG_MODE_STREAM	
ICM426XX_FIFO_CONFIG_MODE_BYPASS	

7.1.3.41 ICM426XX_FSYNC_CONFIG_UI_SEL_t

enum ICM426XX_FSYNC_CONFIG_UI_SEL_t

Enumerator

ICM426XX_FSYNC_CONFIG_UI_SEL_NO	
ICM426XX_FSYNC_CONFIG_UI_SEL_TEMP	
ICM426XX_FSYNC_CONFIG_UI_SEL_GYRO_X	
ICM426XX_FSYNC_CONFIG_UI_SEL_GYRO_Y	
ICM426XX_FSYNC_CONFIG_UI_SEL_GYRO_Z	
ICM426XX_FSYNC_CONFIG_UI_SEL_ACCEL↩ _X	
ICM426XX_FSYNC_CONFIG_UI_SEL_ACCEL↩ _Y	
ICM426XX_FSYNC_CONFIG_UI_SEL_ACCEL↩ _Z	

7.1.3.42 ICM426XX_GYRO_AAF_DIS_t

enum ICM426XX_GYRO_AAF_DIS_t

Enumerator

ICM426XX_GYRO_AAF_EN	
ICM426XX_GYRO_AAF_DIS	

7.1.3.43 ICM426XX_GYRO_ACCEL_CONFIG0_ACCEL_FILT_AVG_t

enum ICM426XX_GYRO_ACCEL_CONFIG0_ACCEL_FILT_AVG_t

Enumerator

ICM426XX_GYRO_ACCEL_CONFIG0_ACCEL_FILT_AVG_16	
ICM426XX_GYRO_ACCEL_CONFIG0_ACCEL_FILT_AVG_1	

7.1.3.44 ICM426XX_GYRO_ACCEL_CONFIG0_ACCEL_FILT_BW_t

`enum ICM426XX_GYRO_ACCEL_CONFIG0_ACCEL_FILT_BW_t`

Enumerator

ICM426XX_GYRO_ACCEL_CONFIG0_ACCEL_FILT_BW_40	
ICM426XX_GYRO_ACCEL_CONFIG0_ACCEL_FILT_BW_20	
ICM426XX_GYRO_ACCEL_CONFIG0_ACCEL_FILT_BW_16	
ICM426XX_GYRO_ACCEL_CONFIG0_ACCEL_FILT_BW_10	
ICM426XX_GYRO_ACCEL_CONFIG0_ACCEL_FILT_BW_8	
ICM426XX_GYRO_ACCEL_CONFIG0_ACCEL_FILT_BW_5	
ICM426XX_GYRO_ACCEL_CONFIG0_ACCEL_FILT_BW_4	
ICM426XX_GYRO_ACCEL_CONFIG0_ACCEL_FILT_BW_2	

7.1.3.45 ICM426XX_GYRO_ACCEL_CONFIG0_GYRO_FILT_BW_t

`enum ICM426XX_GYRO_ACCEL_CONFIG0_GYRO_FILT_BW_t`

Enumerator

ICM426XX_GYRO_ACCEL_CONFIG0_GYRO_FILT_BW_40	
ICM426XX_GYRO_ACCEL_CONFIG0_GYRO_FILT_BW_20	
ICM426XX_GYRO_ACCEL_CONFIG0_GYRO_FILT_BW_16	
ICM426XX_GYRO_ACCEL_CONFIG0_GYRO_FILT_BW_10	
ICM426XX_GYRO_ACCEL_CONFIG0_GYRO_FILT_BW_8	
ICM426XX_GYRO_ACCEL_CONFIG0_GYRO_FILT_BW_5	
ICM426XX_GYRO_ACCEL_CONFIG0_GYRO_FILT_BW_4	
ICM426XX_GYRO_ACCEL_CONFIG0_GYRO_FILT_BW_2	

7.1.3.46 ICM426XX_GYRO_CONFIG0_FS_SEL_t

`enum ICM426XX_GYRO_CONFIG0_FS_SEL_t`

Gyroscope FSR selection.

Enumerator

ICM426XX_GYRO_CONFIG0_FS_SEL_16dps	16dps
ICM426XX_GYRO_CONFIG0_FS_SEL_31dps	31dps
ICM426XX_GYRO_CONFIG0_FS_SEL_62dps	62dps
ICM426XX_GYRO_CONFIG0_FS_SEL_125dps	125dps
ICM426XX_GYRO_CONFIG0_FS_SEL_250dps	250dps
ICM426XX_GYRO_CONFIG0_FS_SEL_500dps	500dps
ICM426XX_GYRO_CONFIG0_FS_SEL_1000dps	1000dps
ICM426XX_GYRO_CONFIG0_FS_SEL_2000dps	2000dps

7.1.3.47 ICM426XX_GYRO_CONFIG0_ODR_t

`enum ICM426XX_GYRO_CONFIG0_ODR_t`

Gyroscope ODR selection.

Enumerator

ICM426XX_GYRO_CONFIG0_ODR_500_HZ	500 Hz (2 ms)
ICM426XX_GYRO_CONFIG0_ODR_12_5_HZ	12.5 Hz (80 ms)
ICM426XX_GYRO_CONFIG0_ODR_25_HZ	25 Hz (40 ms)
ICM426XX_GYRO_CONFIG0_ODR_50_HZ	50 Hz (20 ms)
ICM426XX_GYRO_CONFIG0_ODR_100_HZ	100 Hz (10 ms)
ICM426XX_GYRO_CONFIG0_ODR_200_HZ	200 Hz (5 ms)
ICM426XX_GYRO_CONFIG0_ODR_1_KHZ	1 KHz (1 ms)
ICM426XX_GYRO_CONFIG0_ODR_2_KHZ	2 KHz (500 us)
ICM426XX_GYRO_CONFIG0_ODR_4_KHZ	4 KHz (250 us)
ICM426XX_GYRO_CONFIG0_ODR_8_KHZ	8 KHz (125 us)
ICM426XX_GYRO_CONFIG0_ODR_16_KHZ	16 KHz (62.5 us)
ICM426XX_GYRO_CONFIG0_ODR_32_KHZ	32 KHz (31.25 us)

7.1.3.48 ICM426XX_GYRO_CONFIG_GYRO_UI_FILT_ORD_t

`enum ICM426XX_GYRO_CONFIG_GYRO_UI_FILT_ORD_t`

Enumerator

ICM426XX_GYRO_CONFIG_GYRO_UI_FILT_ORD_1ST_ORDER	
ICM426XX_GYRO_CONFIG_GYRO_UI_FILT_ORD_2ND_ORDER	
ICM426XX_GYRO_CONFIG_GYRO_UI_FILT_ORD_3RD_ORDER	

7.1.3.49 ICM426XX_GYRO_NF_DIS_t

enum ICM426XX_GYRO_NF_DIS_t

Enumerator

ICM426XX_GYRO_NF_EN	
ICM426XX_GYRO_NF_DIS	

7.1.3.50 ICM426XX_INT_CONFIG1_ASY_RST_t

enum ICM426XX_INT_CONFIG1_ASY_RST_t

Enumerator

ICM426XX_INT_CONFIG1_ASY_RST_DISABLED	
ICM426XX_INT_CONFIG1_ASY_RST_ENABLED	

7.1.3.51 ICM426XX_INT_CONFIG_INT1_DRIVE_CIRCUIT_t

enum ICM426XX_INT_CONFIG_INT1_DRIVE_CIRCUIT_t

Enumerator

ICM426XX_INT_CONFIG_INT1_DRIVE_CIRCUIT_PP	
ICM426XX_INT_CONFIG_INT1_DRIVE_CIRCUIT_OD	

7.1.3.52 ICM426XX_INT_CONFIG_INT1_POLARITY_t

enum ICM426XX_INT_CONFIG_INT1_POLARITY_t

Enumerator

ICM426XX_INT_CONFIG_INT1_POLARITY_HIGH	
ICM426XX_INT_CONFIG_INT1_POLARITY_LOW	

7.1.3.53 ICM426XX_INT_CONFIG_INT2_DRIVE_CIRCUIT_t

enum ICM426XX_INT_CONFIG_INT2_DRIVE_CIRCUIT_t

Enumerator

ICM426XX_INT_CONFIG_INT2_DRIVE_CIRCUIT_PP	
ICM426XX_INT_CONFIG_INT2_DRIVE_CIRCUIT_OD	

7.1.3.54 ICM426XX_INT_CONFIG_INT2_POLARITY_t

enum ICM426XX_INT_CONFIG_INT2_POLARITY_t

Enumerator

ICM426XX_INT_CONFIG_INT2_POLARITY_HIGH	
ICM426XX_INT_CONFIG_INT2_POLARITY_LOW	

7.1.3.55 ICM426XX_INT_TDEASSERT_t

enum ICM426XX_INT_TDEASSERT_t

Enumerator

ICM426XX_INT_TDEASSERT_DISABLED	
ICM426XX_INT_TDEASSERT_ENABLED	

7.1.3.56 ICM426XX_INT_TPULSE_DURATION_t

enum ICM426XX_INT_TPULSE_DURATION_t

Enumerator

ICM426XX_INT_TPULSE_DURATION_8_US	
ICM426XX_INT_TPULSE_DURATION_100_US	

7.1.3.57 ICM426XX_INTF_CONFIG0_DATA_ENDIAN_t

enum ICM426XX_INTF_CONFIG0_DATA_ENDIAN_t

Enumerator

ICM426XX_INTF_CONFIG0_DATA_BIG_ENDIAN	
ICM426XX_INTF_CONFIG0_DATA_LITTLE_ENDIAN	

7.1.3.58 ICM426XX_INTF_CONFIG0_FIFO_COUNT_ENDIAN_t

enum ICM426XX_INTF_CONFIG0_FIFO_COUNT_ENDIAN_t

Enumerator

ICM426XX_INTF_CONFIG0_FIFO_COUNT_BIG_ENDIAN	
ICM426XX_INTF_CONFIG0_FIFO_COUNT_LITTLE_ENDIAN	

7.1.3.59 ICM426XX_INTF_CONFIG0_FIFO_COUNT_REC_t

enum ICM426XX_INTF_CONFIG0_FIFO_COUNT_REC_t

Enumerator

ICM426XX_INTF_CONFIG0_FIFO_COUNT_REC_RECORD	
ICM426XX_INTF_CONFIG0_FIFO_COUNT_REC_BYTE	

7.1.3.60 ICM426XX_INTF_CONFIG0_FIFO_SREG_INVALID_IND_t

enum ICM426XX_INTF_CONFIG0_FIFO_SREG_INVALID_IND_t

Enumerator

ICM426XX_INTF_CONFIG0_FIFO_SREG_INVALID_IND_DIS	
ICM426XX_INTF_CONFIG0_FIFO_SREG_INVALID_IND_EN	

7.1.3.61 ICM426XX_INTF_CONFIG0_SPI_MODE_OIS1_t

enum ICM426XX_INTF_CONFIG0_SPI_MODE_OIS1_t

Enumerator

ICM426XX_INTF_CONFIG0_SPI_MODE_OIS1_1↩_2	
ICM426XX_INTF_CONFIG0_SPI_MODE_OIS1_0↩_3	

7.1.3.62 ICM426XX_INTF_CONFIG0_SPI_MODE_OIS2_t

enum ICM426XX_INTF_CONFIG0_SPI_MODE_OIS2_t

Enumerator

ICM426XX_INTF_CONFIG0_SPI_MODE_OIS2_1↩_2	
ICM426XX_INTF_CONFIG0_SPI_MODE_OIS2_0↩_3	

7.1.3.63 ICM426XX_INTF_CONFIG1_ACCEL_LP_CLK_t

enum ICM426XX_INTF_CONFIG1_ACCEL_LP_CLK_t

Enumerator

ICM426XX_INTF_CONFIG1_ACCEL_LP_CLK_WUOSC	
ICM426XX_INTF_CONFIG1_ACCEL_LP_CLK_RCOSC	

7.1.3.64 ICM426XX_INTF_CONFIG1_RTC_MODE_t

enum ICM426XX_INTF_CONFIG1_RTC_MODE_t

Enumerator

ICM426XX_INTF_CONFIG1_RTC_MODE_DIS	
ICM426XX_INTF_CONFIG1_RTC_MODE_EN	

7.1.3.65 ICM426XX_INTF_CONFIG4_AP_SPI_t

enum ICM426XX_INTF_CONFIG4_AP_SPI_t

Enumerator

ICM426XX_INTF_CONFIG4_AP_SPI4W	
ICM426XX_INTF_CONFIG4_AP_SPI3W	

7.1.3.66 ICM426XX_INTF_CONFIG4_AUX1_SPI_t

enum ICM426XX_INTF_CONFIG4_AUX1_SPI_t

Enumerator

ICM426XX_INTF_CONFIG4_AUX1_SPI4W	
ICM426XX_INTF_CONFIG4_AUX1_SPI3W	

7.1.3.67 ICM426XX_OIS1_CONFIG1_ACCEL_EN_t

enum ICM426XX_OIS1_CONFIG1_ACCEL_EN_t

Enumerator

ICM426XX_OIS1_CONFIG1_ACCEL_EN	
ICM426XX_OIS1_CONFIG1_ACCEL_DIS	

7.1.3.68 ICM426XX_OIS1_CONFIG1_ACCEL_LP_CLK_SEL_t

enum ICM426XX_OIS1_CONFIG1_ACCEL_LP_CLK_SEL_t

Enumerator

ICM426XX_OIS1_CONFIG1_ACCEL_LP_CLK_SEL_WUOSC	
ICM426XX_OIS1_CONFIG1_ACCEL_LP_CLK_SEL_RCOSC	

7.1.3.69 ICM426XX_OIS1_CONFIG1_DEC_t

enum ICM426XX_OIS1_CONFIG1_DEC_t

OIS1 rate selection (base clock fixed by OTP divided by decimator value)

Enumerator

ICM426XX_OIS1_CONFIG1_DEC_1	OTP_OIS_clock / 1.
ICM426XX_OIS1_CONFIG1_DEC_2	OTP_OIS_clock / 2.
ICM426XX_OIS1_CONFIG1_DEC_4	OTP_OIS_clock / 4.
ICM426XX_OIS1_CONFIG1_DEC_8	OTP_OIS_clock / 8.
ICM426XX_OIS1_CONFIG1_DEC_16	OTP_OIS_clock / 16.
ICM426XX_OIS1_CONFIG1_DEC_32	OTP_OIS_clock / 32.

7.1.3.70 ICM426XX_OIS1_CONFIG1_GYRO_EN_t

enum ICM426XX_OIS1_CONFIG1_GYRO_EN_t

Enumerator

ICM426XX_OIS1_CONFIG1_GYRO_EN	
ICM426XX_OIS1_CONFIG1_GYRO_DIS	

7.1.3.71 ICM426XX_OIS1_CONFIG2_ACCEL_FS_SEL_t

enum ICM426XX_OIS1_CONFIG2_ACCEL_FS_SEL_t

OIS1 accelerometer FSR selection.

Enumerator

ICM426XX_OIS1_CONFIG2_ACCEL_FS_SEL_RESERVED	
ICM426XX_OIS1_CONFIG2_ACCEL_FS_SEL_2g	2g
ICM426XX_OIS1_CONFIG2_ACCEL_FS_SEL_4g	4g
ICM426XX_OIS1_CONFIG2_ACCEL_FS_SEL_8g	8g
ICM426XX_OIS1_CONFIG2_ACCEL_FS_SEL_16g	16g

7.1.3.72 ICM426XX_OIS1_CONFIG2_GYRO_FS_SEL_t

enum ICM426XX_OIS1_CONFIG2_GYRO_FS_SEL_t

OIS1 gyroscope FSR selection.

Enumerator

ICM426XX_OIS1_CONFIG2_GYRO_FS_SEL_16dps	15.625 dps
ICM426XX_OIS1_CONFIG2_GYRO_FS_SEL_31dps	31.25 dps
ICM426XX_OIS1_CONFIG2_GYRO_FS_SEL_62dps	62.5 dps
ICM426XX_OIS1_CONFIG2_GYRO_FS_SEL_125dps	125 dps
ICM426XX_OIS1_CONFIG2_GYRO_FS_SEL_250dps	250 dps
ICM426XX_OIS1_CONFIG2_GYRO_FS_SEL_500dps	500 dps
ICM426XX_OIS1_CONFIG2_GYRO_FS_SEL_1000dps	1000 dps
ICM426XX_OIS1_CONFIG2_GYRO_FS_SEL_2000dps	2000 dps

7.1.3.73 ICM426XX_OIS2_CONFIG1_ACCEL_EN_t

`enum ICM426XX_OIS2_CONFIG1_ACCEL_EN_t`

Enumerator

ICM426XX_OIS2_CONFIG1_ACCEL_EN	
ICM426XX_OIS2_CONFIG1_ACCEL_DIS	

7.1.3.74 ICM426XX_OIS2_CONFIG1_ACCEL_LP_CLK_SEL_t

`enum ICM426XX_OIS2_CONFIG1_ACCEL_LP_CLK_SEL_t`

Enumerator

ICM426XX_OIS2_CONFIG1_ACCEL_LP_CLK_SEL_WUOSC	
ICM426XX_OIS2_CONFIG1_ACCEL_LP_CLK_SEL_RCOSC	

7.1.3.75 ICM426XX_OIS2_CONFIG1_DEC_t

`enum ICM426XX_OIS2_CONFIG1_DEC_t`

OIS2 rate selection (base clock fixed by OTP divided by decimator value)

Enumerator

ICM426XX_OIS2_CONFIG1_DEC_1	OTP_OIS_clock / 1.
ICM426XX_OIS2_CONFIG1_DEC_2	OTP_OIS_clock / 2.
ICM426XX_OIS2_CONFIG1_DEC_4	OTP_OIS_clock / 4.
ICM426XX_OIS2_CONFIG1_DEC_8	OTP_OIS_clock / 8.
ICM426XX_OIS2_CONFIG1_DEC_16	OTP_OIS_clock / 16.
ICM426XX_OIS2_CONFIG1_DEC_32	OTP_OIS_clock / 32.

7.1.3.76 ICM426XX_OIS2_CONFIG1_GYRO_EN_t

enum ICM426XX_OIS2_CONFIG1_GYRO_EN_t

Enumerator

ICM426XX_OIS2_CONFIG1_GYRO_EN	
ICM426XX_OIS2_CONFIG1_GYRO_DIS	

7.1.3.77 ICM426XX_OIS2_CONFIG2_ACCEL_FS_SEL_t

enum ICM426XX_OIS2_CONFIG2_ACCEL_FS_SEL_t

OIS2 accelerometer FSR selection.

Enumerator

ICM426XX_OIS2_CONFIG2_ACCEL_FS_SEL_RESERVED	
ICM426XX_OIS2_CONFIG2_ACCEL_FS_SEL_2g	2g
ICM426XX_OIS2_CONFIG2_ACCEL_FS_SEL_4g	4g
ICM426XX_OIS2_CONFIG2_ACCEL_FS_SEL_8g	8g
ICM426XX_OIS2_CONFIG2_ACCEL_FS_SEL_16g	16g

7.1.3.78 ICM426XX_OIS2_CONFIG2_GYRO_FS_SEL_t

enum ICM426XX_OIS2_CONFIG2_GYRO_FS_SEL_t

OIS2 gyroscope FSR selection.

Enumerator

ICM426XX_OIS2_CONFIG2_GYRO_FS_SEL_16dps	15.625 dps
ICM426XX_OIS2_CONFIG2_GYRO_FS_SEL_31dps	31.25 dps
ICM426XX_OIS2_CONFIG2_GYRO_FS_SEL_62dps	62.5 dps
ICM426XX_OIS2_CONFIG2_GYRO_FS_SEL_125dps	125 dps
ICM426XX_OIS2_CONFIG2_GYRO_FS_SEL_250dps	250 dps
ICM426XX_OIS2_CONFIG2_GYRO_FS_SEL_500dps	500 dps
ICM426XX_OIS2_CONFIG2_GYRO_FS_SEL_1000dps	1000 dps
ICM426XX_OIS2_CONFIG2_GYRO_FS_SEL_2000dps	2000 dps

7.1.3.79 ICM426XX_PWR_MGMT_0_ACCEL_MODE_t

enum ICM426XX_PWR_MGMT_0_ACCEL_MODE_t

Enumerator

ICM426XX_PWR_MGMT_0_ACCEL_MODE_LN	
ICM426XX_PWR_MGMT_0_ACCEL_MODE_LP	
ICM426XX_PWR_MGMT_0_ACCEL_MODE_OFF	

7.1.3.80 ICM426XX_PWR_MGMT_0_GYRO_MODE_t

enum ICM426XX_PWR_MGMT_0_GYRO_MODE_t

Enumerator

ICM426XX_PWR_MGMT_0_GYRO_MODE_LN	
ICM426XX_PWR_MGMT_0_GYRO_MODE_STANDBY	
ICM426XX_PWR_MGMT_0_GYRO_MODE_OFF	

7.1.3.81 ICM426XX_PWR_MGMT_0_IDLE_t

enum ICM426XX_PWR_MGMT_0_IDLE_t

Enumerator

ICM426XX_PWR_MGMT_0_IDLE_DIS	
ICM426XX_PWR_MGMT_0_IDLE_EN	

7.1.3.82 ICM426XX_PWR_MGMT_0_TEMP_t

enum ICM426XX_PWR_MGMT_0_TEMP_t

Enumerator

ICM426XX_PWR_MGMT_0_TEMP_DIS	
ICM426XX_PWR_MGMT_0_TEMP_EN	

7.1.3.83 ICM426XX_SENSOR_CONFIG2_OIS_MODE_t

enum ICM426XX_SENSOR_CONFIG2_OIS_MODE_t

Enumerator

ICM426XX_SENSOR_CONFIG2_OIS_MODE_32KHZ	
ICM426XX_SENSOR_CONFIG2_OIS_MODE_8KHZ	
ICM426XX_SENSOR_CONFIG2_OIS_MODE_DIS	

7.1.3.84 ICM426XX_SIGNAL_PATH_RESET_DMP_INIT_t

enum ICM426XX_SIGNAL_PATH_RESET_DMP_INIT_t

Enumerator

ICM426XX_SIGNAL_PATH_RESET_DMP_INIT_EN	
ICM426XX_SIGNAL_PATH_RESET_DMP_INIT_DIS	

7.1.3.85 ICM426XX_SIGNAL_PATH_RESET_DMP_MEM_RESET_t

enum ICM426XX_SIGNAL_PATH_RESET_DMP_MEM_RESET_t

Enumerator

ICM426XX_SIGNAL_PATH_RESET_DMP_MEM_RESET_EN	
ICM426XX_SIGNAL_PATH_RESET_DMP_MEM_RESET_DIS	

7.1.3.86 ICM426XX_SIGNAL_PATH_RESET_FIFO_FLUSH_t

enum ICM426XX_SIGNAL_PATH_RESET_FIFO_FLUSH_t

Enumerator

ICM426XX_SIGNAL_PATH_RESET_FIFO_FLUSH_EN	
ICM426XX_SIGNAL_PATH_RESET_FIFO_FLUSH_DIS	

7.1.3.87 ICM426XX_SIGNAL_PATH_RESET_TMST_STROBE_t

enum ICM426XX_SIGNAL_PATH_RESET_TMST_STROBE_t

Enumerator

ICM426XX_SIGNAL_PATH_RESET_TMST_STROBE_EN	
ICM426XX_SIGNAL_PATH_RESET_TMST_STROBE_DIS	

7.1.3.88 ICM426XX_SMD_CONFIG_SMD_MODE_t

enum ICM426XX_SMD_CONFIG_SMD_MODE_t

Enumerator

ICM426XX_SMD_CONFIG_SMD_MODE_LONG	
ICM426XX_SMD_CONFIG_SMD_MODE_SHORT	
ICM426XX_SMD_CONFIG_SMD_MODE_WOM	
ICM426XX_SMD_CONFIG_SMD_MODE_DISABLED	

7.1.3.89 ICM426XX_SMD_CONFIG_WOM_INT_MODE_t

enum ICM426XX_SMD_CONFIG_WOM_INT_MODE_t

Enumerator

ICM426XX_SMD_CONFIG_WOM_INT_MODE_ANDED	
ICM426XX_SMD_CONFIG_WOM_INT_MODE_ORED	

7.1.3.90 ICM426XX_SMD_CONFIG_WOM_MODE_t

enum ICM426XX_SMD_CONFIG_WOM_MODE_t

Enumerator

ICM426XX_SMD_CONFIG_WOM_MODE_CMP_PREV	
ICM426XX_SMD_CONFIG_WOM_MODE_CMP_INIT	

7.1.3.91 ICM426XX_TMST_CONFIG_RESOL_t

enum ICM426XX_TMST_CONFIG_RESOL_t

Enumerator

ICM426XX_TMST_CONFIG_RESOL_16us	
ICM426XX_TMST_CONFIG_RESOL_1us	

7.1.3.92 ICM426XX_TMST_CONFIG_TMST_EN_t

enum ICM426XX_TMST_CONFIG_TMST_EN_t

Enumerator

ICM426XX_TMST_CONFIG_TMST_EN	
ICM426XX_TMST_CONFIG_TMST_DIS	

7.1.3.93 ICM426XX_TMST_CONFIG_TMST_FSYNC_EN_t

enum ICM426XX_TMST_CONFIG_TMST_FSYNC_EN_t

Enumerator

ICM426XX_TMST_CONFIG_TMST_FSYNC_EN	
ICM426XX_TMST_CONFIG_TMST_FSYNC_DIS	

7.1.3.94 ICM426XX_TMST_CONFIG_TMST_TO_REGS_EN_t

enum ICM426XX_TMST_CONFIG_TMST_TO_REGS_EN_t

Enumerator

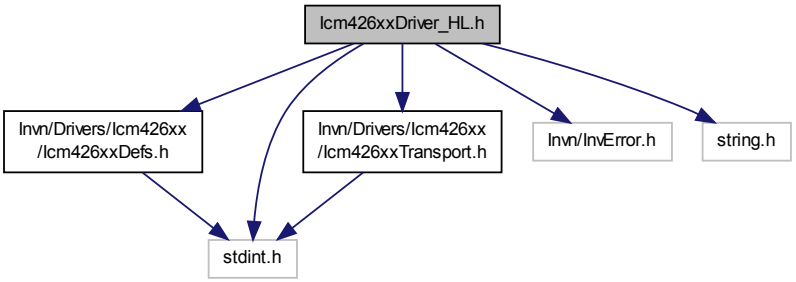
ICM426XX_TMST_CONFIG_TMST_TO_REGS_EN	
ICM426XX_TMST_CONFIG_TMST_TO_REGS_DIS	

7.2 Icm426xxDriver_HL.h File Reference

```
#include "Invn/Drivers/Icm426xx/Icm426xxDefs.h"
```

```
#include "Invn/Drivers/Icm426xx/Icm426xxTransport.h"
#include "Invn/InvError.h"
#include <stdint.h>
#include <string.h>
```

Include dependency graph for Icm426xxDriver_HL.h:



Classes

- struct inv_icm426xx_sensor_event_t

  Sensor event structure definition.
- struct inv_icm426xx

  Icm426xx driver states definition.
- struct inv_icm426xx_interrupt_parameter_t

  Icm426xx set of interrupt enable flag.

Macros

- #define INV_ICM426XX_LIGHTWEIGHT_DRIVER 0

  Lighten driver logic by stripping out procedures on transitions.
- #define PLL_SCALE_FACTOR_Q24 (1UL << 24)

  Scale factor and max ODR Dependant of chip.
- #define ICM_PART_DEFAULT_OIS_MODE ICM426XX_SENSOR_CONFIG2_OIS_MODE_8KHZ
- #define ACCEL_CONFIG0_FS_SEL_MAX ICM426XX_ACCEL_CONFIG0_FS_SEL_16g

  Max FSR values for accel and gyro Dependant of chip.
- #define GYRO_CONFIG0_FS_SEL_MAX ICM426XX_GYRO_CONFIG0_FS_SEL_2000dps
- #define ACCEL_OFFUSER_MAX_MG 1000
- #define GYRO_OFFUSER_MAX_DPS 64
- #define RTC_SUPPORTED 0

  RTC Support flag Define whether the RTC mode is supported Dependant of chip.
- #define ICM426XX_FIFO_MIRRORING_SIZE 16 * 129

  Icm426xx maximum buffer size mirrored from FIFO at polling time.
- #define ICM426XX_DEFAULT_WOM_THS_MG 52 >> 2 /* = 52mg/4 */

  Default value for the WOM threshold Resolution of the threshold is ~= 4mg.
- #define ICM426XX_ACC_STARTUP_TIME_US 20000U

  Icm426xx Accelerometer start-up time before having correct data.
- #define ICM426XX_GYR_STARTUP_TIME_US 60000U

  Icm426xx Gyroscope start-up time before having correct data.

Enumerations

- enum inv_icm426xx_sensor { INV_ICM426XX_SENSOR_ACCEL , INV_ICM426XX_SENSOR_GYRO , INV_ICM426XX_SENSOR_FSYNC_EVENT , INV_ICM426XX_SENSOR_OIS , INV_ICM426XX_SENSOR_TEMPERATURE , INV_ICM426XX_SENSOR_TAP , INV_ICM426XX_SENSOR_DMP_PEDOMETER , INV_ICM426XX_SENSOR_DMP_PEDOMETER_COUNT , INV_ICM426XX_SENSOR_DMP_TILT , INV_ICM426XX_SENSOR_MAX }

  Sensor identifier for UI control and OIS function.
- enum INV_ICM426XX_FIFO_CONFIG_t { INV_ICM426XX_FIFO_DISABLED = 0 , INV_ICM426XX_FIFO_ENABLED = 1 }

  Configure Fifo usage.
- enum inv_icm426xx_interrupt_value { INV_ICM426XX_DISABLE = 0 , INV_ICM426XX_ENABLE }

Functions

- int inv_icm426xx_set_reg_bank (struct inv_icm426xx *s, uint8_t bank)

  Set register bank index.
- int inv_icm426xx_init (struct inv_icm426xx *s, struct inv_icm426xx_serif *serif, void(*sensor_event_cb)(inv_icm426xx_sensor_event_t *event))

  Initializes device.
- int inv_icm426xx_device_reset (struct inv_icm426xx *s)

  Perform a soft reset of the device.
- int inv_icm426xx_get_who_am_i (struct inv_icm426xx *s, uint8_t *who_am_i)

  return WHOAMI value
- int inv_icm426xx_force_clock_source (struct inv_icm426xx *s, ICM426XX_INTF_CONFIG1_ACCEL_LP_CLK_t clk_src)

  Configure Accel clock source.
- int inv_icm426xx_enable_accel_low_power_mode (struct inv_icm426xx *s)

  Enable accel in low power mode.
- int inv_icm426xx_enable_accel_low_noise_mode (struct inv_icm426xx *s)

  Enable accel in low noise mode.
- int inv_icm426xx_disable_accel (struct inv_icm426xx *s)

  Disable accel.
- int inv_icm426xx_enable_gyro_low_noise_mode (struct inv_icm426xx *s)

  Enable gyro in low noise mode.
- int inv_icm426xx_disable_gyro (struct inv_icm426xx *s)

  Disable gyro.
- int inv_icm426xx_enable_fsync (struct inv_icm426xx *s)

  Enable fsync tagging functionality.
- int inv_icm426xx_disable_fsync (struct inv_icm426xx *s)

  Disable fsync tagging functionality.
- int inv_icm426xx_configure_timestamp_resolution (struct inv_icm426xx *s, ICM426XX_TMST_CONFIG_RESOL_t resol)

  Configure timestamp resolution from FIFO.
- int inv_icm426xx_set_config_ibi (struct inv_icm426xx *s, inv_icm426xx_interrupt_parameter_t *interrupt_to_configure)

  Configure which interrupt source can trigger IBI interruptions.
- int inv_icm426xx_get_config_ibi (struct inv_icm426xx *s, inv_icm426xx_interrupt_parameter_t *interrupt_to_configure)

  Retrieve interrupts configuration.

- int inv_icm426xx_set_config_int1 (struct inv_icm426xx *s, inv_icm426xx_interrupt_parameter_t *interrupt_to_configure)

  Configure which interrupt source can trigger INT1.
- int inv_icm426xx_get_config_int1 (struct inv_icm426xx *s, inv_icm426xx_interrupt_parameter_t *interrupt_to_configure)

  Retrieve interrupts configuration.
- int inv_icm426xx_set_config_int2 (struct inv_icm426xx *s, inv_icm426xx_interrupt_parameter_t *interrupt_to_configure)

  Configure which interrupt source can trigger INT2.
- int inv_icm426xx_get_config_int2 (struct inv_icm426xx *s, inv_icm426xx_interrupt_parameter_t *interrupt_to_configure)

  Retrieve interrupts configuration.
- int inv_icm426xx_get_data_from_registers (struct inv_icm426xx *s)

  Read all registers containing data (temperature, accelerometer and gyroscope).
- int inv_icm426xx_get_data_from_fifo (struct inv_icm426xx *s)

  Read all available packets from the FIFO.
- uint32_t inv_icm426xx_convert_odr_bitfield_to_us (uint32_t odr_bitfield)

  Converts `ICM426XX_ACCEL_CONFIG0_ODR_t` or `ICM426XX_GYRO_CONFIG0_ODR_t` enums to period expressed in us.
- int inv_icm426xx_set_accel_frequency (struct inv_icm426xx *s, const ICM426XX_ACCEL_CONFIG0_ODR_t frequency)

  Configure accel Output Data Rate.
- int inv_icm426xx_set_gyro_frequency (struct inv_icm426xx *s, const ICM426XX_GYRO_CONFIG0_ODR_t frequency)

  Configure gyro Output Data Rate.
- int inv_icm426xx_set_accel_fsr (struct inv_icm426xx *s, ICM426XX_ACCEL_CONFIG0_FS_SEL_t accel_fsr_g)

  Set accel full scale range.
- int inv_icm426xx_get_accel_fsr (struct inv_icm426xx *s, ICM426XX_ACCEL_CONFIG0_FS_SEL_t *accel_fsr_g)

  Access accel full scale range.
- int inv_icm426xx_set_gyro_fsr (struct inv_icm426xx *s, ICM426XX_GYRO_CONFIG0_FS_SEL_t gyro_fsr_dps)

  Set gyro full scale range.
- int inv_icm426xx_get_gyro_fsr (struct inv_icm426xx *s, ICM426XX_GYRO_CONFIG0_FS_SEL_t *gyro_fsr_dps)

  Access gyro full scale range.
- int inv_icm426xx_set_accel_lp_avg (struct inv_icm426xx *s, ICM426XX_GYRO_ACCEL_CONFIG0_ACCEL_FILT_AVG_t acc_avg)

  Set accel Low-Power averaging value.
- int inv_icm426xx_set_accel_ln_bw (struct inv_icm426xx *s, ICM426XX_GYRO_ACCEL_CONFIG0_ACCEL_FILT_BW_t acc_bw)

  Set accel Low-Noise bandwidth value.
- int inv_icm426xx_set_gyro_ln_bw (struct inv_icm426xx *s, ICM426XX_GYRO_ACCEL_CONFIG0_GYRO_FILT_BW_t gyr_bw)

  Set gyro Low-Noise bandwidth value.
- int inv_icm426xx_reset_fifo (struct inv_icm426xx *s)

  reset ICM426XX fifo
- int inv_icm426xx_enable_timestamp_to_register (struct inv_icm426xx *s)

  Enable the 20bits-timestamp register access to read in a reliable way the strobed timestamp.
- int inv_icm426xx_disable_timestamp_to_register (struct inv_icm426xx *s)

  Disable the 20bits-timestamp register access.
- int inv_icm426xx_get_current_timestamp (struct inv_icm426xx *s, uint32_t *icm_time)

Get the timestamp value of icm426xx from register.

- int inv_icm426xx_enable_clkin_rtc (struct inv_icm426xx *s, uint8_t enable)

  Enable or disable CLKIN/RTC capability.
- int inv_icm426xx_get_clkin_rtc_status (struct inv_icm426xx *s)

  Get CLKIN/RTC feature status.
- int inv_icm426xx_enable_high_resolution_fifo (struct inv_icm426xx *s)

  Enable 20 bits raw acc and raw gyr data in fifo.
- int inv_icm426xx_disable_high_resolution_fifo (struct inv_icm426xx *s)

  Disable 20 bits raw acc and raw gyr data in fifo.
- int inv_icm426xx_configure_fifo (struct inv_icm426xx *s, INV_ICM426XX_FIFO_CONFIG_t fifo_config)

  Configure Fifo to select the way data are gathered.
- int inv_icm426xx_configure_fifo_wm (struct inv_icm426xx *s, uint16_t wm)

  Configure Fifo watermark (also referred to as fifo threshold).
- uint32_t inv_icm426xx_get_fifo_timestamp_resolution_us_q24 (struct inv_icm426xx *s)

  Get FIFO timestamp resolution.
- uint32_t inv_icm426xx_get_reg_timestamp_resolution_us_q24 (struct inv_icm426xx *s)

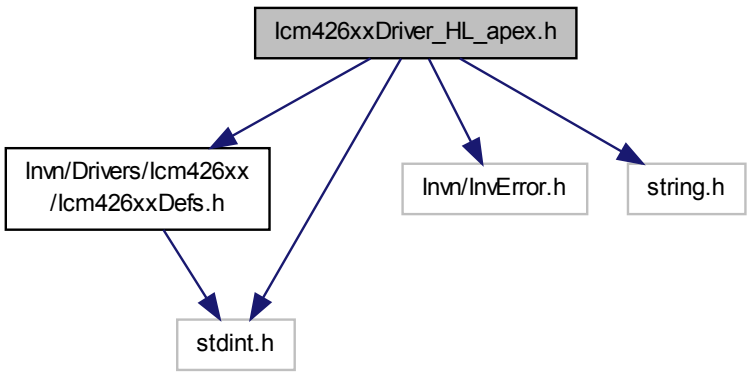
  Get register timestamp resolution.
- const char * inv_icm426xx_get_version (void)

  Return driver version x.y.z-suffix as a char array.

7.3 Icm426xxDriver_HL_apex.h File Reference

```
#include "Invn/Drivers/Icm426xx/Icm426xxDefs.h"
#include "Invn/InvError.h"
#include <stdint.h>
#include <string.h>
```

Include dependency graph for Icm426xxDriver_HL_apex.h:



Classes

- struct inv_icm426xx_tap_parameters_t

  Icm426xx TAP inputs parameters definition.
- struct inv_icm426xx_apex_parameters

  Icm426xx APEX inputs parameters definition.
- struct inv_icm426xx_apex_step_activity

  APEX pedometer outputs.
- struct inv_icm426xx_tap_data

  TAP outputs.

Typedefs

- typedef struct inv_icm426xx_apex_parameters inv_icm426xx_apex_parameters_t

  Icm426xx APEX inputs parameters definition.
- typedef struct inv_icm426xx_apex_step_activity inv_icm426xx_apex_step_activity_t

  APEX pedometer outputs.
- typedef struct inv_icm426xx_tap_data inv_icm426xx_tap_data_t

  TAP outputs.

Functions

- int inv_icm426xx_configure_smd_wom (struct inv_icm426xx ∗s, const uint8_t x_th, const uint8_t y_th, const uint8_t z_th, ICM426XX_SMD_CONFIG_WOM_INT_MODE_t wom_int, ICM426XX_SMD_CONFIG_WOM_MODE_t wom_mode)

  Configure Wake On Motion and SMD thresholds.
- int inv_icm426xx_enable_wom (struct inv_icm426xx ∗s)

  Enable Wake On Motion.
- int inv_icm426xx_disable_wom (struct inv_icm426xx ∗s)

  Disable Wake On Motion.
- int inv_icm426xx_enable_smd (struct inv_icm426xx ∗s)

  Enable Significant Motion Detection.
- int inv_icm426xx_disable_smd (struct inv_icm426xx ∗s)

  Disable Significant Motion Detection.
- int inv_icm426xx_init_tap_parameters_struct (struct inv_icm426xx ∗s, inv_icm426xx_tap_parameters_t ∗tap_inputs)

  Fill the TAP parameters structure with all the default parameters for TAP algorithm.
- int inv_icm426xx_configure_tap_parameters (struct inv_icm426xx ∗s, const inv_icm426xx_tap_parameters_t ∗tap_inputs)

  Configure TAP.
- int inv_icm426xx_get_tap_parameters (struct inv_icm426xx ∗s, inv_icm426xx_tap_parameters_t ∗tap_↩ params)

  Returns current TAP parameters.
- int inv_icm426xx_enable_tap (struct inv_icm426xx ∗s)

  Enable TAP.
- int inv_icm426xx_disable_tap (struct inv_icm426xx ∗s)

  Disable TAP.
- int inv_icm426xx_init_apex_parameters_struct (struct inv_icm426xx ∗s, inv_icm426xx_apex_parameters_t ∗apex_inputs)

  Fill the APEX parameters structure with all the default parameters for APEX algorithms (pedometer, tilt)

- int inv_icm426xx_configure_apex_parameters (struct inv_icm426xx *s, const inv_icm426xx_apex_parameters_t *apex_inputs)

  Configures DMP parameters for APEX algorithms (pedometer, tilt).
- int inv_icm426xx_get_apex_parameters (struct inv_icm426xx *s, inv_icm426xx_apex_parameters_t *apex_params)

  Returns current DMP parameters for APEX algorithms (pedometer, tilt).
- int inv_icm426xx_set_apex_frequency (struct inv_icm426xx *s, const ICM426XX_APEX_CONFIG0_DMP_ODR_t frequency)

  Configure DMP Output Data Rate for APEX algorithms (pedometer, tilt)
- int inv_icm426xx_start_dmp (struct inv_icm426xx *s)

  Start DMP for APEX algorithms.
- int inv_icm426xx_reset_dmp (struct inv_icm426xx *s)

  Reset DMP memory.
- int inv_icm426xx_enable_apex_pedometer (struct inv_icm426xx *s)

  Enable APEX algorithm Pedometer.
- int inv_icm426xx_disable_apex_pedometer (struct inv_icm426xx *s)

  Disable APEX algorithm Pedometer.
- int inv_icm426xx_enable_apex_tilt (struct inv_icm426xx *s)

  Enable APEX algorithm Tilt.
- int inv_icm426xx_disable_apex_tilt (struct inv_icm426xx *s)

  Disable APEX algorithm Tilt.
- int inv_icm426xx_get_apex_data_activity (struct inv_icm426xx *s, inv_icm426xx_apex_step_activity_t *apex_activity)

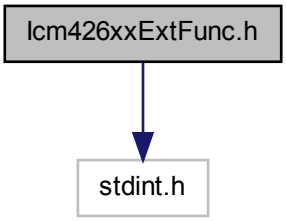
  Retrieve APEX pedometer outputs and format them.
- int inv_icm426xx_get_tap_data (struct inv_icm426xx *s, inv_icm426xx_tap_data_t *tap_data)

  Retrieve tap outputs.
- int inv_icm426xx_load_dmp_sram_code (struct inv_icm426xx *s, const uint8_t *dmp_prog, const uint32_t start_offset, const uint32_t size)

  Load custom DMP image into SRAM.

7.4 Icm426xxExtFunc.h File Reference

`#include <stdint.h>`
Include dependency graph for Icm426xxExtFunc.h:



Functions

- void inv_icm426xx_sleep_us (uint32_t us)

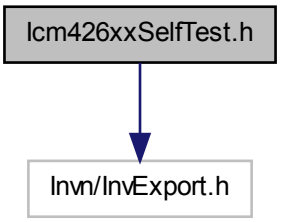
  Hook for low-level high res system sleep() function to be implemented by upper layer ~100us resolution is sufficient.
- uint64_t inv_icm426xx_get_time_us (void)

  Hook for low-level high res system get_time() function to be implemented by upper layer Timer should be on 64bit with a 1 us resolution.

7.5 Icm426xxSelfTest.h File Reference

```
#include "Invn/InvExport.h"
```

Include dependency graph for Icm426xxSelfTest.h:



Functions

- int inv_icm426xx_run_selftest (struct inv_icm426xx *s, int *result)

  Perform hardware self-test for Accel and Gyro.
- int inv_icm426xx_get_st_bias (struct inv_icm426xx *s, int st_bias[6])

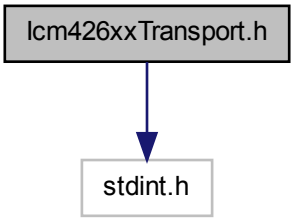
  Retrieve bias collected by self-test.
- int inv_icm426xx_set_st_bias (struct inv_icm426xx *s, const int st_bias[6])

  Apply bias.

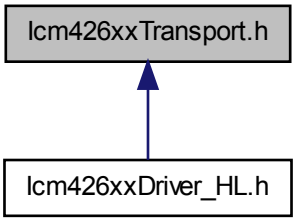
7.6 Icm426xxTransport.h File Reference

```
#include <stdint.h>
```

Include dependency graph for Icm426xxTransport.h:



This graph shows which files directly or indirectly include this file:



Classes

- struct inv_icm426xx_serif
  base sensor serial interface
- struct inv_icm426xx_transport
  transport interface
- struct inv_icm426xx_transport::register_cache
  Contains mirrored values of some IP registers.

Macros

- #define ICM426XX_UI_I2C 0
  identifies I2C interface.
- #define ICM426XX_UI_SPI4 1
  identifies 4-wire SPI interface.
- #define ICM426XX_UI_I3C 2
  identifies I3C interface.
- #define ICM426XX_AUX1_SPI3 3

identifies 3-wire SPI interface for AUX1.

- #define ICM426XX_AUX2_SPI3 4

  identifies 3-wire SPI interface for AUX2.

- #define ICM426XX_AUX1_SPI4 5

  identifies 4-wire SPI interface for AUX1.

Typedefs

- typedef uint32_t ICM426XX_SERIAL_IF_TYPE_t

  Serif type definition.

Functions

- int inv_icm426xx_init_transport (struct inv_icm426xx ∗s)

  Init cache variable.

- int inv_icm426xx_read_reg (struct inv_icm426xx ∗s, uint8_t reg, uint32_t len, uint8_t ∗buf)

  Reads data from a register on Icm426xx.

- int inv_icm426xx_write_reg (struct inv_icm426xx ∗s, uint8_t reg, uint32_t len, const uint8_t ∗buf)

  Writes data to a register on Icm426xx.

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