SELF PROJECT ON
ASYNCHRONOUS FIFO DESIGN

About ASYNCHRONOUS FIFO:

An asynchronous FIFO refers to a FIFO design where data values are written to a FIFO buffer from one clock domain and the data values are read from the same FIFO buffer from another clock domain, where the two clock domains are asynchronous to each other. Asynchronous FIFOs are used to safely pass data from one clock domain to another clock domain.

Designing of a 32 X 16 Asynchronous FIFO:

A 32 x 16 Aysnchronous FIFOis designed in Verilog. FIFO's are used as a solution of Clock Domain Crossing(CDC) for data transfer between two different clock domains.Like here, a Transmitter operating at a frequency of 1000 MHz and a Receiver is operating at a frequency of 100 MHz). Here, a Asynchronous FIFO is designed in verilog and implementation is done in Quartus Prime Lite. A testbench is written in verilog with the appropriate test stimulus and results are verified in ModelSim Altera. Following are results attached below:

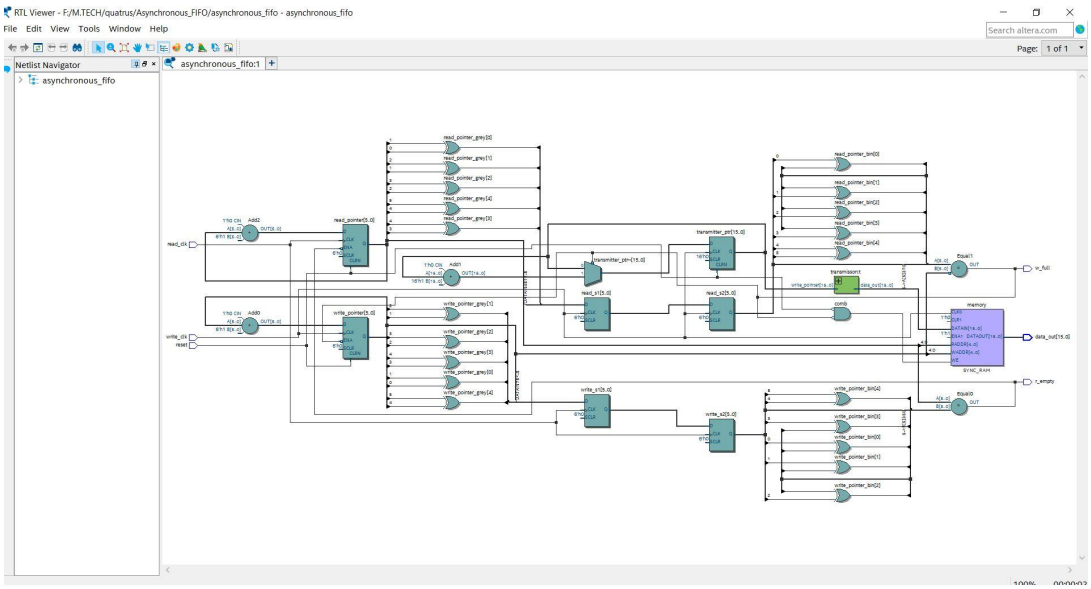

Fig 1. Quartus Netlist Generated

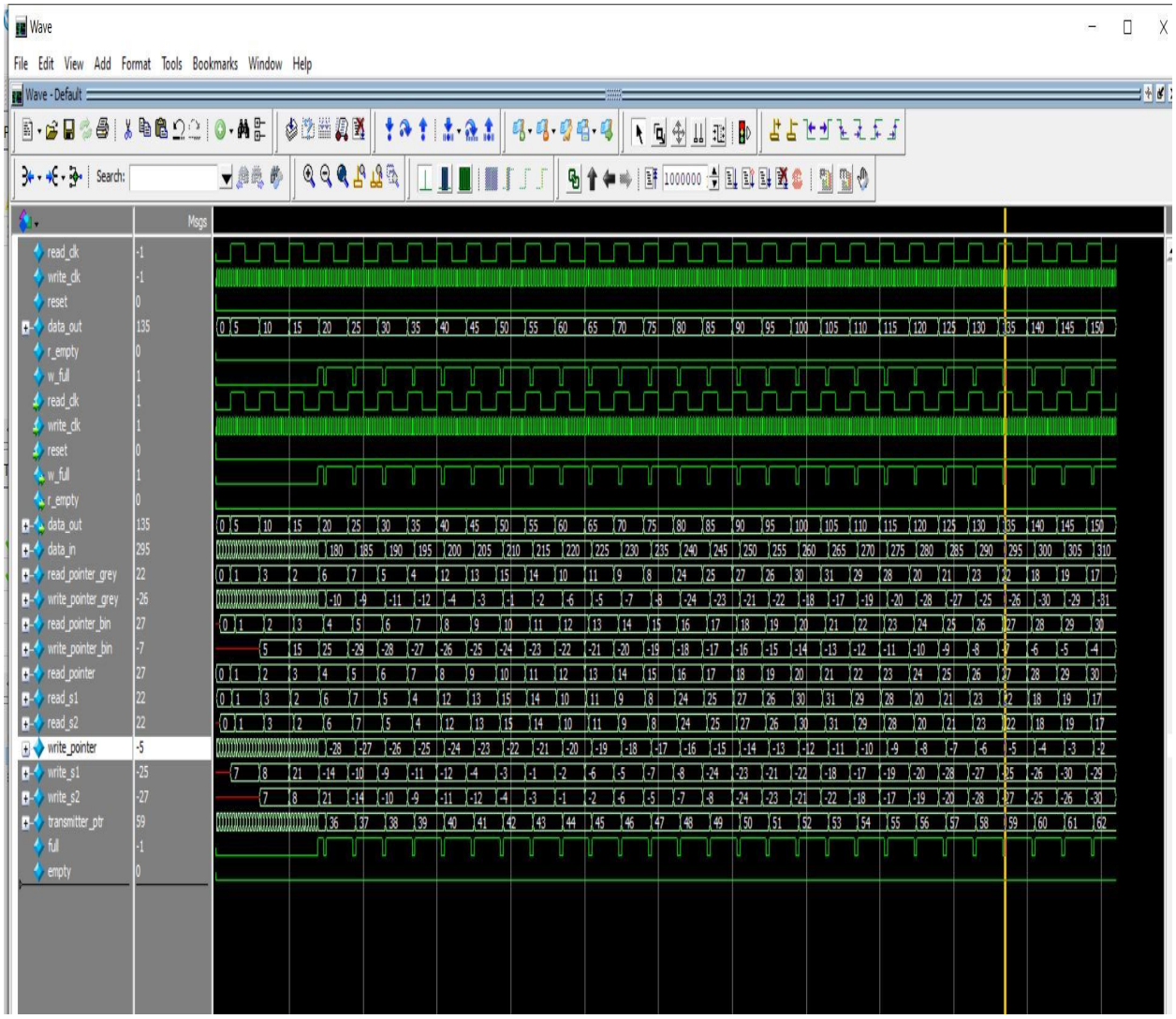

Fig 2. Modelsim Output Waveforms