DIC 作業 5 學號:312510017　宋彥霆

5-1:

前模擬:

Synthesis my design:

1000ps:

面積 = 4989.65 um^2 < 5100 um^2 且 clock_period <= 1ns

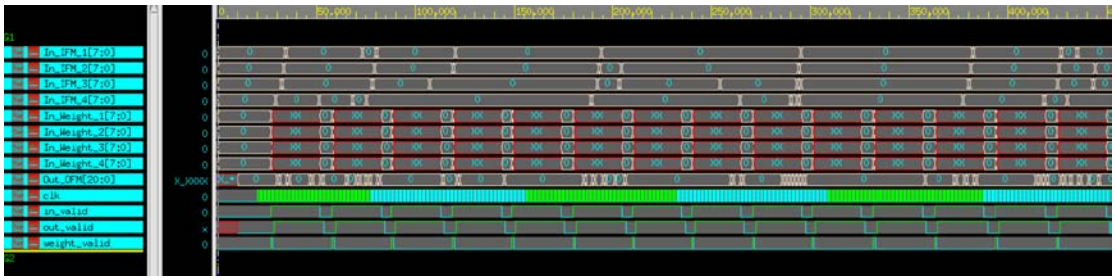
```
Combinational area:               3972.525101
Buf/Inv area:                      388.877765
Noncombinational area:            1017.100791
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  4989.625892
```

```
Startpoint: Weight_reg_8__1_
            (rising edge-triggered flip-flop clocked by clk)
Endpoint: Out_OFM_reg_18_
          (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Point                                                       Incr       Path
-----------------------------------------------------------------------------
clock clk (rise edge)                                       0.00       0.00
clock network delay (ideal)                                 0.00       0.00
Weight_reg_8__1_/CLK (DFFHQNx1_ASAP7_75t_R)                 0.00       0.00 r
Weight_reg_8__1_/QN (DFFHQNx1_ASAP7_75t_R)                 59.05      59.05 f
mult_189_9/b[1] (Convolution_DW_mult_uns_0)                 0.00      59.05 f
mult_189_9/U252/Y (NAND2xp5_ASAP7_75t_R)                   23.39      82.44 r
mult_189_9/U243/Y (NOR2xp33_ASAP7_75t_R)                   26.00     108.44 f
mult_189_9/U146/CON (FAx1_ASAP7_75t_R)                     26.07     134.51 r
mult_189_9/U280/Y (INVx1_ASAP7_75t_R)                      16.05     150.55 f
mult_189_9/U140/SN (FAx1_ASAP7_75t_R)                      50.92     201.47 r
mult_189_9/U334/Y (XOR2xp5_ASAP7_75t_R)                    36.39     237.86 r
mult_189_9/U239/Y (XOR2xp5_ASAP7_75t_R)                    35.37     273.23 r
mult_189_9/product[4] (Convolution_DW_mult_uns_0)           0.00     273.23 r
add_7_root_add_0_root_add_189_8/A[4] (Convolution_DW01_add_7)
                                                            0.00     273.23 r
add_7_root_add_0_root_add_189_8/U1_4/SN (FAx1_ASAP7_75t_R)
                                                           40.12     313.36 r
add_7_root_add_0_root_add_189_8/U23/Y (INVx1_ASAP7_75t_R)
                                                           17.88     331.24 f
add_7_root_add_0_root_add_189_8/SUM[4] (Convolution_DW01_add_7)
                                                            0.00     331.24 f
add_3_root_add_0_root_add_189_8/B[4] (Convolution_DW01_add_5)
                                                            0.00     331.24 f
add_3_root_add_0_root_add_189_8/U1_4/CON (FAx1_ASAP7_75t_R)
                                                           22.90     354.13 r
add_3_root_add_0_root_add_189_8/U16/Y (INVx1_ASAP7_75t_R)
                                                           15.50     369.64 f
add_3_root_add_0_root_add_189_8/U1_5/CON (FAx1_ASAP7_75t_R)
                                                           20.36     389.99 r
add_3_root_add_0_root_add_189_8/U15/Y (INVx1_ASAP7_75t_R)
                                                           15.52     405.51 f
add_3_root_add_0_root_add_189_8/U1_6/CON (FAx1_ASAP7_75t_R)
                                                           20.36     425.87 r
add_3_root_add_0_root_add_189_8/U14/Y (INVx1_ASAP7_75t_R)
                                                           15.51     441.39 f
add_3_root_add_0_root_add_189_8/U1_7/CON (FAx1_ASAP7_75t_R)
                                                           20.36     461.75 r
add_3_root_add_0_root_add_189_8/U13/Y (INVx1_ASAP7_75t_R)
                                                           15.50     477.24 f
add_3_root_add_0_root_add_189_8/U1_8/CON (FAx1_ASAP7_75t_R)
                                                           20.36     497.60 r
add_3_root_add_0_root_add_189_8/U12/Y (INVx1_ASAP7_75t_R)
                                                           15.51     513.10 f
add_3_root_add_0_root_add_189_8/U1_9/CON (FAx1_ASAP7_75t_R)
                                                           20.36     533.46 r
add_3_root_add_0_root_add_189_8/U11/Y (INVx1_ASAP7_75t_R)
                                                           15.50     548.96 f
add_3_root_add_0_root_add_189_8/U1_10/CON (FAx1_ASAP7_75t_R)
                                                           20.36     569.32 r
```

```
add_3_root_add_0_root_add_189_8/U9/Y (INVx1_ASAP7_75t_R)
                                                  15.51     620.69 f
add_3_root_add_0_root_add_189_8/U1_12/CON (FAx1_ASAP7_75t_R)
                                                  20.36     641.05 r
add_3_root_add_0_root_add_189_8/U8/Y (INVx1_ASAP7_75t_R)
                                                  15.50     656.55 f
add_3_root_add_0_root_add_189_8/U1_13/CON (FAx1_ASAP7_75t_R)
                                                  20.36     676.91 r
add_3_root_add_0_root_add_189_8/U7/Y (INVx1_ASAP7_75t_R)
                                                  15.50     692.41 f
add_3_root_add_0_root_add_189_8/U1_14/CON (FAx1_ASAP7_75t_R)
                                                  20.36     712.76 r
add_3_root_add_0_root_add_189_8/U6/Y (INVx1_ASAP7_75t_R)
                                                  15.50     728.26 f
add_3_root_add_0_root_add_189_8/U1_15/SN (FAx1_ASAP7_75t_R)
                                                  37.56     765.82 f
add_3_root_add_0_root_add_189_8/U29/Y (INVx1_ASAP7_75t_R)
                                                  18.83     784.66 r
add_3_root_add_0_root_add_189_8/SUM[15] (Convolution_DW01_add_5)
                                                   0.00     784.66 r
add_2_root_add_0_root_add_189_8/B[15] (Convolution_DW01_add_4)
                                                   0.00     784.66 r
add_2_root_add_0_root_add_189_8/U1_15/SN (FAx1_ASAP7_75t_R)
                                                  35.94     820.60 r
add_2_root_add_0_root_add_189_8/U31/Y (INVx1_ASAP7_75t_R)
                                                  17.51     838.10 f
add_2_root_add_0_root_add_189_8/SUM[15] (Convolution_DW01_add_4)
                                                   0.00     838.10 f
add_0_root_add_0_root_add_189_8/B[15] (Convolution_DW01_add_0)
                                                   0.00     838.10 f
add_0_root_add_0_root_add_189_8/U1_15/CON (FAx1_ASAP7_75t_R)
                                                  22.82     860.93 r
add_0_root_add_0_root_add_189_8/U9/Y (INVx1_ASAP7_75t_R)
                                                  15.27     876.20 f
add_0_root_add_0_root_add_189_8/U1_16/CON (FAx1_ASAP7_75t_R)
                                                  20.30     896.49 r
add_0_root_add_0_root_add_189_8/U8/Y (INVx1_ASAP7_75t_R)
                                                  15.27     911.76 f
add_0_root_add_0_root_add_189_8/U1_17/CON (FAx1_ASAP7_75t_R)
                                                  20.30     932.06 r
add_0_root_add_0_root_add_189_8/U7/Y (INVx1_ASAP7_75t_R)
                                                  15.56     947.62 f
add_0_root_add_0_root_add_189_8/U4/Y (XOR2xp5_ASAP7_75t_R)
                                                  19.97     967.60 f
add_0_root_add_0_root_add_189_8/SUM[18] (Convolution_DW01_add_0)
                                                   0.00     967.60 f
U277/Y (NAND2xp5_ASAP7_75t_R)                     11.33     978.92 r
Out_OFM_reg_18_/D (ASYNC_DFFHx1_ASAP7_75t_R)       0.00     978.92 r
data arrival time                                           978.92

clock clk (rise edge)                           1000.00    1000.00
clock network delay (ideal)                        0.00    1000.00
Out_OFM_reg_18_/CLK (ASYNC_DFFHx1_ASAP7_75t_R)     0.00    1000.00 r
library setup time                               -20.82     979.18
data required time                                          979.18
-------------------------------------------------------------------
data required time                                          979.18
data arrival time                                          -978.92
-------------------------------------------------------------------
slack (MET)                                                   0.25
```

後模擬:

nWave 波型(.fsdb file):



Using PrimePower to measure the power consumption of 3x3 convolution kernel

fsdb for power measurement: 通過 gate level 驗證之後，我們需要將其產生出的.fsdb 檔用來進行 power consumption 量測。

```
  Attributes
  ----------
      i  -  Including register clock pin internal power
      u  -  User defined power group

                      Internal  Switching  Leakage    Total
Power Group           Power     Power      Power      Power   (     %)  Attrs
-------------------------------------------------------------------------------
clock_network            0.0000    0.0000    0.0000    0.0000 ( 0.00%)
register              2.192e-04 2.462e-06 4.836e-08 2.217e-04 (81.07%)  i
combinational         2.208e-05 2.946e-05 2.284e-07 5.177e-05 (18.93%)
sequential               0.0000    0.0000    0.0000    0.0000 ( 0.00%)
memory                   0.0000    0.0000    0.0000    0.0000 ( 0.00%)
io_pad                   0.0000    0.0000    0.0000    0.0000 ( 0.00%)
black_box                0.0000    0.0000    0.0000    0.0000 ( 0.00%)

  Net Switching Power  = 3.192e-05   (11.67%)
  Cell Internal Power  = 2.413e-04   (88.23%)
  Cell Leakage Power   = 2.767e-07   ( 0.10%)
    Intrinsic Leakage  = 2.767e-07
    Gate Leakage       =    0.0000
                         ---------
Total Power            = 2.735e-04  (100.00%)

X Transition Power     = 1.106e-06
Glitching Power        = 7.880e-07
```

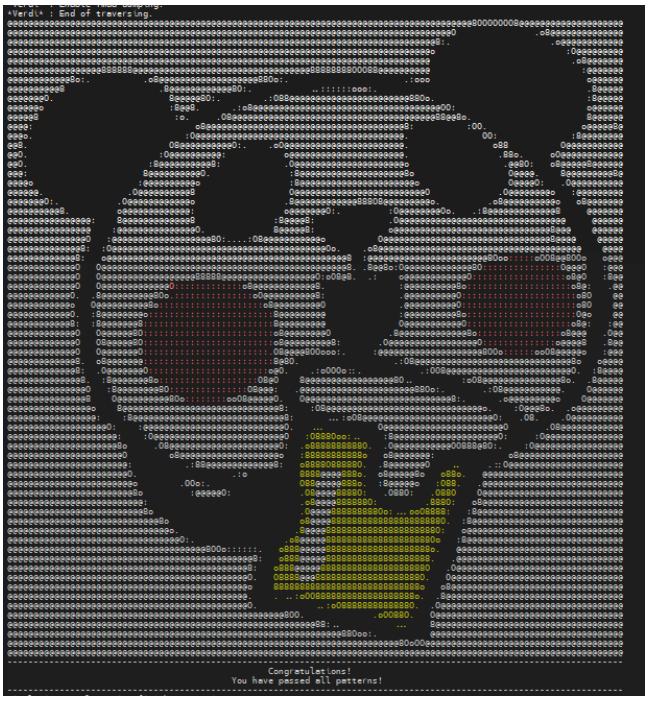
Total Power: 273.5 uW

5-2:

Gating cell: ICGx3_ASAP7_75t_R

```
621  module ICGx3_ASAP7_75t_R (GCLK, ENA, SE, CLK);
622      output GCLK;
623      input ENA, SE, CLK;
624      reg notifier;
625      wire delayed_ENA, delayed_SE, delayed_CLK;
626
627      // Function
628      wire int_fwire_clk, int_fwire_IQ, int_fwire_test;
629
630      not (int_fwire_clk, delayed_CLK);
631      or (int_fwire_test, delayed_ENA, delayed_SE);
632      altos_latch (int_fwire_IQ, notifier, int_fwire_clk, int_fwire_test);
633      and (GCLK, delayed_CLK, int_fwire_IQ);
634
635      // Timing
636
637      // Additional timing wires
638      wire adacond0, adacond1, ENA__bar;
639      wire int_twire_0, SE__bar;
640
641
642      // Additional timing gates
643      not (ENA__bar, ENA);
644      and (int_twire_0, ENA__bar, SE);
645      or (adacond0, ENA, int_twire_0);
646      not (SE__bar, SE);
647      and (adacond1, ENA__bar, SE__bar);
648
649      specify
650          if ((ENA) | (~ENA & SE))
651              (negedge CLK => (GCLK+:1'b0)) = 0;
652          if ((~ENA & ~SE))
653              (negedge CLK => (GCLK+:1'b0)) = 0;
654          ifnone (CLK => GCLK) = 0;
655          $setuphold (posedge CLK &&& ~SE, posedge ENA &&& ~SE, 0, 0, notifier,,, delayed_CLK, delayed_ENA);
656          $setuphold (posedge CLK &&& ~SE, negedge ENA &&& ~SE, 0, 0, notifier,,, delayed_CLK, delayed_ENA);
657          $setuphold (posedge CLK, posedge ENA, 0, 0, notifier,,, delayed_CLK, delayed_ENA);
658          $setuphold (posedge CLK, negedge ENA, 0, 0, notifier,,, delayed_CLK, delayed_ENA);
659          $setuphold (posedge CLK &&& ~ENA, posedge SE &&& ~ENA, 0, 0, notifier,,, delayed_CLK, delayed_SE);
660          $setuphold (posedge CLK &&& ~ENA, negedge SE &&& ~ENA, 0, 0, notifier,,, delayed_CLK, delayed_SE);
661          $setuphold (posedge CLK, posedge SE, 0, 0, notifier,,, delayed_CLK, delayed_SE);
662          $setuphold (posedge CLK, negedge SE, 0, 0, notifier,,, delayed_CLK, delayed_SE);
663          $width (posedge CLK &&& adacond0, 0, 0, notifier);
664          $width (negedge CLK &&& adacond0, 0, 0, notifier);
665          $width (negedge CLK &&& adacond1, 0, 0, notifier);
666      endspecify
667  endmodule
```

前模擬:



Synthesis my design:

1000ps:

面積 = 5450um^2 且 clock_period = 1ns

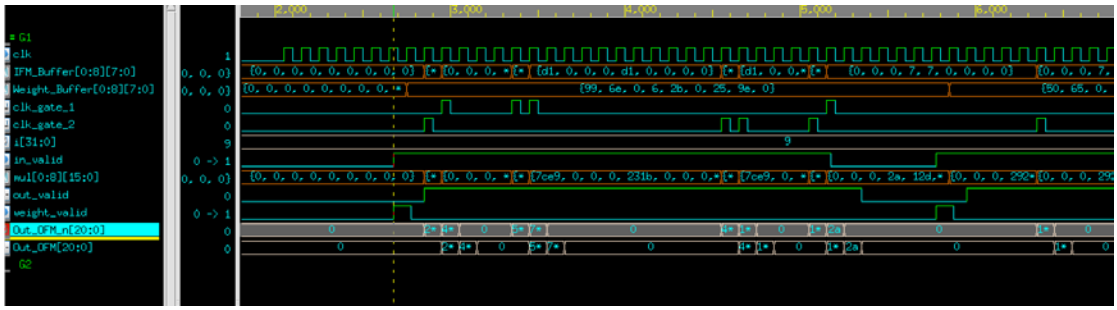
```
Startpoint: IFM_Buffer_reg_0__1_
            (rising edge-triggered flip-flop clocked by clk)
Endpoint: Out_OFM_reg_17_
          (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Point                                                       Incr       Path
-----------------------------------------------------------------------------
clock clk (rise edge)                                       0.00       0.00
clock network delay (ideal)                                 0.00       0.00
IFM_Buffer_reg_0__1_/CLK (ASYNC_DFFHx1_ASAP7_75t_R)         0.00       0.00 r
IFM_Buffer_reg_0__1_/QN (ASYNC_DFFHx1_ASAP7_75t_R)         48.54      48.54 r
U931/Y (BUFx3_ASAP7_75t_R)                                 21.73      70.27 r
mult_266/b[1] (Convolution_clock_gating_DW_mult_uns_7)
                                                            0.00      70.27 r
mult_266/U239/Y (NAND2xp5_ASAP7_75t_R)                     15.67      85.94 f
mult_266/U235/Y (XOR2x2_ASAP7_75t_R)                       36.20     122.15 r
mult_266/U251/Y (XOR2xp5_ASAP7_75t_R)                      27.10     149.24 r
mult_266/U249/Y (XOR2x2_ASAP7_75t_R)                       31.32     180.56 f
mult_266/product[2] (Convolution_clock_gating_DW_mult_uns_7)
                                                            0.00     180.56 f
r452/A[2] (Convolution_clock_gating_DW01_add_4)             0.00     180.56 f
r452/U1_2/SN (FAx1_ASAP7_75t_R)                            35.04     215.60 r
r452/U25/Y (INVx1_ASAP7_75t_R)                             23.56     239.16 f
r452/SUM[2] (Convolution_clock_gating_DW01_add_4)           0.00     239.16 f
add_3_root_add_0_root_add_275_8/B[2] (Convolution_clock_gating_DW01_add_10)
                                                            0.00     239.16 f
add_3_root_add_0_root_add_275_8/U1_2/CON (FAx1_ASAP7_75t_R)
                                                           24.26     263.42 r
add_3_root_add_0_root_add_275_8/U18/Y (INVx1_ASAP7_75t_R)
                                                           16.47     279.89 f
add_3_root_add_0_root_add_275_8/U1_3/CON (FAx1_ASAP7_75t_R)
                                                           20.61     300.50 r
add_3_root_add_0_root_add_275_8/U17/Y (INVx1_ASAP7_75t_R)
                                                           16.17     316.67 f
add_3_root_add_0_root_add_275_8/U1_4/CON (FAx1_ASAP7_75t_R)
                                                           20.53     337.21 r
add_3_root_add_0_root_add_275_8/U16/Y (INVx1_ASAP7_75t_R)
                                                           16.17     353.38 f
add_3_root_add_0_root_add_275_8/U1_5/CON (FAx1_ASAP7_75t_R)
                                                           20.53     373.91 r
add_3_root_add_0_root_add_275_8/U15/Y (INVx1_ASAP7_75t_R)
                                                           16.17     390.08 f
```

```
add_3_root_add_0_root_add_275_8/U1_6/CON (FAx1_ASAP7_75t_R)
                                                 20.53     410.61 r
add_3_root_add_0_root_add_275_8/U14/Y (INVx1_ASAP7_75t_R)
                                                 16.17     426.78 f
add_3_root_add_0_root_add_275_8/U1_7/CON (FAx1_ASAP7_75t_R)
                                                 20.53     447.31 r
add_3_root_add_0_root_add_275_8/U13/Y (INVx1_ASAP7_75t_R)
                                                 16.16     463.47 f
add_3_root_add_0_root_add_275_8/U1_8/CON (FAx1_ASAP7_75t_R)
                                                 20.53     484.00 r
add_3_root_add_0_root_add_275_8/U12/Y (INVx1_ASAP7_75t_R)
                                                 16.17     500.17 f
add_3_root_add_0_root_add_275_8/U1_9/CON (FAx1_ASAP7_75t_R)
                                                 20.53     520.70 r
add_3_root_add_0_root_add_275_8/U11/Y (INVx1_ASAP7_75t_R)
                                                 16.17     536.87 f
add_3_root_add_0_root_add_275_8/U1_10/CON (FAx1_ASAP7_75t_R)
                                                 20.53     557.40 r
add_3_root_add_0_root_add_275_8/U10/Y (INVx1_ASAP7_75t_R)
                                                 16.17     573.57 f
add_3_root_add_0_root_add_275_8/U1_11/CON (FAx1_ASAP7_75t_R)
                                                 20.53     594.10 r
add_3_root_add_0_root_add_275_8/U9/Y (INVx1_ASAP7_75t_R)
                                                 16.17     610.27 f
add_3_root_add_0_root_add_275_8/U1_12/CON (FAx1_ASAP7_75t_R)
                                                 20.53     630.80 r
add_3_root_add_0_root_add_275_8/U8/Y (INVx1_ASAP7_75t_R)
                                                 15.70     646.50 f
add_3_root_add_0_root_add_275_8/U1_13/CON (FAx1_ASAP7_75t_R)
                                                 20.41     666.91 r
add_3_root_add_0_root_add_275_8/U7/Y (INVx1_ASAP7_75t_R)
                                                 16.16     683.07 f
add_3_root_add_0_root_add_275_8/U1_14/CON (FAx1_ASAP7_75t_R)
                                                 20.53     703.60 r
add_3_root_add_0_root_add_275_8/U6/Y (INVx1_ASAP7_75t_R)
                                                 16.17     719.77 f
add_3_root_add_0_root_add_275_8/U1_15/SN (FAx1_ASAP7_75t_R)
                                                 37.73     757.50 f
add_3_root_add_0_root_add_275_8/U29/Y (INVx1_ASAP7_75t_R)
                                                 21.01     778.52 r
add_3_root_add_0_root_add_275_8/SUM[15] (Convolution_clock_gating_DW01_add_10)
                                                  0.00     778.52 r
add_1_root_add_0_root_add_275_8/B[15] (Convolution_clock_gating_DW01_add_9)
                                                  0.00     778.52 r
add_1_root_add_0_root_add_275_8/U1_15/SN (FAx1_ASAP7_75t_R)
```

```
add_1_root_add_0_root_add_275_8/U1_15/SN (FAx1_ASAP7_75t_R)
                                                 36.25     814.76 r
add_1_root_add_0_root_add_275_8/U32/Y (INVx1_ASAP7_75t_R)
                                                 17.80     832.56 f
add_1_root_add_0_root_add_275_8/SUM[15] (Convolution_clock_gating_DW01_add_9
                                                  0.00     832.56 f
add_0_root_add_0_root_add_275_8/B[15] (Convolution_clock_gating_DW01_add_7)
                                                  0.00     832.56 f
add_0_root_add_0_root_add_275_8/U1_15/CON (FAx1_ASAP7_75t_R)
                                                 22.88     855.44 r
add_0_root_add_0_root_add_275_8/U8/Y (INVx1_ASAP7_75t_R)
                                                 15.27     870.71 f
add_0_root_add_0_root_add_275_8/U1_16/CON (FAx1_ASAP7_75t_R)
                                                 20.30     891.01 r
add_0_root_add_0_root_add_275_8/U7/Y (INVx1_ASAP7_75t_R)
                                                 15.27     906.28 f
add_0_root_add_0_root_add_275_8/U1_17/SN (FAx1_ASAP7_75t_R)
                                                 32.19     938.47 r
add_0_root_add_0_root_add_275_8/U4/Y (INVxp67_ASAP7_75t_R)
                                                 10.92     949.39 f
add_0_root_add_0_root_add_275_8/SUM[17] (Convolution_clock_gating_DW01_add_7
                                                  0.00     949.39 f
U730/Y (NAND2xp5_ASAP7_75t_R)                    10.73     960.12 r
U1088/Y (AND3x1_ASAP7_75t_R)                     22.63     982.75 r
Out_OFM_reg_17_/D (ASYNC_DFFHx1_ASAP7_75t_R)      0.00     982.75 r
data arrival time                                          982.75

clock clk (rise edge)                          1000.00    1000.00
clock network delay (ideal)                       0.00    1000.00
Out_OFM_reg_17_/CLK (ASYNC_DFFHx1_ASAP7_75t_R)    0.00    1000.00 r
library setup time                              -16.88     983.12
data required time                                         983.12
-------------------------------------------------------------------------
data required time                                         983.12
data arrival time                                         -982.75
-------------------------------------------------------------------------
slack (MET)                                                  0.37
```

```
Combinational area:                4419.956143
Buf/Inv area:                       483.822726
Noncombinational area:             1030.164473
Macro/Black Box area:                 0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                   5450.120615
```

nWave 波型:



後模擬:

```
  Attributes
  ----------
      i  -  Including register clock pin internal power
      u  -  User defined power group

                     Internal  Switching  Leakage    Total
Power Group          Power     Power      Power      Power   (     %)  Attrs
--------------------------------------------------------------------------------
clock_network          1.241e-06 4.120e-06 8.190e-10 5.361e-06 ( 3.70%)
register               5.739e-05 2.927e-05 5.114e-08 8.672e-05 (59.89%)  i
combinational          2.026e-05 3.221e-05 2.424e-07 5.272e-05 (36.41%)
sequential                0.0000    0.0000    0.0000    0.0000 ( 0.00%)
memory                    0.0000    0.0000    0.0000    0.0000 ( 0.00%)
io_pad                    0.0000    0.0000    0.0000    0.0000 ( 0.00%)
black_box                 0.0000    0.0000    0.0000    0.0000 ( 0.00%)

  Net Switching Power  = 6.561e-05   (45.31%)
  Cell Internal Power  = 7.890e-05   (54.49%)
  Cell Leakage Power   = 2.943e-07   ( 0.20%)
    Intrinsic Leakage  = 2.943e-07
    Gate Leakage       =    0.0000
                         ---------
Total Power            = 1.448e-04  (100.00%)

X Transition Power     = 2.237e-06
Glitching Power        = 7.249e-07

Peak Power             = 9.052e-04
Peak Time              =      1169
```

Power reduction: 144.8 uW (<150uW)

Compare:

	Area(um^2)	Power(uW)	Critical path
Without clock gating	4989.63	273.5	From Weight_reg[8][1] to Out_OFM_reg[18]
With clock gating	5450.12	144.8	From IFM_Buffer_reg[0][1] to Out_OFM_reg[17]

(以上數據皆在 clock period = 1ns 下)

Critical path 截圖:

Without clock gate:

```
Startpoint: Weight_reg_8__1_
            (rising edge-triggered flip-flop clocked by clk)
Endpoint: Out_OFM_reg_18_
          (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max
```

With clock gate:

```
Startpoint: IFM_Buffer_reg_0__1_
            (rising edge-triggered flip-flop clocked by clk)
Endpoint: Out_OFM_reg_17_
          (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max
```

Analyze:

從表中可以得知 without clock gating 的 area 會比加了 clock gating 的 area 來的小，因為 with clock gating 為了降 power 而多加了 flip-flop 和 clock gate 會增加合成的時候的面積，也因此 with clock gating 的 power 會比 without clock gating 的小；再來是 critical path，因為加了 Flip-flop 的關係，with clock gating 中間經過的路徑會變長，而 slack time 了話，with clock gating 的 slack time 剩餘量會更多，使 IFM 或是 Weight=0 的時候，可以不用進到 combinational circuit 裡面做 convolution。然後從兩者的 critical path 來看，會發現整個路徑上，with clock gating 經過的 node 會比較多，所以從 timing report 上會看起來會比較多。