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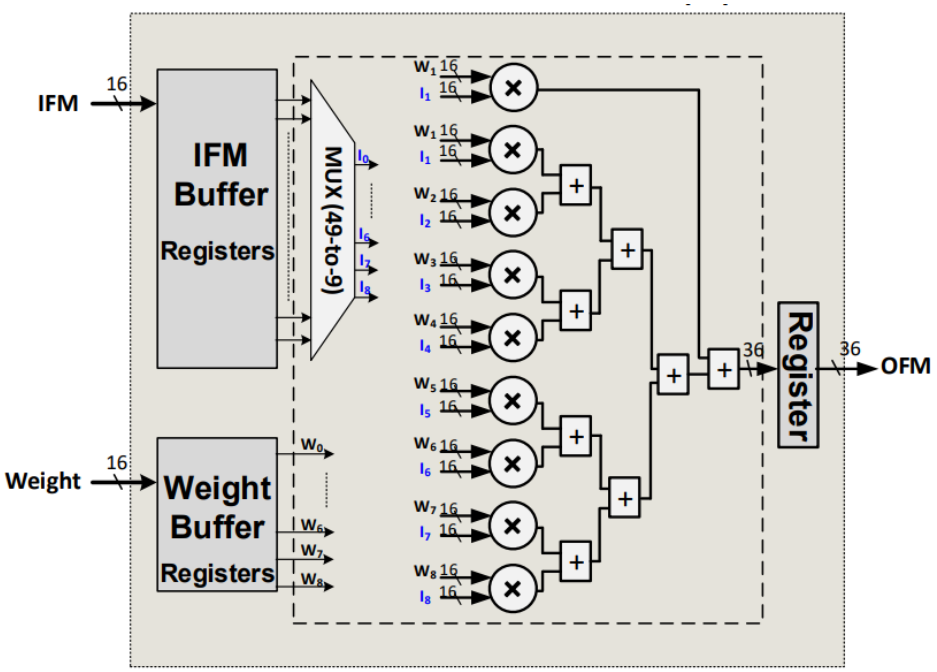
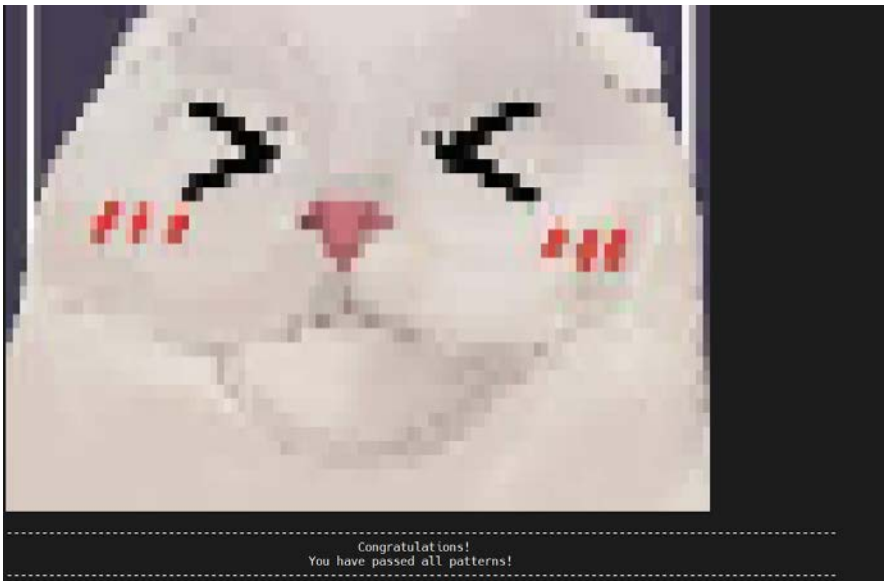
1. without pipeline 的版本:

首先，設計出 convolution 的 Block Diagram 如下圖，接著藉由助教給的 2×2 Example Code 改成 3×3 的版本，基本上只需要將 register 從 4 個改成 9 個便可以完成 without pipeline 的版本。



前模擬:



接著，通過 RTL 驗證後，使用 syn.tcl 合成電路，CLK:1000ps(slack time 為負)，所以把 CLK_period 調大，繼續往上找，最後得到結果如下圖，再從 Report 檔裡

面找 到面積如下下圖。

Clk_period: 1500ps

```
                                                    0.00    1466.33 f
U30035/Y (NAND2xp5_ASAP7_75t_R)                    11.37    1477.69 r
Out_OFM_reg_33_/D (ASYNC_DFFHx1_ASAP7_75t_R)        0.00    1477.69 r
data arrival time                                           1477.69

clock clk (rise edge)                            1500.00    1500.00
clock network delay (ideal)                         0.00    1500.00
Out_OFM_reg_33_/CLK (ASYNC_DFFHx1_ASAP7_75t_R)      0.00    1500.00 r
library setup time                                -22.04    1477.96
data required time                                          1477.96
-------------------------------------------------------------------
data required time                                          1477.96
data arrival time                                          -1477.69
-------------------------------------------------------------------
slack (MET)                                                    0.26
```

```
Combinational area:              32796.368686
Buf/Inv area:                     1996.410262
Noncombinational area:            6229.042520
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                 39025.411206
Total area:                 undefined
```

In_valid positive: 129750 ps

Out_valid negative: 243000ps

Clk_period: 1800ps:

```
clock clk (rise edge)                            1800.00    1800.00
clock network delay (ideal)                         0.00    1800.00
Out_OFM_reg_34_/CLK (ASYNC_DFFHx1_ASAP7_75t_R)      0.00    1800.00 r
library setup time                                -18.98    1781.02
data required time                                          1781.02
-------------------------------------------------------------------
data required time                                          1781.02
data arrival time                                          -1780.84
-------------------------------------------------------------------
slack (MET)                                                    0.18
```

```
14
15    Number of ports:                       1539
16    Number of nets:                       27503
17    Number of cells:                      24815
18    Number of combinational cells:        23770
19    Number of sequential cells:            1027
20    Number of macros/black boxes:             0
21    Number of buf/inv:                     2215
22    Number of references:                    62
23
24    Combinational area:             29131.773130
25    Buf/Inv area:                    1740.035533
26    Noncombinational area:           6229.042520
27    Macro/Black Box area:               0.000000
28    Net Interconnect area:      undefined  (No wire load specified)
29
30    Total cell area:                35360.815650
31    Total area:                undefined
32    1
```

In_valid positive: 155700 ps

Out_valid negative: 291600ps

Clk_period: 2000ps:

```
data required time                                                  1981.01
--------------------------------------------------------------------------
data required time                                                  1981.01
data arrival time                                                  -1980.48
--------------------------------------------------------------------------
slack (MET)                                                           0.53
```

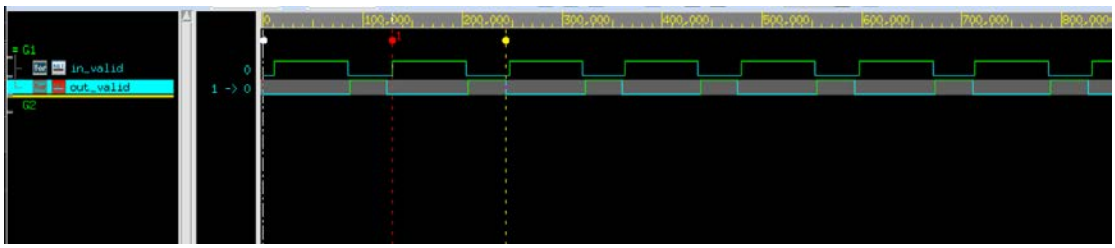
```
23
24    Combinational area:              28706.736968
25    Buf/Inv area:                     1471.996818
26    Noncombinational area:            6229.042520
27    Macro/Black Box area:                0.000000
28    Net Interconnect area:      undefined  (No wire load specified)
29
30    Total cell area:                 34935.779487
31    Total area:                 undefined
```

In_valid positive: 173000ps

Out_valid negative: 324000ps

後模擬:

之後開啟 nWave 查看 operating time(即 out_valid 拉下去減去 in_valid 拉起來)如下圖，從圖中可以得知 operating time=114000 ps，而我們可以從 Block Diagram 中得知從輸入到輸出完第一個的 OFM 總共會經過 (簡化) 2*9 *25 個乘跟加，因此 2*9 *25 /所花時間即為 Throughput，則可算出 Throughput 為 450/114000ps (op/s)，最後 OPS = Throughput/Area。



完成 gate_level 後，再回到合成的步驟更改 syn.tcl 檔案中的 clock_period，並再度合成，比較 面積與時間的結果。我使用的 clock_period 為 1500、1800、2000ps，最後結果如下表。

Clock_period (ps)	Area(um^2)	Operating_time(ps)	Throughput (OPS)	Area efficiency (GOPS/mm^2)
1500	39025.411	113250	3.97*10^9	101.8
1800	35360.82	135900	3.31*10^9	93.64
2000	34935.779	140600	3.20*10^9	91.61

從表中可以得知，隨著限制的 Clock_period 越大，area 就可以做得越小，但也相對的 operating time 上升，導致 Throughput 下降，值得注意的是，Clock_period 而在 1400 時，slack_time 就是負值了，可得知該設計的最小時間限制應為 1400ps 左右。

2. with_pipeline 的版本:

這我在每個乘法器後面皆街上 register 去切 pipeline，在每個乘法器後面皆存一個 register，並在加法器的部份，多切了一極，去使得頻率超過 1.25GHz。

Clk_period: 1000ps:

```
clock clk (rise edge)                                  1000.00    1000.00
clock network delay (ideal)                               0.00    1000.00
Multiple_reg_0__31_/CLK (ASYNC_DFFHx1_ASAP7_75t_R)        0.00    1000.00 r
library setup time                                      -16.38     983.62
data required time                                                 983.62
-------------------------------------------------------------------------
data required time                                                 983.62
data arrival time                                                 -983.51
-------------------------------------------------------------------------
slack (MET)                                                          0.11
```

```
Combinational area:              34513.076252
Buf/Inv area:                     2804.025633
Noncombinational area:            8782.525383
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                 43295.601635
Total area:                 undefined
```

In_valid positive: 88500ps

Out_valid negative: 165000ps

Clk_period: 800ps:

```
clock clk (rise edge)                                  800.00     800.00
clock network delay (ideal)                              0.00     800.00
Multiple_reg_4__25_/CLK (ASYNC_DFFHx1_ASAP7_75t_R)       0.00     800.00 r
library setup time                                     -17.93     782.07
data required time                                                782.07
-------------------------------------------------------------------------
data required time                                                782.07
data arrival time                                                -782.04
-------------------------------------------------------------------------
slack (MET)                                                         0.03
```

```
24   Combinational area:              35205.451290
25   Buf/Inv area:                     2722.144352
26   Noncombinational area:            8782.525383
27   Macro/Black Box area:                0.000000
28   Net Interconnect area:      undefined  (No wire load specified)
29
30   Total cell area:                 43987.976673
31   Total area:                 undefined
```

In_valid positive: 70800ps

Out_valid negative: 132000ps

Clk_period: 750ps (frequency is faster than 1.25GHz)

```
clock clk (rise edge)                                  750.00     750.00
clock network delay (ideal)                              0.00     750.00
Multiple_reg_1__29_/CLK (ASYNC_DFFHx1_ASAP7_75t_R)       0.00     750.00 r
library setup time                                     -17.94     732.06
data required time                                                732.06
-------------------------------------------------------------------------
data required time                                                732.06
data arrival time                                                -732.04
-------------------------------------------------------------------------
slack (MET)                                                         0.02
```

```
4    Combinational area:              36251.012284
5    Buf/Inv area:                     2941.660830
6    Noncombinational area:            8782.525383
7    Macro/Black Box area:                0.000000
8    Net Interconnect area:      undefined  (No wire load specified)
9
0    Total cell area:                 45033.537666
1    Total area:                 undefined
```

In_valid positive: 66375ps

Out_valid negative: 123750ps

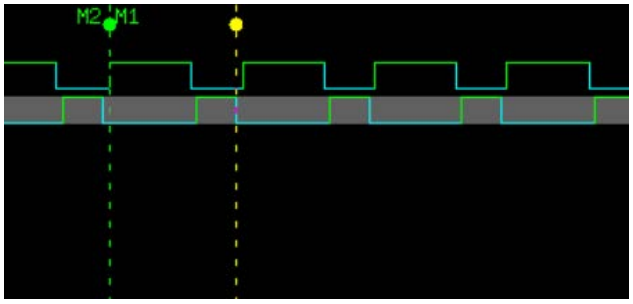
完成 gate_level 後，再次回到合成的步驟更改 syn.tcl 檔案中的 clock_period，並再度合成，比較面積與時間的結果。這裡我使用的 clock_period 為 750、800、1000，結果如下表。

Clock_period (ps)	Area(um^2)	Operating_time(ps)	Throughput (OPS)	Area efficiency (GOPS/mm^2)
750	45033.54	57375	7.84*10^9	174.16
800	43987.98	61200	7.35*10^9	167.16
1000	43295.60	76500	5.88*10^9	135.86

小結論:

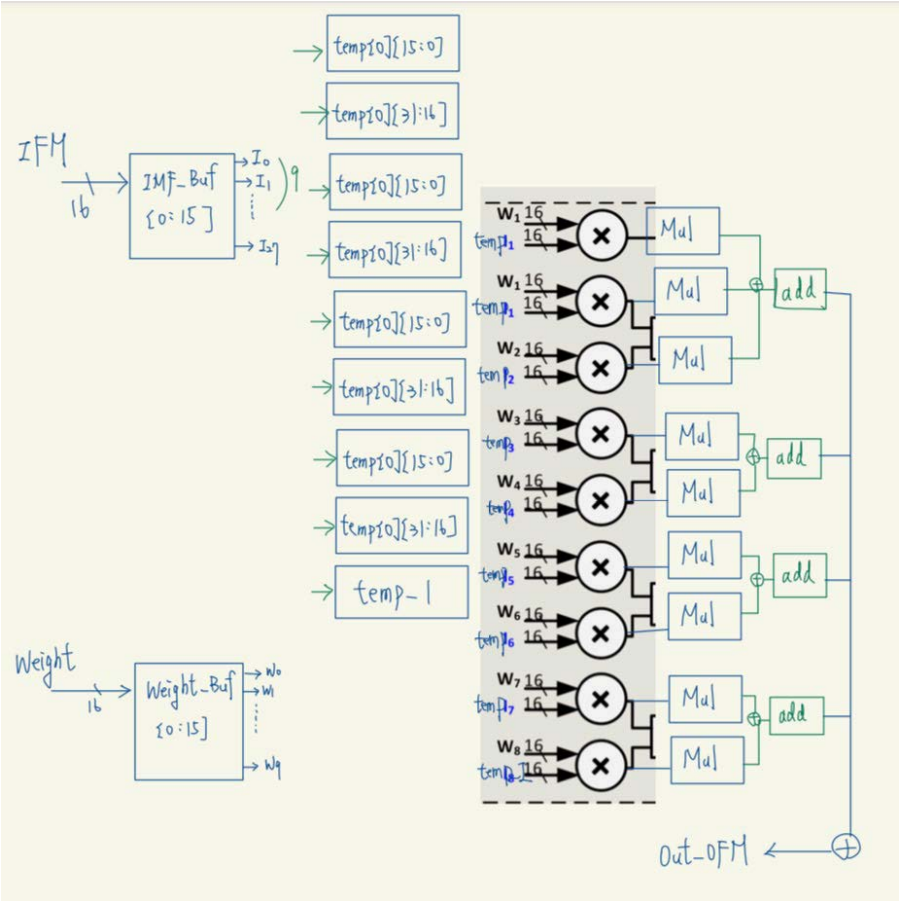
比較兩者結果顯示，在 without pipeline 和 with pipeline 的版本，皆隨著限制的時間縮短，相對應的 area 就會越高、Throughput 則上升。另一方面，觀察是否有 pipeline 的兩者，從電路結構上理解就是多一層 reg 所以面積直觀上會變大，而 clk_period 被統一擋了一次，使過程中訊號對齊一次，所以輸出時，clk_period 可以壓得比較小。從比較也了解到加 pipeline 雖然會花費較多的空間，但是可以讓 Clock period 更低，是個很好拿空間換時間的工具。

下圖為 in_valid postive 到 out_valid negative 的時間差，即為 operating time。



3. optimization

Plot the block diagram of the designed kernel:



Clk_period: 570ps:

```
clock clk (rise edge)                                   570.00     570.00
clock network delay (ideal)                               0.00     570.00
Multiple_reg_1__31_/CLK (DFFHQNx1_ASAP7_75t_R)            0.00     570.00 r
library setup time                                       -7.33     562.67
data required time                                                 562.67
-------------------------------------------------------------------------
data required time                                                 562.67
data arrival time                                                 -562.65
-------------------------------------------------------------------------
slack (MET)                                                         0.03
```

```
Combinational area:              32064.569420
Buf/Inv area:                     3868.015712
Noncombinational area:            6529.740359
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                 38594.309779
```

Operating time: 29925ps

Throughput = 1.50*10^10 (OPS)

Area efficiency: 389.6 (GOPS/mm^2)

Clk_period: 565ps:

```
clock clk (rise edge)                                   565.00     565.00
clock network delay (ideal)                               0.00     565.00
Multiple_reg_1__55_/CLK (DFFHQNx1_ASAP7_75t_R)            0.00     565.00 r
library setup time                                      -17.43     547.57
data required time                                                 547.57
-------------------------------------------------------------------------
data required time                                                 547.57
data arrival time                                                 -547.56
-------------------------------------------------------------------------
slack (MET)                                                          0.01
```

```
  Combinational area:              32331.908319
  Buf/Inv area:                     4048.107872
  Noncombinational area:            6537.905166
  Macro/Black Box area:                0.000000
  Net Interconnect area:      undefined  (No wire load specified)

  Total cell area:                 38869.813485
```

Operating time: 29715ps

Throughput = 1.51*10^10 (OPS)

Area efficiency: 389.6 (GOPS/mm^2)