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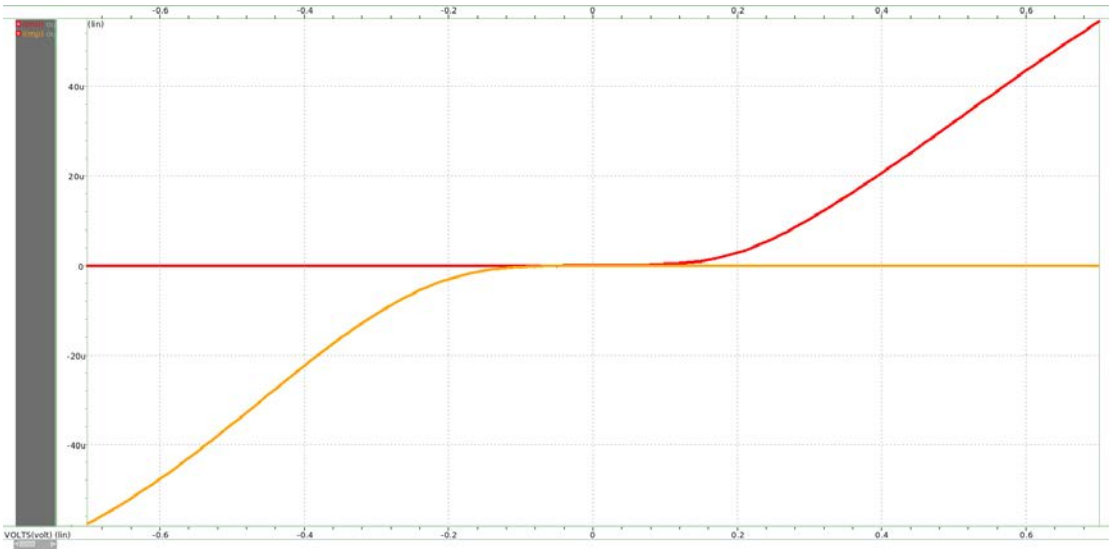
Exercise 1-1: DC characteristics (25%)

- Simulate DC characteristics of FinFETs and planer MOSs by minimal feature sizes
  - V_{gs}-I_{DS} of FinFET (N-FinFET & P-FinFET) in one figure
    - Number of Fin = 1
    - Vdd = 0.7v
  - V_{gs}-I_{DS} of CMOS (NMOS & P-MOS)in one figure
    - minimal width and Length = 16nm
    - Vdd = 0.7v

1_a:

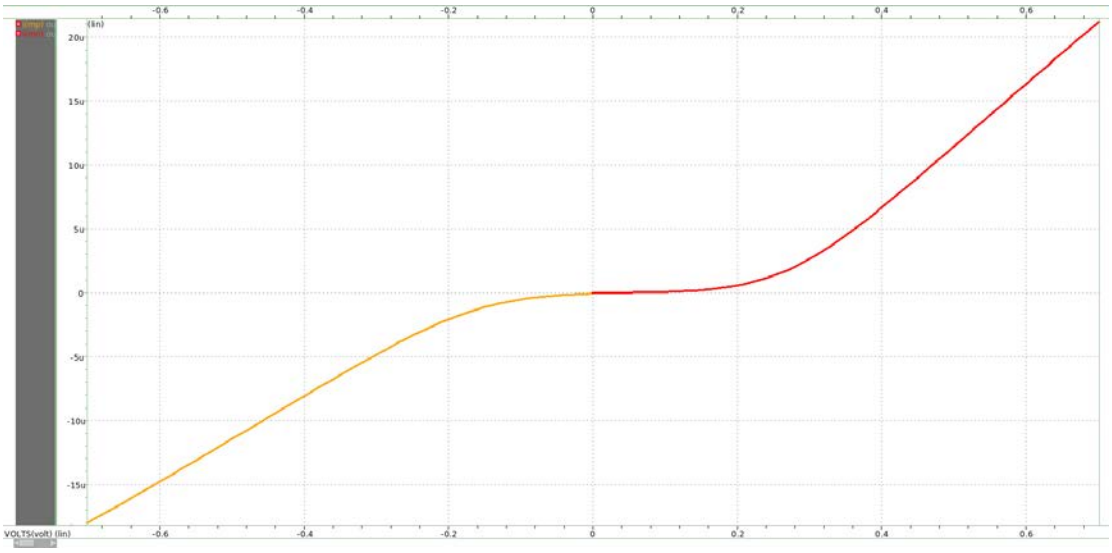
設計 FINFET(N-FinFET & P-FinFET)的 V_{GS}-I_{DS} 圖，FinFET 數量=1，VDD=0.7V。 下圖為將一 DC 電壓源(V_{GS})從 -0.7V 線性升至 0.7V，並觀察 V_{GS}-I_{DS} 圖，可以發現通過 P-FinFET(mp，橘線)的電流隨著 V_{GS} 上升而趨近於 0，反而是通過 N-FinFET(mn，紅線)的電流隨著 V_{GS} 上升而逐漸增加，而電流若從 Drain 端到 Source 端定為正，因此 P-FinFET 的電流為負。



FINFET(N-FinFET & P-FinFET)的 V_{GS}-I_{DS} 圖

1_b:

設計 MOSFET(NMOS & PMOS)的 V_{GS}-I_{DS} 圖，MOS 數量=1，VDD=0.7V。 此題與上題類似，只是將 P-FinFET 改為 PMOS，N-FinFET 改為 NMOS，把尺寸設為 16nm 以後便可以得到下方 V_{GS}-I_{DS} 圖。與上方相似，可以發現通過 PMOS(mp，橘線)的電流隨著 V_{GS} 上升而趨近於 0，反而是通過 NMOS(mn，紅線)的電流隨著 VGS 上升而逐漸增加，與上題比較可以發現，MOSFET 的電流會比 FinFET 來的小。



Planer MOSFET(NMOS & PMOS)的 V_{GS}-I_{DS} 圖

Exercise 1-2: Voltage Transfer Curve (25%)

- Select the smallest and largest inverters from ASAP 7nm standard cell library and simulate the voltage transfer characteristic (VTC).
  - Netlist of standard cells: asap7sc7p5t_INVBUF_RVT.sp
  - Plot VTC curves of these 2 inverters under different voltages (Vdd = 0.7V, 0.6V, 0.5V and 0.4V)

2_a:

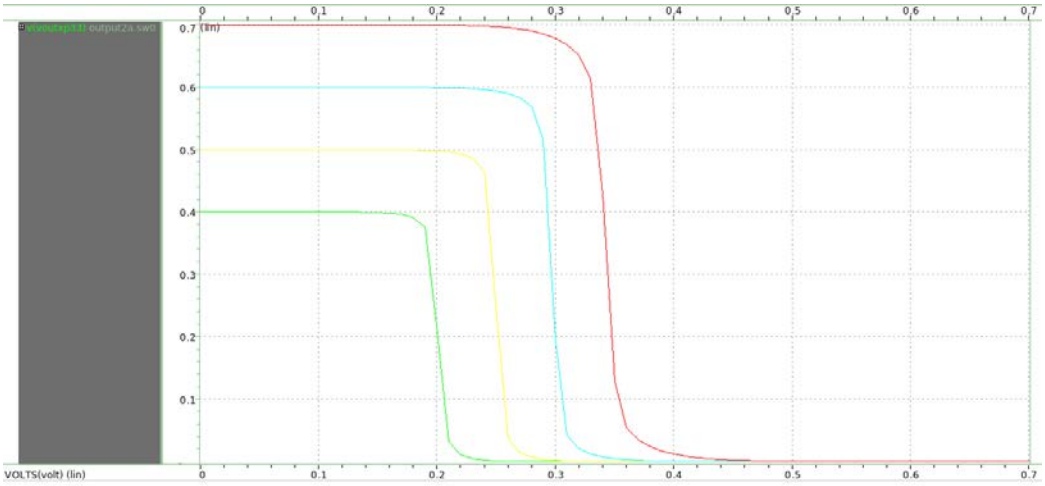
我們從助教提供的 library 中選出最大與與最小的 inverter 分別是 INVx13_ASAP7_75t_R 以及 INVxp33_ASAP7_75t_R，判斷依據是看 Width，因為發現他們 Length 皆相同，由結果可以得知，最小 size 的 inverter 與最大 size 的 inverter 的 VTC 曲線近乎相同，而若 VDD 的輸入較小，也會使 switching point 發生的電壓變小。

Voutxp33(smallest inverter):

nmos_rvt: L=2e-08m，W=2.7e-08m，nfin=1

pmos_rvt: L=2e-08m，W=2.7e-08m，nfin=1

```
.SUBCKT INVxp33_ASAP7_75t_R VSS VDD A Y
*
* VSS VSS
* VDD VDD
* A A
* Y Y
*
*

MM0 N_MM0_d N_MM0_g VSS VSS nmos_rvt L=2e-08 W=2.7e-08 nfin=1
MM1 N_MM1_d N_MM0_g VDD VDD pmos_rvt L=2e-08 W=2.7e-08 nfin=1
```



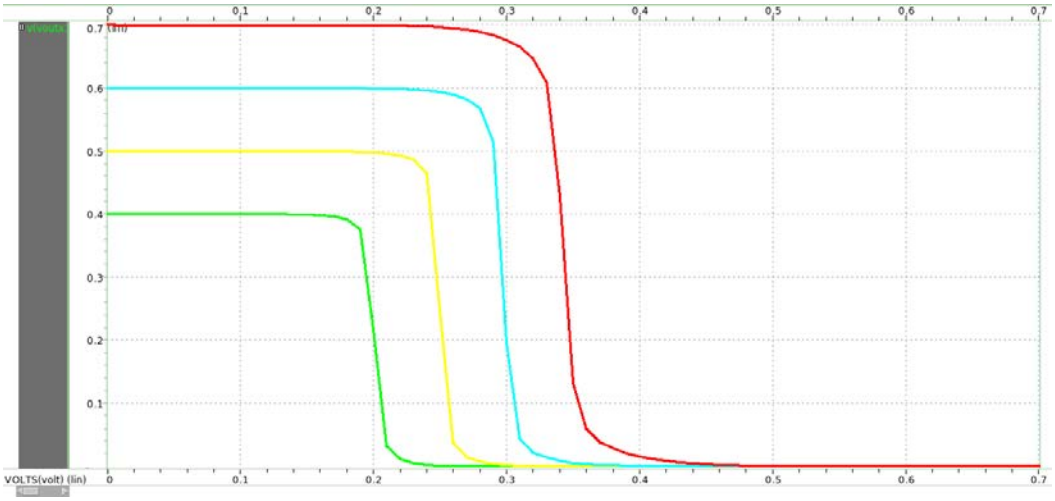
最小 size 的 inverter 之 VTC curve

voutX13(largest inverter):

nmos_rvt: L=2e-08m，W=8.1e-08m，nfin=3

pmos_rvt: L=2e-08m，W=8.1e-08m，nfin=3

```
.SUBCKT INVx13_ASAP7_75t_R VSS VDD A Y
*
* VSS VSS
* VDD VDD
* A A
* Y Y
*
*

MM0 N_MM0_d N_MM0_g VSS VSS nmos_rvt L=2e-08 W=8.1e-08 nfin=3
MM0@13 N_MM0@13_d N_MM1@13_g VSS VSS nmos_rvt L=2e-08 W=8.1e-08 nfin=3
```



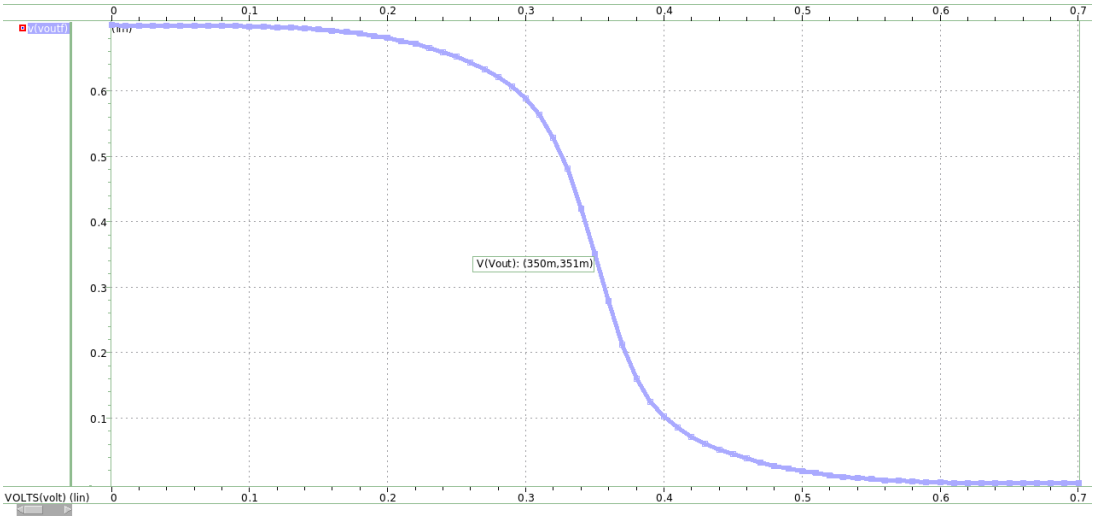
最大 size 的 inverter 之 VTC curve

- Design unit-sized inverters such that their logic threshold voltage is at $\frac{Vdd}{2}$ (vdd = 0.7v)
  - Plot the VTC curve
    - Using FinFETs (7nm_TT.pm)
    - Using Planer MOSs (16mos.pm)

2_b:

FinFET:

藉由調 NFin 數目: mp=6, mn=5，使得 threshold voltage 剛好等於 VDD/2=350mV



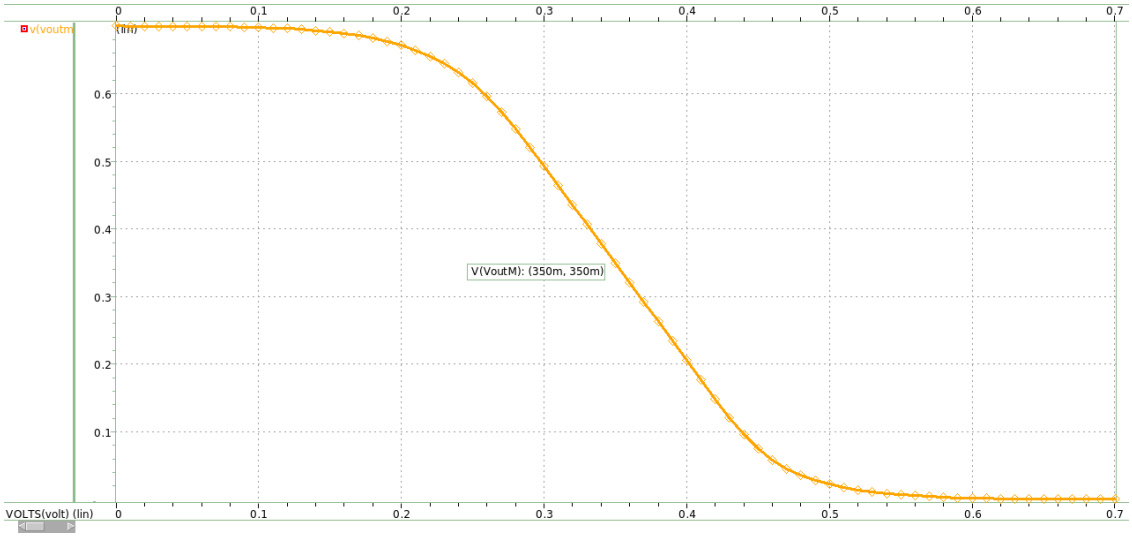
FinFET VTC curve

P-FinFET: W=7nm、L=7nm，nFin=6；N-FinFET: W=7nm、L=7nm，nFin=5

Logic threshold voltage = 0.351V

MOS:

藉由調 m 數目: mp=7, mn=5，使得 threshold voltage 剛好等於 VDD/2=350mV



Planer MOS VTC curve

PMOS: W=16nm、L=16nm，m=7；NMOS: W=16nm、L=16nm，m=5

Logic threshold voltage = 0.35V

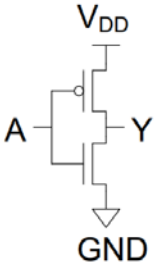
Inverter 的 VTC curve 發生轉折處會隨 K_n/K_p 的大小而改變，當 MOS/ FinFET 的 size 固定，透過調整 mos/Fin 的並聯數目 m，等同調整等效的 W，故可調整 V_{th}。當 pmos 的 m 增加，等效的 Wp 增加，Kp 增加。當 nmos 的 m 增加，等效的 Wn 增加，Kn 增加。

當 Kn>Kp，曲線會往左移動，logic threshold voltage 降低。

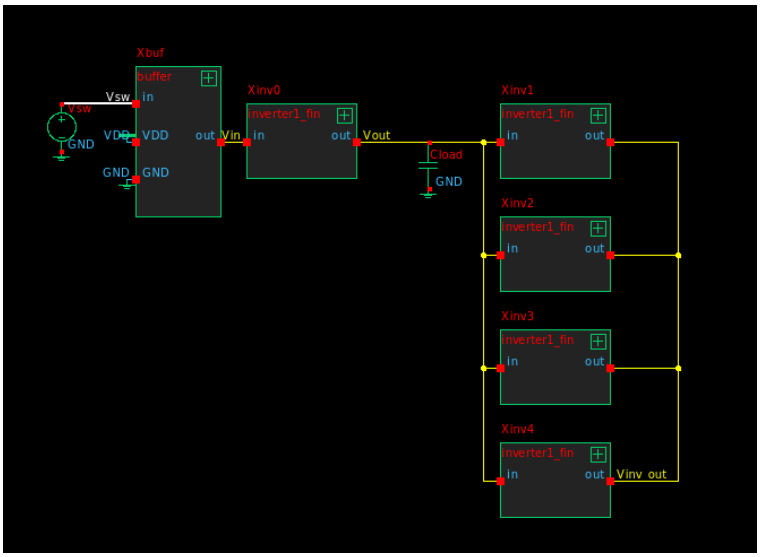
當 Kn<Kp，曲線會往右移動，logic threshold voltage 增加。

Exercise 1-3: Power consumption (25%)

- Measure the power consumption of the inverters, designed in 1-2.
  - Input buffer: Buffer.sp
  - Output loading: FO4 (4 inverters) + 10 fF as wire loading
  - Vdd = 0.7v
  - Input pattern need more than 20.
  - Input signal switching frequency
    - 1GHz
    - 2GHz
    - 4GHz



3_a:



模擬電路示意圖

INV_FinFET:

Input signal switching frequency = 1GHz:

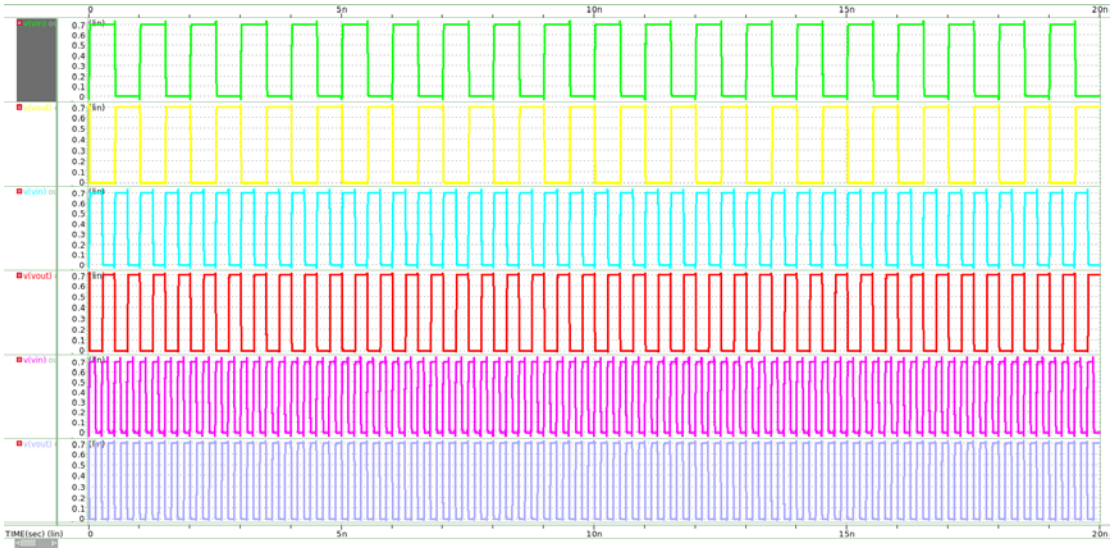
```
****** transient analysis tnom=  25.000 temp=  25.000 ******
static_pwr=   7.4902u  from=   0.            to=  20.0000n

        ***** job concluded
```

Input signal switching frequency = 2GHz:

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
static_pwr=  14.9819u  from=   0.            to=  20.0000n

        ***** job concluded
******
```

Input signal switching frequency = 4GHz:

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
static_pwr=  29.9249u  from=   0.            to=  20.0000n

        ***** job concluded
******
```



Y 軸依序為 Vin(1GHz)、Vout(1GHz)、Vin(2GHz)、Vout(2GHz)、Vin(4GHz)、Vout(4GHz)

3_b:

INV_MOS:

Input signal switching frequency = 1GHz:

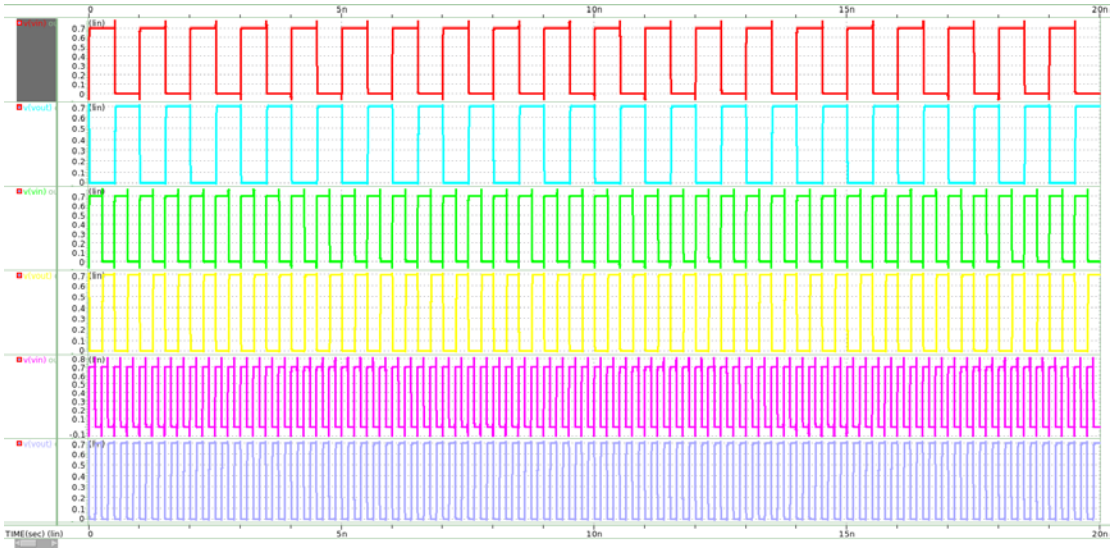
```
title hw3_b

****** transient analysis tnom=  25.000 temp=  25.000 ******
static_pwr=   9.9285u  from=   0.             to=  20.0000n

        ***** job concluded
******
```

Input signal switching frequency = 2GHz:

```
title hw3_b

****** transient analysis tnom=  25.000 temp=  25.000 ******
static_pwr=  18.7971u  from=   0.             to=  20.0000n

        ***** job concluded
```

Input signal switching frequency = 4GHz:

```
******
title hw3_b

****** transient analysis tnom=  25.000 temp=  25.000 ******
static_pwr=  34.2670u  from=   0.             to=  20.0000n
```



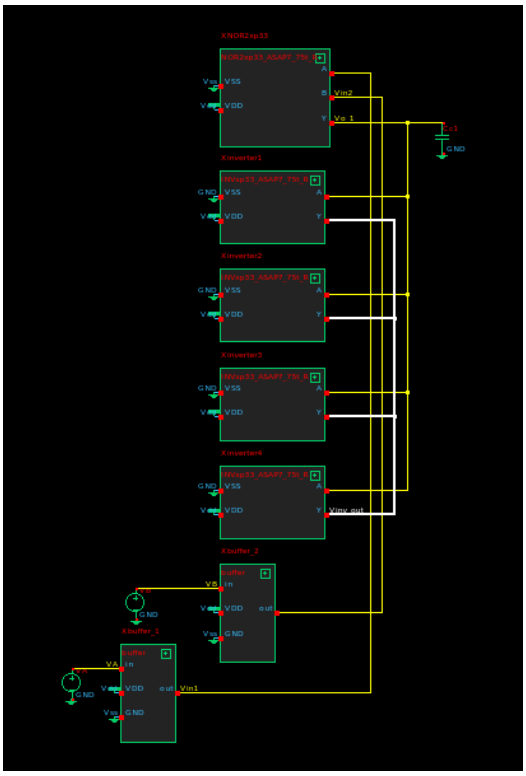
Y 軸依序為 Vin(1GHz)、Vout(1GHz)、Vin(2GHz)、Vout(2GHz)、Vin(4GHz)、Vout(4GHz)

當 input signal switching frequency 增加，測量相同時間的 power consumption，可發現隨著 input signal switching frequency 上升，因為經過更多個 cycles，因此 power consumption 變大。

Exercise 1-4: Characteristics of NOR2/NAND2 (25%)

- Select the smallest **NOR2** and **NAND2** from ASAP 7nm standard cell library
  - Input buffer: Buffer.sp
  - Output loading: FO4 (4 inverters) + 10 fF as wire loading
    - Inverter: smallest inverters in ASAP 7nm standard cell library
  - Netlist of standard cells:
    - asap7sc7p5t_INVBUF_RVT.sp
    - asap7sc7p5t_SIMPLE_RVT.sp
  - Vdd = 0.7v
  - Measure Tr, Tf, Tplh, Tphl

4_a:



模擬電路示意圖

NAND2:

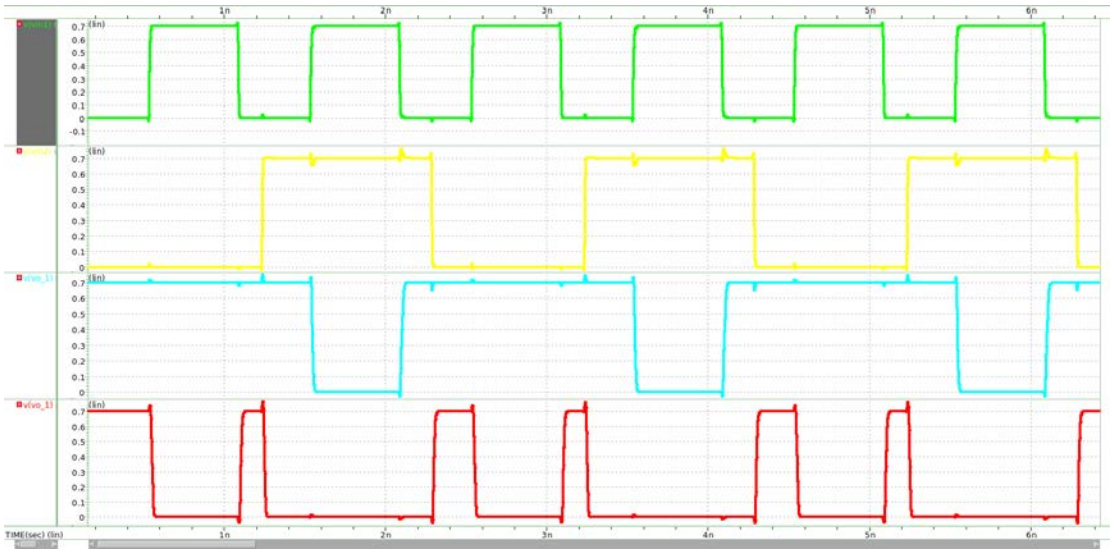
```
* hw1_4a

****** transient analysis tnom=  25.000 temp=  25.000 ******
tr= 227.6794p  targ=   2.3447n   trig=   2.1170n
tf= 191.1884p  targ=   1.7516n   trig=   1.5604n
tplh= 145.8436p  targ=   2.2208n   trig=   2.0750n
tphl= 108.1338p  targ=   1.6331n   trig=   1.5250n
propogation_delay= 126.9887p
```

Tr = 227.6494ps，Tf = 191.1884ps，Tplh = 145.8436ps，Tphl = 108.1338ps

NOR2:

```
hw1_4a

****** transient analysis tnom=  25.000 temp=  25.000 ******
tr= 283.4089p  targ=   2.8649n   trig=   2.5814n
tf= 226.7527p  targ=   1.2835n   trig=   1.0567n
tplh= 185.9399p  targ=   2.6859n   trig=   2.5000n
tphl= 144.7894p  targ=   1.1448n   trig=   1.0000n
propogation_delay= 165.3646p
```

Tr = 283.4089ps，Tf = 226.7527ps，Tplh = 185.9399ps，Tphl = 144.7894ps



Y 軸依序為 INA、INB、Vout1(NAND 的輸出)、Vout2(NOR 的輸出)

Propagation delay 為 Ron(turn-on resistance)和 C_L(parasitic capacitance on output node)的函數，delay 正比於 R_n*C_L，代表 R_n 越大或 C_L 越大，delay 會越大。