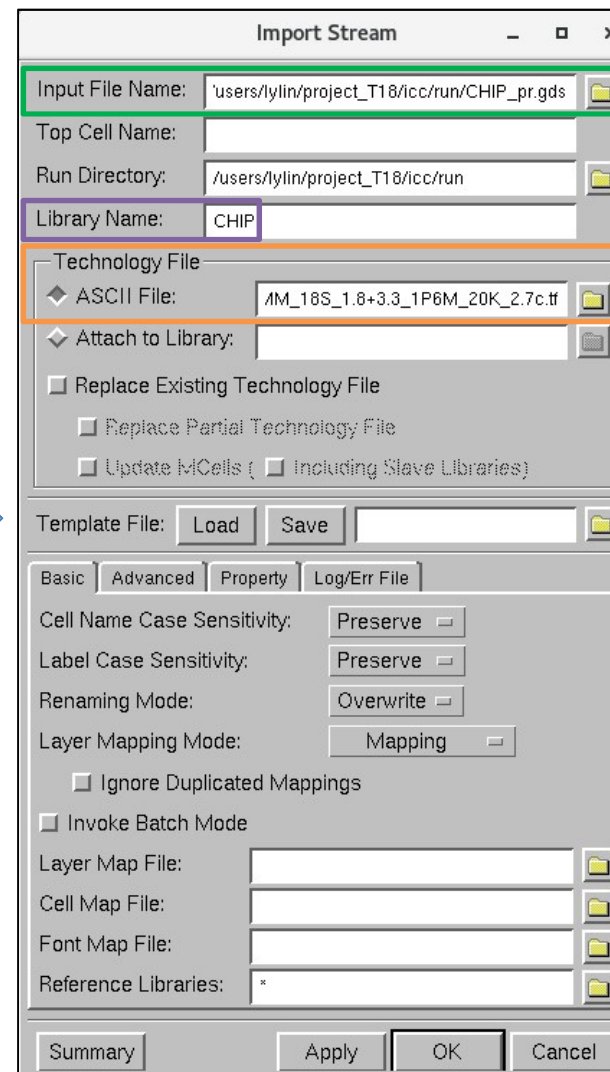
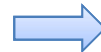
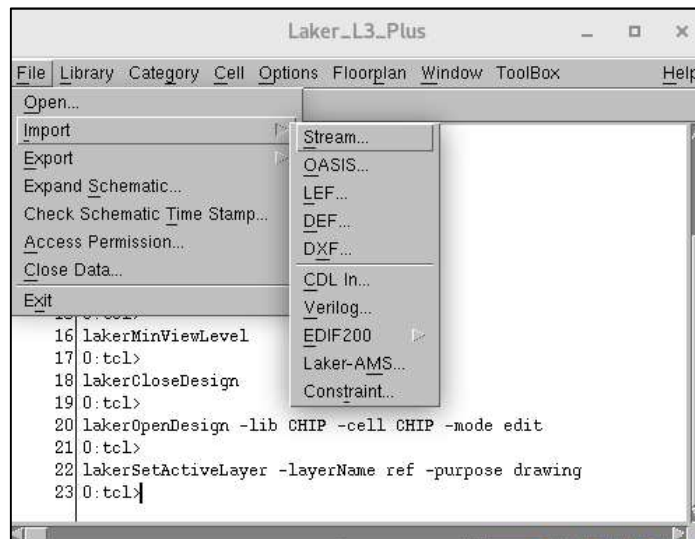


Merge Real GDS – DRC (1/6)

This step is additionally required only when using ICC. If you use ICC2 or INNOVUS, it is not necessary because real gds have already been merged when write GDS.

- Import chip GDS



← ICC steam out GDS

← Tech file @
/process/T18/TECH
/1_TSRI/PDK/Laker
/Laker_MM_18S_1.
8+3.3_1P6M_20K_
2.7c.tf

Merge Real GDS – DRC (2/6)

- Import core library real GDS

Core library real GDS @
/process/T18/IP/CBDK_TSMC018_Arm/CIC/GDS
/tsmc18.gds2

Tech file @
/process/T18/TECH/1_TSRI/PDK/Laker/Laker
_MM_18S_1.8+3.3_1P6M_20K_2.7c.tf

Merge Real GDS – DRC (3/6)

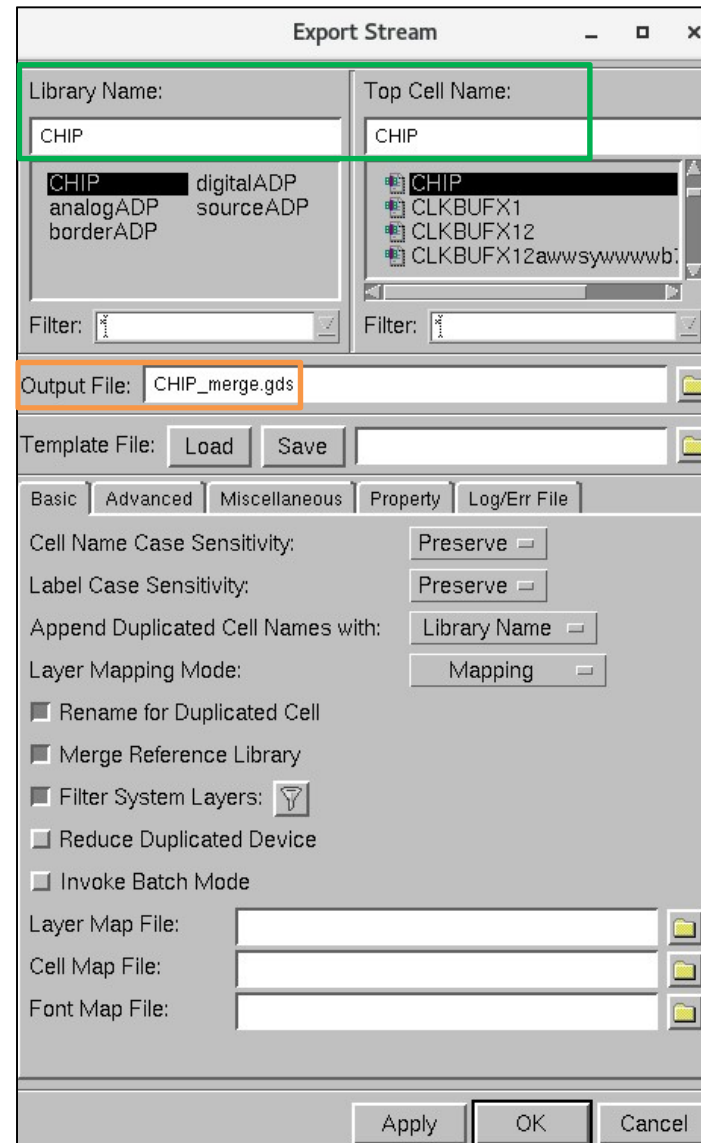
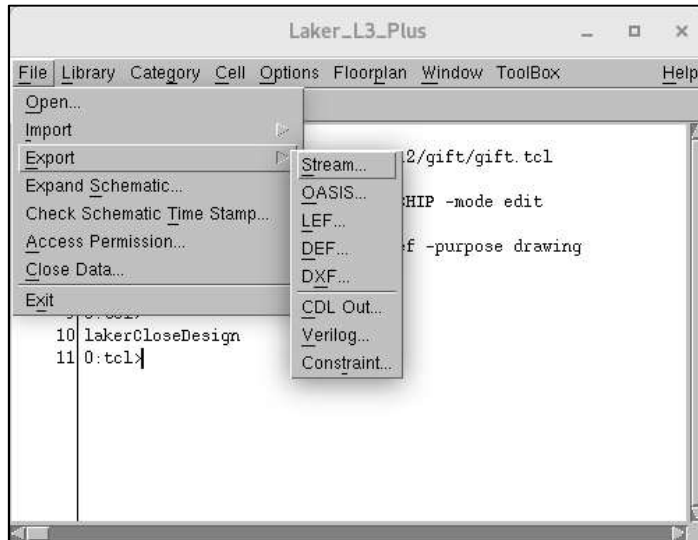
- Import IO library real GDS

IO library real GDS @
/process/T18/IP/CBDK_TSMC018_Arm/CIC/GDS
/tpz973gv_tpb973gv.gds

Tech file @
/process/T18/TECH/1_TSRI/PDK/Laker/Laker
_MM_18S_1.8+3.3_1P6M_20K_2.7c.tf

Merge Real GDS – DRC (4/6)

- Export real chip GDS

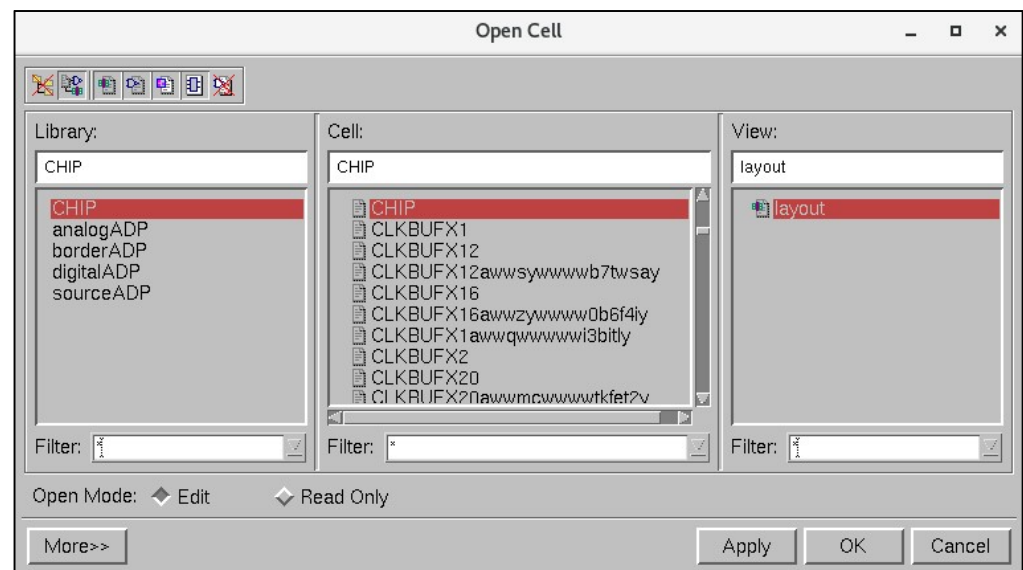
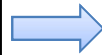
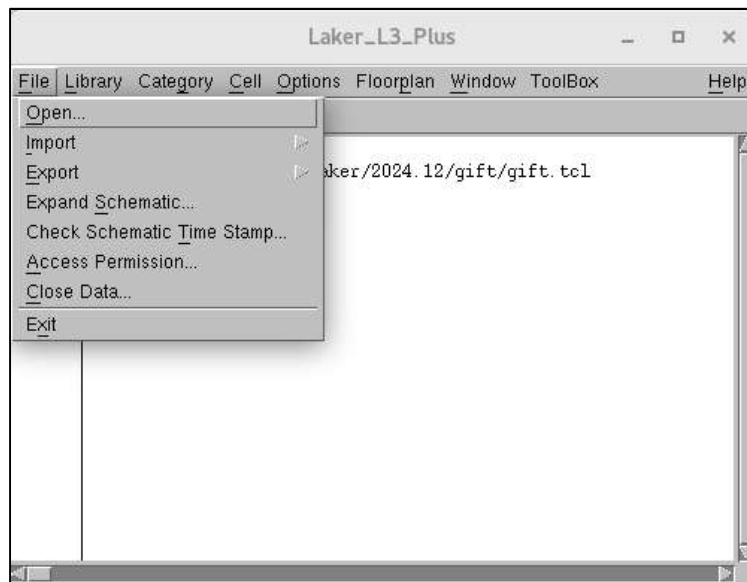


EDA Cloud 2.0

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Merge Real GDS – DRC (5/6)

- Open real chip GDS

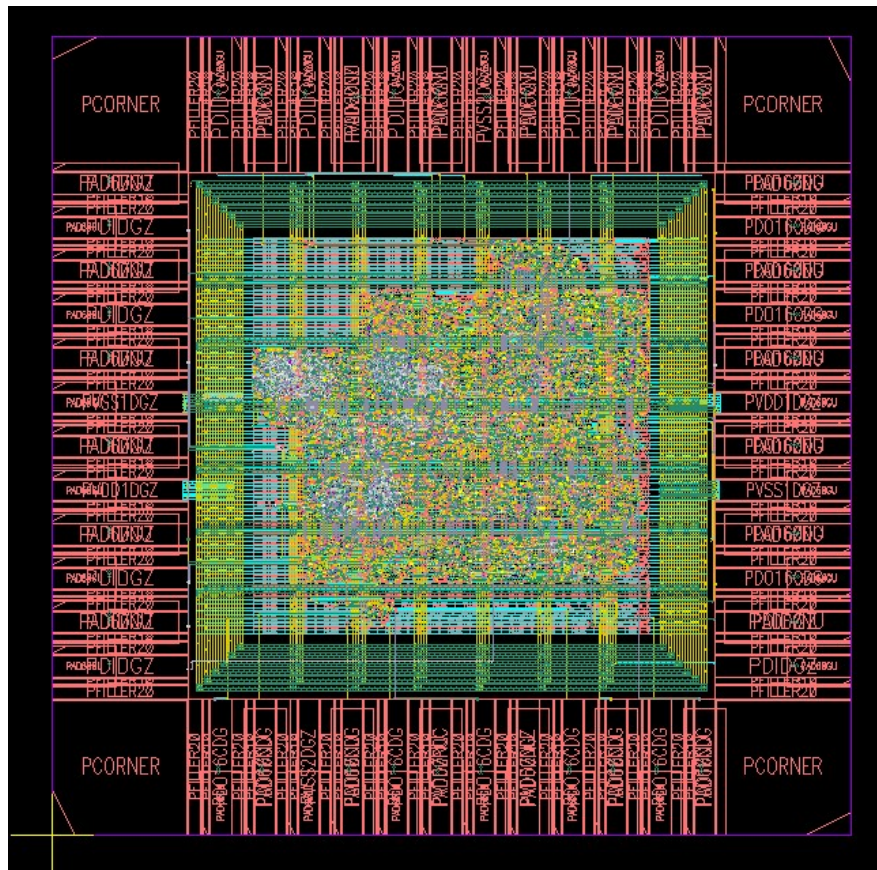


EDA Cloud 2.0

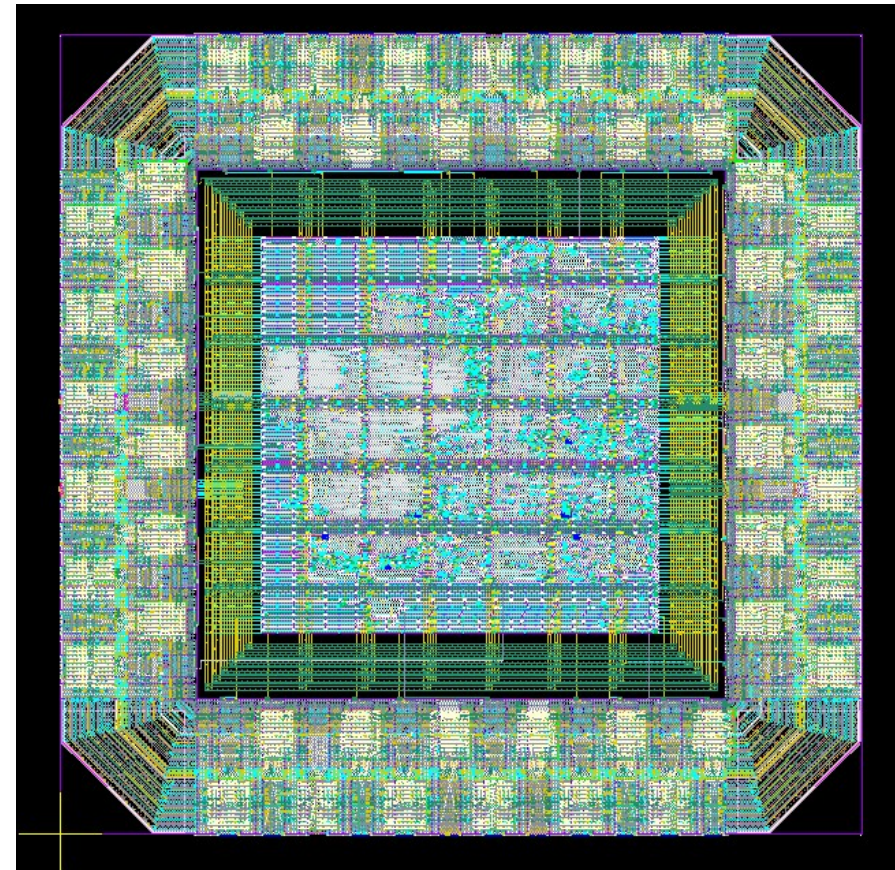
NARLabs

Merge Real GDS – DRC (6/6)

Hot Key : Shift + F



Hot Key : Ctrl + F



EDA Cloud 2.0 Add dummy

1. Copy DRC directory

```
cp -r /process/T18/IP/CBDK_TSMC018_Arm/CIC/Caliber/DRC .
```

2. Modify script: TOP_CELL, LAYOUT_PATH, ruledeck in the scripts:
[runBE.csh](#), [runFE.csh](#), [runmerge.csh](#)

```
set TOP_CELL = "CHIP"  
set LAYOUT_PATH = "../CHIP_merge.gds"
```

```
DRC/  
- rundrc  
- add dummy/  
  - runBE.csh  
  - runFE.csh  
  - runmerge.csh  
- scr/  
- drc/  
  - runDRC.csh  
  - scr/
```

3. Execution with following steps

```
cd add_dummy  
./runBE.csh  
./runFE.csh  
./runmerge.csh
```

4. Check that [BEOL.gds](#), [FEOL.gds](#) and [CHIP_mergedummy.gds.gz](#) are generated.

```
[lylin@edaeng02 add_dummy]$ ll  
total 22680  
-rwxr-xr-x 1 lylin DSD 14501388 Dec 30 14:50 BEOL.gds  
-rw-r--r-- 1 lylin DSD   32064 Dec 30 14:50 BEOL.sum  
-rw-r--r-- 1 lylin DSD  7586949 Dec 30 14:55 CHIP_mergedummy.gds.gz  
-rwxr-xr-x 1 lylin DSD   85430 Dec 30 14:54 FEOL.gds  
-rw-r--r-- 1 lylin DSD   35215 Dec 30 14:54 FEOL.sum
```


EDA Cloud 2.0 DRC

4. Modify script: TOP_CELL, ruledeck in the scripts: [runDRC.csh](#)

```
set TOP_CELL = "CHIP"  
set LAYOUT_PATH = "../add_dummy/${TOP_CELL}_mergedummy.gds.gz"
```

5. Execution with following steps

```
cd ../drc  
./runDRC.csh
```

```
DRC/  
- rundrc  
- add_dummy/  
  - runBE.csh  
  - runFE.csh  
  - runmerge.csh  
  - scr/  
- drc/  
  - runDRC.csh  
  - scr/
```

6. Check DRC results:

```
cd output  
calibre -rve DRC_RES.db &
```

Show Unresolved

The screenshot shows the Calibre RVE v2023.1_34.18 interface for DRC_RES.db. The 'Filter: Show Unresolved' dropdown is selected, and a red arrow points to it with the text 'Show Unresolved'. The main window displays a list of checks and their results, along with a grid of results for the selected check.

Check / Cell	Results
Check RES.4_PO	89
Check RES.8	4
Check VIA2.E.3	1000
Check VIA3.E.3	1000
Check VIA4.E.3	399
Check NO.IND.PO.R.3	1
Check DRM.R.1	1
Check NW.S.1.1	1
Check RES.2	163
Check OD.EX.1	30
Check ESD.28g	8
Check UTM20K.W.1	1
Check DOD.DN.1	1
Check DOD.DN.2	1
Check LUP.5.3g_3.3V	43

The grid shows results for the selected check (Check RES.4_PO) across 84 cells. The results are displayed in a grid of 8 rows and 7 columns.

1	2	3	4	5	6	7
8	9	10	11	12	13	14
15	16	17	18	19	20	21
22	23	24	25	26	27	28
29	30	31	32	33	34	35
36	37	38	39	40	41	42
43	44	45	46	47	48	49
50	51	52	53	54	55	56
57	58	59	60	61	62	63
64	65	66	67	68	69	70
71	72	73	74	75	76	77
78	79	80	81	82	83	84

The bottom status bar shows: RES.4_PO { @ Min. and Max. clearance from RP0 to a contact on the poly resistor and OD resistor = 0.22um. No DRC - ONLY THRESHOLD VIOLATIONS. Check RES.4_PO