ECE 351 – Verilog and FPGA Design

(Last Updated 24-Mar-2020)

Spring 2021 - 4 Credits

Tue, Thu, 2:00 PM – 3:50 PM

Location: Remote teaching via Zoom Meeting

Class Information

Class:	Tue/Thu 2:00 PM – 3:50 PM	CRN = 61016 (ECE 351 - 001)
Quarter:	Spring 2021	
Location:	Remote teaching via Zoom Meeting	
Holidays:	*NONE*	
Credits:	4	
Track(s):	Undergraduate Computer Engineering	
Prerequisites	ECE 172 or ECE 271 (Grade of C or better) or equivalent	Students should be competent in combinatorial and synchronous sequential design C/C++ programming experience is a plus

Contact Information

Instructor:	Roy Kravitz E-mail: roy.kravitz@pdx.edu Profile: https://www.pdx.edu/profile/roy-kravitz Cell phone: 503-913-1678 (please don't call after 9:00 PM)
T/A:	Tyler Hull E-mail : thull@pdx.edu
Grader:	Tiffani Shilts Hartman E-mail: tshilts2@pdx.edu
Open Office hours:	Roy : Mon 3 :00 PM – 4 :30 PM, Tue 10:30 AM – Noon (), Wed 7:00 PM – 7 :30 PM Links: Mon - Tue - Wed - Tyler: TBD WE WILL CONDUCT OFFICE HOURS FOR SPRING TERM VIA ZOOM UNLESS WE AGREE ON OTHER ARRANGEMENTS. MY (ROY'S) OFFICE HOURS ARE DROP-IN; JOIN THE ZOOM OFFICE HOUR MEETING. ZOOM WILL PLACE YOU IN THE WAITING ROOM. I WILL ADMIT YOU, BUT BE PATIENT; I MAY BE TALKING TO ANOTHER STUDENT WHEN YOU JOIN.
Course website:	https://d2l.pdx.edu

Course Description

Introduces the students to the SystemVerilog Hardware Description Language and describes its role in the electronic design automation environment. Students learn how to prototype digital designs using FPGAs. Prerequisite: ECE 172 or ECE 271 or equivalent (with a grade of C or better).

NOTE: The Verilog 2001 specification has been incorporated in the SystemVerilog specification. SystemVerilog retains backwards compatibility with the Verilog 2001 syntax but is a better design/simulation/verification tool.

Course Objective and Learning Outcomes

- Describe complex digital designs using the SystemVerilog Hardware Description Language
- Design testbenches needed to functional verify digital designs
- Apply design automation tools to synthesize designs in FPGAs
- Describe syntax and constructs that promote efficient synthesized designs
- Describe good coding practices for efficient FPGA synthesis
- Describe how embedded systems are implemented in FPGAs

Required Text

- *RTL Modeling with SystemVerilog for Simulation and Synthesis* by Stuart Sutherland. Publisher: CreateSpace, An Amazon Company; ISBN-13: 978-1546776345 (Available from the PSU Bookstore, Amazon.com and other retail outlets)

Optional Texts (Referenced but no reading or assignments)

- *Logic Design and Verification Using SystemVerilog (Revised)* by Donald Thomas. Publisher: CreateSpace, An Amazon.com Company; ISBN-13: 978-1523364022 (Available from the PSU Bookstore, Amazon.com and other retail outlets)
- *Designing Digital Systems with SystemVerilog:v2.0)* by Brent E. Nelson. Independently published (June 2019); ISBN-13: 978-1075968433 (Available from Amazon.com)

Other Readings

- Mentor Graphics *QuestaSim* user documentation
- Xilinx Vivado user documentation
- Digilent Nexys A7 documentation
- Technical papers, reports, datasheets, and application notes as posted to class web page

Software Tools

The course will use the following design automation software tools:

- Mentor Graphics *QuestaSim* logic simulator
- Xilinx Vivado 2019.2 (optional)

QuestaSim is available remotely in several labs on campus, the WCC lab, and from either Windows or Linux. You may have to be connected to the VPN to get access. You will need a user account for access to the PC's. You can set up an account through the MCECS CAT in Engineering Bldg. 82-01.

What about ModelSim PE Student Edition and EDA Playground? ModelSim PE Student Edition is currently unavailable for download (https://eda.sw.siemens.com/en-US/modelsim-student-edition-unavailable) . EDA Playground (https://www.edaplayground.com/) hosts several SystemVerilog-compatible simulators but does not have good support for debug. I occasionally use EDA Playground for quick simulations and test code, but I do not rely on it for class assignments or any "serious" simulation.

You may download a copy of *Xilinx Vivado 2019.2 Webpack Edition* for your personal PC. This is a big program (several GB of disk space) and needs a PC with good performance, but our designs (relatively speaking) are miniscule.

Hardware

There is no required hardware for this course because the ECE Teaching labs are unlikely to be open during Spring term. We may target Xilinx Vivado synthesis to one of the Digilent Inc. FPGA development platforms, but you will not be required to run your implementation on the board until the labs are open for general use.

Course Website

We maintain the course website on D2L. The website has announcements, the class calendar, lecture notes, readings, assignments, links to the Zoom meetings and video recordings, links to websites, other documentation, and the gradebook. **Check D2L for announcements, discussion forum additions, etc. every day; "Oh, I forgot to check…" is not a valid excuse.**

D2L Discussion Forums

We will use the D2L discussion forums as the primary platform for asking and answering written questions related to the course. We have enabled Anonymous posts so there is no reason to be shy. You are likely to get a faster response if you post a question to the discussion forum than you will with an email.

Please user our pdx.edu email addresses to contact us by email. DO NOT USE D2L email.

Course Organization

This course will meet remotely via Zoom meetings for approximately 4 hours a week. Lecture topics include hierarchical design, SystemVerilog syntax and semantics, simulation, FPGA vendor support (IP and coding guidelines) and design automation for synthesis. The course will also introduce implementation of embedded systems using a softcore CPU and on JTAG programming. Students will be tested on this material with two in-class exams. Homework assignments will be assigned approximately every 2 weeks and there will be unannounced quizzes and exercises throughout the term.

Zoom Meetings

PSU decided that most courses for Spring term will be taught remotely. The class will meet during its scheduled time. We will use Zoom for virtual meetings and recordings in this course. Links to the class meetings and scheduled office hours are in D2L at People/Zoom Meetings/Upcoming Meetings. All

lectures will be recorded and accessible through D2L at People/Zoom Meetings/Cloud Recordings, but I have disabled video downloads.

Log into D2L using your ODIN credentials and join the class meeting by clicking on the link at People/Zoom Meetings/Upcoming Meetings. You may join the meeting early either by telephone or using the Zoom Video app. Assuming there is sufficient Zoom bandwidth I would like you to enable your video. Being able to see you makes the course more interesting for me and helps me observe how you all are responding to the material.

Pease mute your microphone unless you wish to speak and then mute the microphone again once you have finished speaking. Please enable your video if your PC can do so. The lack of visual feedback makes it difficult for me to discern whether you are confused about what I am talking about. You have several options for participating in the class meetings. First (and the most likely for me to recognize quickly) is to unmute your microphone and ask the question or make the comment. You may also use the Chat window to ask questions and comment. It may take me a bit to respond, but many times other students in the class will reply.

The Acceptable Use Policy and PSU's Student Code of Conduct govern your use of Zoom. PSU keeps a record of all meetings and recordings, in accordance with the Acceptable Use Policy and FERPA. Individual use and distribution of recordings is limited to academic purposes.

Lecture Recordings

All class meetings will be recorded and made available on the Zoom Cloud server through links in D2L. However:

- There may be cases where the recording is not viewable. You are responsible for the lecture material even if the lecture video is not viewable. This is my not-so-subtle way of saying that skipping the "live" class meetings figuring you can watch the recording later is not a good strategy for successfully completing this course.
- There may be cases where I will record and post a link to a class meeting. I expect you to view the video and complete any assigned work on your own before the next class meeting. I will notify you of the situation via a D2L announcement at least 24 hours before the scheduled lecture unless it is an unplanned emergency.

Attendance Policy

- **You are strongly encouraged to attend *every* class meeting via Zoom**. You will not be able to get a good grade in this class without participating in the class meetings. We will be learning from each other and your voice is important.
- **You are required to be in-class (virtually) for both exams and graded in-class exercises.** If you absolutely cannot attend one of these required meetings, please let me knows as soon as you can so that we can agree on an alternative**.**

Remote Exams

My plan is to conduct exams via Zoom during the scheduled class time with an additional 30 minutes either before or after the exam. The class will vote on this option at least a week before the scheduled exam. You will download the exam from D2L, complete it, and upload your completed exams to D2L within 10 minutes of the end of the exam. You can use the Chat window (either to everybody or a private message to me) to ask questions during the exam. I will make alternate plans for those of you with special accommodations. Please arrange this with me at least a week prior to the scheduled exam date.

Grading and Assignment Due Dates

The course grade will be based on quizzes, homework, and exams scores. All assignments and the exams will be graded on a 100-point scale with possible opportunities for extra credit as we progress in the course.

Homework assignments	50%
Graded in-class quizzes and exercises	10%
Exams	40%

Deliverables for assignments will be due by 10:00 PM on the date listed in the syllabus unless the due date is changed. Due date changes will be posted to D2L. You will submit your assignments electronically to your D2L dropbox for that assignment.

Generally, you will have a 23-hour, 59-minute grace period before an assignment is "late" unless told otherwise. Any assignment that is more than 24 hours late will be subject to a penalty of 2% per day. **I will accept late assignments up to 3:00 PM on the day I review the solution in class. Check the announcements and syllabus for the assignment due dates and for when I will discuss the solution in class.**

We will strive to grade and return an assignment two weeks after the assignment is due but the problem-solving nature of the assignments and some of the exam questions make grading a labor-intensive process. We will give feedback electronically using the feedback mechanism in the D2L dropbox. Please check your graded assignment against the solutions. Grading mistakes do happen, but it is your responsibility to bring the matter to our attention immediately after discovering it. Do not wait until the end of the quarter.

Besides contributing substantially to your grade, assignments have far-reaching benefits. They encourage you to keep current with the readings and lectures, test your comprehension of the material, explore topics in more depth, and generally prepare you for the exams.

Grading Scale

Portland State University utilizes a grading system that recognizes A=excellent, B=good, C=satisfactory, D=inferior and F=failure. In general the points to letter grade conversion for the final grade will be as follows, but we may make changes (usually favorable to the students) based on the overall performance of the class.

Points	Letter grade
≥ 94	A
90 – 93	A-
87 – 89	B+
84 – 86	B
80 – 83	B-
77 – 79	C+
74 – 76	C
70 – 73	C-
67 – 69	D+
64 – 66	D
60 – 63	D-
< 60	F

Assignments are graded on a point basis in this course so do not panic if you see that D2L has assigned a lower letter grade than you expected on a specific assignment. It all works out by the end of the term since all assignments are weighted and your performance is ranked relative to that of your peers.

Pass/No Pass option

Portland State has relaxed the deadlines for selecting the Graded or Pass/No Pass option for your final grade. I support this policy – Covid 19 and the pandemic have placed extraordinary stress on students and instructors. There are pros and cons for selecting the Pass/No Pass option. Understand the benefits and consequences of each choice and consider your situation carefully. I will support appeals to change your grading option unless there is a significant reason not to.

Student Conduct and Plagiarism:

I expect my students to handle themselves in a professional manner, respecting property and treating fellow students and the instructors with respect. You are welcome to collaborate with your fellow students in the design of your solutions, **but the implementation and all of the work you submit must be your own**. I will not tolerate plagiarism of any type and the consequences will be severe.

- If you copy work from another member of the class (either team or individual) with or without permission for an assignment, the person or team doing the copying and the person or team providing the work will both receive no credit for assignment without regard to who is at fault. Cheating on an exam will result in a failing grade for that exam. An unexcused absence from the final exam will result in a failing grade for the entire course.

- Practically speaking, as soon as you decide to submit plagiarized work you destroy not only your chance of earning an A in the course, but also that of your partner(s) and the person(s) who you plagiarized.

It is ECE department policy to report all suspected cases of plagiarism or cheating to the PSU administration. You really do not want to go there…and neither do I.

Professionalism and Mutual Respect:

PSU values diversity and inclusion; we are committed to fostering mutual respect and full participation for all students. Our goal is to create a learning environment that is equitable, useable, inclusive, and welcoming. If any aspects of instruction or course design result in barriers to your inclusion or learning, please notify me. Please be aware that as a faculty member I have the responsibility to report any instances of sexual harassment, sexual violence and/or other forms of prohibited discrimination. If you would rather share information about sexual harassment, sexual violence or discrimination to a confidential employee who does not have this reporting responsibility, you can find a list of those individuals at http://www.pdx.edu/sexual-assault/get-help. For more information about Title IX please complete the required student module Creating a Safe Campus in your D2L.

Disability Resources

Please notify me by email or during my office hours if you have approval for academic accommodations. I will make reasonable accommodations to meet your needs. For more information about the Disability Resource Center, see http://www.pdx.edu/drc/.

Center for Student Health & Counseling (SHAC)

Main SHAC website: https://www.pdx.edu/shac/

Weekly Schedule (Tentative)

Lec	Date	Reading	Lecture	Assignment
1_1	**Week 1** Mar 30	• Sutherland Ch 1	• Course overview • Introduction to SystemVerilog • RTL and gate-level models	
1_2	Apr 1	• Sutherland Ch 2	• FPGA's, ASIC's, ASSP's, and SoC's • SystemVerilog language rules	
2_1	**Week 2** Apr 6	• QuestaSim tutorial	• Modules, ports, and hierarchy • Simulation w/ QuestaSim	
2_2	Apr 8	• Sutherland Ch 3	• Literals, nets, and vars	
	Apr 8	**Graded "In-class" exercise - Modeling and simulating a Ripple Carry Adder** (We will start this exercise during the class meeting. You will finish it and submit it to D2L this evening)		
3_1	**Week 3** Apr 13		• Packed and unpacked arrays • Parameters and constants	• Homework #1 assigned
3_2	Apr 15	• Sutherland Ch 4	• User-defined types	
4_1	**Week 4** Apr 20	• Sutherland Ch 5	• User-defined types (wrap-up) • SystemVerilog packages	
4_2	Apr 22		• RTL expression operators	
	Apr 22	**Graded "In-class" exercise – Logic design with SystemVerilog** (We will start this exercise during the class meeting. You will finish it and submit it to D2L this evening)		
	Week 5 Mon, Apr 26	**Homework #1 due to D2L by 10:00 PM** **NO ASSIGNMENTS ACCEPTED AFTER NOON ON THU, APR 30**		
5_1	Apr 27	• Sutherland Ch 6	• RTL expression operators (wrap-up) • RTL programming Statements	• Homework #2 assigned
5_2	Apr 29		• RTL programming statements (wrap-up) • Review HW #1 solution	
	Week 6 Mon, May 3	**Homework #2 due to D2L by 10:00 PM** **NO ASSIGNMENTS ACCEPTED AFTER NOON ON TUE, MAY 4**		
6_1	May 4		• RTL programming statements (cont'd)	

			• Review HW #2 solution • Review for Midterm Exam	
	May 6	***** MIDTERM EXAM (2:00 PM – 4:30 PM?)*****		
7_1	**Week 7** May 11		• SystemVerilog functions and tasks	
7_2	May 13	• Sutherland Ch 7	• Modeling combinational logic	• Homework #3 assigned
8_1	**Week 8** May 18	• Sutherland Ch 8	• Modeling sequential logic	
8_2	May 20	• Sutherland Ch 9	• Modeling sequential logic (wrap-up) • Avoiding unintended latches • Review Midterm exam solution	
	Week 9 Mon, May 24	**Homework #3 due to D2L by 10:00 PM** **NO ASSIGNMENTS ACCEPTED AFTER NOON ON TUE, JUN 2**		
9_1	Tue, May 25		• Serial communication • Writing testbenches	• Homework #4 assigned
9_2	May 27		• Writing testbenches (wrap-up)	
	May 27	**Graded "In-class" exercise - Testbenches** (We will start this exercise during the class meeting. You will finish it and submit it to D2L this evening)		
10_1	**Week 10** Jun 1Roy	• *What is JTAG*? • *Vivado Design Suite User Guide: Design Flows Overview* (Xilinx UG 892)	• JTAG • Review HW #3 solution • Using Xilinx Vivado for synthesis (PmodSSD example)	
	Wed, Jun 3	**Homework #4 due to D2L by 10:00 PM** **NO ASSIGNMENTS ACCEPTED AFTER NOON ON THU, JUN 4**		
10_2	Jun 4	• Sutherland Appendix A: *Best Practices Coding Guidelines*	• Catch-up, wrap-up • Review Homework #4 solution • Review for Final Exam	
	Week 11 Tue, Jun 8	**TENTATIVE** ***** FINAL EXAM (2:00PM – 4:30PM")*****		