Weekly Schedule (Tentative)

Lec	Date	Reading	Lecture	Assignment
1_1	**Week 1** Mar 30	• Sutherland Ch 1	• Course overview • Introduction to SystemVerilog • RTL and gate-level models	
1_2	Apr 1	• Sutherland Ch 2	• FPGA's, ASIC's, ASSP's, and SoC's • SystemVerilog language rules	
2_1	**Week 2** Apr 6	• QuestaSim tutorial	• Modules, ports, and hierarchy • Simulation w/ QuestaSim	
2_2	Apr 8	• Sutherland Ch 3	• Literals, nets, and vars	
	Apr 8	**Graded "In-class" exercise - Modeling and simulating a Ripple Carry Adder** (We will start this exercise during the class meeting. You will finish it and submit it to D2L this evening)		
3_1	**Week 3** Apr 13		• Packed and unpacked arrays • Parameters and constants	• Homework #1 assigned
3_2	Apr 15	• Sutherland Ch 4	• User-defined types	
4_1	**Week 4** Apr 20	• Sutherland Ch 5	• User-defined types (wrap-up) • SystemVerilog packages	
4_2	Apr 22		• RTL expression operators	
	Apr 22	**Graded "In-class" exercise – Logic design with SystemVerilog** (We will start this exercise during the class meeting. You will finish it and submit it to D2L this evening)		
	Week 5 Mon, Apr 26	**Homework #1 due to D2L by 10:00 PM** **NO ASSIGNMENTS ACCEPTED AFTER NOON ON THU, APR 30**		
5_1	Apr 27	• Sutherland Ch 6	• RTL expression operators (wrap-up) • RTL programming Statements	• Homework #2 assigned
5_2	Apr 29		• RTL programming statements (wrap-up) • Review HW #1 solution	
	Week 6 Mon, May 3	**Homework #2 due to D2L by 10:00 PM** **NO ASSIGNMENTS ACCEPTED AFTER NOON ON TUE, MAY 4**		
6_1	May 4		• RTL programming statements (cont'd)	

			• Review HW #2 solution • Review for Midterm Exam	
	May 6	***** MIDTERM EXAM (2:00 PM – 4:30 PM?)*****		
7_1	**Week 7** May 11		• SystemVerilog functions and tasks	
7_2	May 13	• Sutherland Ch 7	• Modeling combinational logic	• Homework #3 assigned
8_1	**Week 8** May 18	• Sutherland Ch 8	• Modeling sequential logic	
8_2	May 20	• Sutherland Ch 9	• Modeling sequential logic (wrap-up) • Avoiding unintended latches • Review Midterm exam solution	
	Week 9 Mon, May 24	**Homework #3 due to D2L by 10:00 PM** **NO ASSIGNMENTS ACCEPTED AFTER NOON ON TUE, JUN 2**		
9_1	Tue, May 25		• Serial communication • Writing testbenches	• Homework #4 assigned
9_2	May 27		• Writing testbenches (wrap-up)	
	May 27	**Graded "In-class" exercise - Testbenches** (We will start this exercise during the class meeting. You will finish it and submit it to D2L this evening)		
10_1	**Week 10** Jun 1Roy	• *What is JTAG*? • *Vivado Design Suite User Guide: Design Flows Overview* (Xilinx UG 892)	• JTAG • Review HW #3 solution • Using Xilinx Vivado for synthesis (PmodSSD example)	
	Wed, Jun 3	**Homework #4 due to D2L by 10:00 PM** **NO ASSIGNMENTS ACCEPTED AFTER NOON ON THU, JUN 4**		
10_2	Jun 4	• Sutherland Appendix A: *Best Practices Coding Guidelines*	• Catch-up, wrap-up • Review Homework #4 solution • Review for Final Exam	
	Week 11 Tue, Jun 8	**TENTATIVE** ***** FINAL EXAM (2:00PM – 4:30PM")*****		