ECE 351 Verilog and FPGA Design

Week 10_2: Introduction to Xilinx Vivado (wrap-up)
Review Roy's HW #4 solution
General review for final exam

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Introduction to Xilinx Vivado (wrap-up)

Sources:

- FPGA design flow using Vivado workshop, Xilinx Corp.
- ECE 540 lecture notes by Brian Cruickshank
- ECE 540 lecture notes by Roy K. and David B.



Vivado flow stages

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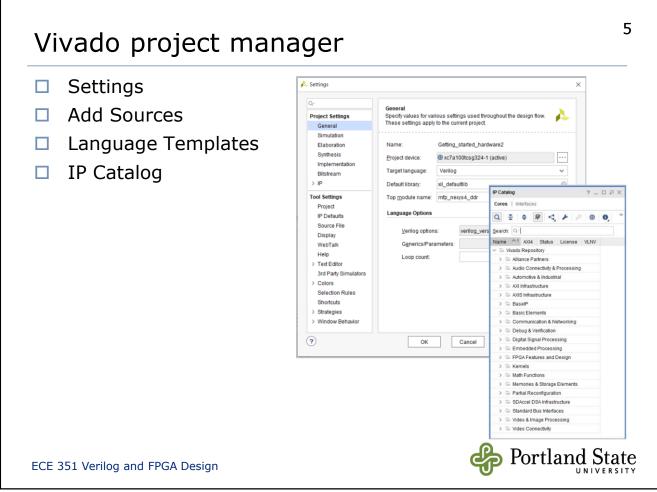
- Project Manager
- IP Integrator
- Simulation
- □ RTL Analysis
- □ Synthesis
- □ Implementation
- Program and Debug





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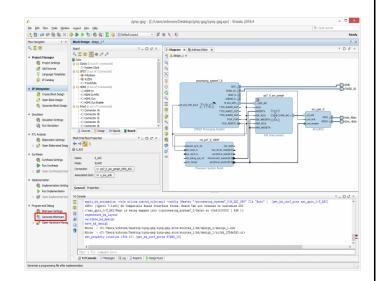
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Vivado **IP I**ntegrator

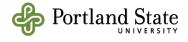
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- ☐ Create Block Design
- □ Open Block Design
- □ Generate Block Design



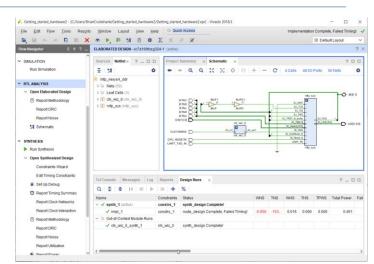
https://reference.digilentinc.com/vivado/getting-started-with-ipi/2018.2

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Vivado RTL analysis

- Open Elaborated design
 - Report Methodology
 - Report DRC
 - Report Noise
 - Schematic
- Schematics at RTL Analysis
 - No optimization, just reading RTL



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Vivado synthesis

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- □ Run Synthesis
- Open Synthesized Design
 - Constraints Wizard
 - Edit Timing Constraints
 - Set Up Debug
 - Report Timing Summary
 - Report Clock Networks
 - Report Clock Interaction
 - Report Methodology
 - Report DRC
 - Report Noise
 - Report Utilization
 - Report Power
 - Schematic



Schematics at Vivado synthesis level

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- Schematics are mapped to a netlist
 - A netlist is a Verilog netlist mapping to LUT cells, Carry Logic, DSP, RAMs, Ios, clock circuits, etc standard elements in the FPGA.
 - No behavioral code is left.
 - □ No always blocks. No functions. No ternary operators.
- □ Schematics/netlist is optimized for timing
 - Serial constructs will be made parallel for area or timing
 - For example, XOR parity structure can be made into a tree instead of xoring each bit in series
- But it is optimized with no physical knowledge
 - Net timing is only approximated
- You can write_verilog from TCL console



Solve problems early

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- Finding timing problem at synthesis saves time
 - Implementation takes a long time to run
 - Many times, the timing problem exists at synthesis
- Debug the timing problems at synthesis first

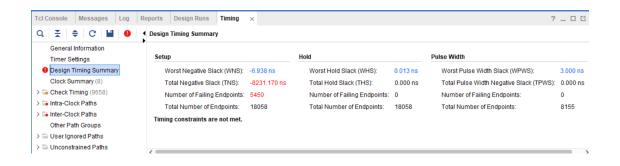
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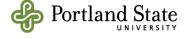
Report timing summary

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- Many categories of reports, lots of terms
 - WNS
 - TNS
 - Failing Endpoints
 - Check Timing



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Vivado implementation

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- □ Run Implementation
- Open Implemented Design
 - Constraints Wizard
 - Edit Timing Constraints
 - Report Timing Summary
 - Report Clock Networks
 - Report Clock Interaction
 - Report Methodology
 - Report DRC
 - Report Noise
 - Report Utilization
 - Report Power
 - Schematic

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Implementation

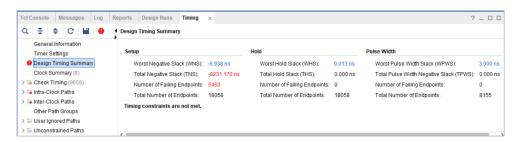
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- Maps the LUTs, SRAMs, I/O's, etc. to physical locations on the desired FPGA
- □ Nets are mapped to global, section, local nets
- □ Real net delays are used.
- Locations of components are moved around to improve timing
- □ Nets are split, re-driven
- Iteration happens on the worst paths until nothing more can be improved.
 - Sometimes only the worst is optimized (WNS based), sometimes all paths down to passing is optimized (TNS based)
- □ Different settings to trade-off runtime, area, performance

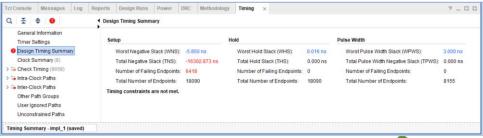


Report timing summary

Many categories of reports, lots of termsSynthesis

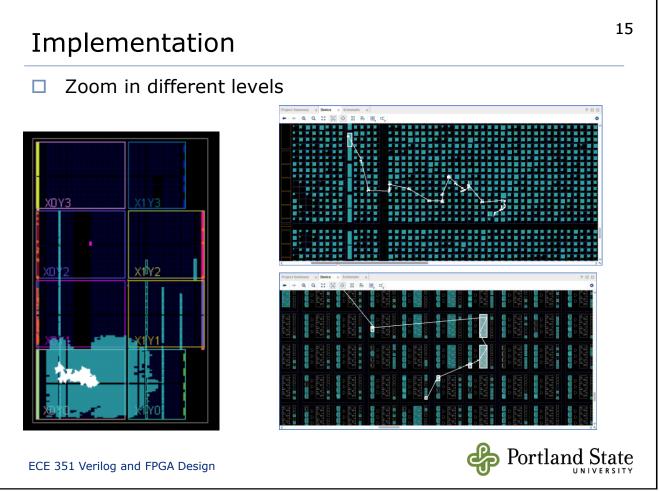


Implementation



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Portland State



Roy's Homework #4 solution

Write-up: ece351sp21 hw4 release r1 1\docs\ece351sp21 hw4.pdf

Roy's solution: ..\..\assignments\hw4\hdl

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Review for final exam



Review for final exam

- Exam will be open book, open notes, open internet
 - You will need internet and D2L access to complete the exam
 - Unless the problem specifically says so we are not going to deduct points for syntax errors (missing; etc.) but we do expect your code to be indented and formatted so that we can read it
 - I do not recommend trying to simulate your answers it will take too long, and you have a strict deadline...however using a context-sensitive text editor like Notepad++ for the programming questions is allowed and encouraged.
- □ The exam will be:
 - ~60% T/F, multiple choice, short answer
 - ~40% SystemVerilog programming
- All students in the class who have not made special arrangements with me are expected to take the exam on Mon, 07-Jun in the AM
 - Time will depend on poll results posted Friday evening



Review for midterm exam (cont'd)

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- □ Exam will focus on the material covered since the midterm and will (hopefully) include some questions you submitted.
- Topics covered since the midterm:
 - Blocking and non-blocking assignments
 - Modeling sequential logic
 - Avoiding unintended latches
 - SystemVerilog functions
 - Testbenches (incl. implicit FSM's)
- You can expect to write SystemVerilog code using the constructs you've learned this term

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Test process (cont'd)

- You will provide your answers to a problem in the associated .txt or.sv file (ex: prob1.txt) using a text editor
- When you have completed the exam, please create a <u>single</u> .zip or .rar file with all of your answers and upload it to your D2L midterm exam dropbox
 - IMPORTANT: You will be able to submit more than once until the dropbox closes...no submissions after the dropbox closes!
 - We will keep/grade your latest submission so submit the full package
 - Make sure that you submit what you want us to grade there are no do-overs
- ☐ The dropbox will close **10 minutes after the exam "ends**" so allow time to bundle your answers and upload them to D2L before then



Next Time

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- □ End of term activities (see email and announcements for details)
 - Final exam review sessions Fri 04-Jun, Sat 05-Jun
 - Please complete the Doodle poll on Final exam times
 - Please complete the course/instructor evaluation
- ☐ You should:
 - Extra credit opportunity: Submit final exam questions/solutions to D2L by 10:00 PM on Friday, 04-Jun (up to 8 points added to your midterm exam score)
- ☐ Homework, projects and quizzes
 - Homework #4 deadline extended to 5:00 PM today
- □ Final exam scheduled for Mon 07-Jun in the AM
 - Time to be posted Friday evening based on poll results
 - Please email me if you need and have approval for special accommodations

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