

Tri_pipe_h1.v
Test Bench Example for stored test vectors

tri_pipe_h1.v

```
// tri_pipe_h1.v - Example for a Test Bench that reads vectors from a
// separate system file
// Source: HDL Chip Design by Douglas J. Smith p 343-344
//
`timescale 1ns/100ps

module TRI_PIPE_H1;
    parameter    ClockPeriod = 20,
                TestCycles = 3;

    // inputs to RTL hardware module
    logic          Clock, Reset, InDataReady;
    logic  [1:0]    A, B, C;

    // outputs from RTL hardware model
    wire           OutDataReady;
    wire  [8:0]    Y;

    // set up register (memory) arrays to hold input data
    logic  [7:1]    ABC_Arr[TestCycles];

    int            N;
```

```

logic                PassFail,
                    FailTime;

// instantiate the model under test
TRI_PIPE TRI_PIPE_1 (
    .Clock(Clock),
    .Reset(Reset),
    .InDataReady(InDataReady),
    .A({6'b000000, A}),
    .B({6'b000000, B}),
    .C({6'b000000, C}),
    .OutDataReady(OutDataReady),
    .Y(Y)
);

// set up free running clock
initial Clock = 1;
always
    #(ClockPeriod / 2) Clock = !Clock;

// apply stimulus to model under test
initial begin
    // loads contents of file "tri_pipe_h1.v_vec" into ABC_Arr[]
    $readmemb("tri_pipe_h1.v_vec", ABC_Arr);

    // set initial values
    Clock = 1'b0;    Reset = 1'b1;
    InDataReady = 1'b0; A = 2'b00;  B = 2'b00;  C = 2'b00;

```

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// perform reset
#ClockPeriod Reset = 1'b1;
#ClockPeriod Reset = 1'b0;    //reset is active low
#ClockPeriod Reset = 1'b1;

// Cycle through the test vectors
for (N = 0; N <= TestCycles; N = N + 1) begin
    @posedge Clock
        {InDataReady, A, B, C} = ABC_Arr[N];
end

// Flush the pipeline at the end of the test
repeat(3)
    #ClockPeriod;
$stop;
end // stimulus block

endmodule

```

tri_pipe_h1.v_vec – external file of test vectors

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// Test vector file in a format that can be read w/ $readmemb()
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1011011 // InDataReady = 1, A = 1, B = 2, C = 3
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0100010 // InDataReady = 0, A = 2, B = 0, C = 2
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0111110 // InDataReady = 0, A = 3, B = 3, C = 2
```