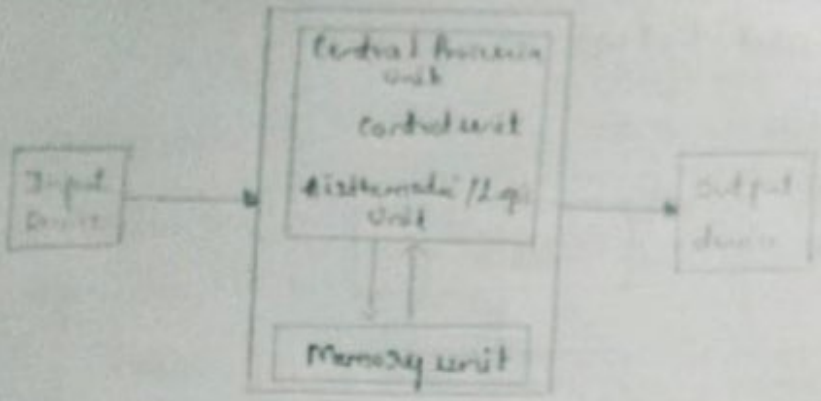
3 With a neat diagram explain Von neuman and Harvard Architecture

Von-neuman



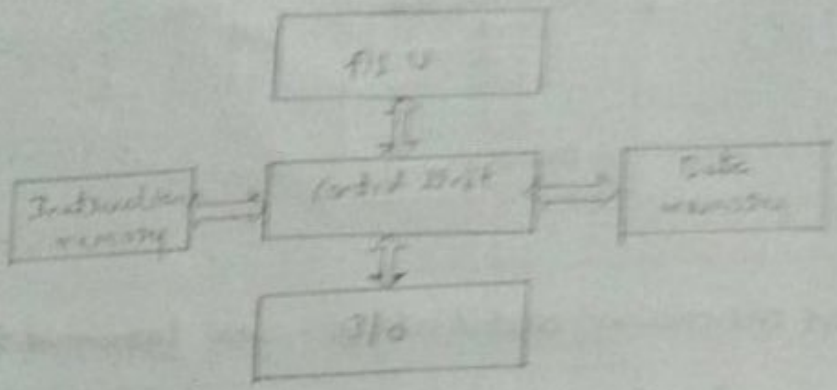
* The Von Neumann architecture - also known as the von-neumann model or princeton architecture.

* The term "von-neumann architecture" has evolved to mean any stored-program computer in which an instruction fetch and a data operation cannot occur at the same time because they share a common bus.

* The design of a von-neuman architecture machine is simpler than a Harvard architecture machine which is also a stored-program system but has one dedicated set of address and data buses for reading and writing to memory, and another set of address and data buses to fetch instructions.

* A stored-program digital computer keeps both program instructions and data in read-write, random-access memory.

Harvard architecture



The Harvard architecture is a computer architecture with separate storage and signal pathways for instructions and data. It contrasts with the Von-Neumann architecture where program instructions and data share the same memory and pathways.

Harvard architecture has two separate buses for instruction and data. Hence, CPU can access instruction and read/write data at the same time. This is the major advantage of Harvard architecture.

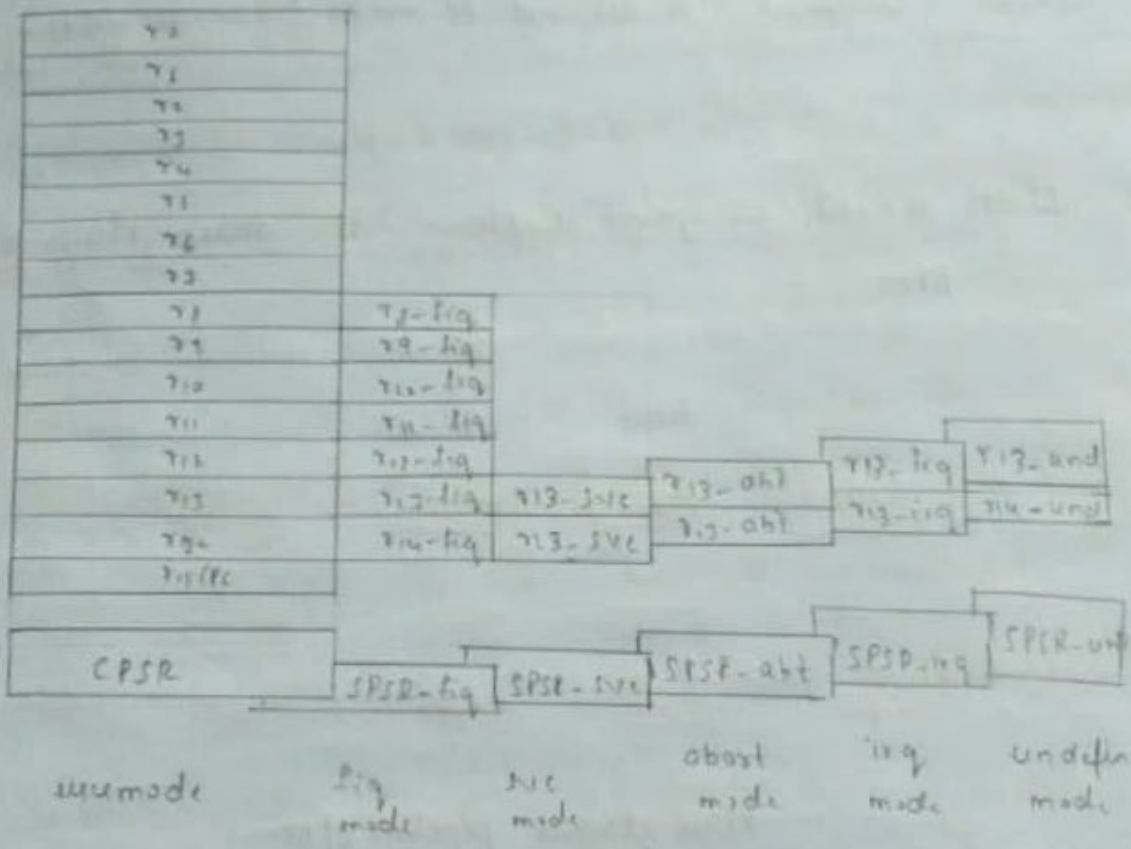
2. List the difference RISC v/s CISC machine

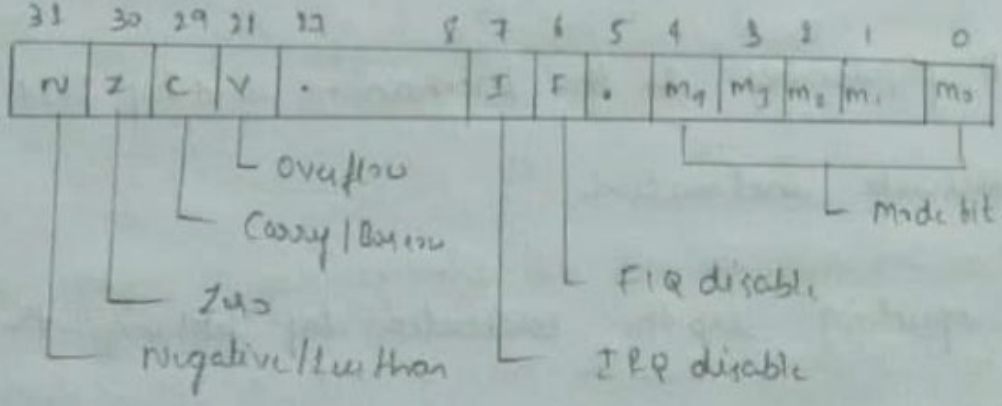
RISC	CISC
* An instructed set architecture that is designed to perform a smaller number of computer instructions so that it can operate at a higher speed.	* A full set of computer instructions that intends to provide the necessary capabilities in an efficient way.
* Stands for Reduced Instruction set computer	* Stands for complex Instruction set computer
* Utilizes a small highly optimized set of instructions	* Utilizes a large, specifilized and a complex set of instructi
* More machine oriented	* More programmer oriented
* Simple and requires one clock cycle to execute instructions	* Complex and requires multi clock cycle to execute an instructions
* More registers	* Fewer registers
* Has simple instructions the program length is long	* Has complex instructions the program length is short
* Requires more RAM	* Requires a minimum amount of RAM.

- 16 registers are R0 to R15. In this three registers (R13, R14, R15) are special purpose registers

These three registers used for only important functions in the program

ARM Programming model.





format of the Program status register

The ARM processor consists of

* Arithmetic Logic unit (32 bit)
* One boothm multiplier (32-bit)
* One barallel shifter
* One control unit
* Register file of 37 registers each of 32 bits

ARM Registers: ARM 7 has a total 37 registers. In which 31 are general-purpose registers of 32 bits and six status registers. But all these registers are not seen at once. At any time among the 31 registers only 16 registers are available to the user.

r0	r1	r2	r3	r4	r5	r6	r7	fiq r8	fiq r9	fiq r10	fiq r11	fiq r12	fiq r13	fiq r14	r15
								r8	r9	r10	r11				
														SP	LR	PC

fig: Fast Interrupt request.

In this 15 registers, the r13 acts as a stack pointer register and r14 acts as a link register and r15 acts as a program counter register

(4) With a neat diagram, explain the programming model of ARM.

* ARM is a flexible programming designed architecture with different applications.

* Design is simple, optimum and economic

* A processor's instruction set defines the operations that the programmer can use to change the state of the system incorporating the processor

* This state usually comprises the value of the data stream in the processor's visible registers and the system memory.

* Each instruction can be viewed as performing a defined transformation from the state before the instruction is executed to state after it has completed.

ARM Registers:

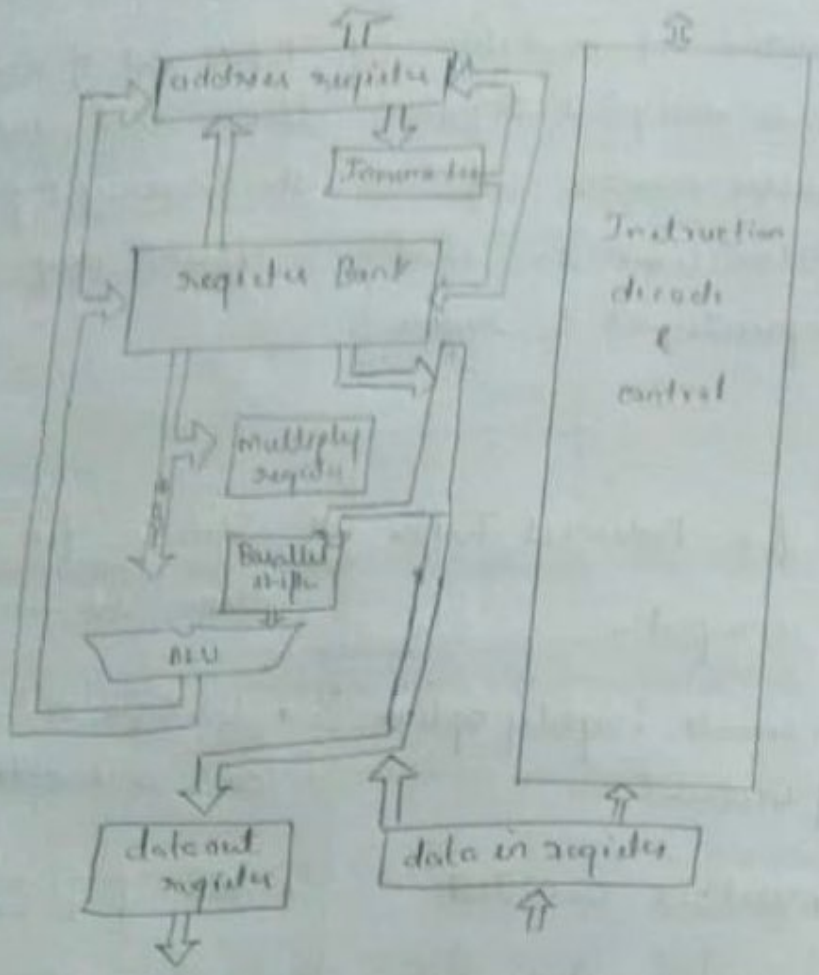
* ARM has 31 general purpose 32 bit registers.

* 16 registers only visible register

* 16 registers are user mode registers.

* Other registers are used to speed up execution processing

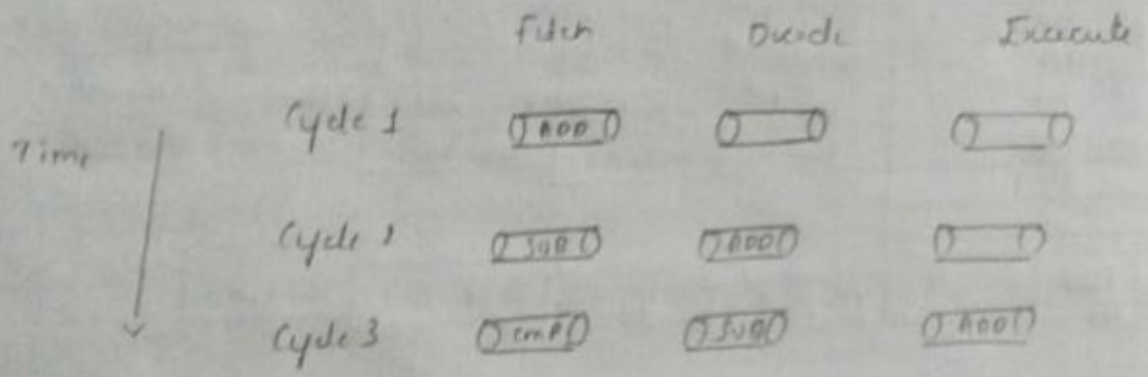
3. With a neat diagram, explain the ARM 7 architecture.



The ARM 7 processor is based on Von. neuman model with a single bus for both data and instructions. Though this will decrease the performance of ARM, it is overcome by the pipeline concept. ARM uses the Advanced Microcontroller bus Architecture. This AMBA include two system buses: the AMBA High-speed bus (AHB) or the advanced system bus (ASB), and the advanced Peripheral bus

M[4:0]	Mode	Accessible register set	
10000	User	PC, R14..R0	CPSR
10001	FIQ	PC, R14-fiq..R8-fiq, R7..R0	CPSR, SPSR-fiq
10010	IRQ	PC, R14-irq..R13-irq, R12..R0	CPSR, SPSR-irq
10011	Supervisor	PC, R14-svc..R13-svc, R7..R0	CPSR, SPSR-svc
10111	Abort	PC, R14-abt..R13-abt, R7..R0	CPSR, SPSR-abt
11011	Undefined	PC, R14-und..R13-und, R7..R0	CPSR, SPSR-undefined

⑥ With a neat diagram, explain the three-stage pipeline of ARM



three staged pipeline of ARM

ARM Pipelining:

* A pipelining is the mechanism used by RISC processor to execute instruction.
* by speeding up the execution by fetching the instruction while other instruction are being decoded and executed simultaneously

. which in turn allows the memory system and processor to work continously

. The pipeline design for each ARM family is different

Pipelining is a design technique or a process which plays an important role in increasing the efficiency of data processing in the processor of a computer and microcontroller. By keeping the processor in a continous process of fetching decoding and executing called (F & E cycle)

Pipelining :

- Fetch loads an instruction from memory.
- Decode identifies the instruction to be executed.
- Execute process the instruction and writes the result back to the register.
- By over lapping the above stages of execution of different instructions, the speed of execution is increased
- The pipelining allows the core to execute an instruction every cycle. which results in increased throughput.

Features of I2C

> It supports multiple data speed : standard mode, fast mode, Fast-mode plus, high speed mode, and ultra fast mode I2C communication

* Independent master, slave, and monitor functions

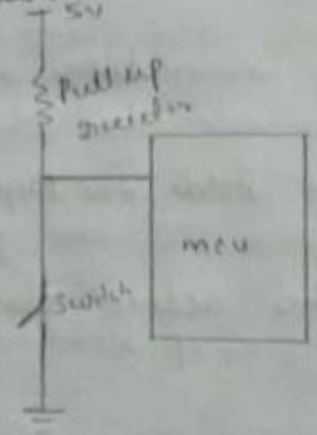
* Supports both Multi-master and multi master with slave function

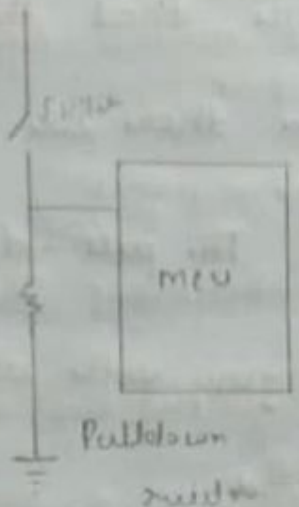
* Multiple I2C slave address supported in hardware

* 10-bit addressing supported with software assist

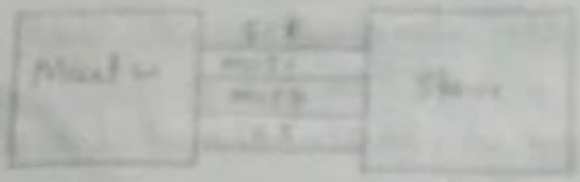
* I2C operates in 3 speeds 100kbps, 400kbps and 3.4mbps.

25 With a neat diagram, explain the pull up and pull down resistor





SPI is called as a 4 wire bus as it requires four wires for communication. In case of single slave select (SS) is not required. So it requires more communication lines as compared to UART, I²C, USB etc.



- SCK or SCLK: Serial clock, clock generated by master.
- MOSI or SDO: Master Output slave Input: data output from master.
- MISO or SDI: Master Input slave Output: data output from slave.
- SS: Slave select, often an active low input of a slave.

When multiple slave devices are used, an independent slave select line is connected from master to each slave device.

Bit rate: Bit rate refers to the rate at which data is processed or transferred. It is usually measured in units ranging bps for smaller values to Kbps and Mbps.

Bit rate is also known as bitrate & data rate.

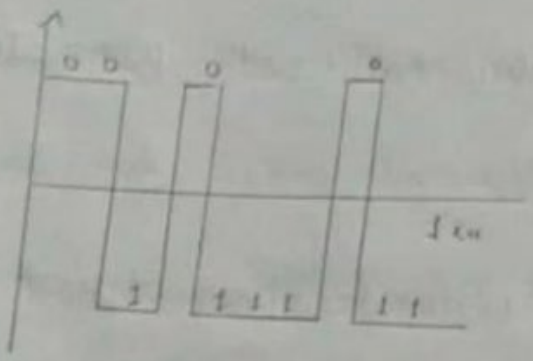
BR(Bit rate) = D ÷ T

Where

BR: Bit rate

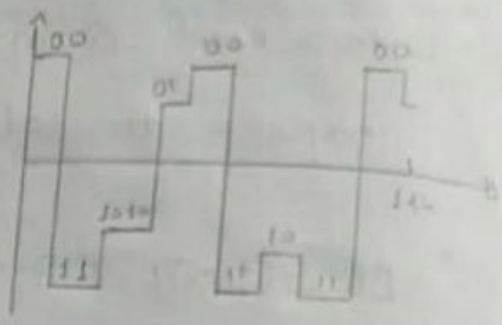
D: Amount of Data

T: Time (in seconds)



Baud = 10

Bit rate = 10 bps



Baud = 10

Bit rate = 20 bps

* CPOL significance: This defines whether the clock signal will be high (CPOL = 1) or low (CPOL = 0) before the chip select goes low

* CPHA significance: It tells whether the data is sampled during first edge of the clock signal or the second edge of the clock signal.

If CPHA = 0, CPOL has to be 0 so that sampling can happen during the rising edge of the signal

If CPHA = 1, CPOL has to be 1 so that the sampling can happen during the rising edge of the signal.

Mode	CPOL	CPHA
0	0	0
1	0	1
2	1	0
3	1	1

24) With a neat diagram explain the features of I2C and its working

I2C stands for Inter-Integrated circuit. It is a bus interface connection protocol incorporated into devices for serial communication

20. Explain the LPC2148 microcontroller GPIO pins

GPIO: General Purpose Parallel Input/output

GPIO registers control the device pins which are not linked to a particular peripheral function. The device pins can be arranged as i/p or o/p. Individual registers allow for clearing any number of o/p's concurrently. The output register value can be read back and the present condition of the port pins.

General-purpose input/output registers are mapped to the processor bus and used for the best probable I/O time.

- These registers are addressable bytes
- The total value of a port can be written in the only instruction

10 bit ADC

The microcontrollers like LPC2148 has 32 bit GPIO.

1. Port 0
2. Port 1

Working of I2C communication Protocol.

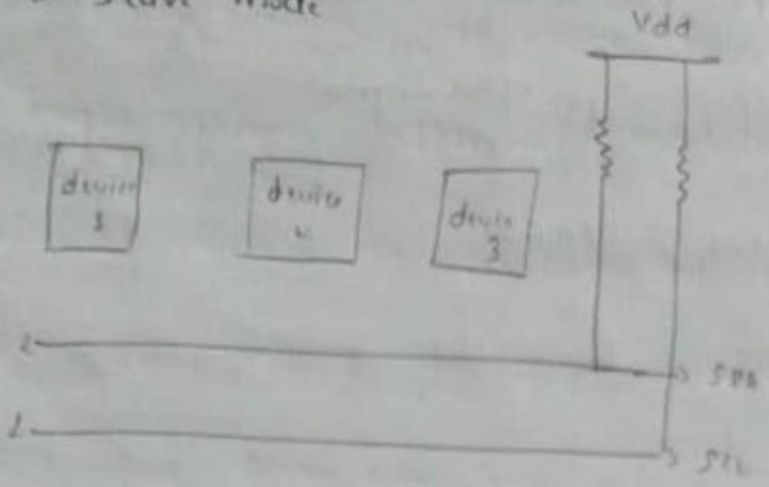
It use only 2 bi directional open-drain lines for data communication called SDA & SCL. Both these lines are pulled high

Serial Data (SDA): Transfer of data take place through this pin.

Serial clock (SCL): It carries the clock signal.

I2C operate in 2 modes:

* Master mode
* Slave mode



According to I2C protocol, the data line can not cha when the clock line is high, it can change only when the clock line is low.

1. Start condition - 1 bit
2. Slave address - 8 bit
3. Acknowledge - 1 bit

Port 0 is a 32 bit port

- Out of these 32 pins, 29 pins can be configured as either general purpose input or output
- 1 of these 32 bit can be configured as general purpose output only
- 3 of these 32 pins are reserved hence they are not available for use

Port 1 is also a 32 bit port. Only 16 of these 32 pins are available for use as general-purpose input or output

21. With a neat diagram, explain baud rate, Bit rate explain the calculations

Baud rate: Baud rate is number of signal units per second. It can be defined as per second number of changes Baud rate focuses on data transmission. Baud rate can be calculated as Baud rate, r = Bitrate, P / the number of bit per baud n

Baud rate calculator use baud - rate = Bit Rate / Number of bits to calculate the Baud rate, Baud rate refers to the number of signal or symbol changes that occur per second.

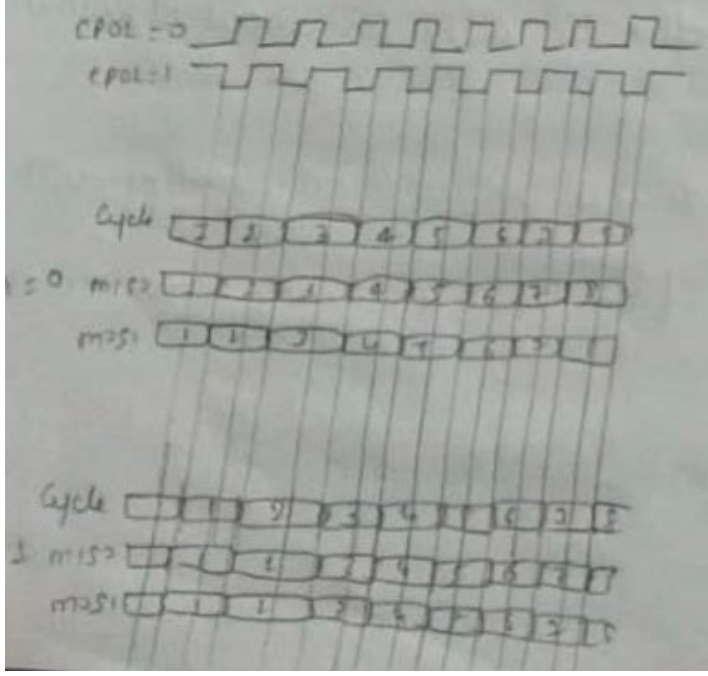
Working of SPI

Master will generate clock whenever it wants to write data to a slave device After 8 clock pulses data in the master device and data in the slave device ($B_7 - B_0$) is transferred to the master device

Features of SPI:

SPI signals include the standard serial clock, master in slave out, master out slave in, bidirectional serial data and slave select. The SPI master component should be used any time the PSoC device is required to interface with one or more SPI slave devices

23. In SPI, with a neat timing diagram, explain the CPHA and CPOL usage.



19) Explain the LPC 2148 Microcontroller Block diagram

The ARM has launched several processors that have different features as well as the different cores for a wide variety of applications. The first ARM architecture design has 32 bit processor, but now it reached 64 bit processor.

ARM7 based LPC2148 Microcontroller

The ARM7 is a 32 bit general purpose microprocessor, and it offers some of the features like little power utilization and high performance. The architecture of an ARM is depended on the principle of RISC

Interrupt sources

Every peripheral device consists of a single interrupt line allied to the VIC (vector interrupt controller), although it can have various interrupt flags inside.

On chip flash program Memory

The microcontroller LPC2148 includes a flash memory like 32 KB, 128 KB, 256 KB. This flash memory can be used for both data storage as well as code

(8) Explain the following addressing modes in ARM.

a) Three addressing modes b) Two addressing modes

c) Single addressing mode instructions with respect to ARM

a) Three address Instruction: This is common in Two

commercial computers. Here two addresses can be specified in the instruction. the result can be stored at different locations rather than just accumulator. but requires more number of bit to represent address

ex: ADD P, P, P, P, ← P, + P,

b) Three address Instruction: This has three address fields to specify a register or a memory location. Program created are much short in size but number of bits per instruction increases. These instructions make creation of Program much easier but it doesn't mean that program will run much faster

ADD P, , A, B P, ← A + B

c) One addressing mode :- One address instruction uses implied accumulator (AC) register for all data manipulation. For multiplication and division there is a need for a second register

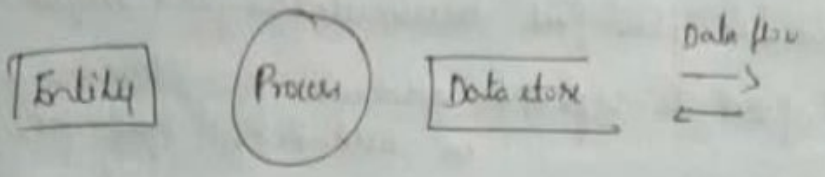
Load A AC ← M(A)

Type of data flow diagram (DFD)

* Logical DFD : this type of DFD concentrates on the system process and flow of data in the system.

* Physical DFD : this type of DFD shows how the data flow is actually implemented in system

DFD component



Structure Chart.

Structure chart is a chart derived from Data flow diagram. It represents the system in more detail than DFD

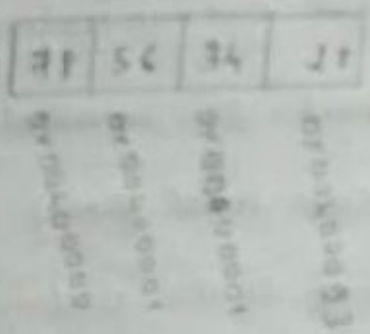
HIPO Diagram

HIPO diagram is a combination of two organized method to analyse the system and provide the means of documentation

Structure English:

It is the responsibility of higher software management to provide accurate information to the programmer to develop accurate yet fast code

Little endian byte order: The least significant byte of the data is placed at the byte with the lowest address. The rest of the data is placed in order on the next three bytes in memory.



(iv) Write a C program to find the endianness of a given number

```
#include <stdio.h>
int main()
{
 unsigned int x = 0x76543210;
  char *c = (char *) &x;
 Printf ("*c is: 0x%x\n", *c);
  if (*c == 0x10)
    {
      Printf ("underlying architecture is little endian.\n");
    }
  else
    {
     Printf ("underlying architecture is big endian.\n");
    }
 return 0;
}
```

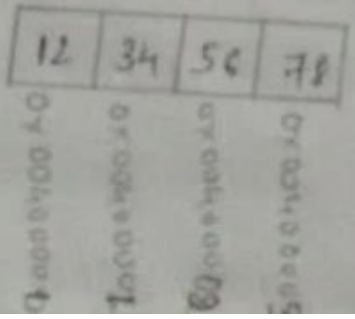
(13) What is Endianness? List the types with example.

Endianness: In computing endianness is the order of sequence of bytes of a word of digital data in computer memory. On most modern computers, the smallest data group with an endianness address is eight bits long and is called byte. Longer groups contain two or more bytes. For example, a 32 bit word contains four bytes.

There are two type of endianness they are:

* Big endian
* Little endian

Big endian byte order: The most significant byte (the big end) of the data is placed at the byte with the lowest address. The rest of the data is placed in order in the next three bytes in memory.



with extra zeros to fill 32 bits

0000 0000 0000 0000 0000 0001 0000 1010

If instructions aligned as half word will be read by a word aligned machine each two instructions will be considered by the machine as single instructions leading to error

(A) Explain the software tools involved and processing the C source file with a neat diagram

Software analysis and design includes all activities which help the transformation of requirement specification into implementation. Requirement specification specify all functional and non functional expectations from the software. These requirements specifications come in the shape of human readable and understandable documents. to which a computer has nothing to do

Design Tools:

Data flow diagram: Data flow diagram is graphical presentation of flow of data in an information system. It is capable of depicting incoming data flow, outgoing data flow and stored data

Word: A word is a fixed sized piece of data handled as a unit by the instruction set or the hardware of the processor. The number of bits in a word is an important characteristics of any specific processor design or computer architecture word is 32 bit.

(8) Explain word align and half word align in ARM memory

Word alignment & half word alignment

Word alignment with respect to machine instruction is how the instruction should be broken into blocks, and how instruction which are shorter than full block should be handled. for short, the alignment is the size of the blocks our machine can access. Suppose we have a computer architecture for which a "word" is 32 bits, and a half word is 16 bits.

Suppose that we have an instruction: 0x010A. This instruction is only 16 bit, a half word. if our system use half word alignment, two consecutive instruction will look like this 0000 0000, 0000 1010, 0000 0001 0000 1010

But when using word alignment, an instruction must fill up an entire word. then 0x010A will be padded

(13) Explain a) Bit b) Byte c) Nibble d) Half word
e) Word

Bit :- The bit is the most basic unit of information in computing and digital communications

A bit is a binary digit, the smallest increment of data on a computer. A bit can hold only one of two values : 0 or 1, corresponding to the electrical values of off and on

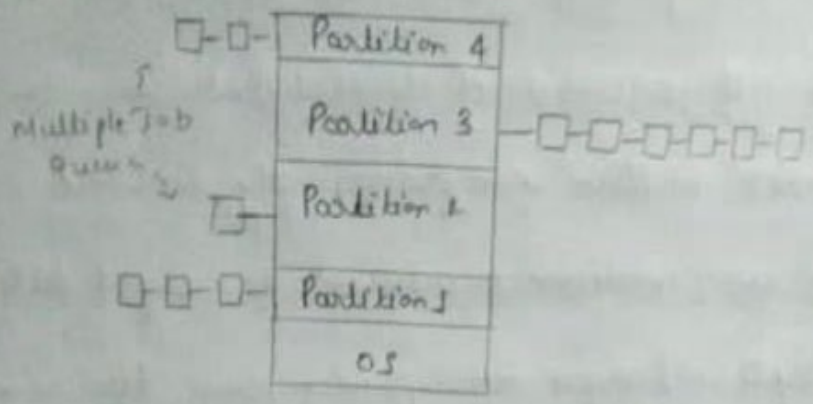
Byte: Byte is the basic unit of information in computer storage and processing. A byte consists of 8 bits.

Nibble: In computer and digital technology, a nibble is four binary digits or half of an eight-bit byte.

A nibble can be conveniently represented by one hexadecimal digit

Half word: The half word and word for a 16-bit quantity, while long word refered to a 32 bit quantity. This was in contrast to earlier machines, where the natural unit of addressing memory would be called a word, while a quantity that is one half a word would be called a half word.

- Three partitions are defined at system start-up and can be used to store all the segments of the process



Example of Process with MMU support

ARM architecture based application processor implement an MMU defined by ARM's virtual memory system architecture. The current architecture defines PTEs for describing 4KB and 64KB pages, 1MB sections and 16MB super-sections; legacy version also defined a 1KB tiny page. ARM uses a two-level page table if using 4KB and 64KB pages, or just a one-level page table for 1MB sections and 16MB sections

(12) What is MMU? Why MMU required? give example of Processor with MMU support

MMU: A memory management unit is a computer hardware component that handles all memory and caching operations associated with the processor. In other words, the MMU is responsible for all aspects of memory management. It is usually integrated into the processor, although in some time system it occupies a separate IC.

Why MMU required: An important function of the memory management unit is to enable the system to run multiple tasks, as independent programs running in their own private virtual memory space.

Simple Memory Management

- In a multiprogramming environment, a simple memory management scheme is to divide up memory into fixed-size partitions

* Disconnecting

Disconnecting from distracting information and communications such as social media, mail and messaging apps. Depending on your responsibilities, it might be possible to completely disconnect for a few hours.

* Work Ritual

Establishing a work ritual that gets you in the right frame of mind for the task or activity at hand.

* Tools

Using tools that allow us to flow. For example, avoiding using clunky user interfaces that force us through technical hurdles.

* Flow

Learning to intensely concentrate on things and be in the moment

The state machine progresses on the test clock (TCK) edge with the value of the test mode select (TMS) pin controlling the behaviour

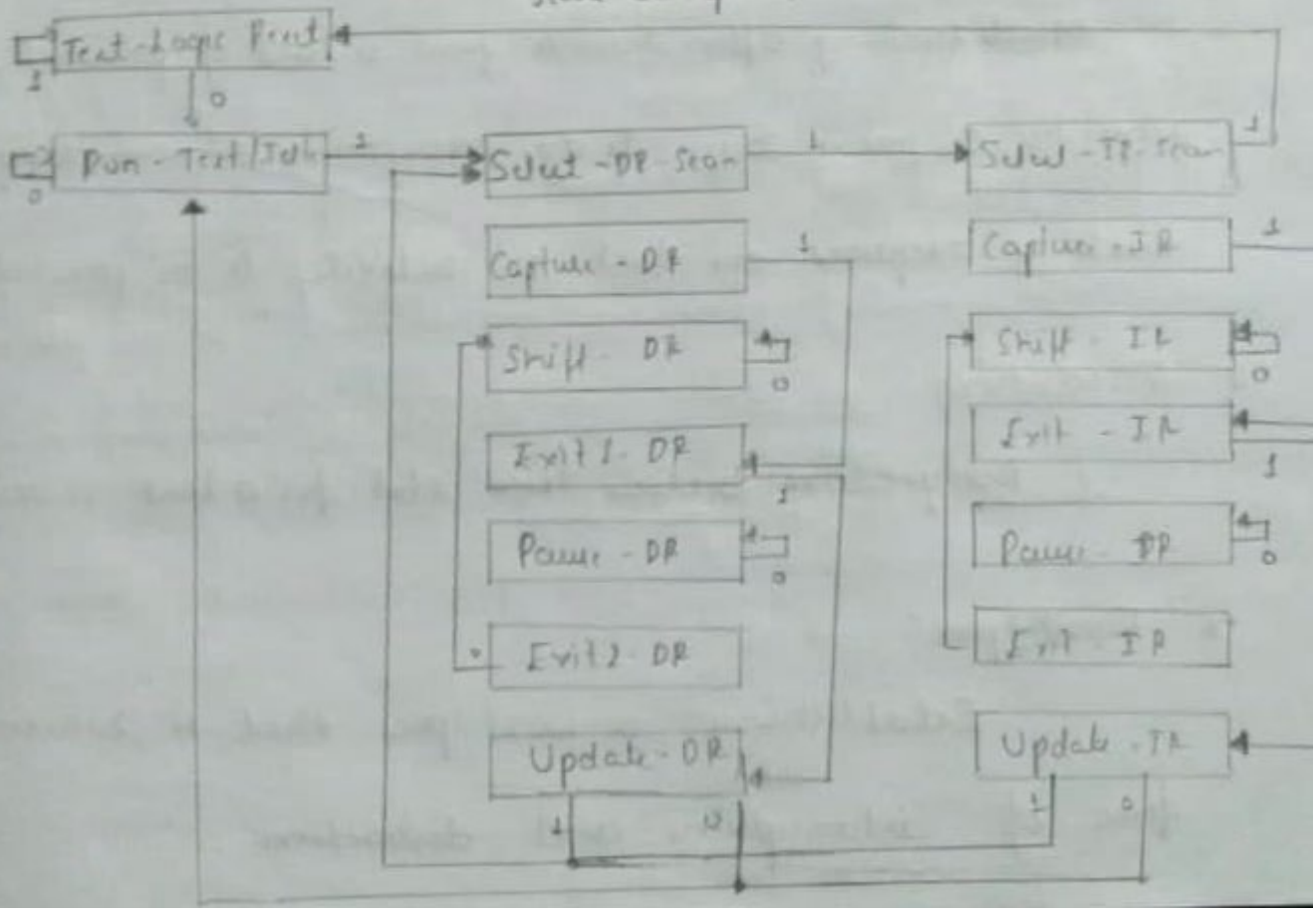
Assuming the state machine begins at Test-Logic Reset (or by applying a TMS = 0. To enter the Run Test/Idle state, then clock a TMS = 1 to begin selecting a path.

The TAP controller manages the state machine, and depending on the state selected, the output MUX is switched.

The two paths are:

* The instruction capture shift path.
* The data capture shift path

State diagram



Q What is single Tasking. Give example of single Tasking application

Monotasking. also known as single-tasking is the practice of dedicating oneself to a given task and maximizing potential interruption until the task is completed or a significant period of time has elapsed

Example of single Tasking application

* Meeting Management

Managing meetings to address one issue at a time as opposed to talking about so issues concurrently

* Prioritization

Multitasking often results from a lack of prioritization whereby a person tries to do everything at once single tasking requires one task or activity to be prioritized

* Scheduling:

Designating a clear time slot for a task or activity

* Work space:

Establishing a workspace that is reasonably free of interruptions and distraction

Explanation of the features

T- Thumb Instruction set

ARM Processors support both the 32 bit ARM Instruction set and 16 bit thumb Instruction set. The original 32 bit ARM instructions consist of 32 bit opcodes which have to be aligned to 4 byte binary pattern. Thumb Instructions consists of 16 bit opcodes or 2 byte binary pattern to improve the code density

D- JTAG Debug

JTAG is a serial protocol used by ARM to transfer the debug information between the processor and the test equipment

M- Fast Multiplier

older ARM Processor used a small and simple multiplier unit This multiplier unit required more clock cycles to complete a single multiplication

E- Enhanced Instructions

ARM Processors with this mode will support the extended DSP Instruction set for high performance DSP applications

J- Jazelle

ARM Processor with Jazelle Technology can be used in accelerated execution of Java bytecode

- Undefined mode is entered when an undefined instruction is executed

Modes other than User mode are collectively known as privileged modes. Privileged modes are used to handle interrupt or exception or to access protected resources

④ Explain the ARM Nomenclature

The letters or words after "ARM" are used to indicate the features of a processor

* X → family
* Y → Memory Management / Protection unit
* Z → Cache
* T → 16 bit thumb decoder
* D → JTAG Debugger
* M → Fast Multiplier
* I → Embedded In-circuit Emulator (ICE) Macrocell.
* E → Enhanced Instruction for DSP (Common TDMI)
* J → Jazelle
* F → Vector floating-point Unit
* S → Synthesizable Version

F-> Vector floating point unit

The floating Point Architecture in ARM Processor provides execution of floating point arithmetic Operations

S-> Synthesizable

ARM processor core is available as source code. The software core can be compiled into a format that can be easily understood by the EDA Tools

(10) What is JTAG, explain the JTAG state diagram

JTAG: It is an industry standard for verifying designs and testing printed circuit boards after manufacture

JTAG implements standard for on-chip instrumentation in electronic design automation.

JTAG state Machine

The state machine is simple, comprising two paths

* The data register path, used for loading instructions
* The instruction register (IR) path, used for reading/writing data from/to data register, including the boundary scan register (BSR)

* If the result is negative and N=0 if it is positive or zero

Z:

- Is set to 1 if the result of the instruction is zero and to 0 otherwise
- This often indicates an equal result from a comparison

C

- Is set in one of four ways

-> For an addition, including the comparison instruction CMN, C is set to 1 if the addition produced a carry and to 0 otherwise

-> For a subtraction, including the comparison instruction CMP, C is set to 0 if the subtraction produced a borrow, and to 1 otherwise

-> For non-addition/subtractions that incorporate a shift operation, C is set to the last bit shifted out of the value by the shifter

-> For other non-addition/subtractions, C is normally left unchanged

V

- It is set if two msb

-> For an addition or subtraction, V is set to 1 if signed overflow occurred. Suppose the operands and result are two's complement signed integers

-> For non addition/subtraction, V is normally left unaffected

I-Interrupt bit

I

-> Disable IRQ interrupts when it is set

F

-> Disable FIQ interrupt when it is set

T-thumb mode bit

T

-> Thumb mode

Mode bits

m[4:0]	Mode	Accessible registers
10000	usr	PC, R14 to R0, CPSR
10001	FIQ	PC, R14_fiq to R8_fiq, R7 to R0
10010	IRQ	PC, R14_irq, R13_irq, R12 to R0
10011	Supervisor	PC, R14_svc, R13_svc, R12 to R0
10111	Abort	PC, R14_abt, R13_abt, R12 to R0
11011	Undefined	PC, R14_und, R13_und, R12 to R0
11111	System	PC, R14 to R0, CPSR

Q Explain the seven different modes of ARM

Seven modes are:

Mode	Mode identifier
* User	usr
* FIQ	fiq
* IRQ	irq
* Supervisor	svc
* Abort	abt
* Undefined	und
* System	sys

The ARM7 processor has seven modes of operation.

* user mode is the usual ARM program execution state, and is used for executing application programs

* Fast interrupt (FIQ) mode supports a data transfer or channel process

* Interrupt (IRQ) mode is used for general-purpose interrupt handling

* Supervisor mode is a protected mode for the operating system

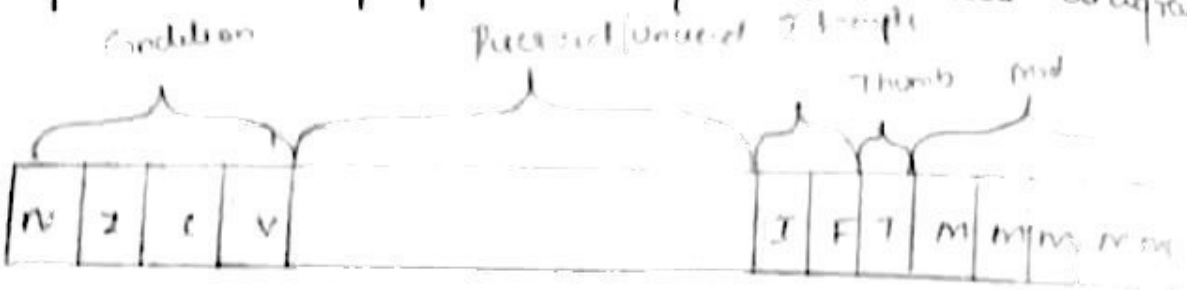
* Abort mode is entered after a data or instruction Prefetch Abort

* System mode is a privileged user mode [illegible]

ARM pipeline characteristics

- The ARM pipeline doesn't process an instruction until it has passed completely through the execution stage.
- In the execution stage the PC always points to the instruction address + 8 bytes
- When the processor is in thumb state PC always points to the instruction address + 4 byte
- Whit executing branch instruction or branching by doing modification of PC causes the ARM core to flush it's pipeline.
- An instruction in the execution stage will complete its execution even though an interrupt has been raised

(7) Explain current program status register with neat diagram



The status register bits

N:

- It set to bit 31 of the result of the instruction
- If this result is regarded as a two's complement signed integer, then N=1

36 With a neat diagram explain the concept of arbitration in I2C

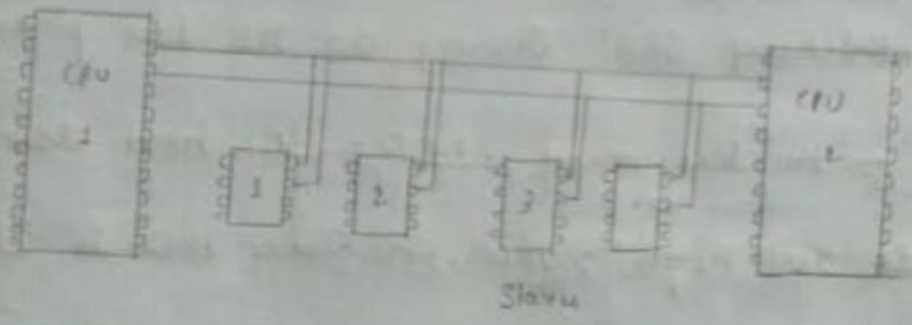
I2C Bus arbitration

- I2C is designed for multimaster purpose this means that more than one device can initiate transfer

- Bus arbitration occurs when two or more masters start a transfer at the same time

- The I2C bus was originally developed as a multimaster bus. This means that more than one device initiating transfer can be active in the system.

- When using only one master on the bus there is no risk of corrupted data, except if a slave device is malfunctioning or if there is a fault condition involving the SDA/SCL bus



When MCU1 issues a start condition and sends out address all slaves will listen. If the address does not match the

Pull-up resistor

A pull up resistor is used to establish an additional logic over the critical components while making sure that the voltage is well defined even when the switch is open. It is used to ensure that a wire is pulled to a high logic level in the absence of an input signal. Pull up resistor with a fixed value was used to connect the voltage supply and a particular pin in the digital logic circuit.

Pull down resistor. It used to ensure that input to logic system will be at expected logic level when external devices are disconnected or of high impedance. It ensures that the wire is at a defined low logic level when there are no active connections with other devices. The pull-down resistor holds the logic signal may be zero volts when no other active device is connected

address of that device has to hold back any activity using the bus becomes idle again after a stop condition.

As long as the two wires monitor what is going on the bus and as long as they are aware that a transaction is going on because the last issued command was not STOP then, no problem.

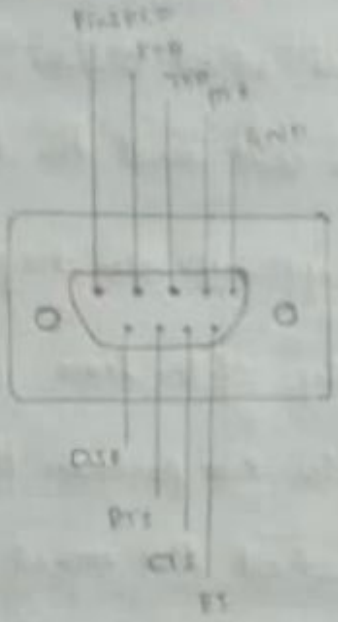
27 What is clock stretching. Explain clock stretching in I2C

clock stretching: clock stretching allows an I2C slave device to force the master device into a wait state. A slave device may perform clock stretching when it needs more time to manage data. such as store received data, or prepare to transmit another byte of data.

clock stretching in I2C: I2C devices can slow down communication by stretching SCL. During an SCL low phase, any I2C device on the bus may additionally hold down SCL to prevent it to rise high again, enabling them to slow down the SCL clock rate or to stop I2C communication for while. This is also referred to as clock synchronization

In an I²C communication the master device determines the clock speed. Unlike RS232 the I²C bus provides an explicit clock signal which subservient master and slave keep themselves exactly to a predefined baud rate.

2. Explain the working of DB9 pins and handshaking with the modem.



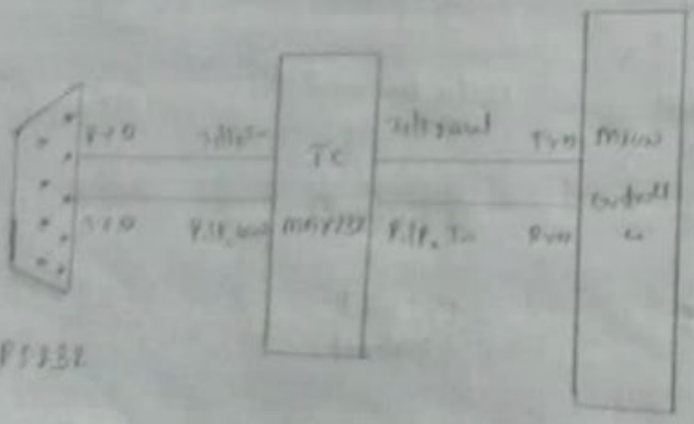
Pin	Signal	Signal name	DTE signal direction
1	DCD	Data carrier detect	In
2	RXD	Receive data	In
3.	TXD	Transmit data	Out
4	DTR	Data terminal ready	Out
5.	GND	Ground	-
6.	DSR	Data set ready	In
7.	RTS	Request to send	Out

Pin	Signal	Signal name	DTE signal direction
8	CTS	clear to send	In
9	RI	ring indicator	In

Handshaking modem

A modem handshake is what occurs when the receiving modem answers the phone call and the two modems begin to communicate. Before anything else happens, the modems must evaluate the quality of the line, negotiate error control protocols and data compression that they can both recognize, and work out what the most suitable connection speed should be, based on the conditions. This process is called as Handshake.

29. Explain the RS232 connection with a Microcontroller.



RS232

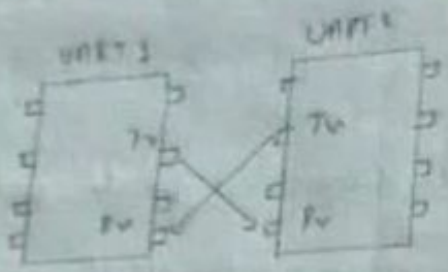
Serial devices collect data from sensors and send it to another unit like a computer for further processing. Data transfer / communication is generally done in two ways serial and parallel. In parallel mode data transfer is fast but uses more number of lines.

Serial communication on the other hand uses only one or two lines to transfer data and is generally used for long distance communication. In serial communication the data is sent as one bit at a time.

An important parameter considered while interfacing serial port is the Baud rate which is the speed at which data is transmitted serially. Microcontroller can be made to transfer and receive signal data at different baud rate using software instructions.

30 Explain the frame in UART communication

In UART communication, two UARTs communicate directly with each other. The transmitting UART converts parallel data from a controlling device like a CPU into serial form and transmits it in serial to the receiving UART. Which then converts the serial data back into parallel data for the receiving device.



UARTs transmit data asynchronously, which means there is no clock signal to synchronize the output of bits from the transmitting UART to the sampling of bits by the receiving UART.

How UART Works

The UART that is going to transmit data receives the data from a data bus. The data bus is used to send data to the UART by another device like a CPU, memory or microcontroller. Data is transferred from the data bus to the

transmitting data in parallel line

21 Explain the difference between a) serial v/s parallel
b) Analog v/s digital c) Synchronous v/s Asynchronous

Serial	Parallel
• Data is transmitted bit-after the bit in a single line	• Data is transmitted simultaneously through group of lines (wires)
• Data conversion takes place	• No. Data conversion
• Low speed transmission	• High speed transmission
• Implementation of serial links is not an easy task	• Parallel data links are easily implemented in systems.
• No. crosstalk problem	• Crosstalk occurs interference between the parallel lines.
• The Bandwidth of serial links is much higher	• The bandwidth of parallel wires is much lower

Analog	Digital
* Transmitted modulated signal is analog in nature.	* Transmitted signal is digital in form of digital pulses.
* Amplitude, frequency or phase variation in the transmitted signal represent the information or message.	* Amplitude width, or position of the transmitted pulse is constant. The message is transmitted in the form of combination
* Noise immunity is poor for AM, but improved for FM and PM.	* Noise immunity is excellent
* Coding is not possible	* Coding technique can be used to detect and correct the error.
* FDM is used for multiplexing	* TDM is used for multiplexing
* Analog modulation system are AM, FM, PM, PAM, PWM etc	* Digital modulation system are PCM, DM, ADM, DPCM etc

Synchronous	Asynchronous
* Communication in real time	* Communication is not real time
* Creates interruptions in work day	* Eliminates interruptions
* A data transfer method that sends a continuous stream of data to the receiver using regular timing signals that ensures both transmitter and receiver are synchronized with each other	* A data transfer method that sends data from transmitter to receiver with parity bits
* Sender and receiver operate on the same clock frequency	* Sender and receiver operate on different clock frequency
* Faster	* Slow
* There is no overhead of extra start and stop bit	* Uses start and stop bit
* Uses constant time interval	* Uses random or irregular time intervals
* Used in chat room and video conferencing	* Used in emails.