A CMOS Direct-Digital BPSK Modulator Using an Active Balun and Common-Gate Switches

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***Abstract* — A 0.18 μm CMOS binary phase shift keying (BPSK) modulator circuit is proposed and demonstrated that can achieve high data rates and strong carrier suppression while having low DC power consumption and a very compact layout. The modulator accepts a single-ended microwave signal (2.4 GHz) and converts it to a balanced signal using an active balun. Complementary common-gate switches are then used to select one of the two balun outputs in correspondence with the digital data to produce BPSK modulation. Excellent performance is obtained with measured phase and amplitude errors of less than 1º and 0.1 dB, respectively, and data rates up to 200 Mbps with a carrier frequency of 2.4 GHz. The insertion loss for the modulator is approximately 3 dB. Additionally, the active balun provides input matching and obtains an input reflection coefficient of -13 dB. The circuit layout area is 310 μm x 260 μm and the power consumption is 7.2 mW.**

I. INTRODUCTION

There has been considerable interest in direct-digital modulation due to the potential cost and performance benefits of using this technique, particularly in mobile communications. Binary phase shift keying (BPSK) modulation is used in several important applications such as CDMA 2000, GPS, and RFID. Common methods of achieving direct-carrier BPSK modulation include the use of reflection-type topologies [1], Gilbert-cell mixers [2], or ring-mixers [3]. Many BPSK modulators rely on passive transmission-line structures (couplers) that have a size proportional to the wavelength of the carrier. In order for these components to be a reasonable on-chip size, a relatively high carrier frequency (millimeter-wave) must be used. In CMOS technology, at these high frequencies the transmission line losses will be significant due to the low resistivity of the silicon substrate. It is for this reason that CMOS has not often been used for this application. However, there are methods of achieving BPSK modulation without using couplers such as with using an active balun to generate the 180º phase shift [4], which is more applicable to CMOS technology.

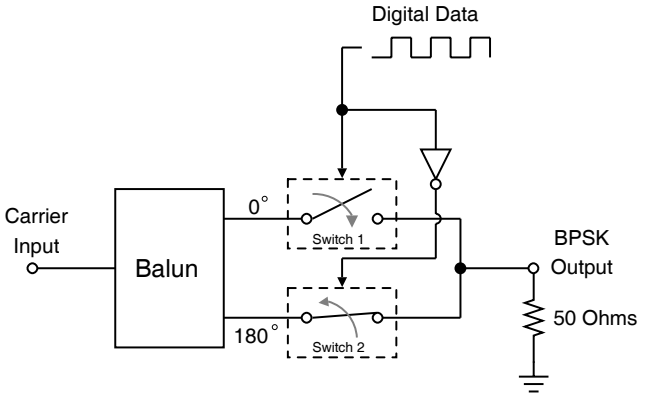

Figure 1. BPSK modulator block diagram

A block diagram of the BPSK modulator is shown in Figure 1. It consists of a balun circuit that converts the carrier from single-ended to differential and two complementary switches that are controlled by the baseband data. This method was used in [5] with a passive balun and a MEMS SPDT switch. Due to the relatively slow speed of the MEMS switch only low data rates are possible using this circuit. Similarly, in [6] this technique was used, but its data rate was limited because it was not a fully monolithic implementation. Lastly, this topology was employed in [4] with an active balun and FET switches using HEMT technology.

Many wireless communications systems have been developed using the unlicensed 2.4 GHz band. The ability to use CMOS technology at this band is particularly attractive due to its modest relative cost. Furthermore, it may be possible to realize a system-on-a-chip if the RF/microwave circuitry can be implemented with acceptable performance on CMOS along with the baseband digital processing circuitry, which could yield significant cost benefits.

In this work, a 0.18 μm CMOS direct-digital BPSK modulator is described that is suitable for mobile communications. The BPSK modulator circuit is discussed in detail in Section II, followed by the measurement results in Section III and conclusions in Section IV.

II. BPSK MODULATOR CIRCUIT

In order to generate the differential outputs shown for the balun in Figure 1, an active balun circuit was used. This allows for a very compact layout compared to passive techniques, especially for applications at low microwave frequencies. To implement the switches, two common-gate FETs were used along with an inverter to generate the complementary control voltages. The proposed BPSK modulator circuit is shown in Figure 2. Compared to the circuit in [4], CMOS technology is used in this design, along with simplified FET switches and a modified active balun circuit, which significantly reduces the required chip area. The active balun and common-gate switches will each be discussed in detail in the following sections.

A. Active Balun

There are several techniques that have been used to implement an active balun. The most basic active balun consists of a single FET with resistors in the source and drain [7]. The output at the drain will be 180º out of phase with the output at the source, and if appropriately designed, the amplitudes can be made equal. This simple topology has serious high-frequency limitations as the parasitic capacitances in the device can severely degrade the amplitude and phase balance. Another common balun circuit topology is a differential pair. Improved high-frequency performance can be obtained with this circuit; however, since the input is to the gate of a FET which is predominately capacitive, a matching network would likely be required to provide an acceptable input reflection coefficient.

An active balun that has improved performance over the single-FET balun, and can also potentially provide input matching is the common-gate, common-source pair, consisting of transistors M1 and M2 in Figure 2 [8]. The output from the common-source device provides the 180º phase shift and an appropriate design can yield equal amplitudes. Since the input to the common-source device is a high impedance, the active balun's input impedance will be approximately that of the common-gate device (the resistor R_b is large). The input impedance to the common-gate device is approximately $1/g_m$, and therefore input matching can be obtained by biasing and device sizing with this goal in mind. A basic design procedure is to first design the common gate device to provide a 50 Ω input impedance and the desired gain, and second, to design the common-source device to have equal gain to the common-gate device. A 50 Ω system impedance was chosen in this design for measurement purposes, however, the circuit could easily be modified for higher system impedances that may be used in an on-chip RF system to minimize power consumption.

In order to isolate the balun outputs from the switches, source-follower buffers were used, as shown in Figure 2. This provides a high input impedance so that the effect on the balun is very small and also provides a relatively low loss. The gate bias voltages for the source-followers are set using a resistive voltage divider (not shown in Figure 2).

B. Common-Gate Switches

To implement the switches, a common-gate topology was used along with an inverter to provide complementary gate control voltages. When the data is a logic 1 the voltage on the gate of M5 is high, thus providing a relatively low impedance path to the output 50 Ω load. Meanwhile, an inverter creates the opposite level for the gate of M6, which turns off M6 and creates a high-impedance block to the output since the gate voltage is below the threshold.

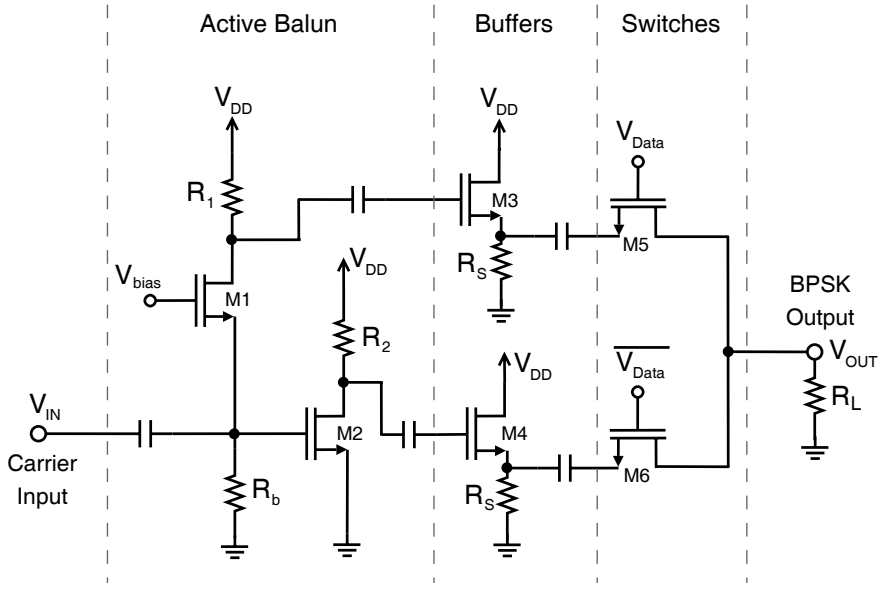

Figure 2. CMOS BPSK modulator circuit

Therefore, the 0º signal is essentially connected to the load during a bit '1' and during a bit '0' the opposite occurs with the 180º signal being connected to the load because M6 is on and M5 is off, thus achieving BPSK modulation.

III. MEASUREMENTS

To measure the performance of the CMOS BPSK modulator, coplanar waveguide (CPW) probes were used. The first measurements performed were with the network analyzer while the common-gate switches were toggled in the on/off states. The input reflection coefficient was measured from 1.5 to 4 GHz and is shown in Figure 3. The common-gate device in the active balun is providing relatively wideband input matching with an S_{11} better than approximately -10 dB from 1.5 to 4 GHz. At the intended operational frequency of the BPSK modulator of 2.4 GHz in particular, the input reflection coefficient is -13 dB. Also shown in Figure 3 is the loss through the circuit, or S_{21}, in one of the two possible states. From this figure, the insertion loss is approximately 3 dB at 2.4 GHz.

To determine the amplitude and phase balance, the difference in magnitude and phase of S_{21} was measured while the data signal was held constant at the two DC voltages corresponding to binary 0 and 1. The results are shown in Figure 4. The variation in amplitude is less than 1 dB from 1.5 to 4 GHz, and at the desired carrier frequency of 2.4 GHz it is approximately 0.1 dB. The phase difference is within 5º of the ideal 180º from 1.5 – 4 GHz and at 2.4 GHz there is less than 1º of phase balance. The active balun is clearly functioning very accurately at the desired carrier frequency, with approximately 0.1 dB and 1º of amplitude and phase balance, respectively, and it is therefore expected that the BPSK modulator will have very high carrier suppression.

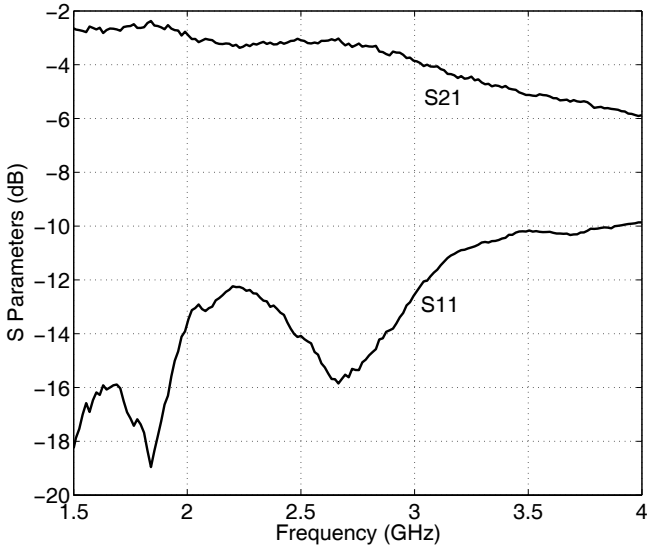

Figure 3. Measured input return loss and insertion loss

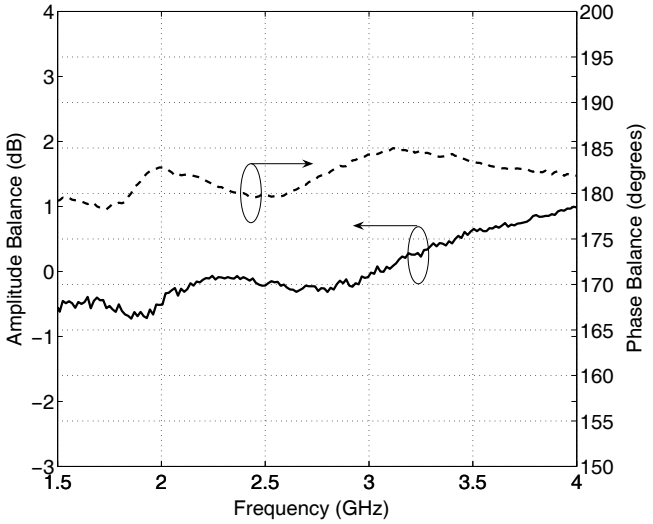

Figure 4. Measured amplitude and phase balance

Shown in Figure 5 is the output power spectrum of the BPSK modulator (relative to the highest sideband) with an input carrier of -12 dBm at 2.4 GHz, and a square wave data signal at 100 MHz (a data rate of 200 Mbps). The carrier suppression is very good at approximately -30 dB and the spectrum is very close to the ideal BPSK spectrum for a square wave modulation signal up to 100 MHz. There was no significant degradation in the quality of the BPSK spectrum shown in simulations using a non-ideal 50 Ω load, or when using large loads that may be present in circuits with a high system impedance.

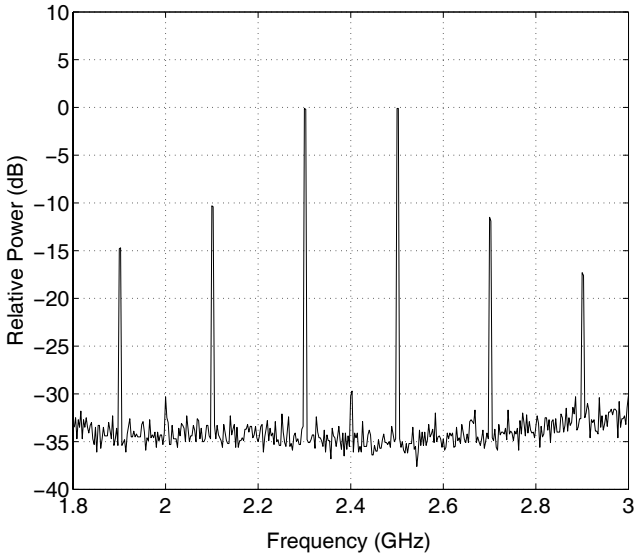

Figure 5. Measured spectrum with a 100 MHz square wave (200 Mbps) modulation signal (relative to the highest sideband power)

The power consumption of the modulator circuit is 7.2 mW (1.8 V x 4.0 mA), which makes this modulator suitable for battery powered mobile communications devices. This power measurement was made while the circuit was operating with a -12 dBm input at 2.4 GHz and a 200 Mbps data signal. Since there is no quiescent DC current flowing through the switches M5 and M6 regardless of whether they are in the "on" or "off" state, the DC power consumption of this modulator circuit is independent of the data rate. The circuit layout area is 310 µm x 260 µm (420 µm x 420 µm including pads). A photograph of the fabricated chip is shown in Figure 6.

IV. Conclusion

A CMOS 0.18 µm direct-digital BPSK modulator has been designed, fabricated, and experimentally verified. The circuit has low power consumption and doesn't require a large chip area compared to BPSK modulators that use passive couplers. An active balun was used that provides an input reflection coefficient of better than -10 dB from 1.5 to 4 GHz. The performance of the active balun is outstanding at 2.4 GHz with measured amplitude and phase balances of 0.1 dB and 1°, respectively. The BPSK modulator has excellent performance at data rates up to 200 Mbps and a carrier suppression of -30 dB. The insertion loss of the modulator is approximately 3 dB. This circuit could be used in a low-cost system-on-a-chip wireless communication device operating in the unlicensed 2.4 GHz band.

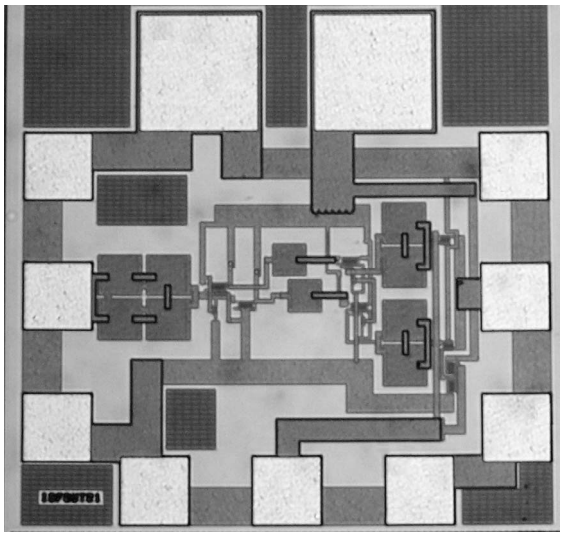

Figure 6. CMOS BPSK modulator chip photo

References

[1] H.-Y. Chang, P.-S. Wu, T.-W. Huang, Y.-C. Tsai, and C.-H. Chen, "An Ultra Compact and Broadband 15-75 GHz BPSK Modulator Using 0.13-um CMOS Process," *IEEE MTT-S International Microwave Symposium Digest*, pp. 41-44, June 12-17, 2005.

[2] B. Gilbert, "A Precise Four-Quadrant Multiplier with Subnanosecond Response," *IEEE Journal of Solid-State Circuits*, Vol. 3, Issue 4, Dec. 1968, pp. 365 – 373.

[3] A. Teetzel, "A stable 250 to 4000 MHz GaAs IQ modulator IC," *IEEE International Solid-State Circuits Conference Digest*, pp. 364-365, 1997.

[4] T. Tokumitsu, A. Oya, B. Piernas, K. Sakai, and Y. Hasegawa, "A K-band bi-phase modulator MMIC for UWB application," *IEEE Microwave and Wireless Components Letters*, Vol. 15, Issue 3, March 2005, pp. 159 - 161 .

[5] B. R. Jackson and C. E. Saavedra, "2.4 GHz Direct-Digital Binary Phase Shift Keying Modulator using a MEMS Switch," *IEE Electronics Letters*, Vol. 40, No. 24, pp. 1539-1540, Nov. 2004.

[6] C. E. Saavedra and Y. Zheng, "A BPSK Modulator using a Ring Hybrid and HFET Switches," *Asia-Pacific Microwave Conference*, pp. 1665-1668, Yokohama, Japan, December 2006.

[7] M. Goldfarb, J. B. Cole, and A. Platzker, "A Novel MMIC Biphase Modulator with Variable Gain using Enhancement-Mode FETs Suitable for 3 V Wireless Applications," *IEEE Microwave and Millimeter-Wave Monolithic Circuits Symposium*, 1994, pp. 99 – 102.

[8] L. M. Devlin, B.J. Buck, J.C. Clifton, A.W. Dearn, and A.P.O. Long, "A 2.4 GHz Single Chip Tranceiver," *IEEE Microwave and Millimeter-Wave Monolithic Circuits Symposium*, June 1993, pp. 23 – 26.

[9] Y. Sun and A.P. Freundorfer, "A New Overlay Coupler for Direct Digital Modulator in GaAs HBT*," IEEE Transactions on Microwave Theory and Techniques*, Vol. 52, No. 8, pp. 1830-1835, August 2004.