School of Computing
Computer Science Program

CDA 3101

Introduction to Computer Logic

Lab # 3

Student Name			
Lab Name	**Lab 3: Universal Gates**		
Lab Checklist	**Available Points**	**Received Points**	**Information**
Printed Schematic	20		See note 7 below
Documents	10		Truth table and the reduced SOP and POS functions.
Documents	10		All work necessary to reduce the function.
Documents	10		All work necessary to implement using universal gates
Documents	10		Proof that your designed circuit will provide the same results as the given function.
Proper operation of the built circuit	40		
Circuit Demo (worked correctly)	Yes / No		Must fully function to receive a grade above zero. Note 1 below
Date:			
Verified by:			
Final Lab Grade			

Notes for Scoring:

Note 1: A final grade of "0" will be assigned if the circuit demonstration fails to work completely.

Note 2: Lab assignments will not be accepted late.

Note 3: Any assigned quizzes that are associated with this lab will be taken on Canvas unless otherwise noted.

Note 4: All submitted documents from CAD software (ex: Multisim) must contain the student's name and UNF n-number printed via the software (insert text). No name and number; no points!!!!

Note 5: No "print screens" will be accepted from CAD software. Print all documents using the print function within the software.

Note 6: The entire lab assignment must be printed and submitted with any other required documents.

Note 7: *A wiring diagram (schematic) must reflect what is actually built on your hardware trainer. All chip pin numbers, switches, lights, and etc. must be labeled. All input and output signals must be labeled as well as all input and output bit-weights. Do not include any equipment or components that are not used with your lab (ex: logic analyzer).*

Note 8: The lab must be demonstrated and submitted to either a lab TA or the instructor during a scheduled lab session. Labs will not be graded outside of this time unless authorized by the instructor.

Lab 3: Universal Gates

The purpose of this lab is to help the student become familiar with the concept of universal (NAND / NOR) gates.

Equipment needed:

Chips: NAND gates
Logic Trainer
CAD Software

Pre-lab:

A) Create a truth table and the resulting Minterm and Maxterm Expansions of the function given below.

B) Reduce the function using any method covered in class.

C) Design a circuit that will implement the reduced function using only NAND gates using the procedure demonstrated in class.

D) Show all work on paper and attach with this document with grading.

$$F(wxyz) = \sum m(0,1,2,3,4,5,7,14,15)$$

E) Use CAD software to create wiring schematics for this lab.

F) Print the schematics for use when building your circuits. The printed schematics must also be attached to this document for final grading.

Note: *Your prelab material should be complete prior to the lab session!*

Using the Hardware Trainer:

A) Implement the designed circuit using only NAND gates. Use the previously derived truth table to prove that your circuit is working correctly. Note that only the reduced NAND circuit needs to be constructed.

Grading:

A) Submit the following for lab validation in class:

a. The reduced SOP and POS functions.
b. All work necessary to reduce the function.
c. All work necessary to implement using universal gates using the procedure demonstrated in class.
d. The printed wiring diagram.
e. Proof that your designed circuit will provide the same results as the given function.

B) Be prepared to demonstrate your working project in class. You must provide all printed materials at the time of inspection or the lab will not be graded.