School of Computing
Computer Science Program

CDA 3101

Introduction to Computer Logic

Assignment 7 - C

Rubric

Student Name			
Assignment Name	**Assignment 7 - Part C : Sequential State Machines Analysis and Design**		
Assignment Checklist	**Maximum Available Points**	**Received Points**	**Information**
Waveform of State Machine using JK-FF	20		Waveform via Multisim Grapher View. Must compare to state table.
Logic Diagram of State Machine using JK-FF	30		Inputs and outputs clearly marked. Use clock with logic analyzer to prove proper operation. Use push-button for Reset
New State Table	20		Correctly populated state table
State Diagram	10		Diagram reflecting state table
Other Documents	20		K-Maps and resultant functions. All other work.
Final Assignment Grade	**Total =**		

Notes for Scoring:

Note 1: A final grade of "0" will be assigned if the circuit demonstration fails to work completely.

Note 2: Assignments will not be accepted late.

Note 3: Any assigned quizzes that are associated with this assignment will be taken on Bb unless otherwise noted.

Note 4: All submitted documents from MultiSim must contain the student's name and UNF n-number printed via the software (insert text). No name and number; no points!!!!

Note 5: No "print screens" will be accepted from Multisim. Print all documents using the print function within the software.

Assignment 7: Sequential State Machines
Analysis and Design
Part - C

The purpose of this assignment is to give the student experience in analysis and design of a Mealy State Machines using JK Flip-Flops.

Equipment needed:

Various TTL Gates and Flip-Flops
Multisim Software

Objectives:

Perform the following using the state table and state diagram obtained from Lab 7 Part A.

A) Redesign the state machine using JK flip-flops. This design will require a new, or modified, state table and new functions to feed the JK inputs. Use k-maps to derive the new fully reduced functions using traditional combinational logic (ORs, ANDs, XORs, NANDs & etc.).

The new state machine must also be designed as self-correcting for any unused state. For these states, the next state must point to state zero (0 0 0 0) with the Z output equaling zero. This condition must be reflected in your new state diagram and state table for this new design.

Use the TTL clock to feed the flip-flops, but be able to use a pushbutton as an alternative clock input if needed (see diagram). Also included a Reset / Clear switch.

This design will require a new, or modified, state table. Submit a copy of the Kmaps, state table, and state diagram for grading.

B) Build this new circuit using Multisim and confirm that operation of the circuit matches your state table and state diagram. . Printout the circuit and submit a copy for grading. Also submit a copy of the Multisim circuit.

C) Observe the waveforms of your new circuit to confirm that your designs are correct. Printout and submit the accompanying waveforms for this new circuit. Label all inputs and outputs on all waveforms through the Grapher. Ensure that all inputs and outputs are properly labeled on the logic diagrams as well.