School of Computing
Computer Science Program

CDA 3101

Introduction to Computer Logic

Lab # 2

Student Name			
Lab Name	**Lab 2 : Boolean Expressions.**		
Lab Checklist	**Available Points**	**Received Points**	**Information**
Printed Schematic	40		Both circuits. See note 7 below.
Proper circuit operation	40		Both circuits must have the same output.
Required documents	20		Truth table & Printed lab. Reduction work using Boolean laws.
Circuit Demo (worked correctly)	Yes / No		Must fully function to receive a grade above zero. See note 1 below.
Date:			
Verified by:			
Final Lab Grade			

Notes for Scoring:

Note 1: A final grade of "0" will be assigned if the circuit demonstration fails to work completely.

Note 2: Lab assignments will not be accepted late.

Note 3: Any assigned quizzes that are associated with this lab will be taken on Canvas unless otherwise noted.

Note 4: All submitted documents from CAD software (ex: Multisim) must contain the student's name and UNF n-number printed via the software (insert text). No name and number; no points!!!!

Note 5: No "print screens" will be accepted from CAD software. Print all documents using the print function within the software.

Note 6: The entire lab assignment must be printed and submitted with any other required documents.

Note 7: *A wiring diagram (schematic) must reflect what is actually built on your hardware trainer. All chip pin numbers, switches, lights, and etc. must be labeled. All input and output signals must be labeled as well as all input and output bit-weights. Do not include any equipment or components that are not used with your lab (ex: logic analyzer).*

Note 8: The lab must be demonstrated and submitted to either a lab TA or the instructor during a scheduled lab session. Labs will not be graded outside of this time unless authorized by the instructor.

Lab 2: Boolean Expressions.

The purpose of this lab is to help the student to become familiar with Boolean functions, their reduction, and their implementation using TTL logic.

Equipment needed:

Chips: Various TTL Gates
Logic Trainer
CAD Software

Pre-lab:

A) Note the Boolean function given below. Use this function to create a truth table.

B) Use Boolean laws and theorems to reduce the given function. Record this new function and use it to create another truth table. The two truth tables should match if your new function is the logical equivalence of the given function. Show your work in this document.

$$F_{(a,b,c)} = \bar{a}\bar{c} + abc + a\bar{c}$$

C) These two functions will be constructed on the hardware trainer; therefore, use CAD software to create wiring schematics for both of these circuits.

D) Print the schematics for use when building your circuits. The printed schematics must also be attached to this document for final grading.

Note: *Your prelab material should be complete prior to the lab session!*

Using the Hardware Trainer:

A) Implement the original function using TTL logic. Use only AND, NAND, OR, NOR, and NOT gates. Use the previously derived truth table to prove that your circuit is working correctly.

B) Implement the reduced function using TTL logic. Use only AND, NAND, OR, NOR, and NOT gates. Again, use the derived truth table to prove that your circuit is working correctly.

C) Submit both working circuits along with the schematics and truth tables for lab validation.

Grading:

A) Be prepared to demonstrate your working project in class. Include in your submitted material all work showing the reduction of the function. You must provide all required documents at the time of inspection or the lab will not be graded.