School of Computing
Computer Science Program

CDA 3101

Introduction to Computer Logic

Lab # 9

Student Name: _____

Student N-Number: _____

Student Name			
Lab Name	**Lab 09 : Memory, Functions, and the 7 Seg Display**		
Lab Checklist	**Available Points**	**Received Points**	**Information**
Printed Schematic	30		Wiring Diagram See note 7 below
Proper operation of 7-segment circuit.	50		Letters **A b C d E F g** should be displayed.
Required documents	20		Memory Map
Circuit Demo (worked correctly)	Yes / No		Must fully function to receive a grade above zero. Note 1 below
Date:			
Verified by:			
Final Lab Grade			

Notes for Scoring:

Note 1: A final grade of "0" will be assigned if the circuit demonstration fails to work completely.

Note 2: Lab assignments will not be accepted late.

Note 3: Any assigned quizzes that are associated with this lab will be taken on Canvas unless otherwise noted.

Note 4: All submitted documents from CAD software (ex: Multisim) must contain the student's name and UNF n-number printed via the software (insert text). No name and number; no points!!!!

Note 5: No "print screens" will be accepted from CAD software. Print all documents using the print function within the software.

Note 6: The entire lab assignment must be printed and submitted with any other required documents.

Note 7: *A wiring diagram (schematic) must reflect what is actually built on your hardware trainer. All chip pin numbers, switches, lights, and etc. must be labeled. All input and output signals must be labeled as well as all input and output bit-weights. Do not include any equipment or components that are not used with your lab (ex: logic analyzer).*

Note 8: The lab must be demonstrated and submitted to either a lab TA or the instructor during a scheduled lab session. Labs will not be graded outside of this time unless authorized by the instructor.

The purpose of this lab is cover the use of a Seven-Segment Display.

Equipment needed:

7- segment display object
2016 / 6116 SRAM
74LS244 / 74LS126
Other Assorted TTL gates
Logic Trainer

Pre-lab:

Refer to your class notes on implementation of complex circuits using ROMs. A SRAM will behave in the same manner; however, the memory will have to be loaded after each power cycle of the trainer due to the volatile characteristics of this type of device.

A) Using the **2016 / 6116 SRAM**, design a circuit that displays the letters **A** through **g** on a seven-segment display. The circuit will have three inputs (X, Y, Z) which represent the last 3 bits of the ASCII code for the letter to be displayed. For example, if XYZ = 001, "A" will be shown. You are welcome to display any character or nothing for the input of "000." The letters should be displayed in the following form: **A b C d E F g** (note case). Design your circuit using the SRAM to implement the required functions for each segment. Use a seven-segment display module for the output. Connect the segments of the 7-segment display directly to the output of the SRAM.

B) Create separate memory maps for the required circuits. Use this data to populate your memories during circuit operation and/or demonstration. Include these maps with your lab for final grading.

C) Use CAD software to create wiring schematics for this lab.

D) Print the schematics for use in class and for final grading.

Note: *Your prelab material should be complete prior to the lab session!*

Using the Hardware Trainer:

Construct the circuit using the appropriate RAM chip, and any required TTL logic gates. Note that the BCD / Seven-Segment Display located on the PB-505 model trainer cannot be used for this lab. See notes at the end of this paper for additional information and tips.

Grading:

Provide your hardware circuit along with the printed memory map, logic diagrams, and lab for proof of lab completion. You must provide the printed materials at the time of inspection or the lab will not be counted as completed.

Building Notes:

A) Apply ground or high (+5Volta) to all unused address lines. Do not ground output data lines

B) Ground CS' and OE' control pins.

C) Only the required memory locations must be programmed. Any unused memory locations can be ignored.

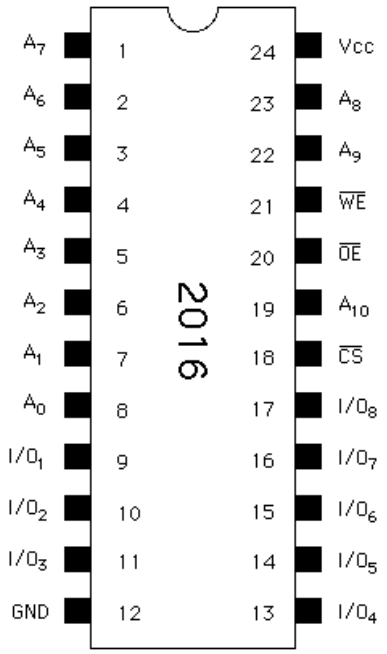
D) Use separate pushbuttons for the RD/WE' signal of each RAM. (See next page)

E) Suggested Switch Layout:

Part A (seven-segment display)
Use logic switches 1 – 3 for address lines
Use logic switches 4 – 10 for data lines
Use Push-Button for RD/WE'

F) Note that the Seven-Segment display on the trainer is only accessible through a BCD decoder; therefore, your circuit must use a separate seven-segment display module supplied in your parts kit.

G) The I/O lines of the 2016 / 6116 SRAM can be connected directly to the segments of the 7-segment display; however, a buffer can be used if the total load appears to be too great for the RAM. Only 7 I/O lines are required. The 8th output line need not be connected to anything.



Description

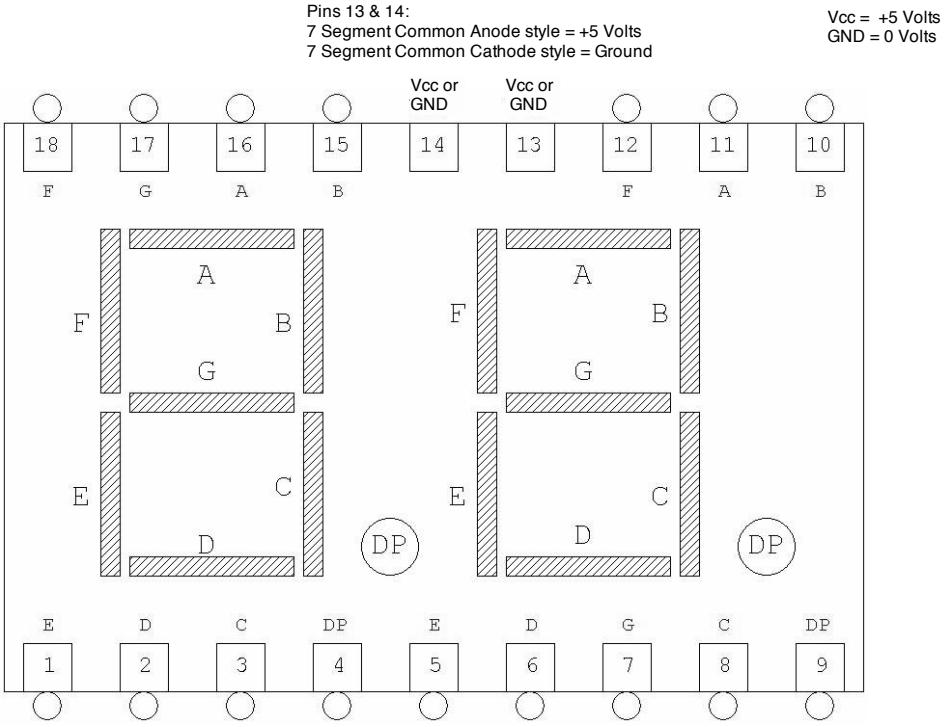
The 2016/6116 series of Static RAMs are 16,384 bit memories organized as 2,048 words by 8 bits and operates on a single +5V supply. 2016's and equivalents are generally NMOS or MOS process parts, where the 6116 and compatibles are built from CMOS technology. All provide three state outputs, are TTL compatible, and allow for direct interfacing with common system bus structures.

- **Access Time**
  - **25 to 450ns depending on part speed grade**
- **Fully TTL compatible**
- **Three-State Outputs**
- **Single Supply (Vcc = +5V +-10%)**
- **Fully Static Operation, no clock or refreshing required**
- **Current varies from 10-100mA, CMOS versions are generally lower power**
- **Standby power (deselected chip) varies from 1-100uA**

I) There are two types of 7-segment displays (Common Anode / Cathode).

a) Common Anode – This type requires +5Volts to be connected to pins 13 & 14. A low (0Volts) applied to any segment will case it to illuminate. This can be thought of as an active low device. If using this type of display, simply invert the data in your memory map, or use an inverter on the output I/O lines of the RAM.

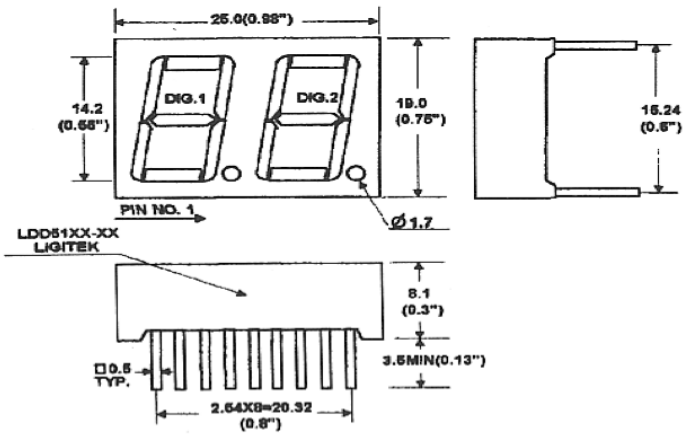
b) Common Cathode - The other type of display requires ground (0Volts) to be connected to pins 13 & 14. A high (+5Volts) applied to any segment will case it to illuminate. This can be thought of as an active high device, and is the most common display in the lab. This display should work as indicated in your notes and text.



7 Segment Display Pinouts

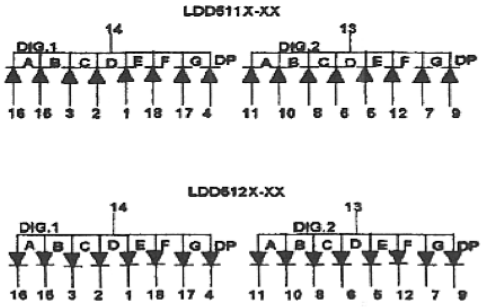
DUAL DIGIT LED DISPLAY (0.56Inch) **LDD511X/2X** *series* Page 1/2

PACKAGE DIMENSION



NOTE: All Dimension Are In Millimeters And (Inch)
Tolerance Is ±0.25(0.01") Unless Otherwise Noted

INTERNAL CIRCUIT DIAGRAM



- **Connection To Electrical Schematic**

Electrical Connection

PIN NO.	LDD511X-XX	PIN NO.	LDD512X-XX
1	Anode E Dig.1	1	Cathode E Dig.1
2	Anode D Dig.1	2	Cathode D Dig.1
3	Anode C Dig.1	3	Cathode C Dig.1
4	Andoe DP Dig.1	4	Cathode DP Dig.1
5	Anode E Dig.2	5	Cathode E Dig.2
6	Andoe D Dig.2	6	Cathode D Dig.2
7	Anode G Dig.2	7	Cathode G Dig.2
8	Anode C Dig.2	8	Cathode C Dig.2
9	Anode DP Dig.2	9	Cathode DP Dig.2
10	Anode B Dig.2	10	Cathode B Dig.2
11	Anode A Dig.2	11	Cathode A Dig.2
12	Anode F Dig.2	12	Cathode F Dig.2
13	Common Cathode Dig.2	13	Common Anode Dig.2
14	Common Cathode Dig.1	14	Common Anode Dig.1
15	Anode B Dig.1	15	Cathode B Dig.1
16	Anode A Dig.1	16	Cathode A Dig.1
17	Anode G Dig.1	17	Cathode G Dig.1
18	Anode F Dig.1	18	Cathode F Dig.1

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