

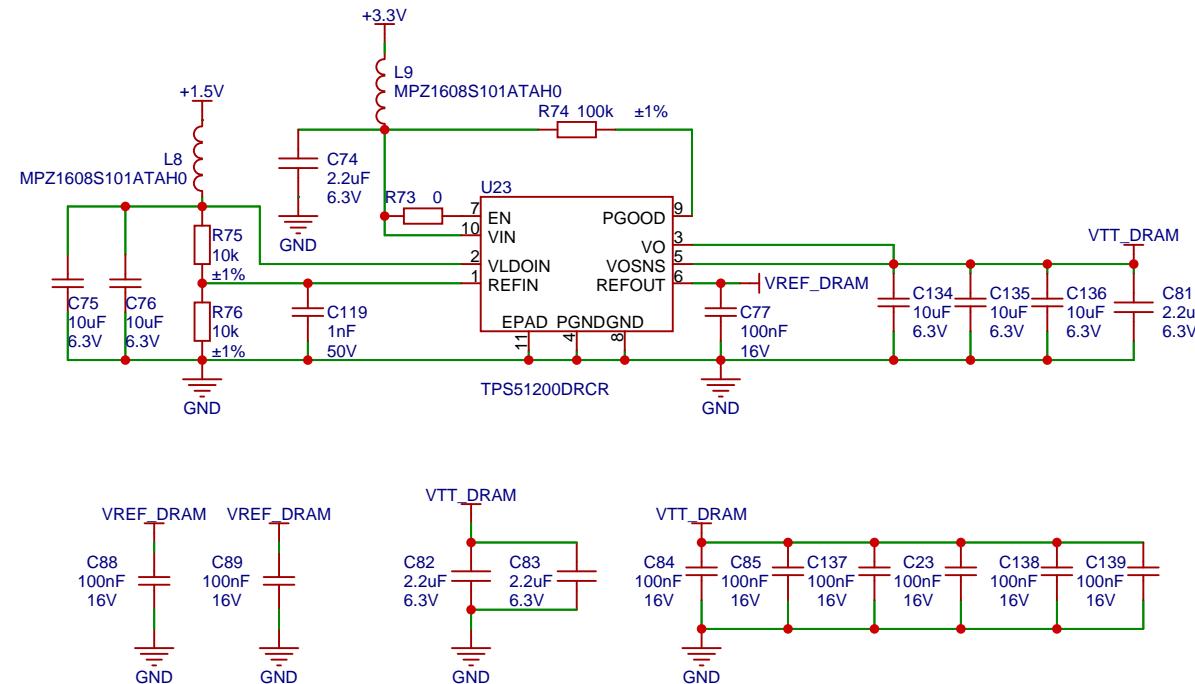
DDR3

A

8

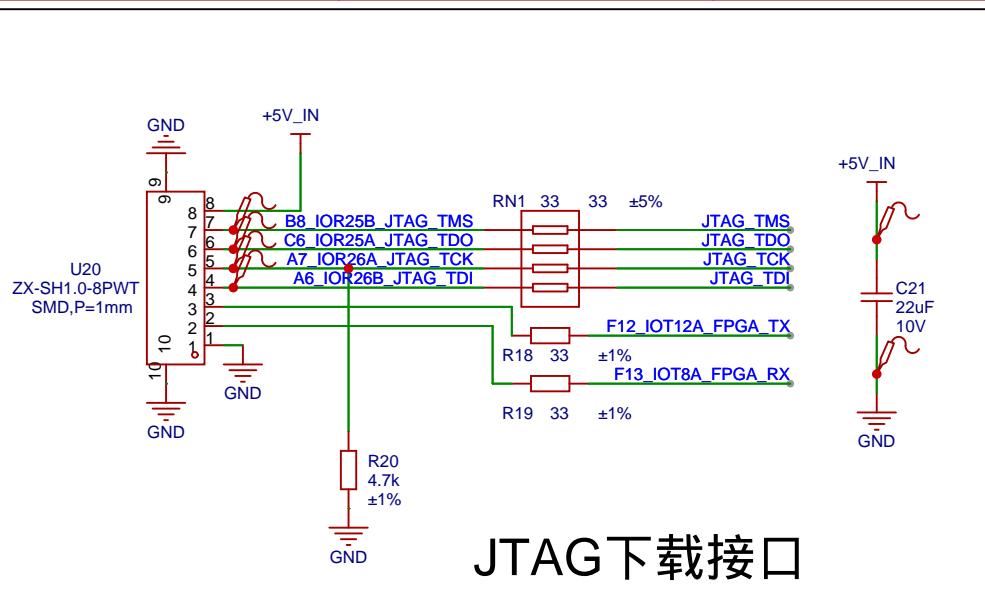
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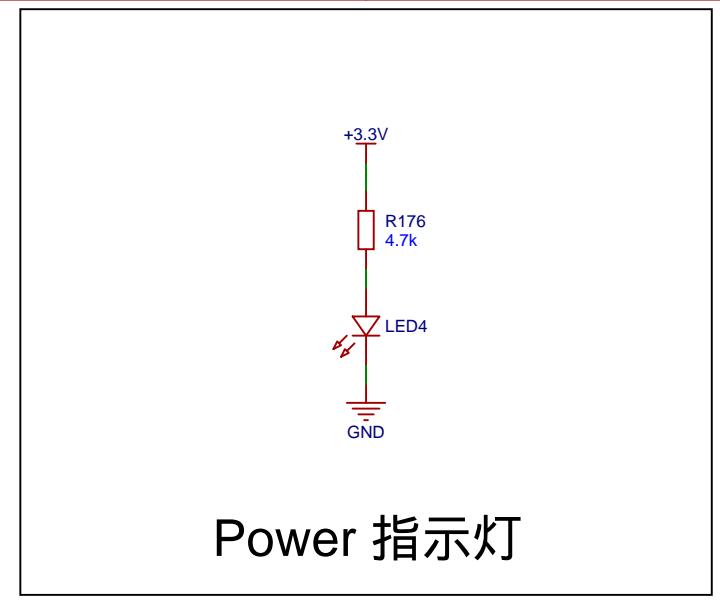


线性终端稳压器

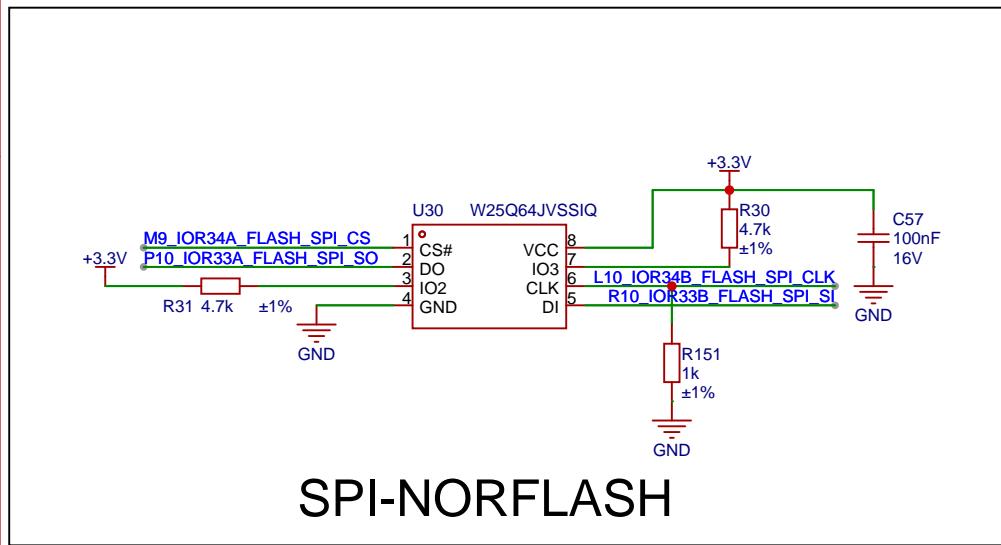
原理图	原理图	创建日期	2025-10-31
		更新日期	2025-11-01
板子	PCB3	图页	FPGA DDR3 Power
绘制			
审阅			立创逻辑派开发板
		版本	尺寸
		V1.0	A4
嘉立创EDA		页 3 共 10	
嘉立创EDA		嘉立创EDA	
3	4	5	6



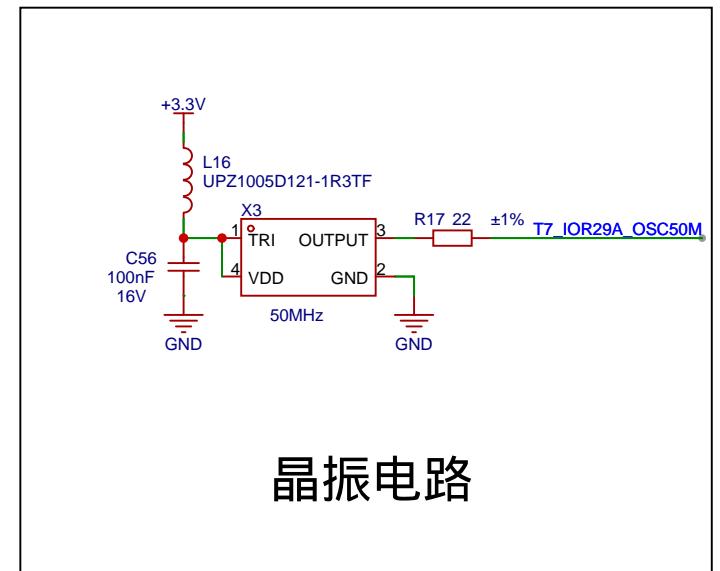
JTAG下载接口



Power 指示灯

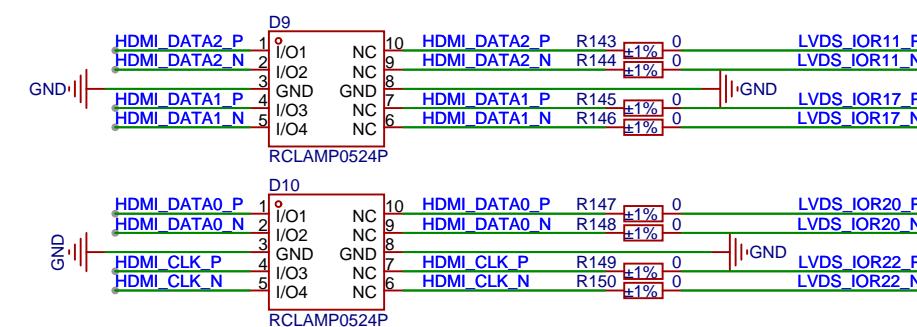
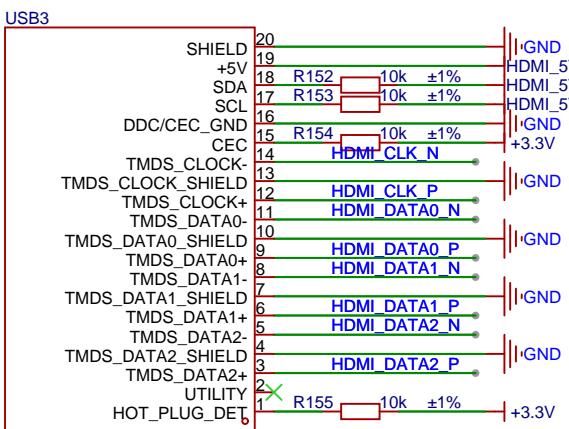
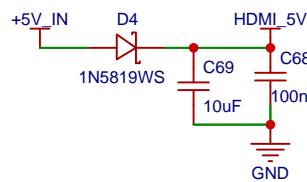


SPI-NORFLASH



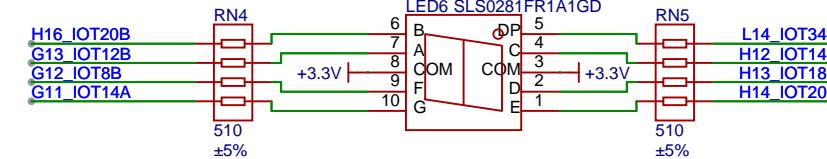
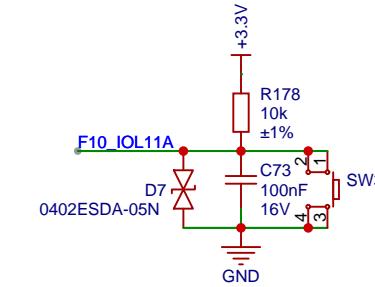
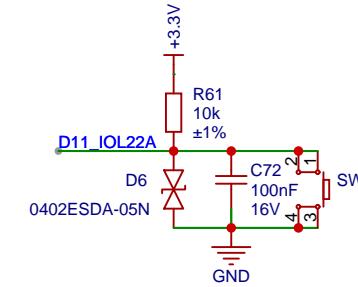
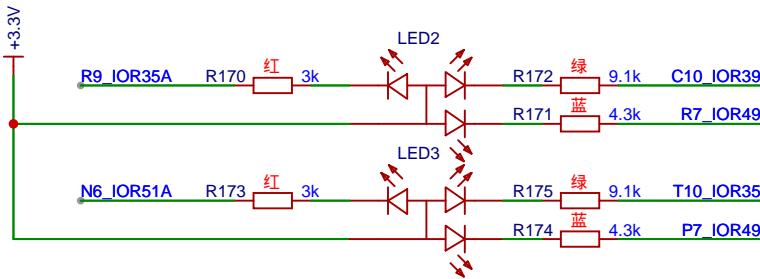
晶振电路

原理图	原理图	创建日期	2025-10-31
		更新日期	2025-11-01
板子	PCB3	图页	FPGA JTAG
绘制			
审阅			
		立创逻辑派开发板	
	版本	尺寸	页 4 共 10
 嘉立创EDA	V1.0	A4	嘉立创EDA



HDMI 接口

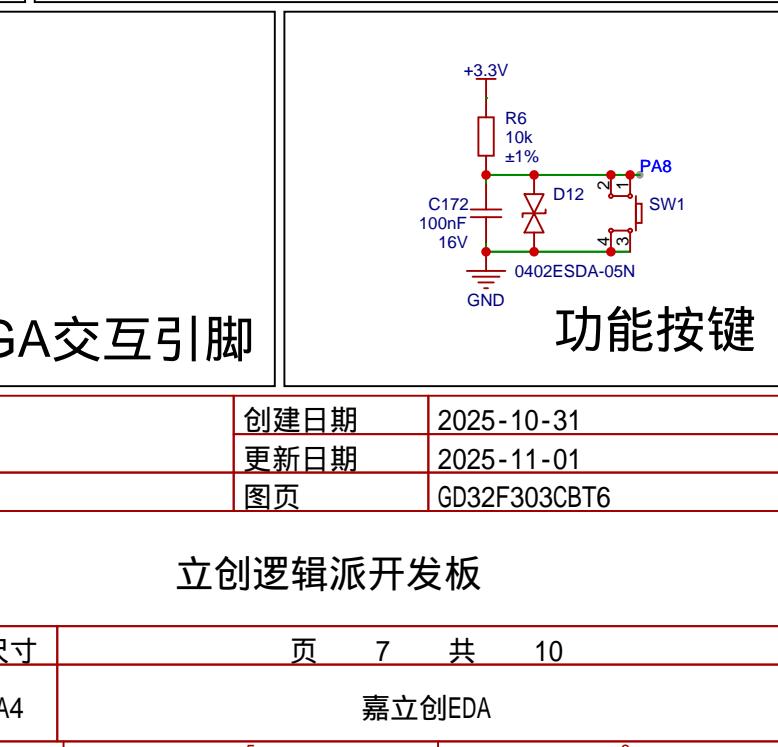
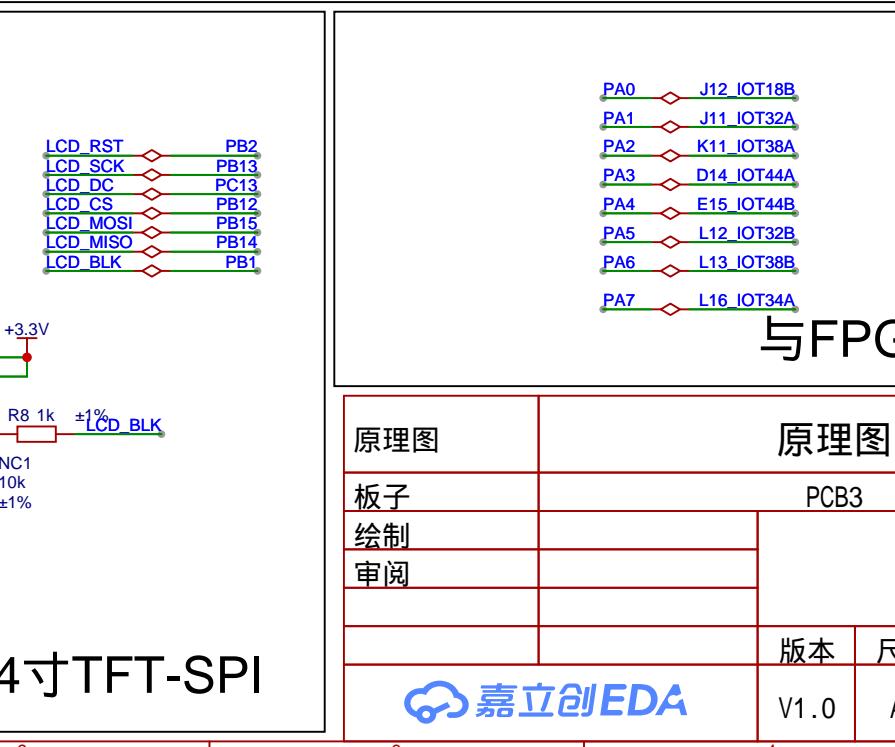
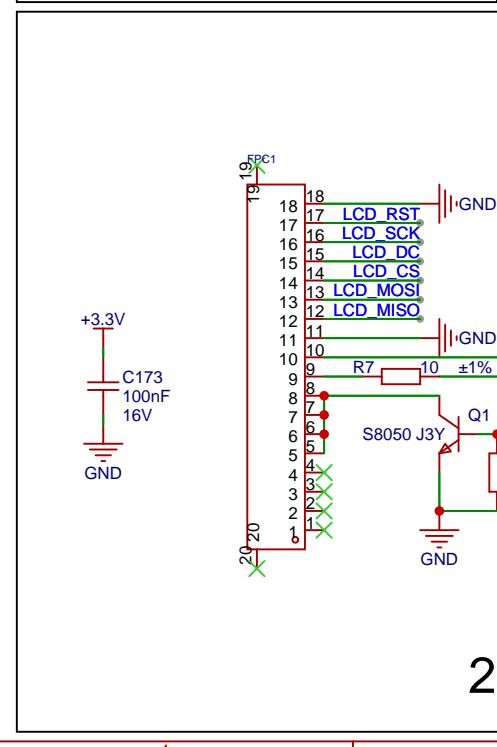
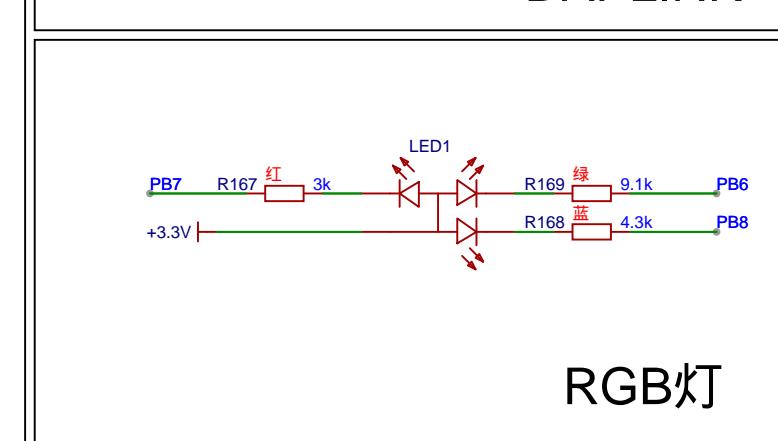
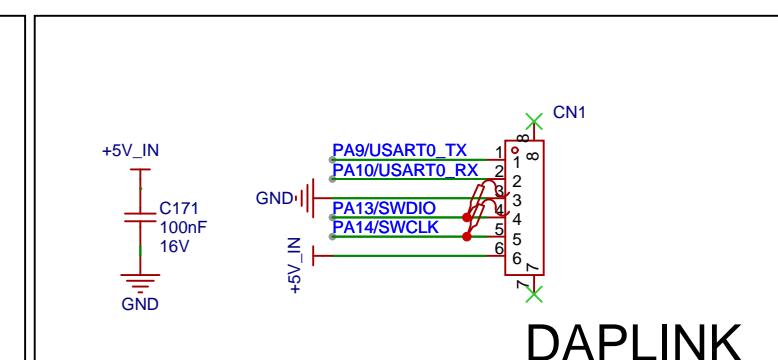
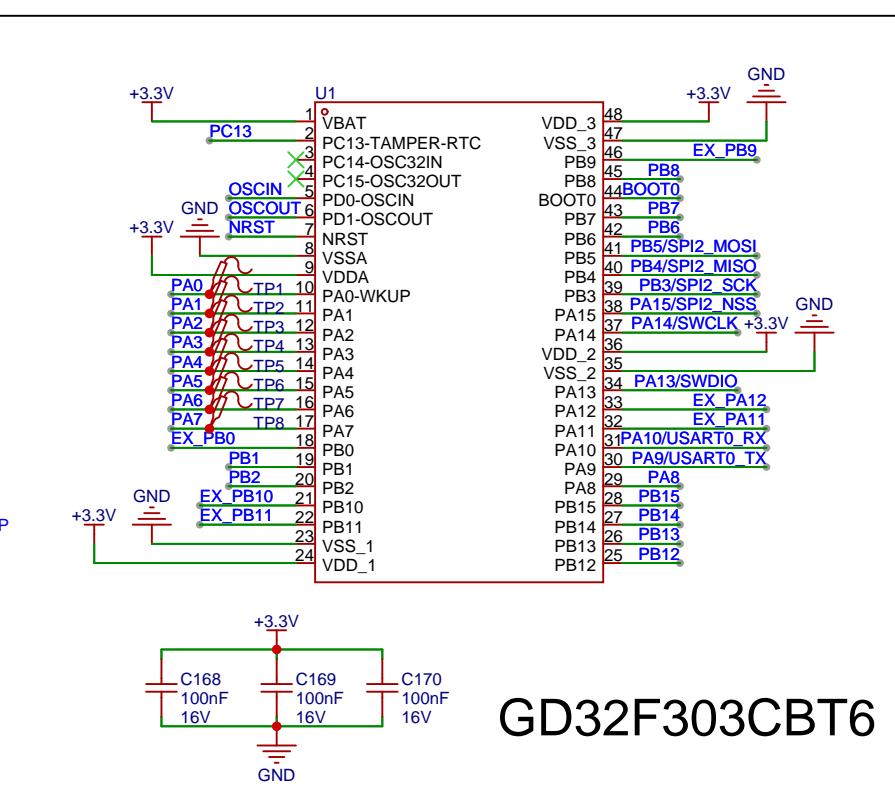
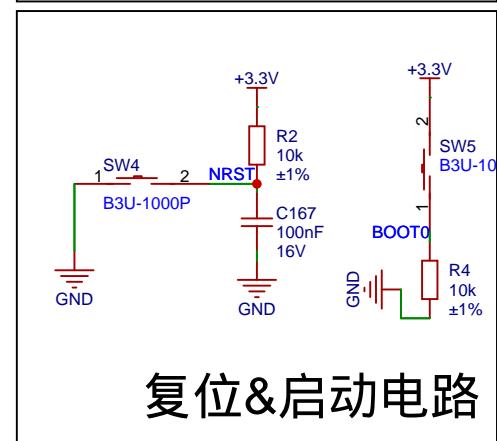
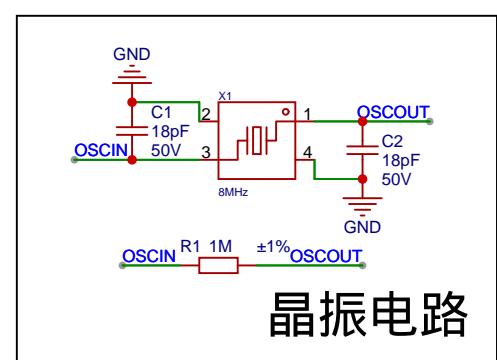
原理图	原理图			创建日期	2025-10-31
板子	PCB3			更新日期	2025-11-01
绘制	PCB3			图页	FPGA_HDMI
审阅					
				版本	尺寸
				V1.0	A4
				页 5 共 10	
嘉立创EDA			嘉立创EDA		



LED&&按键&&数码管

原理图	原理图		创建日期	2025-10-31
板子	PCB3		更新日期	2025-11-01
绘制			图页	FPGA Peripheral
审阅				
	版本	尺寸	页	6 共 10
嘉立创EDA		V1.0	A4	嘉立创EDA

立创逻辑派开发板



A

A

B

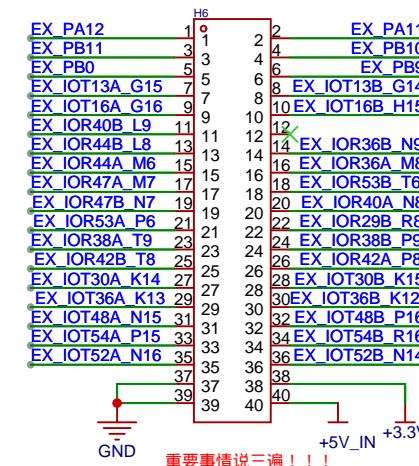
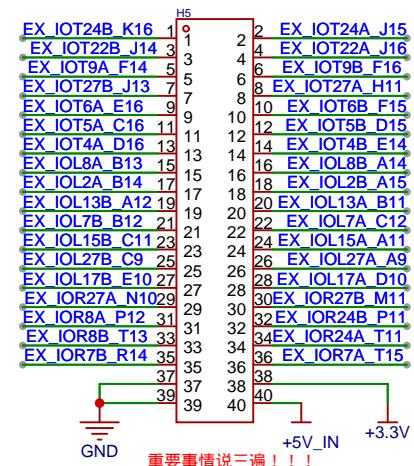
B

C

C

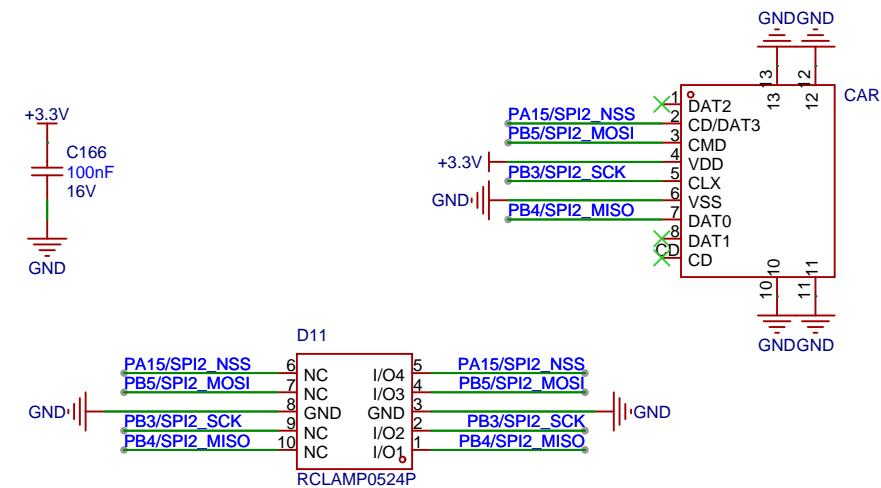
D

D

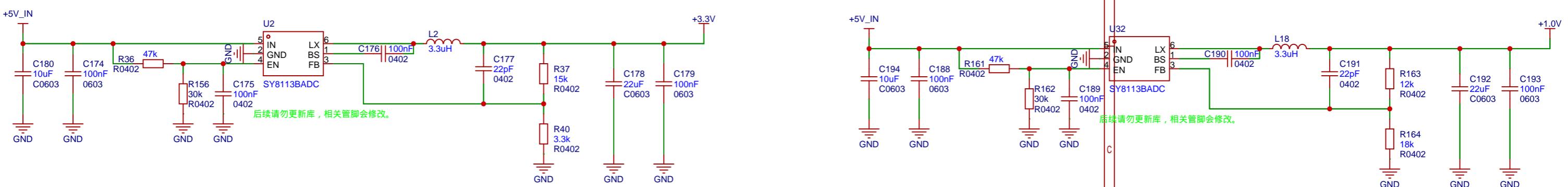
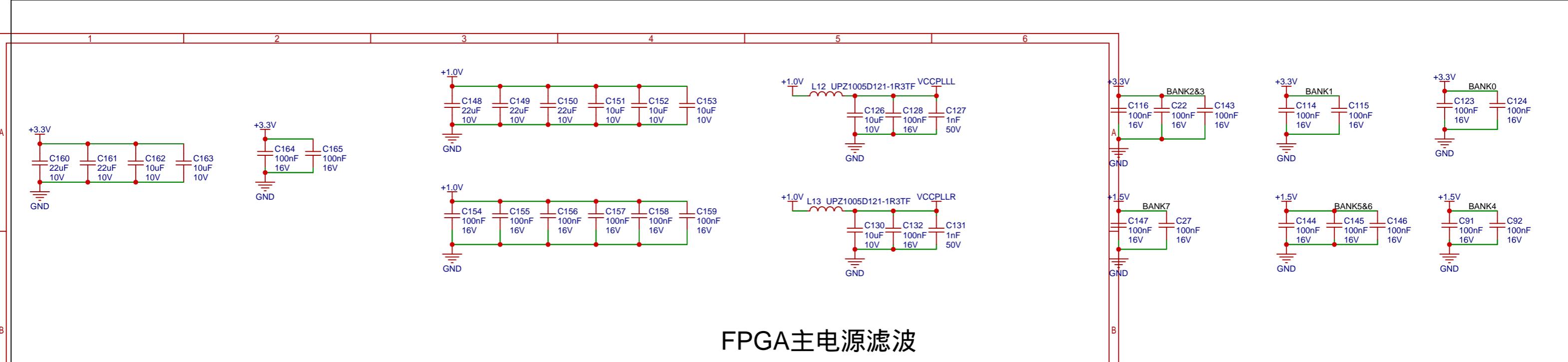
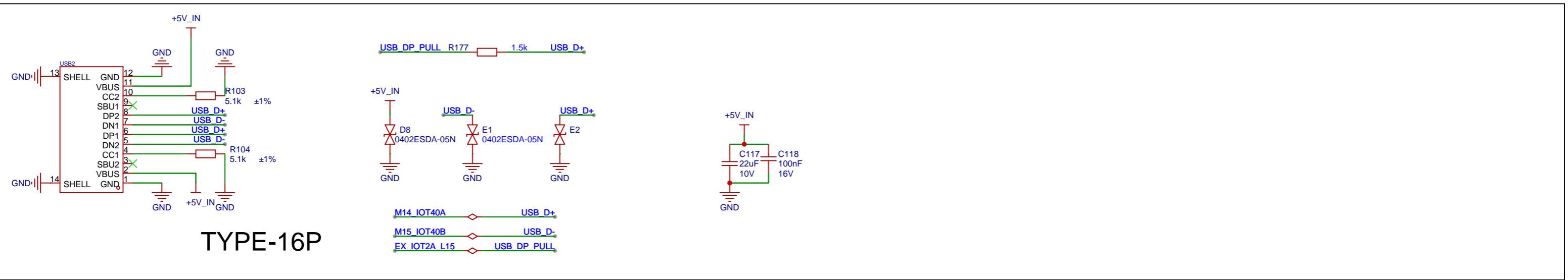


拓展排针接口

原理图	原理图		创建日期	2025-10-31
板子	PCB3		更新日期	2025-11-01
绘制			图页	Expand
审阅				
	版本	尺寸	页	8 共 10
嘉立创EDA		V1.0	A4	嘉立创EDA



原理图	原理图		创建日期	2025-10-31
板子	PCB3		更新日期	2025-11-01
绘制			图页	GD32_MicroSD
审阅				
	版本	尺寸	页	9 共 10
 嘉立创EDA		V1.0	A4	嘉立创EDA



Vout = 0.6 * (1 + R163/R164)

主控电源部分

