82562EZ(EX)/82551ER(IT) & 82541ER Combined Footprint LOM Design Guide

Application Note (AP-456)

Networking Silicon

Revision 1.7
April 2005

Revision History

Revision	Revision Date	Description
1.0	August 2003	Initial release.
1.1	April 2004	Added information for oscillator support. Updated reference schematics.
1.2	October 2004	Updated reference schematics to reflect MDI-X feature (82551ER(IT) only). Added crystal start-up information. Information includes: • New crystal parameters • Crystal selection guidelines • Crystal validation methods • Crystal testing methods Added new values for TX and RX terminations (next to LAN silicon). New values are now 110 Ω for both TX and RX terminations. Added new starting values for RBIAS100 and RBIAS10. New starting values are now 649 Ω for RBIAS100 and 619 Ω for RBIAS10. Added 82562EX applicability. Updated reference schematics to reflect new Tx and Rx termination values, new LAN disable circuit, RBIAS100/RBIAS10 values, VIO signaling connection and pullup resistor value.
1.3	November 2004	Updated pin descriptions for Ball C8 and L8.
1.4	December 2004	• Added an oscillator solution for the 82541ER. • Changed text in the Catalyst EEPROM revision H table note from “Revision H or higher not supported” to “Revision H is not supported”. • Added a 0.01 µf capacitor between Ball C2 (M66EN) and ground to meet IEEE PCI specification (sheet 3 of reference schematics). • Removed the Self-Review Checklist for Combined Footprint LOM. This checklist is now a separate Microsoft* Excel spreadsheet.
1.5	January 2005	Updated reference schematics to: • Reflect current differential pair termination resistor values for the 82541ER. • Removed 0.01µf capacitors attached between center nodes and ground (82562EZ/EX and 82551ER/IT only). • Removed center tap connection to VCC 2.5 V (82562EZ/EX and 82551ER/IT only). Added Section 5.1.2.1 “Terminating Differential Pairs for 82562EZ/EX and 82551ER/IT-Based Designs”. Added Section 5.1.2.2 “Terminating Differential Pairs for 82541ER-Based Designs”.
1.6	February 2005	Added Appendix B “GigConf.exe Register Settings for 82541ER Devices”.
1.7	April 2005	For the 82541ER only, removed CLK_RUN# signal reference from sheet 03 of the reference schematics and from the Ball Number to Signal Mapping table.

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Tables

1.0 Introduction

The 82541ER Gigabit Ethernet Controller and the 82551ER(IT)/82562EZ(EX) Fast Ethernet Controllers are all manufactured in a footprint compatible 15 mm x 15 mm, 196-ball grid array package. Many of the critical signal pin locations on the 82541ER are identical to signals on the 82562EZ(EX) and 82551ER(IT) allowing designers to create a single design that accommodates these three parts. Because the usage of some pins on the 82541ER differ from the usage on the 82551ER(IT) and the 82562EZ(EX), the three parts are not referred to as "pin compatible". The term "footprint compatible" refers to the fact that the parts share the same package size, same number and pattern of pins, and layout of signals that allow for the flexible, cost effective, multipurpose design. Therefore, it is easy to populate a single board design with any of the three parts to maximize value while matching your customers' performance needs.

1.1 Scope

This application note identifies the design differences between the 82541ER, 82551ER(IT), and 82562EZ(EX). The table in Section 8.0 lists the stuffing (population) options for the three parts.

For other necessary design collateral, please refer to “Reference Documents” (Section 1.2).

1.2 Reference Documents

This application note assumes that the designer is acquainted with high-speed design and board layout techniques. The following documents provide additional information:

- 82541ER Datasheet, Intel Corporation.
- 82551ER Datasheet, Intel Corporation.
- 82551IT Datasheet, Intel Corporation.
- 82562EZ 10/100 Mbps Platform LAN Connect (PLC) Networking Silicon Datasheet, Intel Corporation.
- I/O Control Hub 2, 3, and 4 EEPROM Map and Programming Information, Intel Corporation.
- I/O Control Hub 5, 6, and 7 EEPROM Map and Programming Information, Intel Corporation.
- 82551QM/ER/IT EEPROM Map and Programming Information, Intel Corporation
- 82541GI(EI)/82547GI(EI) EEPROM Map and Programming Information, Intel Corporation
- PCI Local Bus Specification, PCI Special Interest Group
- PCI Bus Power Management Interface Specification, Rev. 1.1, PCI Special Interest Group
- IEEE Standard 802.3, 1996 Edition, Institute of Electrical and Electronics Engineers
- IEEE Standard 802.3u, 1995 Edition, Institute of Electrical and Electronics Engineers
- IEEE Standard 802.3x, 1997 Edition, Institute of Electrical and Electronics Engineers
- IEEE Standard 802.3z, 1998 Edition, Institute of Electrical and Electronics Engineers
- IEEE Standard 802.3ab, 1999 Edition, Institute of Electrical and Electronics Engineers
- Oscillation Circuit Design Guide Application Note, Epson Electronics America, Inc. (www.eea.epson.com).

- Quartz Crystal Theory of Operation and Design Notes. Fox Electronics (www.foxonline.com).
- Crystal Technical Glossary. Fox Electronics.
- Crystal Frequently Asked Questions. Fox Electronics.
- Resonator Terminology and Formulas. Piezo Technology, Inc. (www.piezotech.com).

1.3 Product Codes

Table 1 lists the product ordering codes for the 82562EZ(EX), 82551ER(IT), and 82541ER.

Table 1. Product Ordering Codes

Device	Product Code	Product Code (Lead Free)
82562EZ	GD82562EZ	LU82562EZ
82562EX	GD82562EX	LU82562EX
82551ER	GD82551ER	LU82551ER
82551IT	GD82551IT	LU82551IT
82541ER	GD82541ER	LU82541ER

2.0 Frequency Control Device Design Considerations

This section provides information regarding frequency control devices, including crystals and oscillators, for use with all Intel® Ethernet controllers. Several suitable frequency control devices are available; none of which present any unusual challenges in selection. The concepts documented herein are applicable to other data communication circuits, including Physical Layer devices (PHYs).

The Intel® Ethernet controllers contain amplifiers which, when used with the specific external components, form the basis for feedback oscillators. These oscillator circuits, which are both economical and reliable, are described in more detail in “Crystal Selection Parameters”.

The Intel® Ethernet controllers also have bus clock input functionality, however a discussion of this feature is beyond the scope of this document, and will not be addressed.

The chosen frequency control device vendor should be consulted early in the design cycle. Crystal and oscillator manufacturers familiar with networking equipment clock requirements may provide assistance in selecting an optimum, low-cost solution.

2.1 Frequency Control Component Types

Several types of third-party frequency reference components are currently marketed. A discussion of each follows, listed in preferred order.

2.2 Quartz Crystal

Quartz crystals are generally considered to be the mainstay of frequency control components due to their low cost and ease of implementation. They are available from numerous vendors in many package types and with various specification options.

2.3 Fixed Crystal Oscillator

A packaged fixed crystal oscillator is comprised of an inverter, a quartz crystal, and passive components conveniently packaged together. The device renders a strong, consistent square wave output. Oscillators used with microprocessors are supplied in many configurations and tolerances.

Crystal oscillators should be restricted to use in special situations, such as shared clocking among devices or multiple controllers. As clock routing can be difficult to accomplish, it is preferable to provide a separate crystal for each device.

For Intel® Ethernet controllers, it is acceptable to overdrive the internal inverter by connecting a 25 MHz external oscillator to the X1 lead, leaving the X2 lead unconnected. The oscillator should be specified to drive CMOS logic levels, and the clock trace to the controller should be as short as possible. Controller specifications typically call for a 40% (minimum) to 60% (maximum) duty cycle and a ±50 ppm frequency tolerance.

Note: Please contact your Intel Customer Representative to obtain the most current device documentation prior to implementing this solution.

2.4 Programmable Crystal Oscillators

A programmable oscillator can be configured to operate at many frequencies. The device contains a crystal frequency reference and a phase lock loop (PLL) clock generator. The frequency multipliers and divisors are controlled by programmable fuses.

A programmable oscillator's accuracy depends heavily on the Ethernet controller's differential transmit lines. The Physical Layer (PHY) uses the clock input from the device to drive a differential Manchester (for 10 Mbps operation), an MLT-3 (for 100 Mbps operation) or a PAM-5 (for 1000 Mbps operation) encoded analog signal across the twisted pair cable. These signals are referred to as self-clocking, which means the clock must be recovered at the receiving link partner. Clock recovery is performed with another PLL that locks onto the signal at the other end.

PLLs are prone to exhibit frequency jitter. The transmitted signal can also have considerable jitter even with the programmable oscillator working within its specified frequency tolerance. PLLs must be designed carefully to lock onto signals over a reasonable frequency range. If the transmitted signal has high jitter and the receiver's PLL loses its lock, then bit errors or link loss can occur.

PHY devices are deployed for many different communication applications. Some PHYs contain PLLs with marginal lock range and cannot tolerate the jitter inherent in data transmission clocked with a programmable oscillator. The American National Standards Institute (ANSI) X3.263-1995 standard test method for transmit jitter is not stringent enough to predict PLL-to-PLL lock failures, therefore, the use of programmable oscillators is generally not recommended.

2.5 Ceramic Resonator

Similar to a quartz crystal, a ceramic resonator is a piezoelectric device. A ceramic resonator typically carries a frequency tolerance of ±0.5%, – inadequate for use with Intel® Ethernet controllers, and therefore, should not be utilized.

3.0 Crystal Selection Parameters

All crystals used with Intel® Ethernet controllers are described as "AT-cut," which refers to the angle at which the unit is sliced with respect to the long axis of the quartz stone.

Table 2 lists the crystal electrical parameters and provides suggested values for typical designs. These parameters are described in the following subsections.

Table 2. Crystal Parameters

Parameter	Suggested Value
Vibrational Mode	Fundamental
Nominal Frequency	25.000 MHz at 25° C (required)
Frequency Tolerance	• ±30 ppm recommended • ±50 ppm across the entire operating temperature range (required by IEEE specifications)
Temperature Stability	±50 ppm at 0° C to 70° C
Calibration Mode	Parallel
Load Capacitance	16 pF to 20 pF
Shunt Capacitance	6 pF maximum
Equivalent Series Resistance	50 Ω maximum
Drive Level	0.5 mW maximum
Aging	±5 ppm per year maximum

3.1 Vibrational Mode

Crystals in the above-referenced frequency range are available in both fundamental and third overtone. Unless there is a special need for third overtone, use fundamental mode crystals.

At any given operating frequency, third overtone crystals are thicker and more rugged than fundamental mode crystals. Third overtone crystals are more suitable for use in military or harsh industrial environments. Third overtone crystals require a trap circuit (extra capacitor and inductor) in the load circuitry to suppress fundamental mode oscillation as the circuit powers up. Selecting values for these components is beyond the scope of this document.

3.2 Nominal Frequency

Intel® Ethernet controllers use a crystal frequency of 25.000 MHz. The 25 MHz input is used to generate a 125 MHz transmit clock for 100BASE-TX and 1000BASE-TX operation – 10 MHz and 20 MHz transmit clocks, for 10BASE-T operation.

3.3 Frequency Tolerance

The frequency tolerance for an Ethernet physical layer device is dictated by the IEEE 802.3 specification as ±50 parts per million (ppm). This measurement is referenced to a standard temperature of 25° C. Intel recommends a frequency tolerance of ±30 ppm.

3.4 Temperature Stability and Environmental Requirements

Temperature stability is a standard measure of how the oscillation frequency varies over the full operational temperature range (and beyond). Several optional temperature ranges are currently available, including -40° C to +85° C for industrial environments. Some vendors separate operating temperatures from temperature stability. Manufacturers may also list temperature stability as 50 ppm in their data sheets.

Note: Crystals also carry other specifications for storage temperature, shock resistance, and reflow solder conditions. Crystal vendors should be consulted early in the design cycle to discuss the application and its environmental requirements.

3.5 Calibration Mode

The terms “series-resonant” and “parallel-resonant” are often used to describe crystal oscillator circuits. Specifying parallel mode is critical to determining how the crystal frequency is calibrated at the factory.

A crystal specified and tested as series resonant oscillates without problem in a parallel-resonant circuit, but the frequency is higher than nominal by several hundred parts per million. The purpose of adding load capacitors to a crystal oscillator circuit is to establish resonance at a frequency higher than the crystal’s inherent series resonant frequency.

Figure 1 illustrates a simplified schematic of the 82551QM’s oscillator circuit. Note that 82541ER controllers are similar. The crystal and the capacitors form a feedback element for the internal inverting amplifier. This combination is called parallel-resonant, because it has positive reactance at the selected frequency. In other words, the crystal behaves like an inductor in a parallel LC circuit. Oscillators with piezoelectric feedback elements are also known as “Pierce” oscillators.

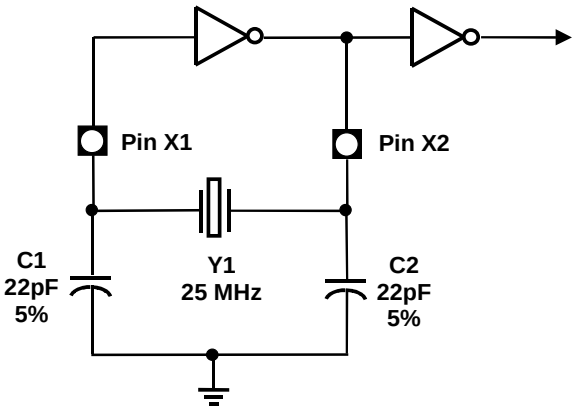

Figure 1. 82551QM Oscillator Circuit

3.6 Load Capacitance

The formula for crystal load capacitance is as follows:

$$C_L = \frac{(C1 \cdot C2)}{(C1 + C2)} + C_{stray}$$

where C1 = C2 = 22 pF (as suggested in most Intel reference designs)

and C_{stray} = allowance for additional capacitance in pads, traces and the chip carrier within the Ethernet controller package

An allowance of 3 pF to 7 pF accounts for lumped stray capacitance. The calculated load capacitance is 16 pF with an estimated stray capacitance of about 5 pF.

Individual stray capacitance components can be estimated and added. For example, surface mount pads for the load capacitors add approximately 2.5 pF in parallel to each capacitor. This technique is especially useful if Y1, C1 and C2 must be placed farther than approximately one-half (0.5) inch from the controller. It is worth noting that thin circuit boards generally have higher stray capacitance than thick circuit boards.

Standard capacitor loads used by crystal manufacturers include 16 pF, 18 pF and 20 pF. Any of these values will generally operate with the controller. However, a difference of several picofarads between the calibrated load and the actual load will pull the oscillator slightly off frequency.

The oscillator frequency should be measured with a precision frequency counter where possible. The 82551ER(IT) Fast Ethernet controller has a FLA16/CLK25 signal output for this purpose. The load specification or values of C1 and C2 should be fine tuned for the design. As the actual capacitance load increases, the oscillator frequency decreases.

Note: C1 and C2 may vary by as much as 5% (approximately 1 pF) from their nominal values.

3.7 Shunt Capacitance

The shunt capacitance parameter is relatively unimportant compared to load capacitance. Shunt capacitance represents the effect of the crystal's mechanical holder and contacts. The shunt capacitance should equal a maximum of 6 pF (7 pF is also acceptable).

3.8 Equivalent Series Resistance

Equivalent Series Resistance (ESR) is the real component of the crystal's impedance at the calibration frequency, which the inverting amplifier's loop gain must overcome. ESR varies inversely with frequency for a given crystal family. The lower the ESR, the faster the crystal starts up. Use crystals with an ESR value of 50 Ω or better.

Note: Check the specific controller documentation carefully; some devices may have tighter ESR requirements.

3.9 Drive Level

Drive level refers to power dissipation in use. The allowable drive level for a Surface Mounted Technology (SMT) crystal is less than its through-hole counterpart, because surface mount crystals are typically made from narrow, rectangular AT strips, rather than circular AT quartz blanks.

Some crystal data sheets list crystals with a maximum drive level of 1 mW. However, Intel® Ethernet controllers drive crystals to a level less than the suggested 0.5 mW value. This parameter does not have much value for on-chip oscillator use.

3.10 Aging

Aging is a permanent change in frequency (and resistance) occurring over time. This parameter is most important in its first year because new crystals age faster than old crystals. Use crystals with a maximum of ±5 ppm per year aging.

3.11 Reference Crystal

The normal tolerances of the discrete crystal components can contribute to small frequency offsets with respect to the target center frequency. To minimize the risk of tolerance-caused frequency offsets causing a small percentage of production line units to be outside of the acceptable frequency range, it is important to account for those shifts while empirically determining the proper values for the discrete loading capacitors, C1 and C2.

Even with a perfect support circuit, most crystals will oscillate slightly higher or slightly lower than the exact center of the target frequency. Therefore, frequency measurements (which determine the correct value for C1 and C2) should be performed with an ideal reference crystal. When the capacitive load is exactly equal to the crystal's load rating, an ideal reference crystal will be perfectly centered at the desired target frequency.

3.11.1 Reference Crystal Selection

There are several methods available for choosing the appropriate reference crystal:

- If a Saunders and Associates (S&A) crystal network analyzer is available, then discrete crystal components can be tested until one is found with zero or nearly zero ppm deviation (with the appropriate capacitive load). A crystal with zero or near zero ppm deviation will be a good reference crystal to use in subsequent frequency tests to determine the best values for C1 and C2.

- If a crystal analyzer is not available, then the selection of a reference crystal can be done by measuring a statistically valid sample population of crystals, which has units from multiple lots and approved vendors. The crystal, which has an oscillation frequency closest to the center of the distribution, should be the reference crystal used during testing to determine the best values for C1 and C2.
- It may also be possible to ask the approved crystal vendors or manufacturers to provide a reference crystal with zero or nearly zero deviation from the specified frequency when it has the specified CLoad capacitance.

When choosing a crystal, customers must keep in mind that to comply with IEEE specifications for 10/100 and 10/100/1000Base-T Ethernet LAN, the transmitter reference frequency must be precise within ±50 ppm. Intel® recommends customers to use a transmitter reference frequency that is accurate to within ±30 ppm to account for variations in crystal accuracy due to crystal manufacturing tolerance. For information about measuring transmitter reference frequency, refer to Appendix A, “Measuring LAN Reference Frequency Using a Frequency Counter”.

3.11.2 Circuit Board

Since the dielectric layers of the circuit board are allowed some reasonable variation in thickness, the stray capacitance from the printed board (to the crystal circuit) will also vary. If the thickness tolerance for the outer layers of dielectric are controlled within ±17 percent of nominal, then the circuit board should not cause more than ±2 pF variation to the stray capacitance at the crystal. When tuning crystal frequency, it is recommended that at least three circuit boards are tested for frequency. These boards should be from different production lots of bare circuit boards.

Alternatively, a larger sample population of circuit boards can be used. A larger population will increase the probability of obtaining the full range of possible variations in dielectric thickness and the full range of variation in stray capacitance.

Next, the exact same crystal and discrete load capacitors (C1 and C2) must be soldered onto each board, and the LAN reference frequency should be measured on each circuit board.

The circuit board, which has a LAN reference frequency closest to the center of the frequency distribution, should be used while performing the frequency measurements to select the appropriate value for C1 and C2.

3.11.3 Temperature Changes

Temperature changes can cause the crystal frequency to shift. Therefore, frequency measurements should be done in the final system chassis across the system’s rated operating temperature range.

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4.0 Ethernet Component Design Guidelines

This section provides recommendations for selecting components and connecting special pins. The main design elements are the 82562EZ(EX) Platform LAN Connect device, the 82541ER Gigabit Ethernet Controller, and the 82551ER(IT) Fast Ethernet Controller, a magnetics module with RJ-45 connector, and a crystal clock source.

4.1 Designing with the 82562EZ(EX) Platform LAN Connect Device

This section provides design guidelines specific to the PLC device.

4.1.1 Power Supplies for 82562EZ(EX) PLC Implementations

The 82562EZ(EX) PLC device uses a single 3.3 V power supply. The 3.3 V supply must provide approximately 90 mA current for full speed operation. Standby power must be furnished in order to wake up from a power down.

4.1.2 82562EZ(EX) Device Test Capability

The device contains an XOR test tree mechanism for simple board tests. Details of the XOR tree operation are contained in the 82562ET LAN on Motherboard Design Guide.

4.1.3 82562EZ(EX) PCL Device LAN Disable Guidelines

Note: ICHx Integrated LAN Controller resides on the ICHx VccSus3_3 and VccSus1_8 power wells (typically referred to as “auxiliary” (“aux”) or “standby” supplies at the platform level).

The ICHx Integrated LAN’s RST# is the ICHx Resume-Well input. This input can be held low to keep the ICHx Integrated LAN Controller in a reset state. The LAN Reset (RST#) signal must not be de-asserted sooner than 10 ms after the Resume power supply reaches it nominal voltage. This ensures that the ICHx Integrated LAN Controller is initialized. Figure 2 illustrates a possible solution for ICHx Integrated LAN disable.

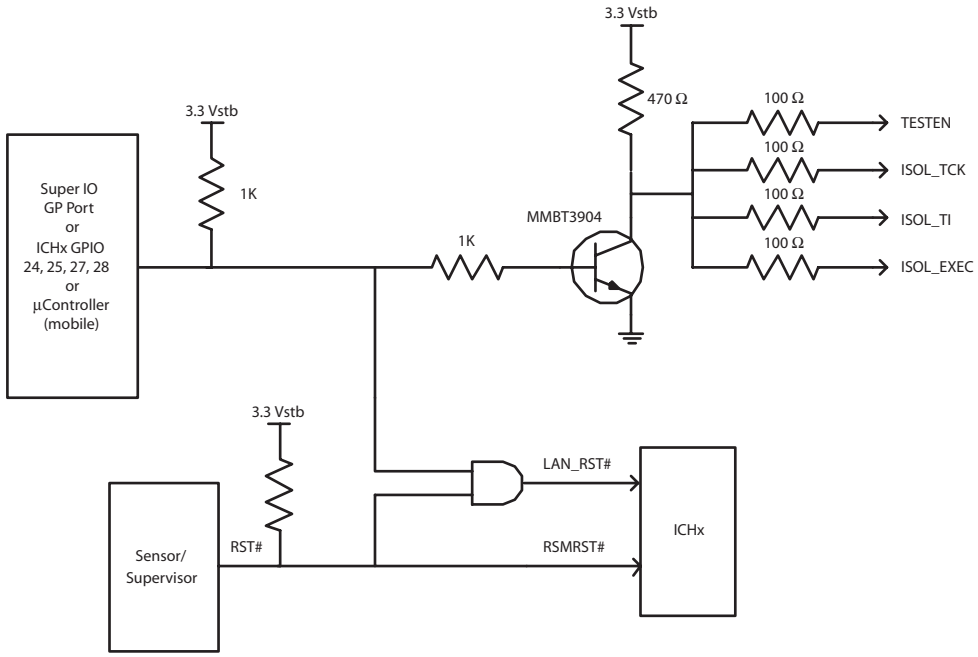


Figure 2. 82562EZ(EX) LAN Disable Circuitry

Note: The 100 Ω resistors for the Test Mode signals are required for the Exclusive OR (XOR) Tree and Isolate Mode.

4.2 Designing with the 82541ER Gigabit Controllers

This section provides design guidelines specific to the 82541ER Gigabit Ethernet Controllers.

4.2.1 82541ER Ethernet Controller LAN Disable Guidelines

The 82541ER controller has a LAN disable function that is present on FLSH_SO, ball P9. This pin can be connected to a Super IO component to allow the BIOS to disable the Ethernet port (see Figure 3). If the serial Flash interface is populated, the Flash serial output pin must not interfere with this function.

Do not attempt to use the LAN_POWER_GOOD signal for a LAN disable input on the 82541ER device. This pin is intended to operate as a power-on reset connected to a power monitor circuit.

The input of the 82541ER FLSH_SO (pin P9) is the LAN_DISABLE# signal. It is sampled on the rising edge of LAN_PWR_GOOD or RST#. The signal must be held valid for 80 ns after either rising edge.

If it is sampled high, the LAN functions normally. If it is sampled low, then the following occurs:

1. The LAN is disabled.
2. The PHY is powered down.
3. Most MAC clock domains are gated.
4. Most functional blocks are held in reset.
5. PCI inputs and outputs are floated.
6. The device will not respond to PCI cycles (including configuration cycles).
7. The device is put in a low power state, which is equivalent to D3 without wakeup or manageability.

Note: To use this configuration for the 82562EZ(EX) Platform LAN Connect device, be sure the AND gate U1 is populated. Depopulate the 0 Ω resistor R2.

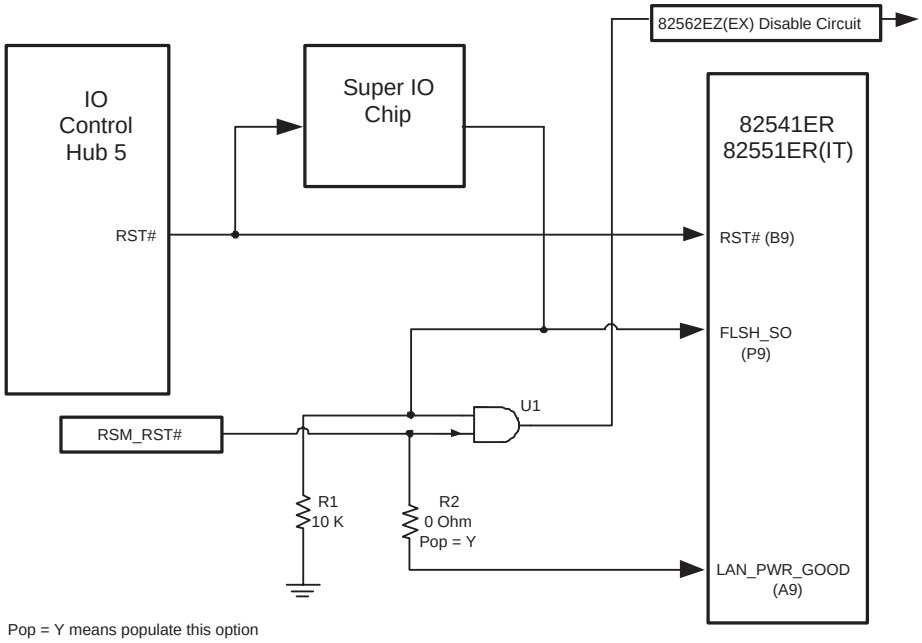


Figure 3. 82541ER LAN Disable Circuitry

4.2.2 Power Supplies for the 82541ER Controller

The 82541ER controller requires three power supplies: 1.2 V, 1.8 V, and 3.3 V. The 1.2 V supply must provide approximately 500 mA current, and the 1.8 V supply, approximately 230 mA current. The 3.3 V supply must provide only 30 mA current.

A central power supply can provide all the required voltage sources, or the power can be derived and regulated locally near the Ethernet control circuitry. All voltage sources must remain present during lower power states in order to use the 82541ER LAN wake up capability. This consideration makes it more likely that at least some of the voltage sources will be local.

Instead of using external regulators to supply 1.2 V and 1.8 V, power transistors can be used in conjunction with on-chip regulation circuitry. (See the reference schematic for an implementation example.)

The 82541ER controller has a LAN_PWR_GOOD input. Treat this signal as an external device reset which works in conjunction with the internal power-on reset circuitry. In the situation where a central power supply furnishes all the voltage sources, LAN_PWR_GOOD can be tied to the POWER_GOOD output of the power supply. Designs that generate some of the voltages locally can connect LAN_PWR_GOOD to a power monitor chip.

The power sources are all expected to ramp up during a brief power-up interval (approximately 20 ms) with LAN_PWR_GOOD de-asserted. The 82541ER controller must not be left in a prolonged state where some, but not all, voltages are applied. The 3.3 V source should be powered up prior to the 1.2 V or 1.8 V sources. The 1.2 V and 1.8 V power supplies may power up simultaneously. At any time during power up, the supply voltages must be: 1.2 V < 1.8 V < 3.3 V.

4.2.3 82541ER Controller Power Supply Filtering

The 82541ER controller switches relatively high currents at high frequencies, requiring generous use of both bulk capacitance and high speed decoupling capacitance adjacent to the device.

Bypass capacitors for each power rail should be 0.1 µF. If possible, orient the capacitors close to the device and adjacent to power pads. Decoupling capacitors should connect to the power and ground planes with short, thick traces (15 mils or 0.4 mm or more), and 14 mil (3.5 mm) vias per capacitor pad.

Furnish approximately 20 µF of bulk capacitance for each of the main 1.2 V and 1.8 V levels. This can be easily achieved by using two 10 µF capacitors, placing them as close to the device power connections as possible.

4.2.4 82541ER Controller Power Management and Wake Up

The 82541ER Gigabit Ethernet Controller supports low power operation as defined in the PCI Bus Power Management Specification. There are two defined power states, D0 and D3. The D0 state provides full power operation and is divided into two sub-states: D0u (uninitialized) and D0a (active). The D3 state provides low power operation and is also divided into two sub-states: D3hot and D3cold.

To enter the low power state, the software driver must stop data transmission and reception. Either the operating system or the driver must program the Power Management Control/Status Register (PMCSR) and the Wakeup Control Register (WUC). If wakeup is desired, the appropriate wakeup LAN address filters must also be set. The initial power management settings are specified by EEPROM bits.

When the 82541ER controller transitions to either of the D3 low power states, the 1.2 V, 1.8 V, and 3.3 V sources must continue to be supplied to the device. Otherwise, it will not be possible to use a wakeup mechanism. The AUX_POWER signal is a logic input to the 82541ER controller that denotes auxiliary power is available. If AUX_POWER is asserted, the 82541ER device will advertise that it supports wake up from a D3cold state.

The 82541ER device supports both Advanced Power Management (APM) wakeup and Advanced Configuration and Power Interface (ACPI) wakeup. APM wakeup has also been known in the past as “Wake on LAN.”

Wakeup uses the PME# signal to wake the system. PME# is an active low signal connected to a GPIO port on the ICH5 that goes active in response to receiving a Magic Packet*, a network wake-up packet, or link status change indication. PME# remains asserted until it is disabled through the Power Management Control/Status Register.

4.2.5 82541ER Device Test Capability

The 82541ER Gigabit Ethernet Controller contains a test access port conforming to the IEEE 1149.1a-1994 (JTAG) Boundary Scan specification. To use the test access port, these balls need to be connected to pads accessible by the test equipment. The TRST# input also needs to be connected to ground through a pull-down resistor (approximately 100 Ω) so that the test capability cannot be invoked by mistake.

A Boundary Scan Definition Language (BSDL) file describing the 82541ER device is available for use in your test environment.

The controller also contains an XOR test tree mechanism for simple board tests. Details of XOR tree operation may be obtained through your Intel representative.

4.2.6 82541ER Oscillator Solution

There are two oscillator solutions for the 82541ER: high voltage and low voltage.

High Voltage Solution (VDD = 3.3 V)

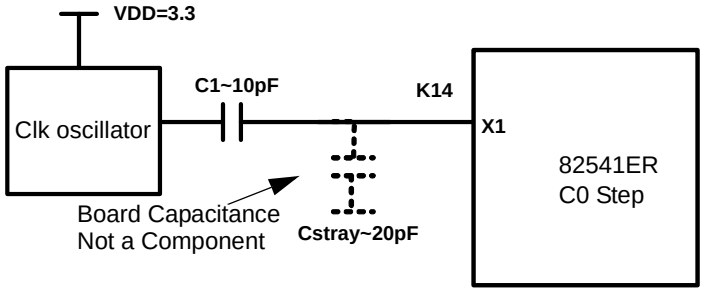
This solution involves capacitor C1, which forms a capacitor divider with C_{stray} of about 20 pF. This attenuates the input clock amplitude and adjusts the clock oscillator load capacitance.

$$V_{in} = VDD * (C1/(C1 + C_{stray}))$$
$$V_{in} = 3.3 * (C1/(C1 + C_{stray}))$$

This enables load clock oscillators of 15 pF to be used. If the value of C_{stray} is unknown, C1 should be adjusted by tuning the input clock amplitude to approximately 1 V_{ptp}. If C_{stray} equals 20 pF, then C1 is 10 pF ±10%.

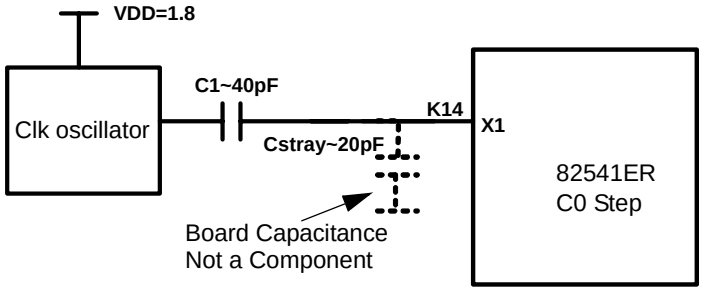
A low capacitance, high impedance probe (C < 1 pF, R > 500 K Ω) should be used for testing. Probing the parameters can affect the measurement of the clock amplitude and cause errors in the adjustment. A test should also be done after the probe has been removed for circuit operation.

If jitter performance is poor, a lower jitter clock oscillator can be implemented.



Low Voltage Solution (VDD = 1.8 V)

The low voltage solution is similar to the high voltage solution. However, the low voltage includes a low consumption and low jitter clock oscillator that uses a 1.8 V external power supply. In this case, C1 will require adjusting according to the stray capacitance from X1.



5.0 PCB Routing Guidelines

5.1 Critical Dimensions for Discrete Magnetics Module and RJ-45

There are four critical dimensions that must be considered during the layout phase of an 82541ER, 82551ER(IT), and 82562EZ(EX) LAN On Motherboard (LOM) implementation. These dimensions are identified in Figure 4 as A, B, C and D.

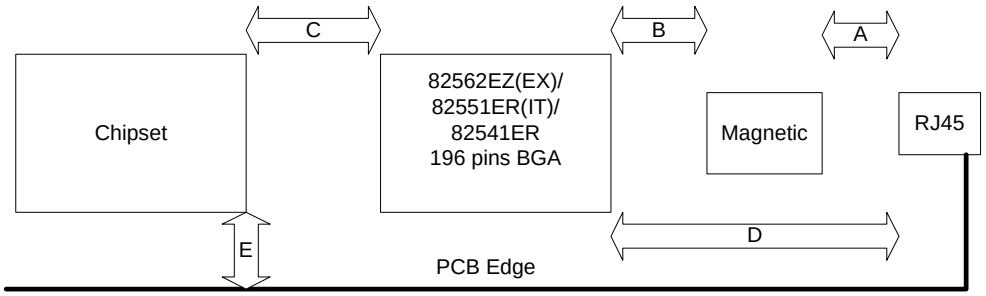


Figure 4. Critical Dimensions for 82562EZ(EX), 82551ER(IT) and 82541ER Component Placement

5.1.1 Distance A: Magnetics to RJ-45

The distance labeled “A” in Figure 1 should be given highest priority in board layout. The distance between the magnetics and RJ-45 should be less than 1 inch of separation. The following trace characteristics are important and should be observed.

- Differential Impedance: The differential impedance should be 100 Ω. The single ended trace impedance will be approximately 50 Ω; however, the differential impedance can also be affected by the spacing between the traces.
- Trace Symmetry: Differential pairs should be routed with consistent separation and with exactly the same lengths and physical dimensions.

5.1.2 Distance B: LAN Controller to Magnetics

The distance labeled “B” should also be designed to be less than one inch between devices. The high-speed nature of the signals propagating through the traces requires that the distance between these components be closely observed. In general, any section of traces intended for use with high-speed signals should observe proper termination practices. Proper termination of signals can reduce reflections caused by impedance mismatches between devices and traces.

5.1.2.1 Terminating Differential Pairs for 82562EZ(EX) and 82551ER(IT)-Based Designs

Two differential pairs are terminated using 54.9 Ω (1% tolerance) resistors, placed near the LAN controller. One resistor connects to the MDI+ (MDI positive) signal trace and another resistor connects to the MDI- (MDI negative) signal trace.

Termination resistor values were recently increased from 49.9 Ω to 54.9 Ω to improve return loss. However, on some designs, this change caused the PCB's output amplitude to be slightly above the peak-to-peak center of the IEEE specification. As a result, RBIAS resistor values were increased (RBIAS10 549 to 619 Ω and RBIAS100 619 to 649 Ω) to reduce the PCB's output amplitude to better meet the IEEE peak-to-peak center specification.

For 100Base-TX designs, the IEEE specification allows a -950 mVpk to -1050 mVpk for the negative peak and +950 mVpk to +1050 mVpk for the positive peak. Ideally, a typical PCB output amplitude should be within -975 mVpk to -1025 mVpk for the negative peak and +975 mVpk to +1025 mVpk for the positive peak.

For 10Base-T designs, the IEEE specification allows a -2.2 mVpk to -2.8 mVpk for the negative peak and +2.2 mVpk to +2.8 mVpk for the positive peak. Ideally, a typical PCB output amplitude should be within -2.35 mVpk to -2.55 mVpk for the negative peak and +2.35 mVpk to +2.55 mVpk for the positive peak.

The RBIAS values previously listed should be considered starting values. Intel recommends that board designers measure each of their PCB's output amplitude and then adjust the RBIAS values as required.

5.1.2.2 Terminating Differential Pairs for 82541ER-Based Designs

Four differential pairs are terminated using 49.9 Ω (1% tolerance) resistors, placed near the LAN controller. One resistor connects to the MDI+ (MDI positive) signal trace and another resistor connects to the MDI- (MDI negative) signal trace. The opposite ends of the resistors connect together and to ground through a single 0.1 µf capacitor. The capacitor should be placed as close as possible to the 49.9 Ω resistors, using a wide trace.

Note: Do not vary the suggested component values. Be sure to lay out symmetrical pads and traces for these components such that the length and symmetry of the differential pairs are not disturbed.

5.1.3 Distance C: LAN Controller to Chipset

This section between the chipset and LAN controller should be addressed separately between the 82562EZ(EX) and 82551ER(IT)/82541ER.

5.1.3.1 LAN Connect Interface (LCI) for 82562EZ(EX)

The 82562EZ(EX) Platform LAN Connect device uses the LAN Connect Interface (LCI) to connect to the I/O Control Hub 5 (ICH5). LCI is a point-to-point interface optimized to support one device.

Line termination mechanisms are not specified for the LCI. Slew rate controlled output buffers achieve acceptable signal integrity by controlling signal reflection, undershoot and ringing.

For details about how to connect the LCI interface between the 82562EZ(EX) Platform LAN Connect device and ICH5, please refer to the 82562ET/EM Platform LAN Connect Printed Circuit Board (PCB) Design Guide, the Intel® 865 Chipset design guide, or the Intel® 875 Chipset design guide.

5.1.3.2 PCI Interface for 82541ER/82551ER(IT)

The PCI bus on 82541ER meets PCI 2.3 specification. The PCI bus on 82551ER(IT) meets PCI 2.2 specification.The trace routing on the bus should follow the appropriate PCI specification.

The Ethernet controllers operate as PCI slave devices for configuration and register programming. After the devices have been properly initialized, they can also operate as PCI masters to fetch memory descriptors and to read/write data buffers.

The devices are capable of operating in either a 5 V or 3.3 V signaling environment. The VIO terminals can be connected to either 3.3 V or 5 V to choose the appropriate PCI bus levels.These connections bias the controller PCI I/O buffers for the correct switching strength. However, all other digital inputs and outputs use 3.3 V signaling unless specified separately.

5.1.4 Distance D: The Overall Length of Differential Traces from LAN to RJ-45

The overall length of differential pairs should be less than four inches measured from the LAN controller to RJ-45 through the magnetics module.

The lengths of the differential traces (within each pair) should be equal within 50 mils (1.25 mm) and as symmetrical as possible.

5.1.5 Distance E: LAN Controller to PCB Edge

The LAN controller should be placed at least two inches from the printed circuit board edge.

5.2 Critical Dimensions for an Integrated Magnetics Module

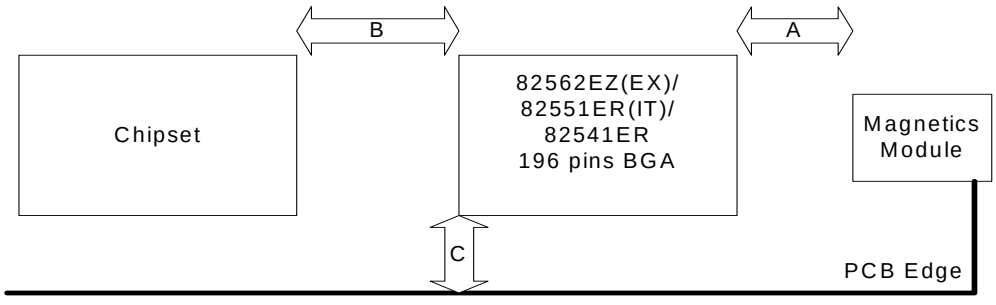


Figure 5. Critical Dimensions for 82562EZ(EX), 82551ER(IT), and 82541ER Component Placement with Integrated Magnetics Module

5.2.1 Distance A: The Overall Length of Differential Traces

The overall length of differential pairs should be less than four inches measured from the LAN controller across the magnetics module to the RJ-45 connector.

5.2.2 Distance B: LAN Controller to Chipset

For LCI on 82562EZ(EX), the maximum length should be less than 12 inches on ICH4 platform. For PCI bus on 82551ER(IT), or the 82541ER, the bus routing should meet respective PCI specifications.

5.2.3 Distance C: LAN Controller to PCB Edge

The LAN controller should be placed at least two inches from the PCB edge.

5.3 General LAN Differential Pair Trace Routing Considerations

Trace routing considerations are important to minimize the effects of crosstalk and propagation delays on sections of the board where high-speed signals exist. Signal traces should be kept as short as possible to decrease interference from other signals, including those propagated through power and ground planes.

Observe the following suggestions to help optimize board performance (Note: Some suggestions are specific to a 4.3 mil stackup.):

- Maintain constant symmetry and spacing between the traces within a differential pair.
- Keep the signal trace lengths of a differential pair equal to each other.
- Keep the total length of each differential pair under four inches. Many customer designs with differential traces longer than five inches have had one or more of the following issues:
  - IEEE PHY conformance failures
  - Excessive Electro Magnetic Interference (EMI)
  - Degraded receive Bit Error Rate (BER)
- Do not route the transmit differential traces closer than 100 mils to the receive differential traces.
- Do not route any other signal traces both parallel to the differential traces and closer than 100 mils to the differential traces (300 mils is recommended).
- Keep maximum separation between differential pairs to seven mils.
- For high-speed signals, the number of corners and vias should be kept to a minimum. If a 90° bend is required, it is recommended to use two 45° bends instead.
- Traces should be routed away from board edges by a distance greater than the trace height above the ground plane. This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards.
- Do not route traces and vias under crystals or oscillators. This prevents coupling to or from the clock. And as a general rule, place traces from clocks and drives at a minimum distance from apertures by a distance that is greater than the largest aperture dimension.

5.3.1 Trace Routing and Geometry

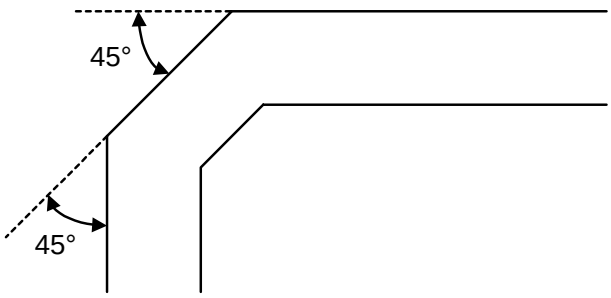


Figure 6. Trace Routing

The key factors in controlling trace EMI radiation are the trace length and the ratio of trace-width to trace-height above the ground plane. To minimize trace inductance, high-speed signals and signal layers that are close to a ground or power plane should be as short and wide as practical. Ideally, this trace width to height above the ground plane ratio is between 1:1 and 3:1. To maintain trace impedance, the width of the trace should be modified when changing from one board layer to another if the two layers are not equidistant from the power or ground plane. Differential trace impedances should be controlled to be ~100 Ω. It is necessary to compensate for trace-to-trace edge coupling, which can lower the differential impedance by up to 10 Ω, when the traces within a pair are closer than 30 mils (edge-to-edge).

Traces between decoupling and I/O filter capacitors should be as short and wide as practical. Long and thin traces are more inductive and would reduce the intended effect of decoupling capacitors. Also for similar reasons, traces to I/O signals and signal terminations should be as short as possible. Vias to the decoupling capacitors should be sufficiently large in diameter to decrease series inductance. Additionally, the PLC should not be closer than one inch to the connector/ magnetics/edge of the board.

5.3.1.1 Signal Isolation

Some rules to follow for signal isolation:

- Separate and group signals by function on separate layers if possible. Maintain a gap of 100 mils between all differential pairs (Ethernet) and other nets, but group associated differential pairs together. Note: Over the length of the trace run, each differential pair should be at least 0.3 inches away from any parallel signal traces.
- Physically group together all components associated with one clock trace to reduce trace length and radiation.
- Isolate I/O signals from high speed signals to minimize crosstalk, which can increase EMI emission and susceptibility to EMI from other signals.
- Avoid routing high-speed LAN traces near other high-frequency signals associated with a video controller, cache controller, CPU, or other similar devices.

5.3.1.2 Magnetics Module General Power and Ground Plane Considerations

To properly implement the common mode choke functionality of the magnetics module the chassis or output ground (secondary side of transformer) should be separated from the digital or input ground (primary side) by a physical separation of 100 mils minimum.

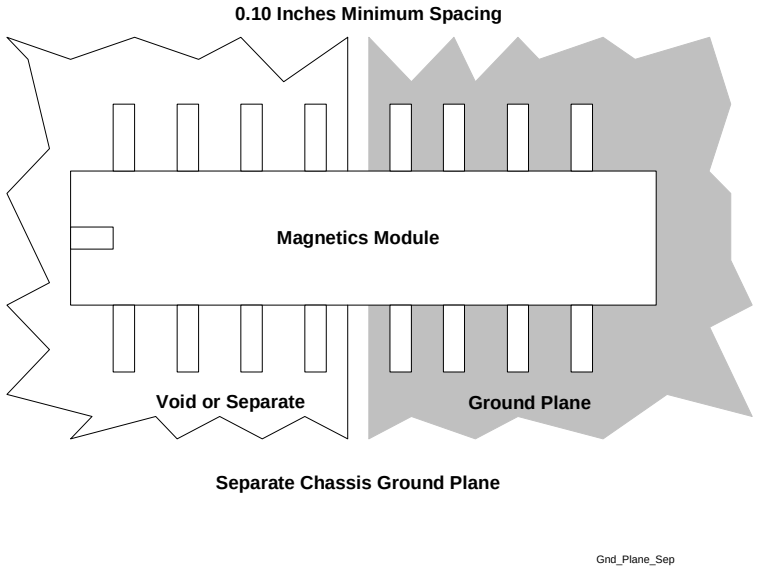


Figure 7. Separate Chassis Ground Plane

5.3.1.3 Separation

Good grounding requires minimizing inductance levels in the interconnections and keeping ground returns short, signal loop areas small, and power inputs bypassed to signal return, will significantly reduce EMI radiation.

Follow these rules to help reduce circuit inductance in both back planes and motherboards:

- Route traces over a continuous plane with no interruptions (don't route over a split plane). If there are vacant areas on a ground or power plane, avoid routing signals over the vacant area. This increases inductance and EMI radiation levels.
- Separate noisy digital grounds from analog grounds to reduce coupling. Noisy digital grounds can affect sensitive DC subsystems.
- All ground vias should be connected to every ground plane. In addition, every power via should be connected to all power planes at equal potential. This helps reduce circuit inductance.
- Physically locate grounds between a signal path and its return. This minimizes the loop area.
- Avoid fast rise/fall times as much as possible. Signals with fast rise and fall times contain many high frequency harmonics which can radiate EMI.

- The ground plane beneath the filter/transformer module should be split (see Figure 7). The RJ-45 connector side of the transformer module should have chassis ground beneath it. By splitting ground planes beneath transformer, noise coupling between the primary and secondary sides of the transformer and between the adjacent coils in the transformer is minimized. There should not be a power plane under the magnetics module.

5.4 Schematic for EEPROM Footprints and LCI Connection

There are two options for EEPROM footprints. OEMs can choose either a common EEPROM footprint for the 82541ER, 82551ER(IT), 82562EZ(EX), and ICHx or an independent EEPROM footprint for each LAN silicon.

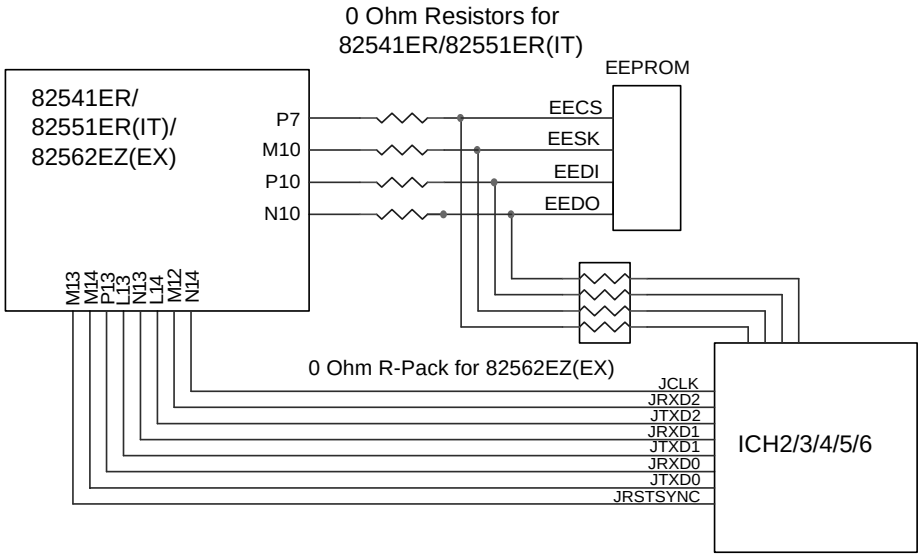


Figure 8. Common EEPROM Footprint for Both 82541ER, 82551ER(IT), and 82562EZ(EX)

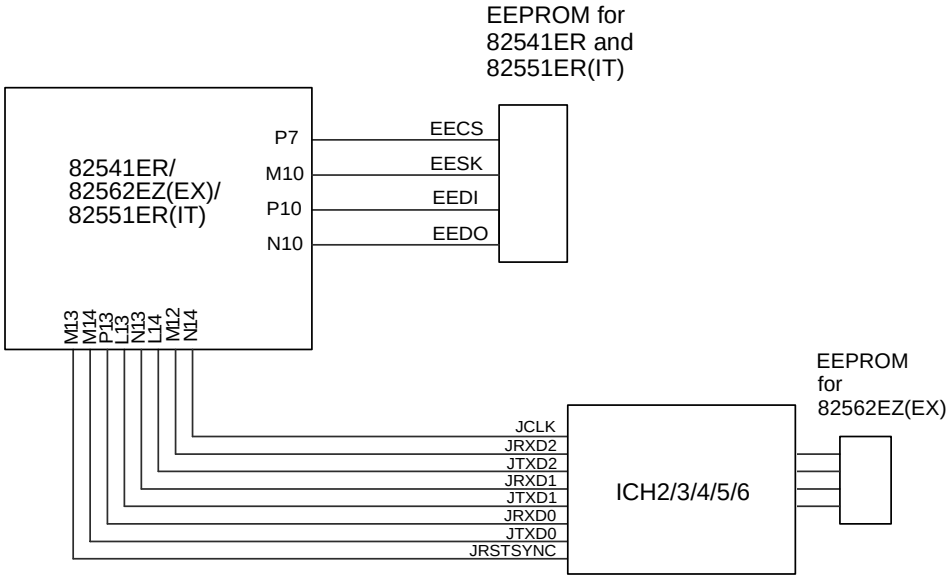


Figure 9. Independent EEPROM Footprints for Individual LAN Silicon

5.5 Termination of Unused Differential Signals on Gb Magnetics for 10/100 LOM Design

Since the number of differential signals are different between a 10/100 LAN silicon and a gigabit LAN silicon, the two major problems confronted in designing the dual footprint LOM design are:

1. Choosing the pin compatible magnetics modules for both 10/100 and gigabit silicon.
2. Terminating unused differential signals for gigabit between the selected magnetics module and RJ-45 connector when a 10/100 LAN design is implemented.

The three sections that follow provide the remedies for this issue.

5.5.1 Option 1: Board Level Stuffing

1. Layout resistor footprints on the pairs three and four of the differential traces for 82541ER LOM design. Refer to Figure 10.
2. Possibly rework the magnetics module for 10/100 to be footprint compatible with the magnetics for gigabit.

3. Replace the magnetics for the 82541ER with the one for the 82551ER(IT), or the 82562EZ(EX) and then populate R1/R2 and R3/R4 for a 82551ER(IT)/82562EZ(EX) LOM design. Refer to Figure 11.

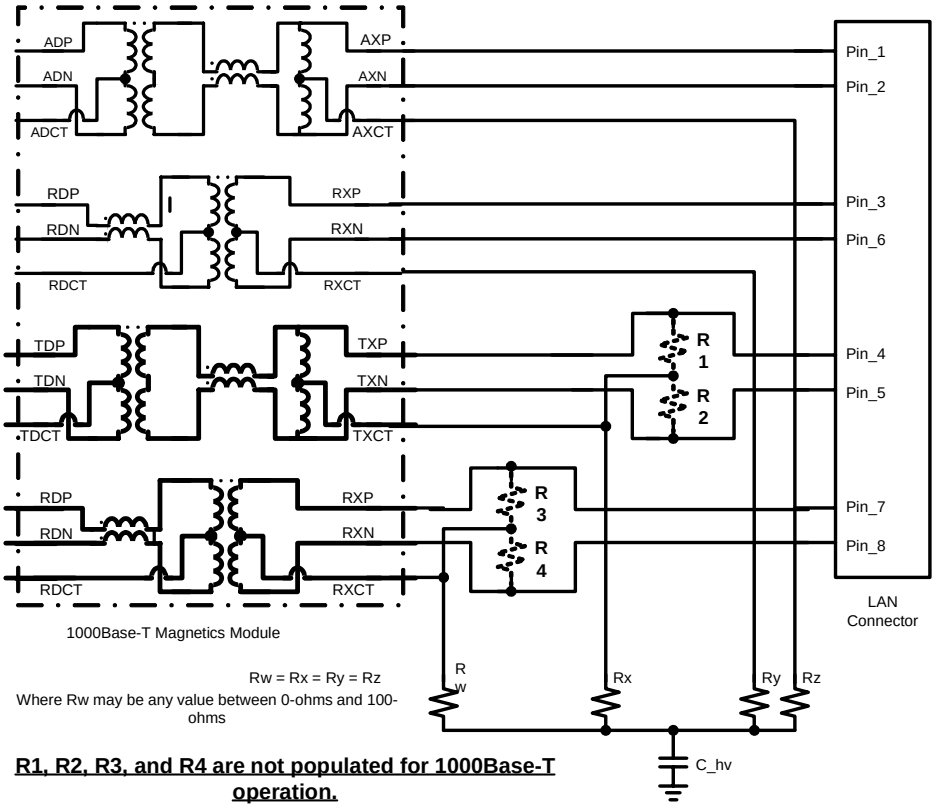


Figure 10. Typical Magnetics for Gb LAN Controller with Optional Resistors Footprint

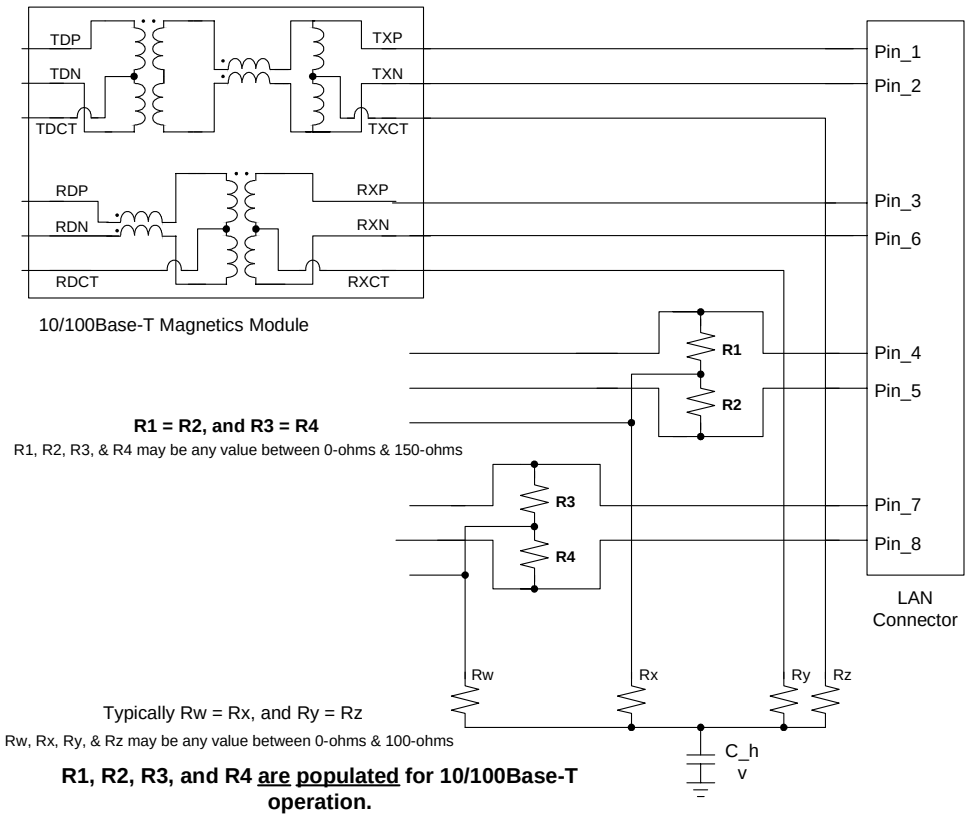


Figure 11. Replacement of Magnetics for 10/100 LAN Controller with Optional Resistors Populated

5.5.2 Option 2: Rework of Gigabit Magnetics[1]

Option two is a rework of a gigabit magnetics component with an internal jumper for 10/100 Mbps design.

In order to make a common footprint on differential pairs between the magnetics and RJ-45 connector for both 10/100 and Gigabit LOM design, one of the approaches is to rework the magnetics module for gigabit controller with internal jumpers to short pair three and four of differential signals. OEMs need to work with their magnetics vendors for this option.

1. Intel is working with some magnetics vendors to standardize the pinout assignments on magnetics modules.

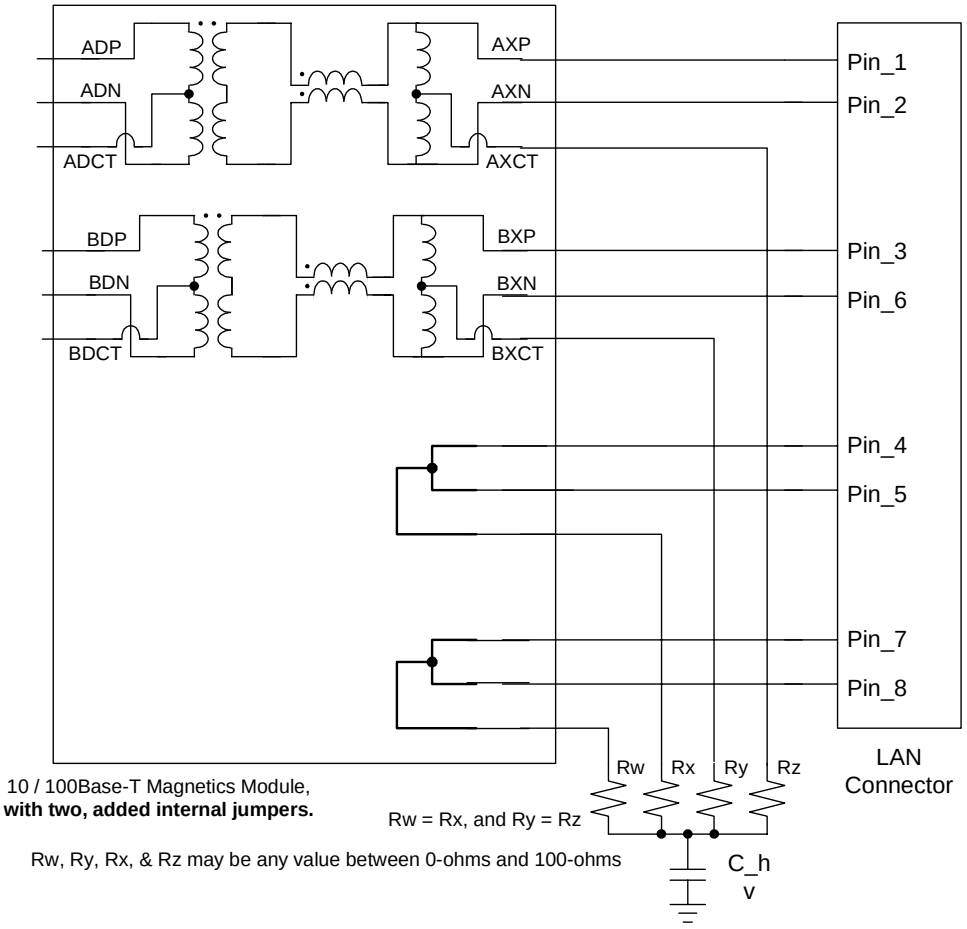


Figure 12. Rework of Gb Magnetics with Shorted Pair Three and Four on Differential Traces for 10/100 LOM Design

5.5.3 Option 3: Integrated Magnetics Module for 10/100 Mbps and Gigabit

Refer to Table 3.

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6.0 Selecting a Magnetics Module for 10/100/1000 LOM Designs

6.1 Qualifying Magnetics for 10/100/1000 LOM Design

One of the most important component choices in a 10/100 and 1000 Mbps Ethernet LOM design is the magnetics module. The module has a critical effect on overall IEEE and emission compliance. The device selected should meet the required design performance. Occasionally, components that meet basic specifications can cause the system (LOM, NIC, Repeater, etc.) to fail because of unintentional interactions with board effects. Examples of these phenomena could be an unexpected series of parallel capacitance values or expected series inductance values within the magnetics module. This can cause the design to fail certain IEEE specifications.

In order to help OEMs qualify a magnetics module, Intel provides the electrical specifications for magnetics modules used with Intel's LOM or NIC designs as a reference.

Table 3. Magnetics Modules Meeting Intel Specifications (Refer to Table 4 and Table 5)

	10/100	1000
Discrete Magnetics	H1012T / S558-5999-46 H1267 (82551ER/IT) MAC/PHY H1267 (82562EZ/EX) PHY)	H5007 (82541ER MAC/PHY)
Pulse (Discrete MDI-X)	H1338 (82551ER/IT only)	

Table 4. Electrical Specifications at 25°C for 10/100 Magnetics

Insertion Loss (TX / RX)	
0.1 through 0.999 MHz	1.0 dB maximum
1.0 through 15 MHz	0.35 dB maximum
15.1 through 6 0MHz	0.7 dB maximum
60.1 through 100 MHz	1.2 dB maximum
Return Loss (TX / RX)	
1.0 through 30 MHz	18 dB minimum
30.1 through 60 MHZ	19 - [20Log(f/30 MHz)] dB minimum
60.1 through 80 MHz	12 dB minimum
Transmit Common Mode-to-Common Mode Reject	
1.0 through 60 MHz	48 dB minimum
60.1 through 100 MHz	43 dB minimum
100.1 through 150 MHz	42 dB minimum
Effective Common Mode-to-Common Mode Reject	
1.0 through 60 MHz	38 dB minimum
60.1 through 100 MHz	34 dB minimum
100.1 through 150 MHz	32 dB minimum
Transmit Differential to Common Mode Reject	
1.0 through 60 MHz	38 dB minimum
60.1 through 100 MHz	35 dB minimum
100.1 through 150 MHz	32 dB minimum
Receive Differential to Common Reject	
1.0 THRU 60 MHz	30 dB minimum
60.1 through 100 MHz	25 dB minimum
100.1 through 150 MHz	20 dB minimum
Crosstalk Isolation (TX / RX)	
1.0 through 60 MHz	48 dB minimum
60.1 through 100 MHz	43 dB minimum
100.1 through 150 MHz	38 dB minimum
High Voltage Isolation	
IEEE 14.3.1.1	2250 V dc for 60 seconds
OCL with 8mA Bias 100 KHz	400 µH

Table 5. Electrical Specifications at 25° C for 1000 Gb Silicon

Insertion Loss (TX / RX)	
0.1 through 999 kHz	1.0 dB maximum
1.0 through 60.0 MHz	0.6 dB maximum
60.1 through 80.0 MHz	0.8 dB maximum
80.1 through 100.0 MHz	1.0 dB maximum
100 through 125.0 MHz	2.4 dB maximum
Return Loss (TX / RX)	
1.0 through 40.0 MHz	18 dB minimum
40.1 through 100 MHZ	12 - [20Log(f/80 MHz)] dB minimum
Common Mode-to-Common Mode Rejection	
1.0 through 60 MHz	48 dB minimum
60.1 through 100 MHz	42 dB minimum
100.1 through 150 MHz	37 dB minimum
Differential-to-Common Mode Rejection	
1.0 through 60 MHz	35 dB minimum
60.1 through 100 MHz	29 dB minimum
100.1 through 150 MHz	22 dB minimum
Crosstalk Isolation (TX / RX)	
1.0 through 80 MHz	36 dB minimum
80.1 through 150 MHz	27dB minimum
High Voltage Isolation	
1500 Vrms minimum, at 50 to 60 Hz, for 60 sec.	2250 V dc for 60 seconds
OCL with 8 mA Bias	400 uH minimum

Note: This page intentionally left blank.

7.0 EEPROM Information

The 82562EZ(EX), 82551ER(IT), and 82541ER EEPROMs are used for hardware and software configuration and are read be software to determine specific design features.

7.1 Serial EEPROM for 82562EZ(EX) Implementations

Serial EEPROM for LAN implementations based on 82562EZ(EX) devices connects to the ICH5. Depending upon the size of the EEPROM, the 82562EZ(EX) may or may not support legacy manageability. Table 6 and Table 7 list the EEPROM map for the 82562EZ(EX) PLC device. For details on the EEPROM, refer to the appropriate *I/O Control Hub 2, 3, 4, 5, 6, and 7 EEPROM Map and Programming Information*.

Table 6. 82562EZ(EX) Memory Layout (128 Byte EEPROM)

00h **3Fh**	HW/SW Reserved Area

NOTE: No manageability provided.

Table 7. 82562EZ(EX) Memory Layout (512 Byte EEPROM)

00h **3Fh**	HW/SW Reserved Area
40h **FFh**	ASF and Legacy Manageability

NOTE: Legacy manageability only.

7.2 Serial EEPROM for 82541ER Controller Implementations

82541ER Gigabit Ethernet Controllers can use either a Microwire* or an SPI* serial EEPROM. The EEPROM mode is selected on the EEMODE input (pin J4). A no connect denotes an SPI EEPROM and a pull-down resistor to ground denotes a Microwire EEPROM. Several words of the EEPROM are accessed automatically by the device after reset to provide pre-boot configuration data before it is accessed by host software. The remainder of the EEPROM space is available to software for storing the MAC address, serial numbers, and additional information.

For non-ASF applications, a 64 register by 16-bit Microwire serial EEPROM should be used, and for ASF 1.0 applications, a larger 93C66 Microwire or AT25040 SPI serial EEPROM. ASF 2.0 requires an 8 KB SPI serial EEPROM.

Intel has an MS-DOS* software utility called EEUPDATE, which can be used to program EEPROM images in development or production line environments. To obtain a copy of this program, contact your Intel representative.

The EEPROM access algorithm programmed into the 82541ER controller is compatible with most, but not all, commercially available 3.3 V Microwire* interface, serial EEPROM devices, with 64 x 16 (or 256 x 16) organization and a 1 MHz speed rating. The 82541ER EEPROM access algorithm drives extra pulses on the shift clock at the beginnings and ends of read and write cycles. The extra pulses may violate the timing specifications of some EEPROM devices. In selecting a serial EEPROM, choose a device that specifies “don't care” shift clock states between accesses.

Microwire EEPROMs that have been found to work satisfactorily with the 82541ER Gigabit Ethernet Controller are listed in Table 8.

Table 8. Microwire 64 x 16 Serial EEPROMs

Manufacturer	Manufacturer's Part Number
Atmel	AT93C46[1]
Catalyst	CAT93C46[1,2]

1. No manageability provided.
2. Revision H is not supported. Product die revision letter is marked on top of the package as a suffix to the production data code (e.g., AYWW**H**.)

SPI EEPROMs that have been found to work satisfactorily with the 82541ER device are listed in Table 9. SPI EEPROMs must be rated for a clock rate of at least 2 MHz.

Table 9. SPI Serial EEPROMs for 82541ER Controller

Application	Manufacturer	Manufacturer's Part Number
ASF 1.0 or IMPI pass through	ATMEL	AT25040
ASF 2.0 or IMPI advanced pass through	ATMEL	AT25080

7.2.1 EEPROM Map Information

Table 10 lists the EEPROM map for the 82541ER Gigabit Ethernet Controller. For details on the EEPROM, refer to the 82547GI(EI)/82541(PI/GI/EI)/82541ER EEPROM Map and Programming Information.

Table 10. 82541ER EEPROM Memory Layout

00h **3Fh**	HW/SW Reserved Area
40h **FFh**	ASF and Legacy Manageability
100h **19F**	Manageability Packet Filter Data
1A0 **...** **EEPROM END**	Loadable Manageability Firmware Code

7.3 82551ER(IT) EEPROM Map Information

Table 11 lists the EEPROM map for the 82551ER(IT) Fast Ethernet Controller. For details on the EEPROM, refer to the 82551QM/ER/IT EEPROM Map and Programming Information.

Table 11. 82551ER(IT) EEPROM Memory Layout

00h **3Fh**	HW/SW Reserved Area

Note: This page intentionally left blank.

8.0 Pin Number to Signal Mapping with Population Options

Table 12 lists the pin names for the three controllers and the corresponding shared ball reference value. Note that the 82541ER pin name in the 82541ER Datasheet/Design Guide is slightly different from the signal name on the reference schematics. The Datasheet/Design Guide signal names maintain consistency with the 64-bit gigabit controller naming conventions, while the schematic names follow the conventions used by our engineers on their design tools.

Table 12. Ball Number to Signal Mapping (Sheet 1 of 8)

				Population Options			
Ball Ref	**82541ER Pin Name**	**82551ER/ 82551IT Pin Name**	**82562EZ(EX) Pin Name**	**82541ER**	**82551ER/ 82551IT**	**82562EZ(EX)**	**Comments**
A1	NC	NC	NC				
A2	SERR#	SERR#	NC	SERR#	SERR#	No stuff	
A3	VCC	VCC	VCC	3.3 V	3.3 V	3.3 V	
A4	IDSEL	IDSEL	NC	IDSEL	IDSEL	No stuff	
A5	AD[25]	AD[25]	NC	AD[25]	AD[25]	No stuff	
A6	NC	PME#	NC	No stuff	PME#	No stuff	
A7	VCC	VCC	VCC	3.3 V	3.3 V	3.3 V	
A8	AD[30]	AD[30]	NC	AD[30]	AD[30]	No stuff	
A9	LAN_PWR_GOOD	ALTRST#	NC	Supervisor IC	3.3 V	No stuff	
A10	VCC	NC	NC	3.3 V			
A11	VCC	VCC	VCCT	3.3 V	3.3 V	3.3 V	VCCT = 3.3 V
A12	LINK_LED#	LILED#	LILED#	LINK_LED#	LINK_LED#	LINK_LED#	Same signal - different names.
A13	TEST	TEST	TESTEN	Pull-down	Pull-down	Pull-down	May have LAN Disable logic connected to this signal for 82562EZ(EX).
A14	NC	NC	NC				
B1	AD[22]	AD[22]	NC	AD[22]	AD[22]	No stuff	
B2	AD[23]	AD[23]	NC	AD[23]	AD[23]	No stuff	
B3	VSS	VSSPP	VSS				
B4	AD[24]	AD[24]	NC	AD[24]	AD[24]	No stuff	
B5	AD[26]	AD[26]	NC	AD[26]	AD[26]	No stuff	
B6	AD[27]	AD[27]	NC	AD[27]	AD[27]	No stuff	
B7	VSS	VSSPP	VSS				
B8	AD[31]	AD[31]	NC	AD[31]	AD[31]	No stuff	
B9	RST#	ISOLATE#	NC	RST#	RST#	No stuff	
B10	VCC	NC	NC	3.3 V			
B11	LINK100#	SPDLED#	SPDLED#	LED	LED	LED	Same signal - different names.

Table 12. Ball Number to Signal Mapping (Sheet 2 of 8)

				Population Options			
Ball Ref	**82541ER Pin Name**	**82551ER/ 82551IT Pin Name**	**82562EZ(EX) Pin Name**	**82541ER**	**82551ER/ 82551IT**	**82562EZ(EX)**	**Comments**
B12	LINK1000#	TO	TOUT	LED	No stuff	No stuff	Testability output for 82562EZ(EX)/ 82551ER(IT).
B13	CTRL18	RBIAS100	RBIAS100	Pwr Regulator	649 pull-down	649 pull-down	Connect to PNP or to pull-down.
B14	IEEE_TEST+	RBIAS10	RBIAS10	NC	619 pull-down	619 pull-down	Install resistor or not.
C1	AD[21]	AD[21]	NC	AD[21]	AD[21]	No stuff	
C2	M66EN	RST#	NC	M66EN	3.3 V	No stuff	
C3	REQ#	REQ#	NC	REQ#	REQ#	No stuff	
C4	C/BE#[3]	C/BE#[3]	NC	C/BE#[3]	C/BE#[3]	No stuff	
C5	NC	NC	NC				
C6	AD[28]	AD[28]	NC	AD[28]	AD28	No stuff	
C7	AD[29]	AD[29]	NC	AD[29]	AD29	No stuff	
C8	NC	CLK_RUN#	NC	CLK_RUN#	CLK_RUN#	No stuff	
C9	VCC	NC	NC	3.3 V			
C10	VSS	VSSPT	VSS				
C11	ACTIVITY#	ACTLED#	ACTLED#	LED	LED	LED	Same signal - different names.
C12	AVSS	VREF	VSS	VSS	VSS	VSS	AVSS = VREF = VSS
C13	MDI[0+]	TDP	TDP	MDI	MDI	MDI	Same signal - different names.
C14	MDI[0-]	TDN	TDN	MDI	MDI	MDI	Same signal - different names.
D1	AD[18]	AD[18]	NC	AD[18]	AD[18]	No stuff	
D2	AD[19]	AD[19]	NC	AD[19]	AD[19]	No stuff	
D3	AD[20]	AD[20]	NC	AD[20]	AD[20]	No stuff	
D4	VSS	VSS	VSS				
D5	VSS	VSS	VSS				
D6	VSS	VSS	VSS				
D7	VSS	VSS	VSS				
D8	VSS	VSS	VSS				
D9	NC	NC	NC				
D10	NC	NC	ISOL_EXEC	NC	NC	NC	May have LAN Disable logic connected to this signal for 82562EZ(EX).
D11	ANALOG_1.8 V	NC	NC	1.8 V	NC	No stuff	PHY Power Plane
D12	CLKR_1.8 V	TI	ISOL_TI	1.8 V	No stuff	No stuff	May have LAN Disable logic connected to this signal for 82562EZ(EX).

Table 12. Ball Number to Signal Mapping (Sheet 3 of 8)

				Population Options			
Ball Ref	**82541ER Pin Name**	**82551ER/ 82551IT Pin Name**	**82562EZ(EX) Pin Name**	**82541ER**	**82551ER/ 82551IT**	**82562EZ(EX)**	**Comments**
D13	AVSS	TEXEC	VSS	VSS	VSS	VSS	AVSS = VSS
D14	IEEE_TEST-	TCK	ISOL_TCK	2-pin header	NC	NC	May have LAN Disable logic connected to this signal for 82562EZ(EX).
E1	VCC	VCC	VCC	3.3 V	3.3 V	3.3 V	
E2	VSS	VSSPP	VSS				
E3	AD[17]	AD[17]	NC	AD[17]	AD[17]	No stuff	
E4	VSS	VSS	VSS				
E5	VSS	VSS	VSS				
E6	VSS	VSS	VSS				
E7	VSS	VSS	VSS				
E8	VSS	VSS	VSS				
E9	VSS	VSS	VSS				
E10	VSS	VSS	VSS				
E11	ANALOG_1.2 V	NC	VCCT	1.2 V	NC	3.3 V	Core Power Plane
E12	ANALOG_1.2 V	VCC	VCCT	1.2 V	3.3 V	3.3 V	Core Power Plane
E13	MDI[1]+	RDP	RDP	MDI	MDI	MDI	Same signal - different names.
E14	MDI[1]-	RDN	RDN	MDI	MDI	MDI	Same signal - different names.
F1	IRDY#	IRDY#	NC	IRDY#	IRDY#	No stuff	
F2	FRAME#	FRAME#	NC	FRAME#	FRAME#	No stuff	
F3	C/BE#[2]	C/BE#[2]	NC	C/BE#[2]	C/BE#[2]	No stuff	
F4	VSS	VSS	VSS				
F5	VSS	VSS	VSS				
F6	VSS	VSS	VSS				
F7	VSS	VSS	VSS				
F8	VSS	VSS	VSS				
F9	VSS	VSS	VSS				
F10	VSS	VSS	VSS				
F11	AVSS	VSS	VSS	VSS	VSS	VSS	AVSS = VSS
F12	NC	FLD2	NC	NC	NC	NC	
F13	MDI[2]+	FLD1	NC	Magnetics	Magnetics	Magnetics	10/100 Magnetics will not have a pin connected here
F14	MDI[2]-	FLD0	NC	Magnetics	Magnetics	Magnetics	10/100 Magnetics will not have a pin connected here
G1	CLK	CLK	NC	CLK	CLK	No stuff	

Table 12. Ball Number to Signal Mapping (Sheet 4 of 8)

				Population Options			
Ball Ref	**82541ER Pin Name**	**82551ER/ 82551IT Pin Name**	**82562EZ(EX) Pin Name**	**82541ER**	**82551ER/ 82551IT**	**82562EZ(EX)**	**Comments**
G2	VIO	VIO	NC	VIO	VIO	VIO	
G3	TRDY#	TRDY#	NC	TRDY#	TRDY#	No stuff	
G4	PLL_1.2 V	NC	NC	1.2 V	NC	NC	
G5	1.2 V	VCC	VCCR	1.2 V	3.3 V	3.3 V	Core Power Plane
G6	1.2 V	VCC	VCC	1.2 V	3.3 V	3.3 V	Core Power Plane
G7	VSS	VSS	VSS				
G8	VSS	VSS	VSS				
G9	VSS	VSS	VSS				
G10	VSS	VSS	VSS				
G11	AVSS	VSS	VSS	VSS	VSS	VSS	AVSS = VSS
G12	ANALOG_1.8 V	FLD3	NC	1.8 V	No stuff	No stuff	PHY Power Plane
G13	ANALOG_1.2 V	VCC	VCC	1.2 V	3.3 V	3.3 V	Core Power Plane
G14	AVSS	VSSPL	VSS				AVSS = VSS = VSSPL
H1	STOP#	STOP#	NC	STOP#	STOP#	No stuff	
H2	INTA#	INTA#	NC	INTA#	INTA#	No stuff	
H3	DEVSEL#	DEVSEL#	NC	DEVSEL#	DEVSEL#	No stuff	
H4	PLL_1.2 V	NC	NC	1.2 V	No stuff	No stuff	
H5	1.2 V	VCC	VCCR	1.2 V	3.3 V	3.3 V	Core Power Plane
H6	1.2 V	VCC	VCC	1.2 V	3.3 V	3.3 V	Core Power Plane
H7	1.2 V	VCC	VCC	1.2 V	3.3 V	3.3 V	Core Power Plane
H8	1.2 V	VCC	VCC	1.2 V	3.3 V	3.3 V	Core Power Plane
H9	VSS	VSS	VSS				
H10	VSS	VSS	VSS				
H11	ANALOG_1.2 V	NC	VCC	1.2 V	No stuff	3.3 V	Core Power Plane
H12	NC	FLD6	NC	NC	NC	NC	
H13	MDI[3]+	FLD5	NC	Magnetics	Magnetics	Magnetics	10/100 Magnetics will not have a pin connected here
H14	MDI[3]-	FLD4	NC	Magnetics	Magnetics	Magnetics	10/100 Magnetics will not have a pin connected here
J1	PAR	PAR	NC	PAR	PAR	No stuff	
J2	PERR#	PERR#	NC	PERR#	PERR#	No stuff	
J3	GNT#	GNT#	NC	GNT#	GNT#	No stuff	

Table 12. Ball Number to Signal Mapping (Sheet 5 of 8)

				Population Options			
Ball Ref	**82541ER Pin Name**	**82551ER/ 82551IT Pin Name**	**82562EZ(EX) Pin Name**	**82541ER**	**82551ER/ 82551IT**	**82562EZ(EX)**	**Comments**
J4	EEMODE	NC	NC	Pull-down or NC	NC	NC	82541ER: Connect a pull-down for Microwire and a NC for SPI
J5	1.2 V	VCC	VCCR	1.2 V	3.3 V	3.3 V	Core Power Plane
J6	1.2 V	VCC	VCC	1.2 V	3.3 V	3.3 V	Core Power Plane
J7	1.2 V	VCC	VCC	1.2 V	3.3 V	3.3 V	Core Power Plane
J8	1.2 V	VCC	VCC	1.2 V	3.3 V	3.3 V	Core Power Plane
J9	1.2 V	VCC	VCC	1.2 V	3.3 V	3.3 V	Core Power Plane
J10	1.2 V	VCCR	VCC	1.2 V	3.3 V	3.3 V	Core Power Plane
J11	1.2 V	VCCR	VCC	1.2 V	3.3 V	3.3 V	Core Power Plane
J12	AUX_PWR	FLA1	NC	AUX_PWR	No stuff	No stuff	
J13	XTAL_1.8 V	FLA0	NC	1.8 V	No stuff	No stuff	PHY Power Plane
J14	XTAL2	FLD7	X2		No stuff		
K1	AD[16]	AD[16]	NC	AD[16]	AD[16]	No stuff	
K2	VSS	VSSPP	VSS				VSSPP = VSS
K3	VCC	VCC	VCC	3.3 V	3.3 V	3.3 V	
K4	VCC	VCC	VCC	3.3 V	3.3 V	3.3 V	
K5	1.2 V	VCC	VCC	1.2 V	3.3 V	3.3 V	Core Power Plane
K6	1.2 V	VCC	VCC	1.2 V	3.3 V	3.3 V	Core Power Plane
K7	1.2 V	VCC	VCC	1.2 V	3.3 V	3.3 V	Core Power Plane
K8	1.2 V	VCC	VCC	1.2 V	3.3 V	3.3 V	Core Power Plane
K9	1.2 V	VCC	VCC	1.2 V	3.3 V	3.3 V	Core Power Plane
K10	1.2 V	VCC	VCC	1.2 V	3.3 V	3.3 V	Core Power Plane
K11	1.2 V	VCC	VCC	1.2 V	3.3 V	3.3 V	Core Power Plane
K12	AVSS	VSSPL	VSS	VSS	VSS	VSS	AVSS = VSSPL =VSS
K13	VCC	VCC	VCC	3.3 V	3.3 V	3.3 V	
K14	XTAL1	FLA2	X1		No stuff		
L1	AD[14]	AD[14]	NC	AD[14]	AD[14]	No stuff	
L2	AD[15]	AD[15]	NC	AD[15]	AD[15]	No stuff	
L3	C/BE#[1]	C/BE#[1]	NC	C/BE#[1]	C/BE#[1]	No stuff	

Table 12. Ball Number to Signal Mapping (Sheet 6 of 8)

				Population Options			
Ball Ref	**82541ER Pin Name**	**82551ER/ 82551IT Pin Name**	**82562EZ(EX) Pin Name**	**82541ER**	**82551ER/ 82551IT**	**82562EZ(EX)**	**Comments**
L4	1.2 V	VCC	VCC	1.2 V	3.3 V	3.3 V	Core Power Plane
L5	1.2 V	VCC	VCC	1.2 V	3.3 V	3.3 V	Core Power Plane
L6	VSS	VSS	VSS				
L7	NC	NC	ADV10	NC	NC	NC	
L8	NC	NC	NC	NC	NC	No stuff	PHY Power Plane
L9	1.2 V	VCC	VCC	1.2 V	3.3 V	3.3 V	Core Power Plane
L10	1.2 V	VCC	VCC	1.2 V	3.3 V	3.3 V	Core Power Plane
L11	VSS	VSS	VSS				
L12	JTAG_TMS	FLA5	NC	NC	NC	NC	
L13	JTAG_TRST#	FLA4	JTXD[1]	LCI	LCI	LCI	ICH drives this signal low. TRST needs to be grounded to disable JTAG. JTAG becomes difficult to use.
L14	JTAG_TCK	FLA3	JTXD[2]	LCI	LCI	LCI	ICH drives this signal low. TCK needs to be biased. JTAG becomes difficult to use.
M1	AD[11]	AD[11]	NC	AD[11]	AD[11]	No stuff	
M2	AD[12]	AD[12]	NC	AD[12]	AD[12]	No stuff	
M3	AD[13]	AD[13]	NC	AD[13]	AD[13]	No stuff	
M4	C/BE#[0]	C/BE#[0]	NC	C/BE#[0]	C/BE#[0]	No stuff	
M5	AD[5]	AD[5]	NC	AD[5]	AD[5]	No stuff	
M6	VSS	VSSPP	VSS				
M7	AD[1]	AD[1]	NC	AD[1]	AD[1]	No stuff	
M8	NC	FLOE#	NC	NC	NC	NC	
M9	FLSH_CE#	FLWE#	NC	NC	NC	NC	
M10	EESK	FLA15/ EESK	NC	EESK	EESK	EESK	If EE from ICH and 82551ER(IT) are shared, a zero Ω pop is required because ICH drives this in reset.
M11	FLSH_SI	FLA12	NC	NC	NC	NC	
M12	SDP[3]	FLA11	JRXD[2]	LCI	LCI	LCI	ICH expects this signal to be high or undriven.
M13	JTAG_TDI	FLA7	JRSTSYNC	LCI	LCI	LCI	ICH expects this signal to be high or undriven. JTAG becomes difficult to use.

Table 12. Ball Number to Signal Mapping (Sheet 7 of 8)

				Population Options			
Ball Ref	**82541ER Pin Name**	**82551ER/ 82551IT Pin Name**	**82562EZ(EX) Pin Name**	**82541ER**	**82551ER/ 82551IT**	**82562EZ(EX)**	**Comments**
M14	JTAG_TDO	FLA6	JTXD[0]	LCI	LCI	LCI	ICH expects this signal to be high or undriven. JTAG becomes difficult to use.
N1	VSS	VSSPP	VSS				VSSPP = VSS
N2	AD[10]	AD[10]	NC	AD[10]	AD[10]	No stuff	
N3	AD[9]	AD[9]	NC	AD[9]	A[D9]	No stuff	
N4	AD[7]	AD[7]	NC	AD[7]	AD[7]	No stuff	
N5	AD[4]	AD[4]	NC	AD[4]	AD[4]	No stuff	
N6	VCC	VCC	VCC	3.3 V	3.3 V	3.3 V	
N7	AD[0]	AD[0]	NC	AD[0]	AD[0]	No stuff	
N8	VCC	VCC	VCC	3.3 V	3.3 V	3.3 V	
N9	FLSH_SCK	FLCS#	NC	NC	NC	NC	
N10	EEDO	FLA14/ EEDO	NC	EEDO	EEDO	EEDO	If desired, this can be shorted to the ICH EEDI b/c it is an input in ICH in reset.
N11	NC	X1	NC	NC	X1	NC	
N12	VSS	VSSPL	VSSP	VSS	VSS	VSS	VSSP = VSSPL = VSS
N13	SDP[2]	FLA10	JRXD[1]	LCI	LCI	LCI	ICH expects this signal to be high or undriven.
N14	SDP[0]	FLA8/ IOCHRDY	JCLK	LCI	LCI	LCI	ICH expects this signal to be low or undriven.
P1	NC	NC	NC				
P2	VCC	VCC	VCC	3.3 V	3.3 V	3.3 V	
P3	AD[8]	AD[8]	NC	AD[8]	AD[8]	No stuff	
P4	AD[6]	AD[6]	NC	AD[6]	AD[6]	No stuff	
P5	AD[3]	AD[3]	NC	AD[3]	AD[3]	No stuff	
P6	AD[2]	AD[2]	NC	AD[2]	AD[2]	No stuff	
P7	EECS	EECS	NC	EECS	EECS	EECS	If EE from ICH and 82551ER(IT) are shared, a zero Ω pop is required because ICH drives this in reset.
P8	VSS	VSSPL	VSS	VSS	VSS	VSS	VSSPL = VSS
P9	FLSH_SO	FLA16	NC	LAN_EN	LAN_EN	LAN_EN	Connect to LAN Enable signal
P10	EEDI	FLA13/ EEDI	NC	EEDI	EEDI	EEDI	If desired, this can be shorted to the ICH EEDI because it is an input in ICH in reset.

Table 12. Ball Number to Signal Mapping (Sheet 8 of 8)

				Population Options			
Ball Ref	**82541ER Pin Name**	**82551ER/ 82551IT Pin Name**	**82562EZ(EX) Pin Name**	**82541ER**	**82551ER/ 82551IT**	**82562EZ(EX)**	**Comments**
P11	CTRL12	X2	NC	Pwr Regulator	X2	No stuff	Connect to PNP. Don't' stuff PNP on 82562EZ(EX).
P12	VCC	VCC	VCC	3.3 V	3.3 V	3.3 V	
P13	SDP[1]	FLA9	JRXD[0]	LCI	LCI	LCI	ICH expects this signal to be high or undriven.
P14	NC	NC	NC	NC	NC	NC	

9.0 Self-Review Checklist for Combined Footprint LOM

A Portable Data Format (PDF) Self-Review Checklist for a Combined Footprint LOM is available to aid designers via:

http://developer.intel.com

Note: This page intentionally left blank.

10.0 Reference Schematic

The following pages contain reference schematics for the 82562EZ(EX)/82551ER(IT) and the 82541ER Combined Footprint LOM Design Guide.

REVISIONS		
REV	DESCRIPTION	DATE

82541ER, 82551ER/IT or 82562EZ/EX REFERENCE DESIGN

15mm x 15mm BGA

1mm pitch

A = Install component if using 82541ER MAC/PHY

B = Install component if using 82551ER/IT MAC/PHY

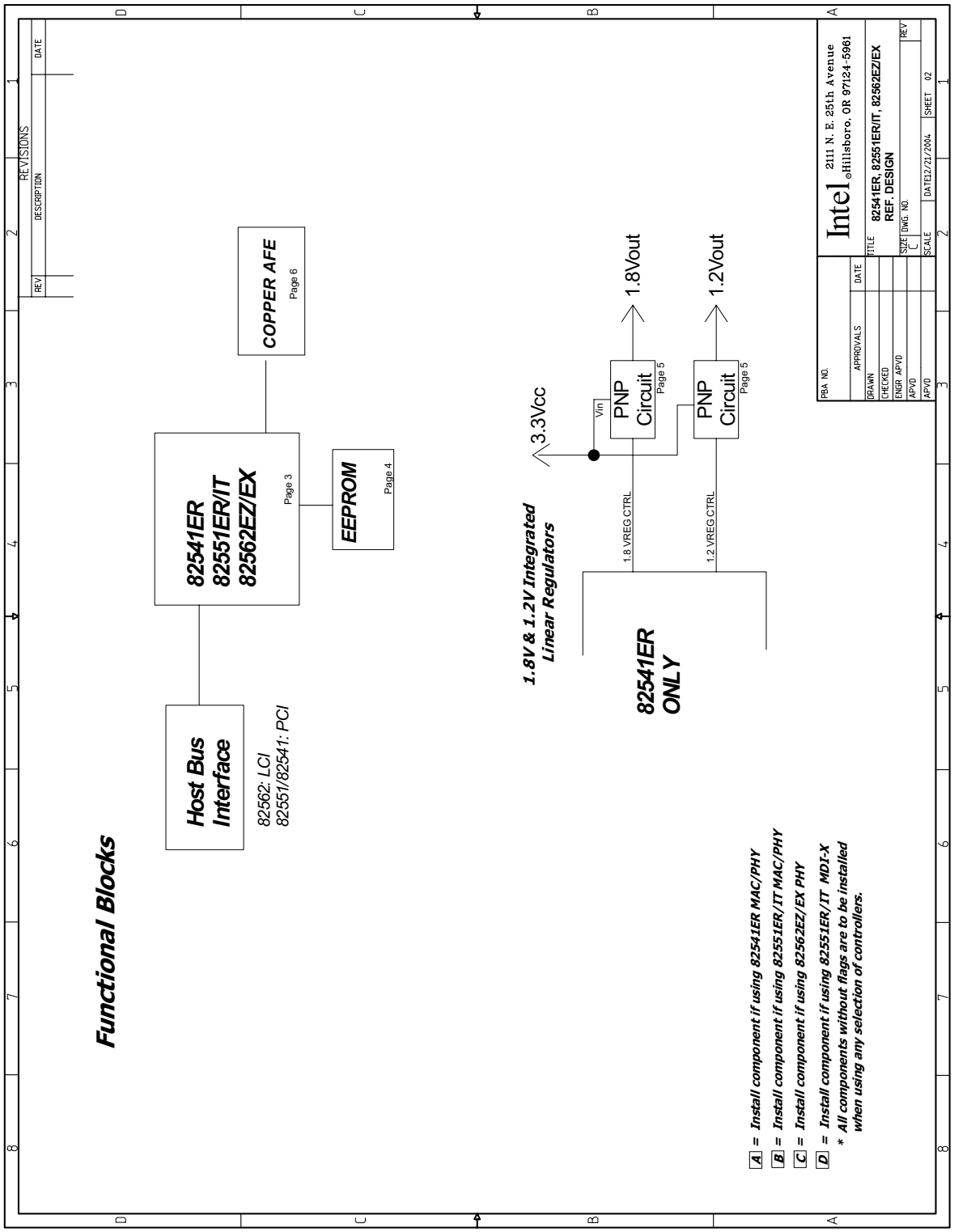
C = Install component if using 82562EZ/EX PHY

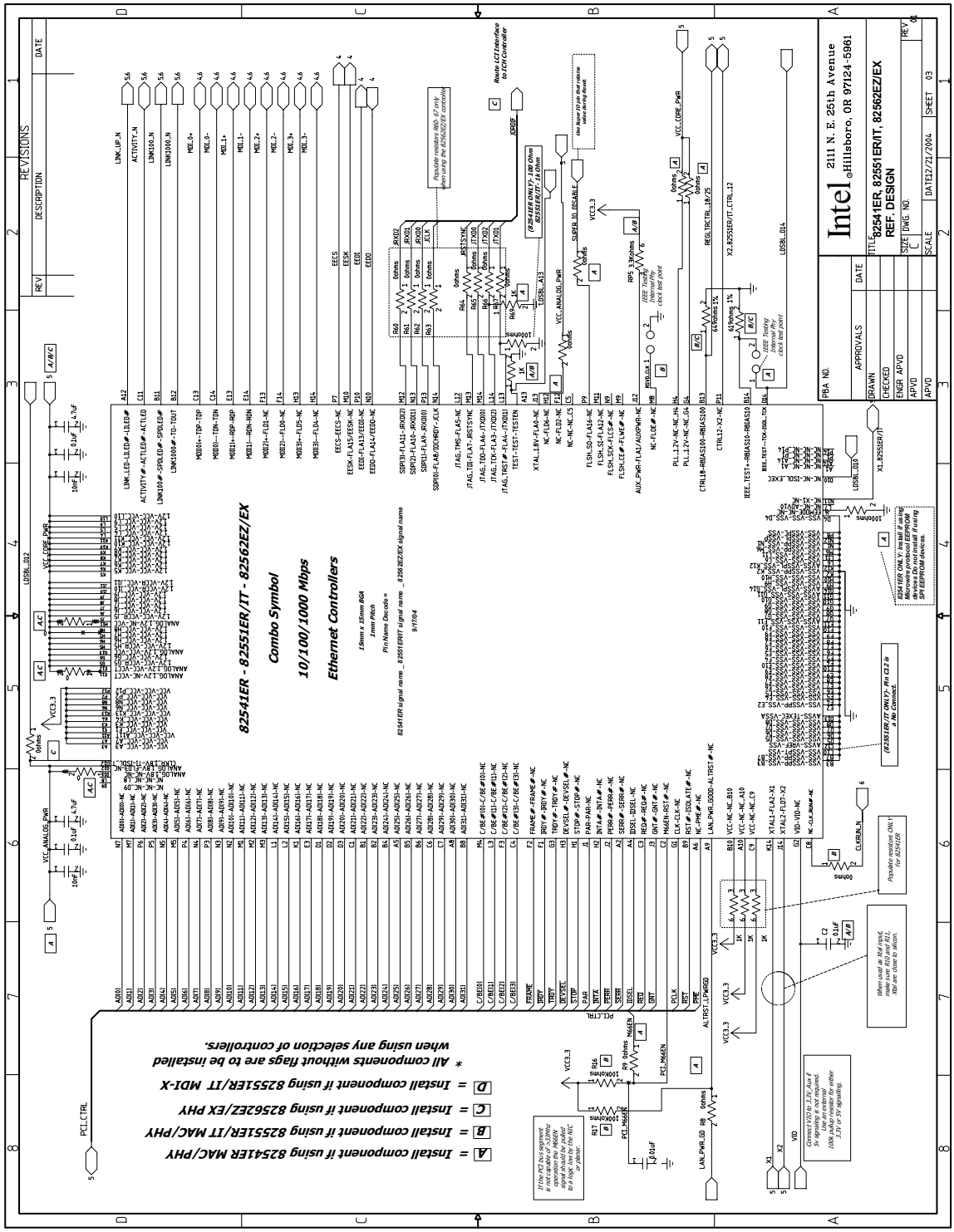
D = Install component if using 82551ER/IT MDI-X

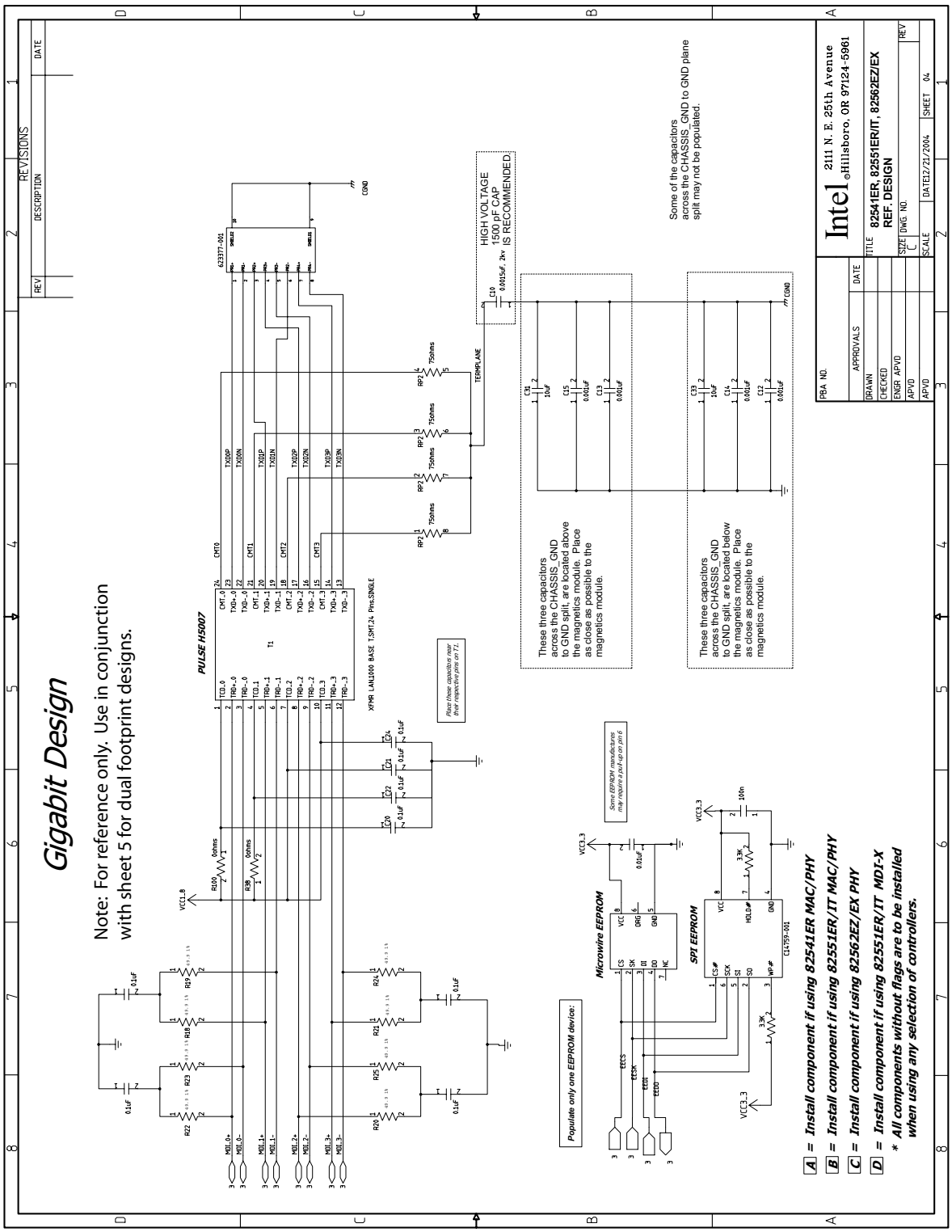
** All components without flags are to be installed when using any selection of controllers.*

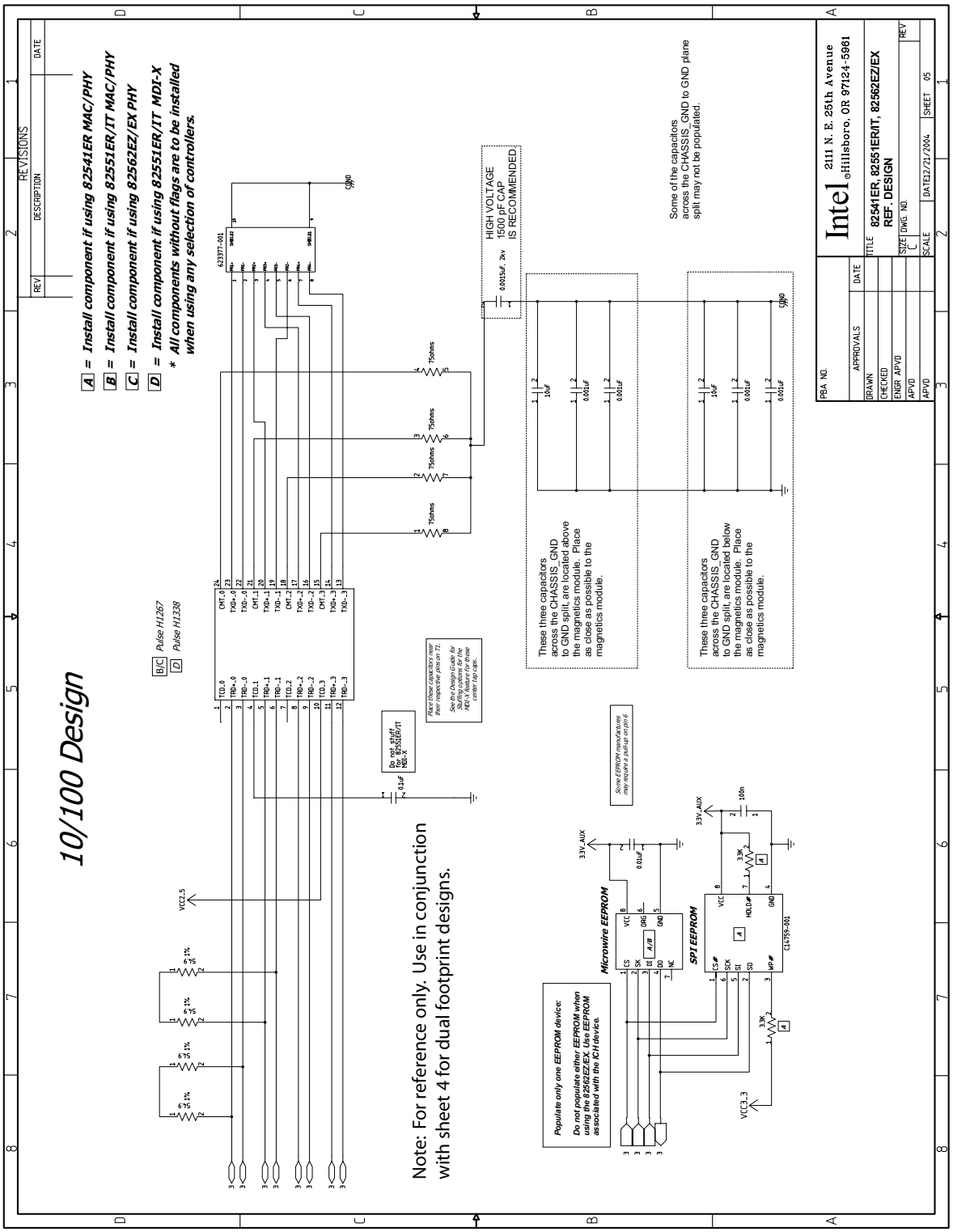
REV 2.6
10/20/04

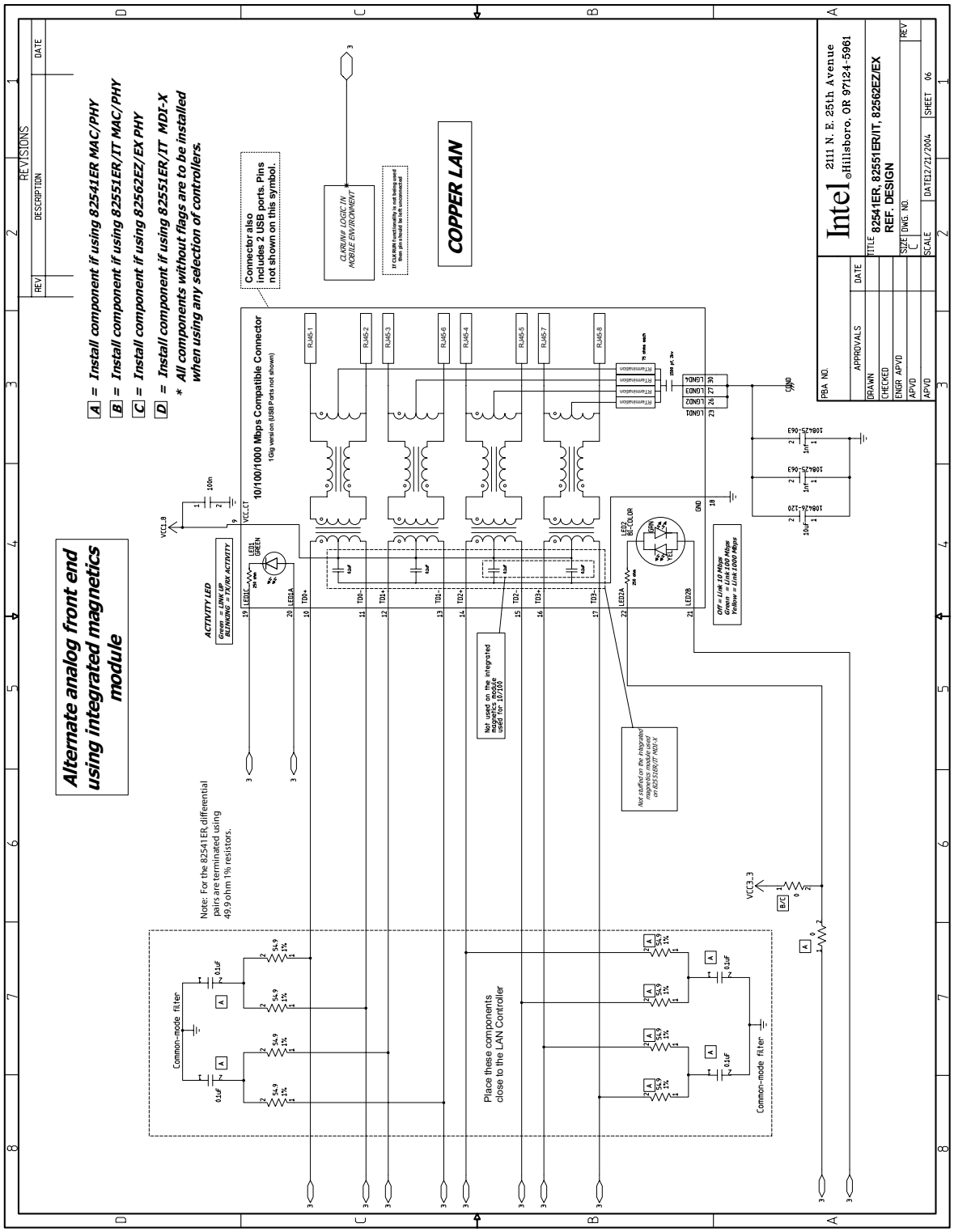
PBA NO.		Intel 2111 N. E. 25th Avenue ©Hillsboro, OR 97124-5961		
APPROVALS	DATE	TITLE	82541ER, 82551ER/IT, 82562EZ/EX REF. DESIGN	
DRAWN		SIZE C	DWG. NO.	REV
CHECKED		SCALE	DATE 12/21/2004	SHEET 01
ENGR APVD				
APVD				
APVD				

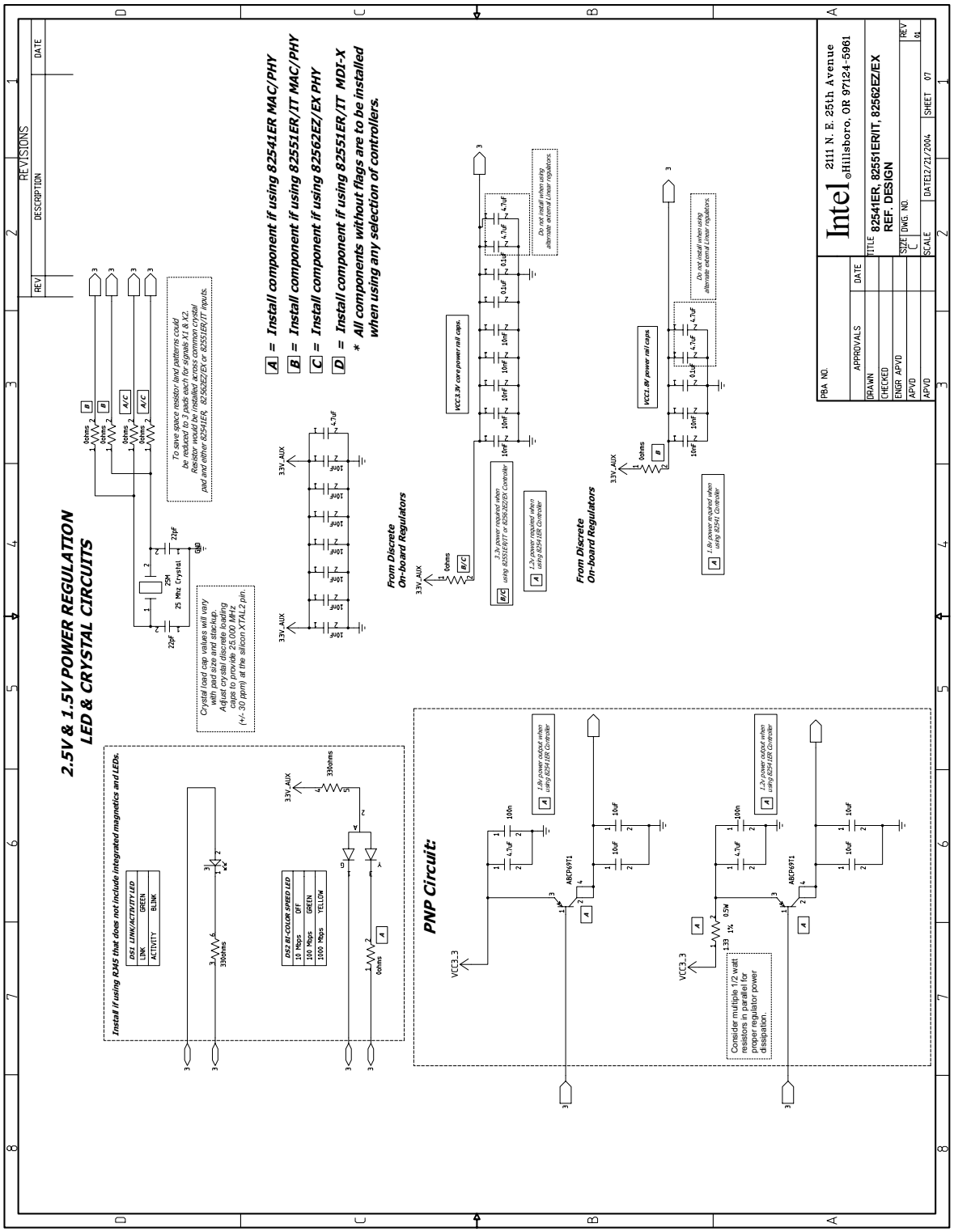

Functional Blocks
Host Bus Interface
82562: LCI
82551/82541: PCI
82541ER
82551ER/IT
82562EZ/EX
Page 3
COPPER AFE
Page 6
EEPROM
Page 4
1.8V & 1.2V Integrated Linear Regulators
3.3Vcc
Vin
PNP Circuit
Page 5
1.8Vout
1.8 VREG CTRL
PNP Circuit
Page 5
1.2Vout
1.2 VREG CTRL
82541ER ONLY
A = Install component if using 82541ER MAC/PHY
B = Install component if using 82551ER/IT MAC/PHY
C = Install component if using 82562EZ/EX PHY
D = Install component if using 82551ER/IT MDI-X
* All components without flags are to be installed when using any selection of controllers.
REVISIONS
REV
DESCRIPTION
DATE
PBA NO.
APPROVALS
DATE
DRAWN
CHECKED
ENGR APVD
APVD
APVD
Intel
2111 N. E. 25th Avenue
Hillsboro, OR 97124-5961
TITLE
82541ER, 82551ER/IT, 82562EZ/EX
REF. DESIGN
SIZE
C
DWG. NO.
REV
SCALE
DATE12/21/2004
SHEET 02

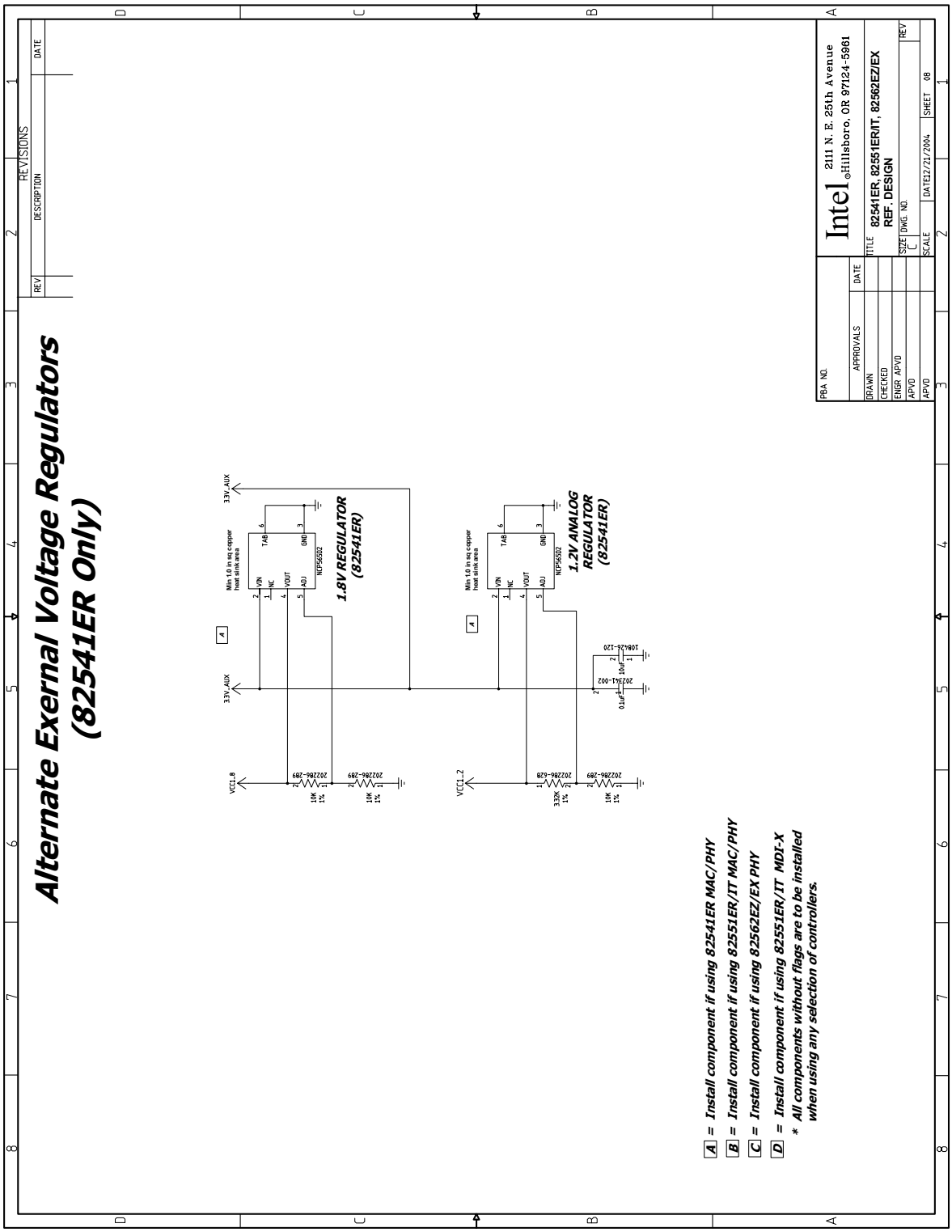

82541ER - 82551ER/IT - 82562EZ/EX
Combo Symbol
10/100/1000 Mbps
Ethernet Controllers
19mm x 19mm BGA
1mm Pitch
Pin Name Decode =
82541ER signal name _ 82551ER/IT signal name _ 82562EZ/EX signal name
9/17/04
A = Install component if using 82541ER MAC/PHY
B = Install component if using 82551ER/IT MAC/PHY
C = Install component if using 82562EZ/EX PHY
D = Install component if using 82551ER/IT MDI-X
* All components without flags are to be installed when using any selection of controllers.
Intel
2111 N. E. 25th Avenue
Hillsboro, OR 97124-5961
82541ER, 82551ER/IT, 82562EZ/EX
REF. DESIGN

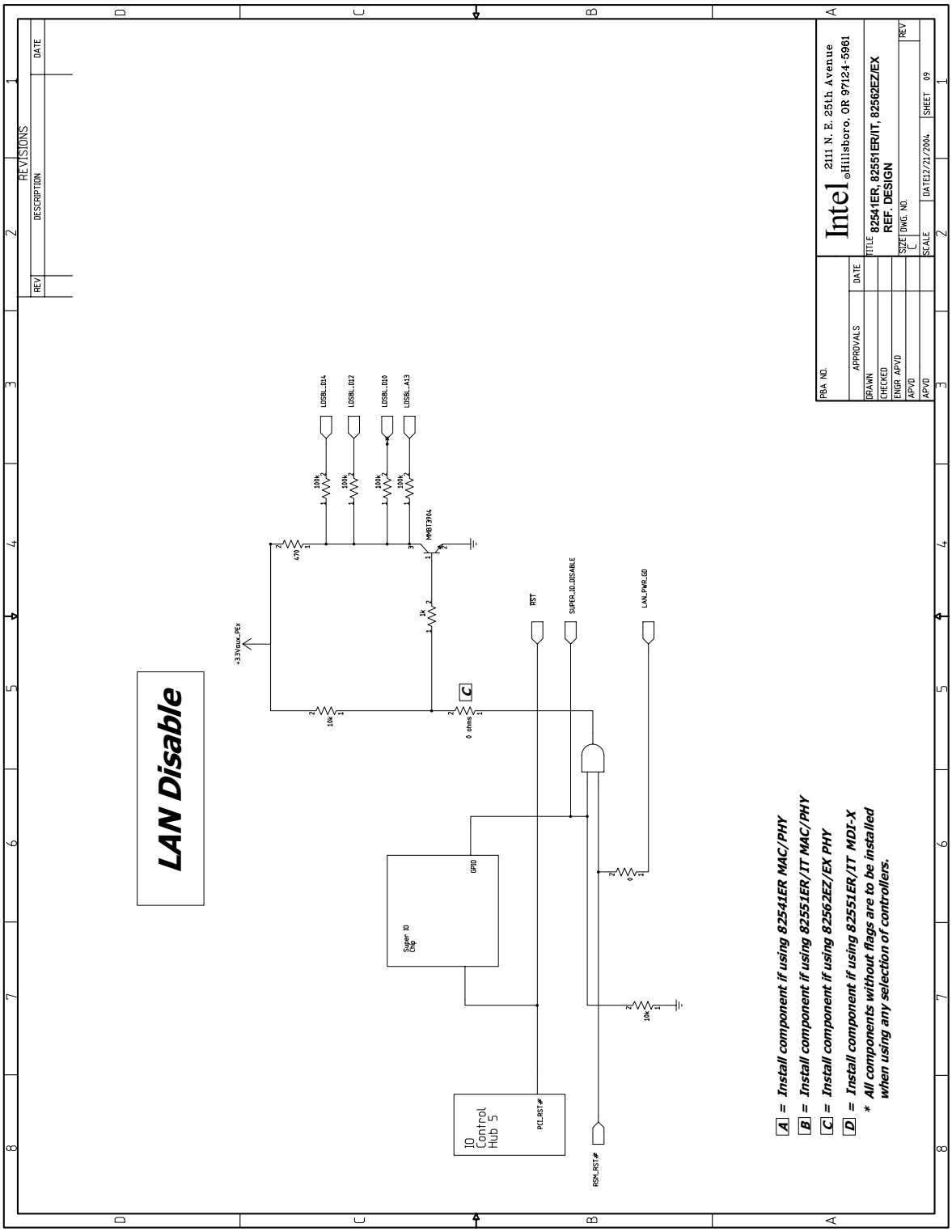

Gigabit Design
Note: For reference only. Use in conjunction with sheet 5 for dual footprint designs.
REVISIONS
REV
DESCRIPTION
DATE
PULSE H5007
XFMR LAN1400 BASE T,SMT,24 Pins,SINGLE
HIGH VOLTAGE 1500 pF CAP IS RECOMMENDED.
These three capacitors across the CHASSIS_GND to GND split, are located above the magnetics module. Place as close as possible to the magnetics module.
These three capacitors across the CHASSIS_GND to GND split, are located below the magnetics module. Place as close as possible to the magnetics module.
Some of the capacitors across the CHASSIS_GND to GND plane split may not be populated.
Microwire EEPROM
SPI EEPROM
Populate only one EEPROM device:
A = Install component if using 82541ER MAC/PHY
B = Install component if using 82551ER/IT MAC/PHY
C = Install component if using 82562EZ/EX PHY
D = Install component if using 82551ER/IT MDI-X
* All components without flags are to be installed when using any selection of controllers.
Intel 2111 N. E. 25th Avenue ©Hillsboro, OR 97124-5961
TITLE 82541ER, 82551ER/IT, 82562EZ/EX REF. DESIGN
SIZE C
DWG. NO.
REV
SCALE
DATE 12/21/2004
SHEET 04
PBA NO.
APPROVALS
DRAWN
CHECKED
ENGR APVD
APVD
APVD


10/100 Design
A = Install component if using 82541ER MAC/PHY
B = Install component if using 82551ER/IT MAC/PHY
C = Install component if using 82562EZ/EX PHY
D = Install components if using 82551ER/IT MDI-X
* All components without flags are to be installed when using any selection of controllers.
B/C Pulse H1267
D Pulse H1338
Note: For reference only. Use in conjunction with sheet 4 for dual footprint designs.
HIGH VOLTAGE 1500 pF CAP IS RECOMMENDED
Some of the capacitors across the CHASSIS_GND to GND plane split may not be populated.
These three capacitors across the CHASSIS_GND to GND split, are located above the magnetics module. Place as close as possible to the magnetics module.
These three capacitors across the CHASSIS_GND to GND split, are located below the magnetics module. Place as close as possible to the magnetics module.
Place these capacitors near their respective pins on IT.
See the Design Guide for stuffing options for the 82551ER/IT MDI-X center tap caps.
Populate only one EEPROM device:
Do not populate either EEPROM when using the 82562EZ/EX. Use EEPROM associated with the ICH device.
Microwire EEPROM
SPI EEPROM
Some EEPROM implementations may require a pull-up on pin 6
Intel 2111 N. E. 25th Avenue Hillsboro, OR 97124-5961
TITLE 82541ER, 82551ER/IT, 82562EZ/EX REF. DESIGN
SIZE C
DWG. NO.
REV
SCALE
DATE 12/21/2004
SHEET 05


A = Install component if using 82541ER MAC/PHY
B = Install component if using 82551ER/IT MAC/PHY
C = Install component if using 82562EZ/EX PHY
D = Install component if using 82551ER/IT MDI-X
* All components without flags are to be installed when using any selection of controllers.
COPPER LAN
Alternate analog front end using integrated magnetics module
10/100/1000 Mbps Compatible Connector
Connector also includes 2 USB ports. Pins not shown on this symbol.
ACTIVITY LED
Green = LINK UP BLINKING = TX/RX ACTIVITY
Note: For the 82541ER, differential pairs are terminated using 49.9 ohm 1% resistors.
Common-mode filter
Place these components close to the LAN Controller
Intel 2111 N.E. 25th Avenue Hillsboro, OR 97124-5961
82541ER, 82551ER/IT, 82562EZ/EX
REF. DESIGN


2.5V & 1.5V POWER REGULATION
LED & CRYSTAL CIRCUITS
A = Install component if using 82541ER MAC/PHY
B = Install component if using 82551ER/IT MAC/PHY
C = Install component if using 82562EZ/EX PHY
D = Install component if using 82551ER/IT MDI-X
* All components without flags are to be installed when using any selection of controllers.
REVISIONS
REV
DESCRIPTION
DATE
Install if using RJ45 that does not include integrated magnetics and LEDs.
DS1: LINK/ACTIVITY LED
LINK GREEN
ACTIVITY BLINK
DS2 BI-COLOR SPEED LED
10 Mbps Off
100 Mbps GREEN
1000 Mbps YELLOW
330ohms
0ohms
25 MHz Crystal
25M
22pF
To save space resistor land patterns could be reduced to 3 pads each for signals X1 & X2. Resistor would be installed across common crystal pad and either 82541ER, 82562EZ/EX or 82551ER/IT inputs.
Crystal load cap values will vary with pad size and stackup. Adjust crystal load capacitor caps to provide 25.000 MHz (+/- 30 ppm) at the silicon XTAL2 pin.
3.3V_AUX
From Discrete On-board Regulators
VCC3.3V core power rail caps.
VCC1.8V power rail caps.
Do not install when using alternate external Linear regulators.
3.3v power required when using 82551ER/IT or 82562EZ/EX Controller
1.8v power required when using 82541ER Controller
PNP Circuit:
VCC3_3
ABCP6971
Consider multiple 1/2 watt resistors in parallel for proper regulator power dissipation.
PBA NO.
APPROVALS
DATE
DRAWN
CHECKED
ENGR APVD
APVD
APVD
Intel 2111 N.E. 25th Avenue ©Hillsboro, OR 97124-5961
TITLE 82541ER, 82551ER/IT, 82562EZ/EX REF. DESIGN
SIZE
DWG. NO.
REV
SCALE
DATE12/21/2004
SHEET 07


Alternate Exernal Voltage Regulators
(82541ER Only)
REVISIONS
REV
DESCRIPTION
DATE
1.8V REGULATOR
(82541ER)
1.2V ANALOG
REGULATOR
(82541ER)
3.3V_AUX
VCC1_8
VCC1_2
NCP5602
Intel
2111 N. E. 25th Avenue
Hillsboro, OR 97124-5961
82541ER, 82551ER/IT, 82562EZ/EX
REF. DESIGN
A = Install component if using 82541ER MAC/PHY
B = Install component if using 82551ER/IT MAC/PHY
C = Install component if using 82562EZ/EX PHY
D = Install component if using 82551ER/IT MDI-X
* All components without flags are to be installed
when using any selection of controllers.


LAN Disable
REVISIONS
REV
DESCRIPTION
DATE
PBA NO.
APPROVALS
DATE
DRAWN
CHECKED
ENGR APVD
APVD
APVD
Intel
2111 N. E. 25th Avenue
Hillsboro, OR 97124-5961
TITLE 82541ER, 82551ER/IT, 82562EZ/EX
REF. DESIGN
SIZE C
DWG. NO.
REV
SCALE
DATE 12/21/2004
SHEET 09
LOSBL_D14
LOSBL_D12
LOSBL_D10
LOSBL_A13
100k
470
MMBT3904
+3.3Vaux_PEx
1k
10k
0 ohms
C
RST
SUSPEND_DISABLE
LAN_PWR_GD
0
Super IO Chip
GPIO
IO Control Hub 5
PCI_RST#
RSM_RST#
A = Install component if using 82541ER MAC/PHY
B = Install component if using 82551ER/IT MAC/PHY
C = Install component if using 82562EZ/EX PHY
D = Install component if using 82551ER/IT MDI-X
* All components without flags are to be installed when using any selection of controllers.

Appendix A Measuring LAN Reference Frequency Using a Frequency Counter

A.1 Background

To comply with IEEE specifications for 10/100 Mbps and 10/100/1000Base-T Ethernet LAN, the transmitter reference frequency must be correct and accurate within ±50 parts per million (ppm).

Note: Intel recommends a frequency tolerance of ±30 (ppm).

Most Intel LAN devices will operate properly with a 25.000 MHz reference crystal, provided it meets the recommended requirements for frequency stability, equivalent series resistance at resonance (ESR), and load capacitance.

Most circuits for series resonant crystals include two discrete capacitors (typically C1 and C2), with values between 5 pF and 36 pF.

The most accurate way to determine the appropriate value for the discrete capacitors is to install the approximately correct values for C1 and C2. Next, a frequency counter should be used to measure the transmitter reference frequency (or transmitter reference clock).

- If the transmitter reference frequency is more than 20 ppm below the target frequency, then the values for C1 and C2 are too big and should be decreased.
- If the transmitter reference frequency is more than 20 ppm above the target frequency, then the values for C1 and C2 are too small and should be increased.

This Appendix provides instructions and illustrations that explain how to use a frequency counter and probe to determine the Ethernet LAN device transmit center frequency. An example describing how to calculate the frequency accuracy of the measured and averaged center frequency with respect to the target center frequency is also included.

A.2 Required Test Equipment

- Tektronix CMC-251, or similar high resolution, digital counter
- Tektronix P6246, or similar high bandwidth, low capacitance (less than 1 pF) probe
- Tektronix 1103, or similar probe power supply or probe amplifier
- BNC, 50 Ω coaxial cable (less than 6 feet long)
- System with power supply and test software for the LAN circuit to be tested

A.3 Indirect Probing Method

The indirect probing test method is applicable foremost devices that support 100BASE-T. Since probe capacitance can load the reference crystal and affect the measured frequency, the preferred method is to use the indirect probing test method when possible.

Almost all Intel LAN silicon that support 1000BASE-T Ethernet can provide a buffered 125 MHz clock, which can be used for indirect probing of the transmitter reference clock. The buffered 125 MHz clock will be a 5X multiple of the crystal circuit's reference frequency (Figure 13).

Different LAN devices may require different register settings, to enable the buffered 125 MHz reference frequency. Please obtain the settings or instructions that are appropriate for the LAN controller you are using.

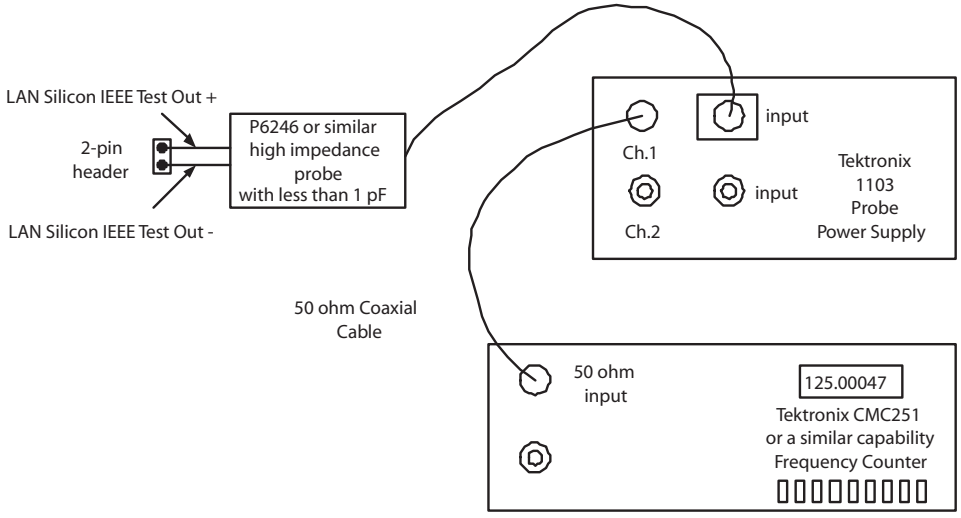


Figure 13. Indirect Probing Setup

A.4 Indirect Frequency Measurement and Frequency Accuracy Calculation Steps

1. Make sure the system BIOS has the LAN controller enabled.
2. Connect the test equipment as shown in Figure 13.
3. Using the appropriate controls for your model of high resolution digital counter, make sure it can display ~125.0000 MHz with at least four decimal places frequency resolution.
4. Enable the 125 MHz buffered reference clock.
5. Determine the center reference frequency as accurately as possible. This can be done by taking 30 to 50 different readings using the frequency counter and then calculating the average results of the readings.
6. Calculate the accuracy of the measured and averaged center frequency with respect to an ideal 125.0000 MHz reference frequency.

$$FrequencyAccuracy(ppm) = \frac{(x-y)}{(y/1000000)}$$

where x = Average measured frequency in Hertz and
y = Ideal reference frequency in Hertz

Example 1.

Given: The measured averaged center frequency is 124.99942 MHz (or 124,999,420 Hertz).

$$FrequencyAccuracy(ppm) = \frac{(124999420 - 125000000)}{(125000000/1000000)} = -4.64ppm$$

Example 2.

Given: The measured averaged center frequency is 125.00087 MHz (or 125,000,870 Hertz).

$$FrequencyAccuracy(ppm) = \frac{(125000870 - 125000000)}{(125000000 / 1000000)} = 6.96ppm$$

Note: The following items should be noted for an ideal reference crystal on a typical printed circuit board.

- If the transmitter reference frequency is more than 8 ppm below the target frequency, then the values for C1 and C2 are too big and they should be decreased. When tests are performed across temperature, it may be acceptable for the center frequency deviation to be a little greater than 8 ppm.
- If the transmitter reference frequency is more than 8 ppm above the target frequency, then the values for C1 and C2 are too small and they should be increased. When tests are performed across temperature, it may be acceptable for the center frequency deviation to be a little greater than 8 ppm.

A.5 Direct Probing Test Method, Applicable for Most 10/100 Devices (Devices that do NOT support 1000Base-T)

Because probe capacitance can load the reference crystal affecting the measured frequency, it is preferable to use a probe with less than 1 pF capacitance.

The probe should be connected between the X2 (or Xout) pin of the LAN device and a nearby ground. Typically, it is possible to connect the probe pins across one of the discrete load capacitors (C2 in Figure 14).

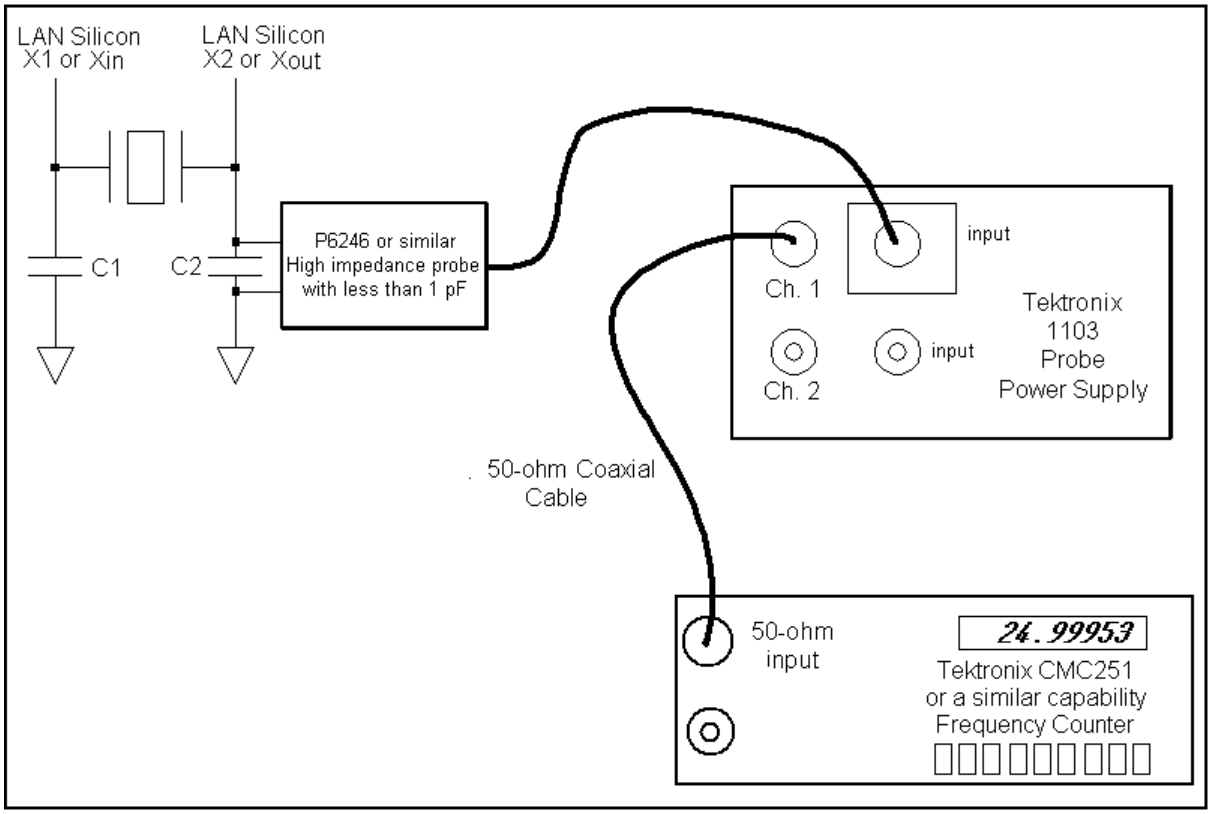


Figure 14. Direct Probing Method

A.6 Direct Frequency Measurement and Frequency Accuracy Calculation Steps

1. Make sure the system BIOS has the LAN controller enabled.
2. Connect the test equipment as shown in Figure 14.
3. Using the appropriate controls for your model of high resolution digital counter, make sure it can display ~25.0000 MHz with at least four decimal places frequency resolution.
4. Ensure the LAN circuits are powered.
5. Determine the center reference frequency as accurately as possible. This can be done by taking 30 to 50 different readings using the frequency counter and then calculating the average results of the readings.
6. Calculate the accuracy of the measured and averaged center frequency with respect to an ideal 25.0000 MHz reference frequency.

$$FrequencyAccuracy(ppm) = \frac{(x - y)}{(y / 1000000)}$$

where x = Average measured frequency in Hertz and
y = Ideal reference frequency in Hertz

Example 3.

Given: The measured averaged center frequency is 24.99963 MHz (or 24,999,630 Hertz).

$$FrequencyAccuracy(ppm) = \frac{(24999630 - 25000000)}{(25000000 / 1000000)} = -14.8ppm$$

Example 4.

Given: The measured averaged center frequency is 25.00027 MHz (or 25,000,270 Hertz).

$$FrequencyAccuracy(ppm) = \frac{(25000270 - 25000000)}{(25000000 / 1000000)} = 10.8ppm$$

Note: The following items should be noted for an ideal reference crystal on a typical printed circuit board.

- If the transmitter reference frequency is more than 8 ppm below the target frequency, then the values for C1 and C2 are too big and they should be decreased. When tests are performed across temperature, it may be acceptable for the center frequency deviation to be a little greater than 8 ppm.
- If the transmitter reference frequency is more than 8 ppm above the target frequency, then the values for C1 and C2 are too small and they should be increased. When tests are performed across temperature, it may be acceptable for the center frequency deviation to be a little greater than 8 ppm.

Appendix B GigConf.exe Register Settings for 82541ER Devices

The following steps describe the indirect probing test method using GigConf.exe for 82541ER devices.

1. Boot to DOS using a DOS Boot Diskette.
2. Launch Gigconf from the diskette (gigconf.exe).
3. Select the Intel network connection to be measured.
   a. If multiple adapters are installed, use the arrow keys to navigate to highlight the selected adapter and press Enter.
4. Select Registers by pressing “R”.
5. Select PHY Registers by pressing “P”.
6. Use the arrow keys to navigate to the value listed next to address 0000.
7. Press Enter when the value is highlighted and then use Backspace to clear out the current value.
8. Type “0100” for the value and then press Enter.
9. Navigate to the value listed next to address 0012.
10. Press Enter to select the highlighted value and use Backspace to clear the current value.
11. Type “8000” for the value and then press Enter.
12. Navigate to the Set Address field on the right side of the screen (use the right arrow key)
13. Press Enter to select the highlighted value and then use Backspace to clear out the current value.
14. Type “4011” for the value and then press Enter.
    This changes the PHY register screen and updates it with new addresses and values.
15. Use the arrow keys to navigate to the value for address 4011.
16. Press Enter when the value is highlighted and then use Backspace to clear the current value.
17. Type “8000” for the value and then press Enter.
18. Use the right arrow key to navigate to the Set Address field on the right side of the screen.
19. Press Enter when the value is highlighted and use Backspace to clear the current value.
20. Enter “2F5B” (capital letters are not required) for the address and then press Enter.
21. Use the arrow keys to navigate to the value for address “2F5B”.
22. Press Enter when the value is highlighted and then use Backspace to clear the current value.
23. Type “0003” for the value and then press Enter.
24. Use the right arrow key to navigate to the Set Address field on the right side of the screen.
25. Press Enter when the value is highlighted and then use Backspace to clear the current value.

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