Started on	Friday, 29 October 2021, 10:25 AM
State	Finished
Completed on	Friday, 29 October 2021, 10:30 AM
Time taken	4 mins 58 secs
Marks	1.00/1.00
Grade	**10.00** out of 10.00 (**100**%)

Question 1

Correct

Mark 1.00 out of 1.00

Consider the following VHDL description of a process.

```
1. architecture sig of dummy is
2. signal sig1: integer := 1;
3. signal sig2: integer := 2;
4. signal sig3: integer := 0;
5. -- clk and sum are defined in the entity declaration as input bit and output integer, respectively.
6. begin
7.   process (clk)
8.   begin
9.     if (rising_edge(clk)) then
10.       sig1 <= sig2;
11.       sig2 <= sig3;
12.       sig3 <= sig1 + sig2;
13.       sum <= sig3;
14.     endif;
15.   end process;
16. end sig;
```

clk is a clock with a period of 10 ns with +ve edges at 5 ns, 15 ns and so on, and –ve edges at 10ns, 20ns and so on. Note that at t = 0 ns, the process is executed, but the statements are not, as the (*rising_edge*(*clk*)) is “false”. Which of the following is the correct value of *sig2* after 18 ns?

Select one:

- 2
- 0
- 1
- None of the given options
- 3 ✓

Your answer is correct.

The correct answer is: 3