COL215 Digital Logic and System Design

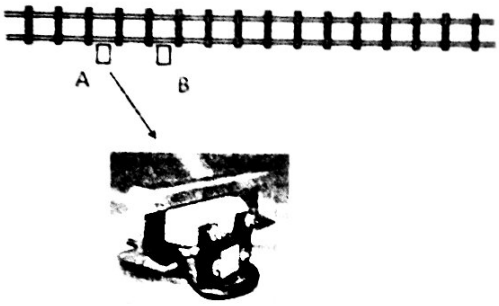
24.11.2016 **Major Test** **Max Marks: 20**

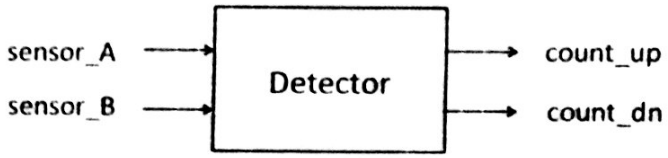
Note: Q 1 to Q 4 are compulsory. Do any 2 out of Q 5 to Q 7.

1. Design a synchronous FSM for sequentially comparing two unsigned numbers. Let the numbers be A = < a_7, a_6, … , a_1, a_0 > and B = < b_7, b_6, … , b_1, b_0 >. The numbers are received bit by bit, synchronised with a clock, going from LSBs (a_0 and b_0) to MSBs (a_7 and b_7). At the end, the FSM produces the result indicating whether A > B or A = B or A < B. You need to only draw a state transition diagram or a state transition table for this FSM.

[4]

2. An axle counter is a system that keeps a count of the number of axles of railway coaches and engines entering and exiting a section of railway track. At each end of the section, a pair of sensors is placed. Each sensor produces a pulse signal as a wheel passes by it. A direction detector at each end identifies the direction of wheel movement by looking at the order in which pulses are produced by the two sensors and sends signals to an up-down counter accordingly. The direction detector is an asynchronous FSM with inputs and outputs as shown below.





If there is a pulse on sensor_A followed by a pulse on sensor_B, a pulse is produced on count_up, coinciding with sensor_B pulse. If the order of the input pulses is reversed, a pulse is output on count_dn. If two consecutive pulses are produced by any of the sensors, it indicates movement of a wheel across a sensor and then reversing and crossing it again. Therefore such pulses are ignored. Construct the flow table for the direction detector FSM.

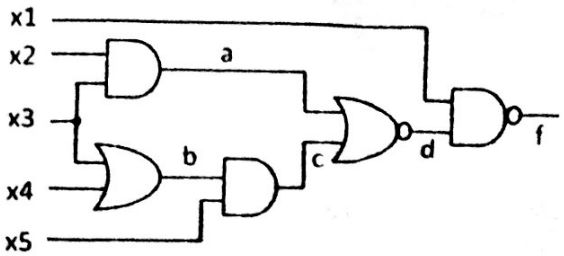
[4]

3. Design an ASM chart for the GCD computation algorithm given below. Show a block diagram of the datapath required to implement your ASM chart.

```
X = A
Y = B
while (X ≠ Y) do
   if (X > Y) X = X - Y
   else Y = Y - X
end while
G = X
```

[4]

4. For the circuit shown below, find a test pattern using D algorithm to detect a single stuck-at-1 fault at c. What other single stuck-at faults can this test pattern detect?



5. Design a static hazard free SOP implementation for the boolean function given below.

$$f = a.b'.c.d' + a.b'.c.d + a'.b'.c'.d' + a'.b.c'.d' + a'.b.c'.d + a.b.c'.d + a'.b.c.d + a.b.c.d$$

[2

6. Suppose the inputs of the circuit of Q 4 are driven by a register consisting of 5 D flip-flops and the signal f forms input of another D flip-flop. Assume that the propagation delay of each gate is 2 ns. Also assume that the output delay, set-up time and hold time of each flip-flop are 1 ns, 2 ns and 1 ns, respectively. Find the maximum clock frequency for this circuit if there is no clock skew. What is the maximum clock skew that this circuit can tolerate?

[2]

7. (a) Give transistor level circuit for a CMOS tri-state buffer or an SRAM cell. Explain in 4 lines how this circuit functions. (b) Show the structure of a floating gate NMOS transistor and explain in 4 lines how it is used as a programmable switch.

Time period > 3ns × 2

[2]