10.10.2016 **COL215 Digital Logic and System Design**
Minor Test 2 **Max Marks: 10**

1. Manually carry out binary unsigned division of 110101 by 000101, showing all the steps that would take place in a sequential divider circuit. The quotient as well as the remainder should be expressed as 6 bit unsigned numbers. [2]

2. Boolean expressions defining a combinational circuit with 4 inputs and 3 outputs are given below. Give realization for this circuit using a NOR-NOR PLA with 4 inputs, 3 outputs and only 5 product terms. Any number of inverters can be used at inputs and outputs.

   x = a'b'd + ab'cd' + a'bd
   y = ab'c' + a'b'cd' + abc'
   z = a'b'c + ab'd' + b'cd' + bcd' [3]

3. Design a parallel array multiplier for multiplying two 4 bit unsigned numbers and producing a 4 bit product using carry save addition. The multiplier has another output to indicate overflow. For example, multiplying 3 and 4 will give the product = 12 and overflow = 0, whereas multiplying 10 and 7 will give product = 6 (i.e., 70 mod 16) and overflow = 1.You can use full adders and two input gates of any type. Try to use as few adders and gates as possible. [3]

4. Why is a transmission gate built using two transistors - one NMOS and one PMOS. Why is it not good to use just one transistor. [2]