You can preview this quiz, but if this were a real attempt, you would be blocked because:

This quiz is not currently available

Question 1

Not yet answered

Not graded

Please carefully read the following statement: "I confirm that during this exam, I will neither give any help to other students nor receive any help from other students. I understand that providing or receiving an answer in this exam is academic misconduct for which I could be penalized as per the decision of the course instructor." Do you agree with this statement?

Select one:

- ○ Yes (I agree with the above statement and would like to continue with this exam.)
- ○ No (I do not agree with the above statement and would like to skip this exam.)

Question 2

Not yet answered

Marked out of 15.00

You are given the following Boolean expression

$y = ((a' \cdot b') + (b \cdot c'))' \cdot ((a' \cdot c) + (b \cdot c))$

(a) Draw a CMOS circuit without transforming or modifying it.

(b) Draw a CMOS circuit after simplifying it.

Question 3

Not yet answered

Marked out of 10.00

Minimize the logic needed to realize the following function, $f(a,b,c,d) = \sum m(0,1,3,9) + \sum d(2,11,15)$. Here, m and d refer to the minterms and don't care terms, respectively. You can use either Karnaugh Map or Quine McCluskey method.

Question 4

Not yet answered

Marked out of 15.00

You are given the following Sum-of-Product (SoP) expression.

$f(a, b, c, d, e) = abcde' + ab'd + ab'ce$

(a) Write the Product-of-Sum (PoS) expression.

(b) Draw a NAND-only circuit to realize the function. You can use NAND gates with up to five inputs.

(c) Draw a NOR-only circuit to realize the function. You can use NOR gates with up to five inputs.

Question 5

Not yet answered

Marked out of 15.00

A circuit takes two inputs: (1) a 4-bit number X = $x_3x_2x_1x_0$ and (2) a 2-bit number $C = c_1c_0$. The output of the circuit is a 4-bit number $Y = y_3y_2y_1y_0$. Based on the numerical value of the input C, the circuit can rotate the bit-vector in X by 0, 1, 2, or 3 positions to the right. In this rotation, the shifted-out bits on the right are placed into the vacated positions on the left. For example, if we have $X = 0110$ and $C = 01$, X is rotated by one position to the right and hence $Y = 0011$. Similarly, if $X = 0110$ and $C = 10$, $Y = 1001$.

(a) Design this circuit using 4:1 multiplexers and a minimal number of 2-input AND and 2-input OR gates.

(b) Identify the critical path (the one causing the largest delay) in your circuit.

Question 6

Not yet answered

Marked out of 15.00

You are given the task to design an overlapping pattern recognition circuit to detect the pattern “0010” in an input stream. As discussed in the class, this can be implemented by storing the count of the number of matched bits at the discrete-time i in a variable c_i.

(a) Write down the truth table using the inputs and outputs for the circuit.

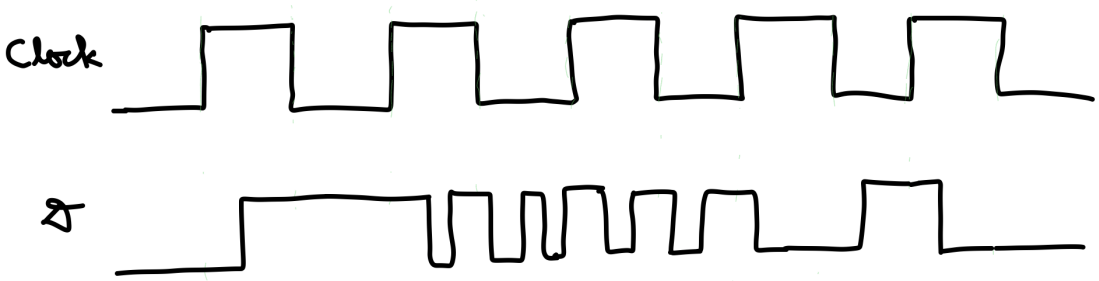
(b) Draw the circuit using 2-input AND and OR gates.

Question 7

Not yet answered

Marked out of 15.00

Draw the output Q given the following *Clock* and *D* inputs to a Master-Slave D Flip-Flop.



Question 8

Not yet answered

Marked out of 15.00

Consider an MN flip-flop that does four operations: complement, set to 1, reset to 0, and no change of state (memory), when the input MN is: 00, 01, 10, and 11, respectively.

(a) Draw the characteristic table of the MN flip-flop, and derive its characteristic equation.

(b) Implement the MN flip-flop using a D flip-flop.

◄ Minor Exam

Jump to...

Minor Exam Set-2 (hidden) ►