

COL216 LAB 2D - MINI RISC-V PROCESSOR

Jahnabi Roy (2022CS11094)
Abhinav Rajesh Shripad (2022CS11596)

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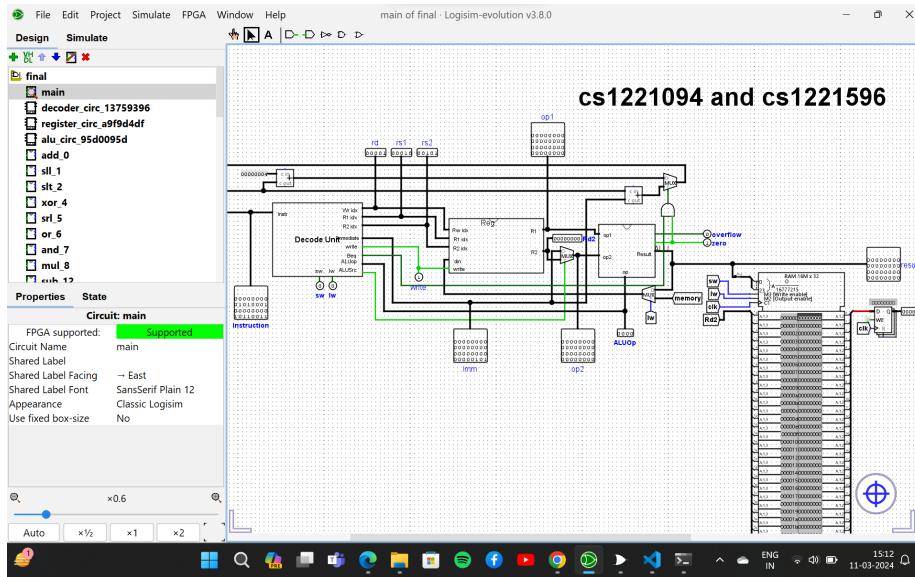
1 Introduction

Logisim evolution was used to make a simple implementation of the single cycle processor for RISC-V ISA.

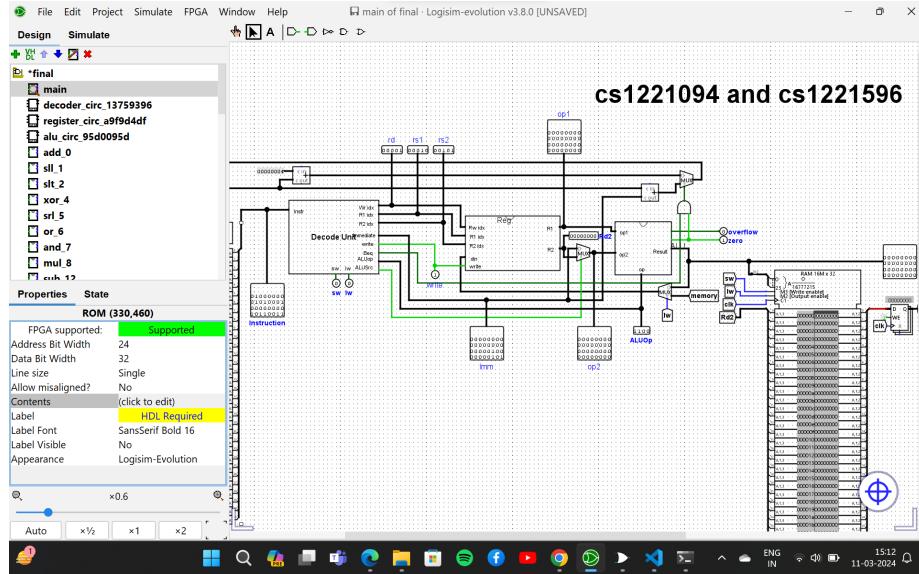
1.1 R-type Instructions

All instructions shown here were of the form <instruction_name> x1, x2, x5.

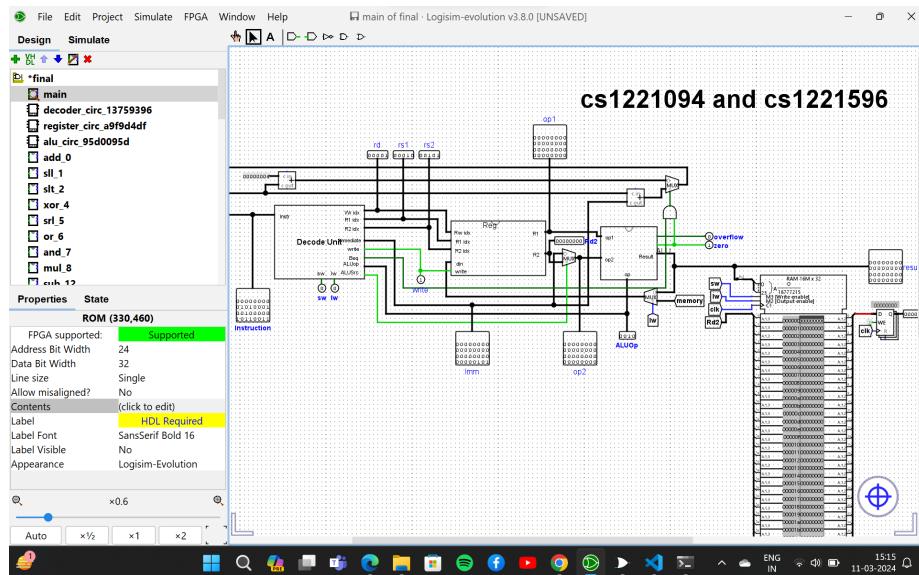
1.1.1 add



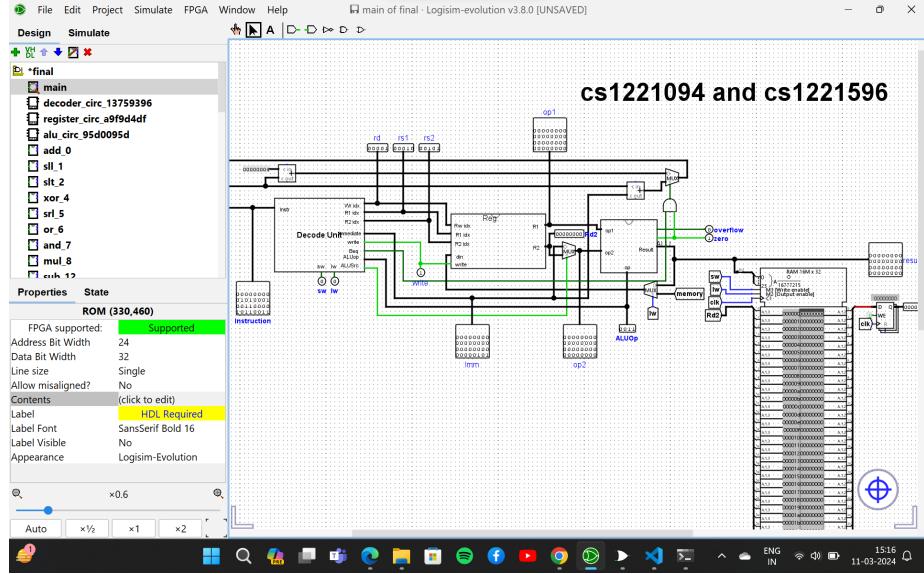
1.1.2 sub



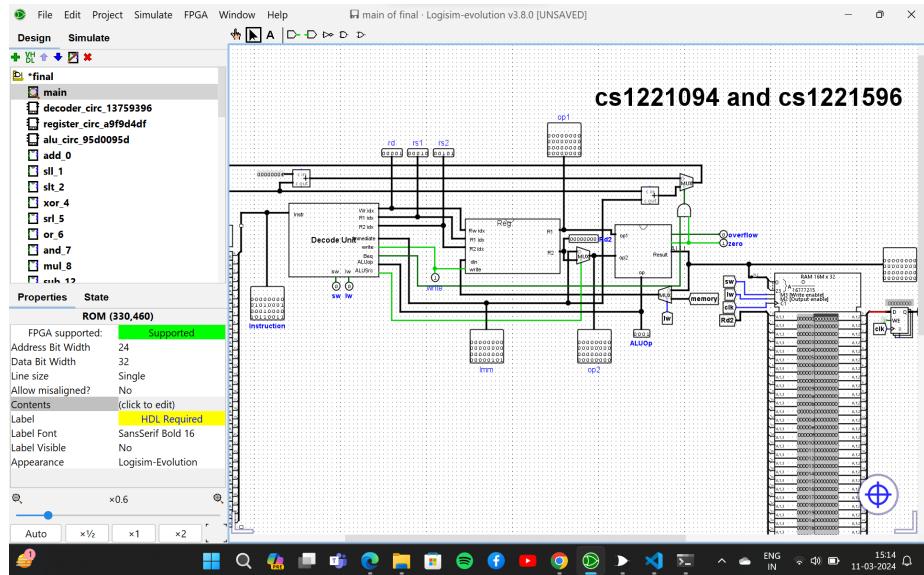
1.1.3 slt



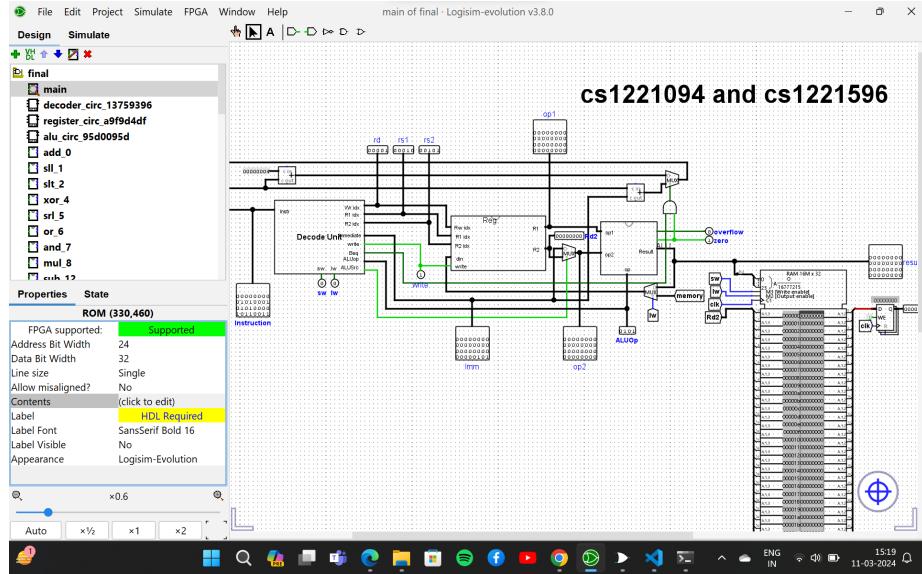
1.1.4 sltu



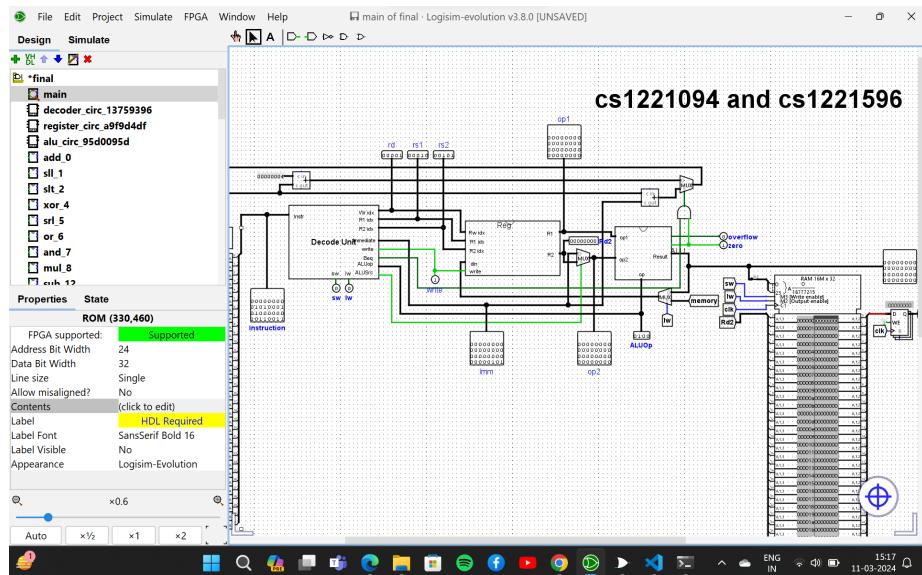
1.1.5 sll



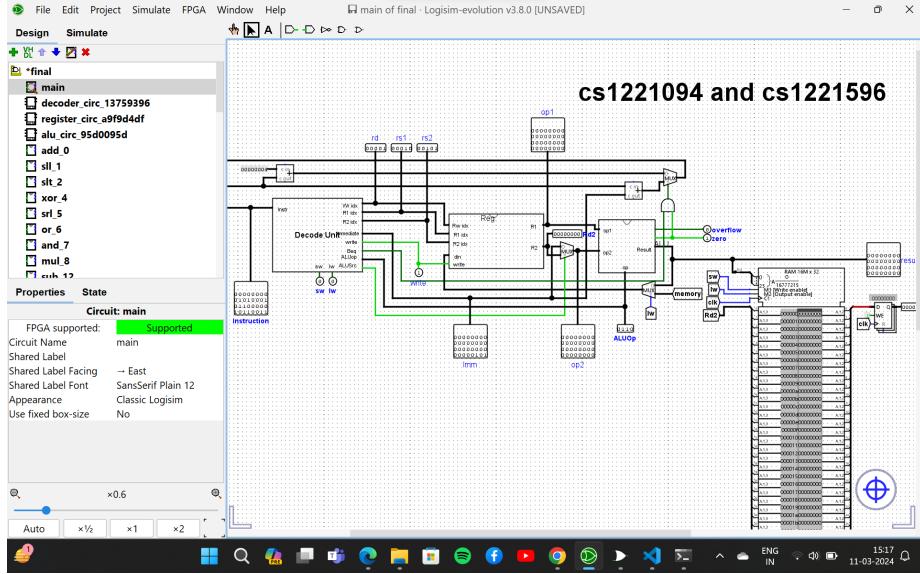
1.1.6 srl



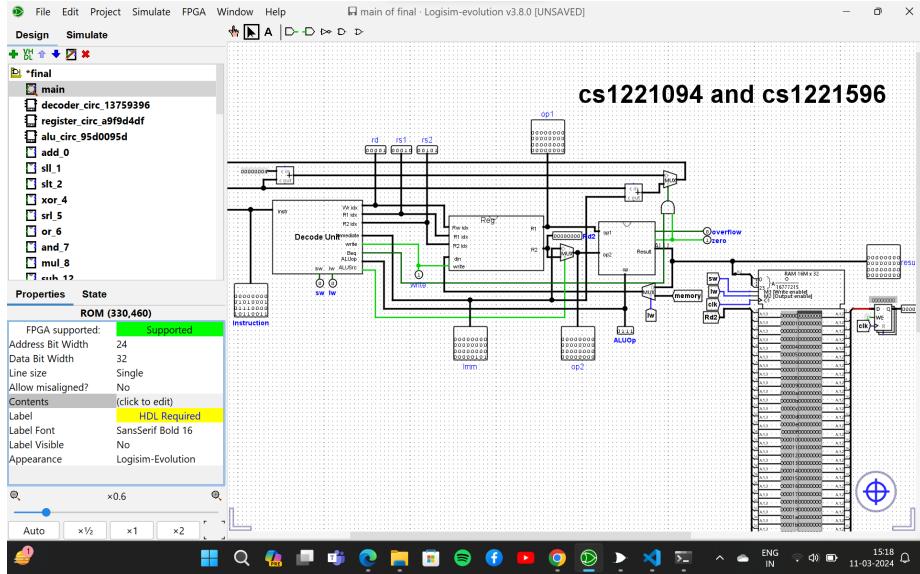
1.1.7 xor



1.1.8 or



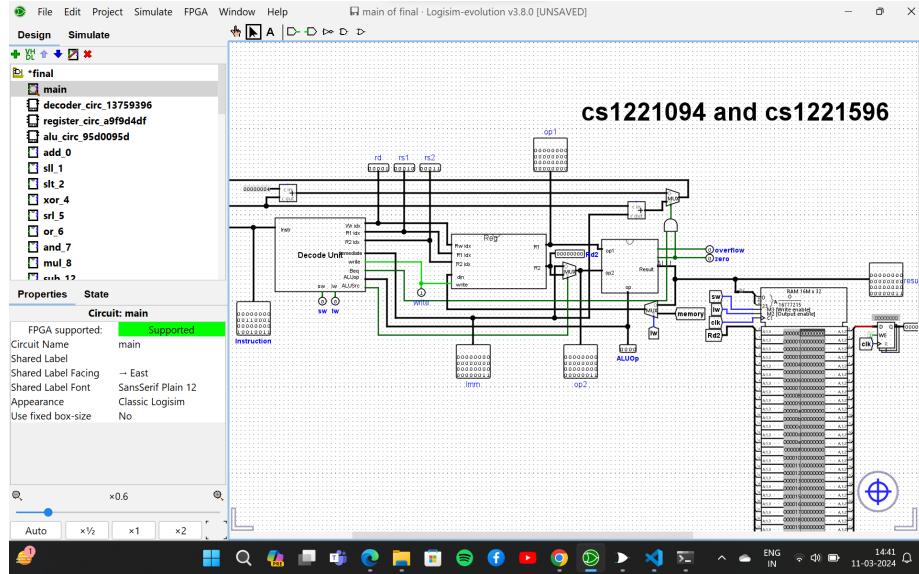
1.1.9 and



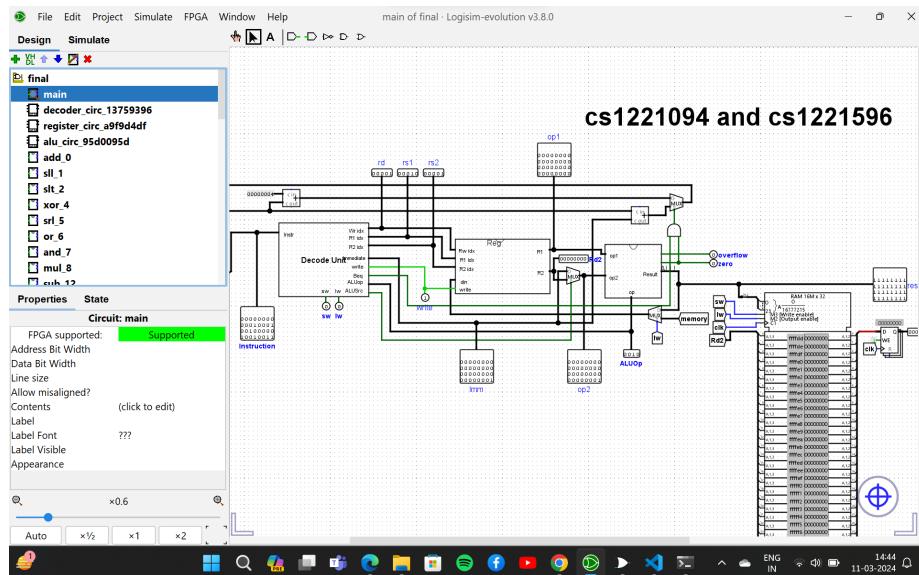
1.2 I-type Instructions

All instructions here were of the form <instruction_name> x1, x2, 5. (except load -_lw x1, 12(x2)).

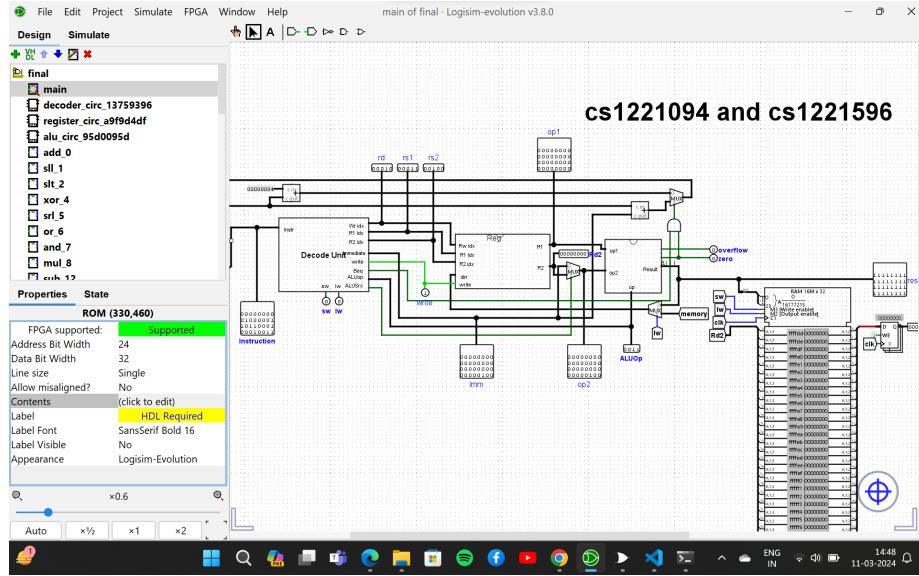
1.2.1 addi



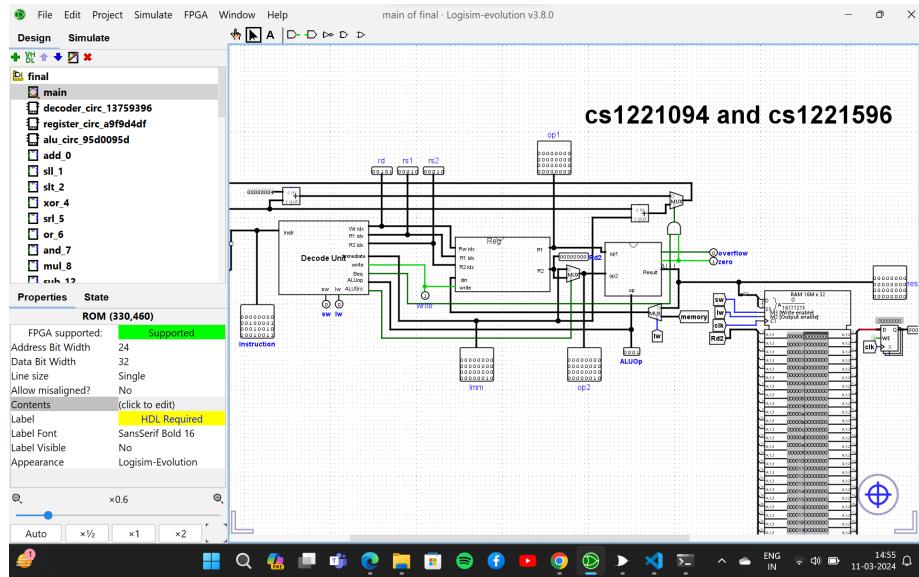
1.2.2 slti



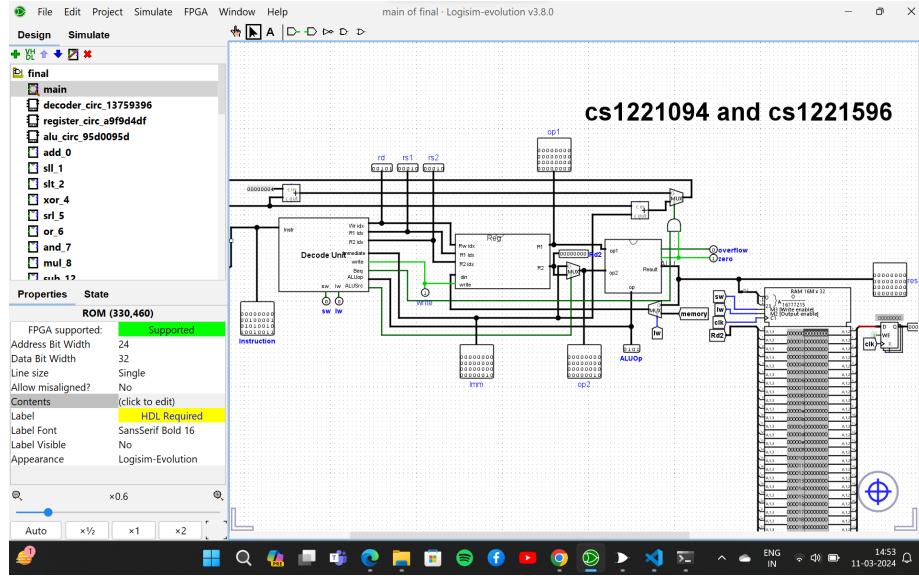
1.2.3 sltiu



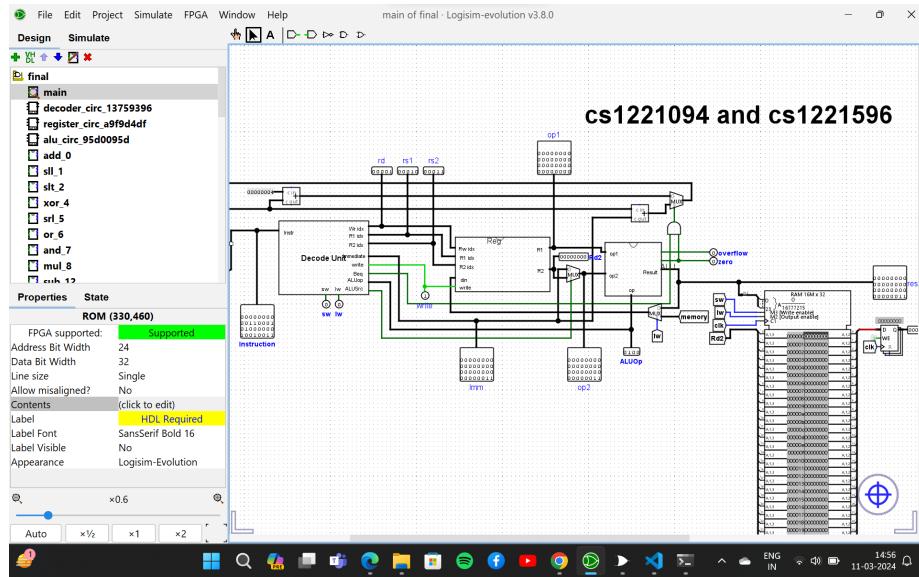
1.2.4 slli



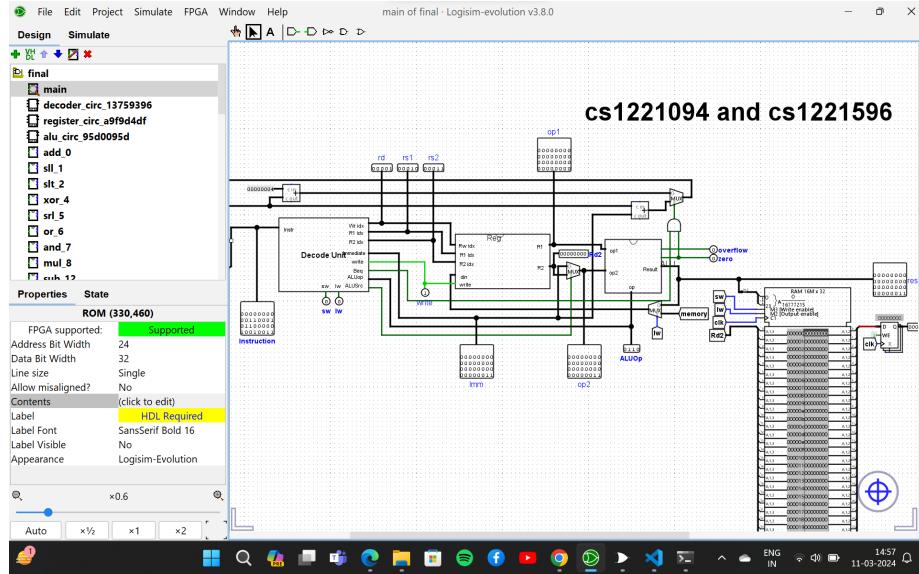
1.2.5 srl1



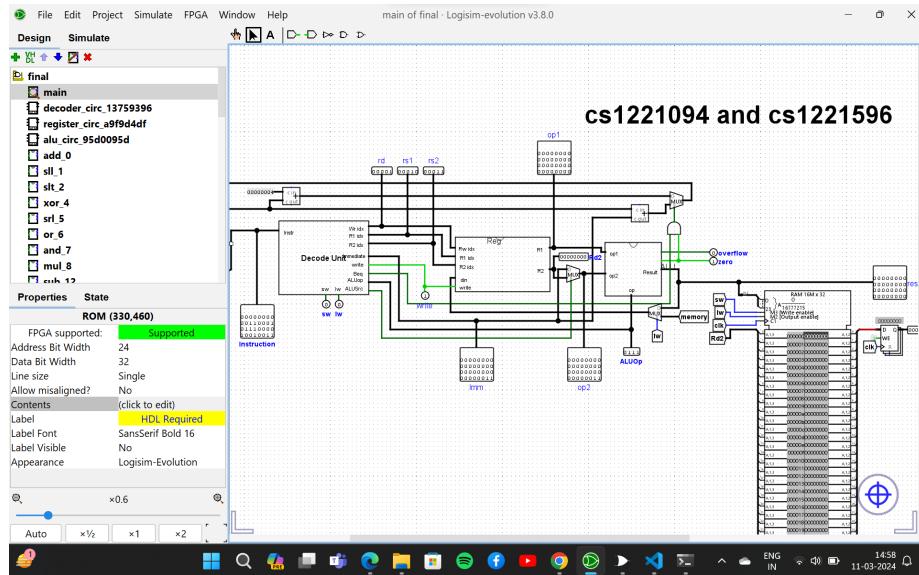
1.2.6 xor1



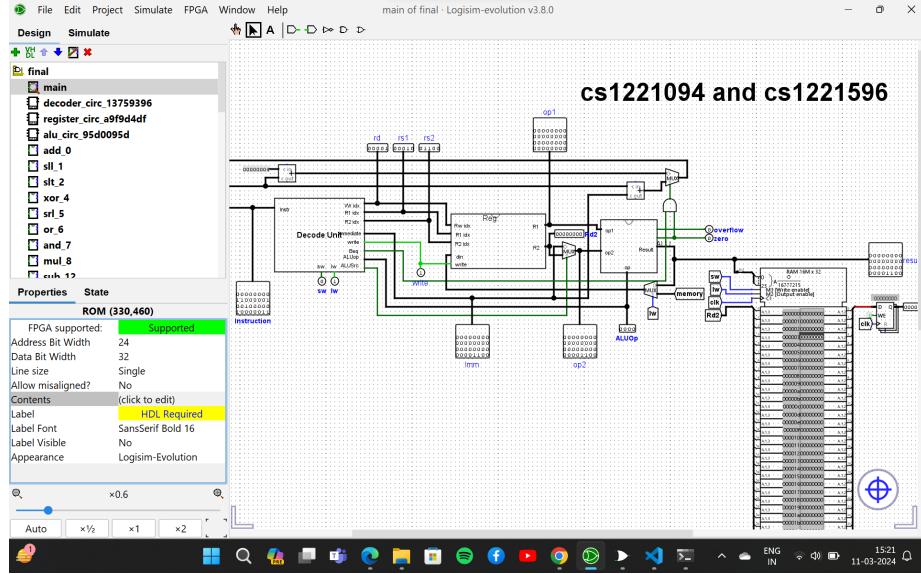
1.2.7 ori



1.2.8 andi



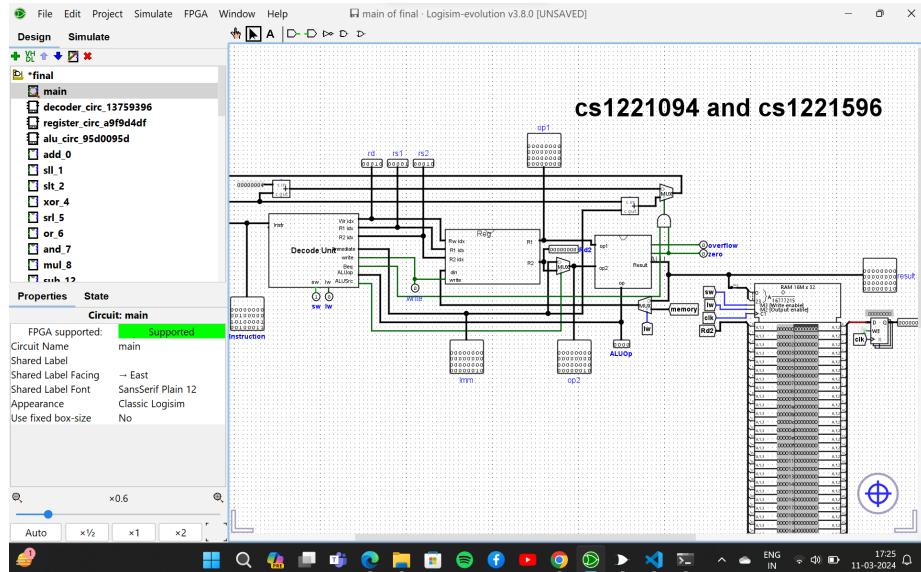
1.2.9 lw



1.3 S-type Instructions

Instruction was sw x1, 2(x2)

1.3.1 sw



1.3.2 SB-type Instruction

Instruction was `beq x1, x2, 00000006`

1.3.3 beq

