CS-301 Computer Architecture
Assignment 9

Name: _____

1. How many bits are required to address a $4M \times 16$ main memory if
   a. Main memory is byte-addressable?

   _____

   b. Main memory is word-addressable?

   _____

2. Assume Assuming a 2^{20} byte memory, what are the lowest and highest addresses of memory if memory is word-addressable, assuming a 32-bit word?

   _____

3. A digital computer has a memory unit with 24 bits per word. The instruction set consists of 150 different operations. All instructions have an operation code (opCode) and an address part (allowing for only one address). Each instruction is stored in one word of memory.
   a. How many bits are needed for the opCode?

   _____

   b. How many bits are left for the address part of the instruction?

   _____

   c. What is the maximum allowable size of memory?

   _____

   d. What is the largest unsigned binary number that can be accommodated in one word of memory?

   _____

4. Given a memory of 2048 bytes consisting of several 64 × 8 RAM chips, and assuming byte addressable memory. Using the space below, show a diagram to indicate a correct way to address this memory. Show the total number of bits needed, how many bits to use to select a chip, and how many bits to use to select an address within a chip.

5. Suppose that a $16M \times 16$ main memory is built using $512K \times 8$ RAM chips and memory is word-addressable.

   a. How many bytes are there per memory word?

   b. How many banks will this memory have?

   c. How many RAM chips are necessary to build the memory?

   d. How many address bits are needed to address a memory location within a RAM chip?

   e. How many address bits are needed for all of memory?

   f. If high-order interleaving is used, where (in which bank) would address 14 (which is E in Hex) be located?

   g. If low-order interleaving is used, where (in which bank) would address 14 be located?

6. Suppose we add the following instruction to MARIE's ISA:

   `IncSZ  Operand`

   This instruction increments the value with effective address "Operand," and if this newly incremented value is equal to 0, the program counter is incremented by 1. Basically, we are incrementing the operand, and if this new value is equal to 0, we skip the next instruction. Show how this instruction would be written using RTN.

7. Decipher the following MARIE machine language instructions (write the assembly language equivalent):

   a. 0010000000000111

   b. 1001000000001011

   c. 0011000000001001

8. What are the potential problems (perhaps more than one) with the following assembly language code fragment (implementing a subroutine) written to run on MARIE? The subroutine assumes the parameter to be passed is in the AC and should double this value. The Main part of the program includes a sample call to the subroutine. You can assume this fragment is part of a larger program.

```
Main,     Load X
          Jump Sub1
Sret,     Store X
          . . .
Sub1,     Add X
          Jump Sret
```