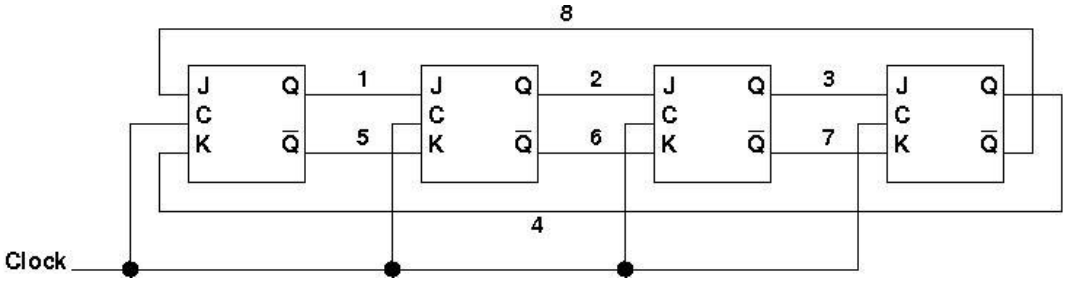
CS-301 Computer Architecture
Assignment 8

Name:_____

1. Investigate the operation of the following circuit. Assume an initial state of 0000. We want to trace the outputs (the Qs) as the clock ticks and determine the purpose of the circuit.



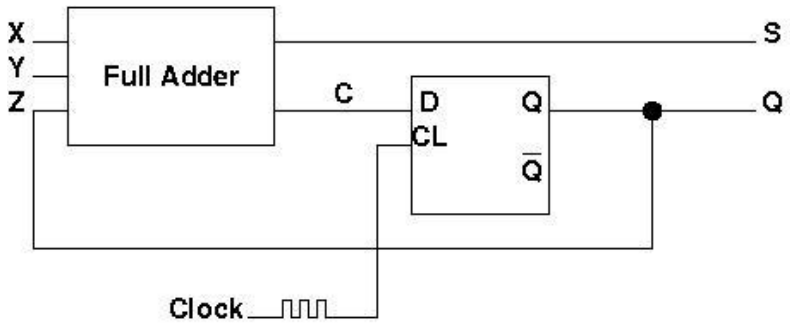
   a. Use the numbering of the lines between the flip-flops to complete the chart below for t = 0, 1, …, 8.

t	Lines that are "on"	Lines that are "off"	*t*	Lines that are "on"	Lines that are "off"
0			**4**		
1			**5**		
2			**6**		
3			**7**		

   b. Now, determine the purpose of the circuit.

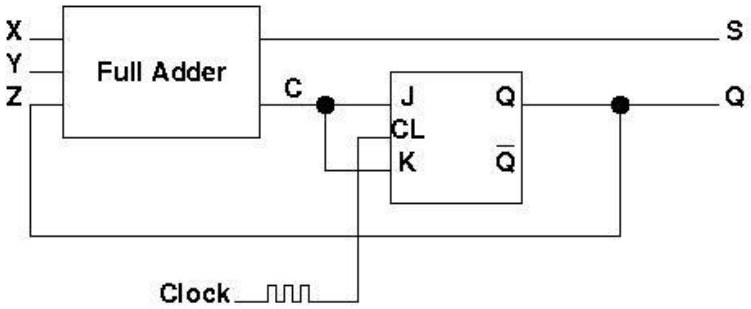
   _____

2. Complete the truth table for the following circuit:



X	Y	Z(Q)	Next State	
			S	C(Q)
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

3. A sequential circuit has one flip-flop; two inputs, X and Y; and one output S. It consists of a full-adder circuit connected to a JK flip-flop, as shown below. Fill in the characteristic table for this circuit by completing the *Next State* and *Output* columns.



Present State	Inputs		Next State	Output
Z=Q(t)	X	Y	Q(t+1)	S
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

4. A Mux-Not flip-flop (MN flip-flop) behaves as follows: If M = 1, the flip-flop complements the current state. If M = 0, the next state of the flip-flop is equal to the value of N.
   a. Derive the characteristic table for the MN flip-flop.

M	N	Q(t+1)

   b. Show how a JK flip-flop can be converted to an MN flip-flop by adding gate(s) and inverter(s).