	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
1	|DE1_SoC	31 (0)	28 (0)	0	0	67	0	|DE1_SoC	DE1_SoC	work
1	| clock_divider:cdiv|	26 (26)	26 (26)	0	0	0	0	|DE1_SoC| clock_divider:cdiv	clock_divider	work
2	|runway:r|	5 (5)	2 (2)	0	0	0	0	|DE1_SoC| runway:r	runway	work