```
1   // Multi-level logic on the FPGA
2   // Michael Humphrey 1/23/2018 SID:1536326
3
4   module DE1_SoC (HEX0, HEX1, HEX2, HEX3, HEX4, HEX5, KEY, LEDR, SW);
5      output logic  [6:0]    HEX0, HEX1, HEX2, HEX3, HEX4, HEX5;
6      output logic  [9:0]    LEDR;
7      input  logic  [3:0]    KEY;
8      input  logic  [9:0]   SW;
9
10     // Default values, turns off the HEX displays
11     assign HEX0 = 7'b1111111;
12     assign HEX1 = 7'b1111111;
13     assign HEX2 = 7'b1111111;
14     assign HEX3 = 7'b1111111;
15     assign HEX4 = 7'b1111111;
16     assign HEX5 = 7'b1111111;
17
18     // U,P,C go to SW[9],SW[8],SW[7] respectively. Mark goes to SW[0].
19     // Discount light goes to LEDR[1].
20     logic uc;
21     and a1 (uc, SW[9], SW[7]);
22     or o1 (LEDR[1], uc, SW[8]);
23
24     // Stolen light goes to LEDR[0].
25     logic notc, temp;
26     not n1 (notc, SW[7]);
27     nor no1 (temp, notc, SW[9]);
28     nor no2 (LEDR[0], temp, SW[0], SW[8]);
29
30
31  endmodule
32
33  module DE1_SoC_testbench();
34     logic  [6:0] HEX0, HEX1, HEX2, HEX3, HEX4, HEX5;
35     logic  [9:0] LEDR;
36     logic  [3:0] KEY;
37     logic  [9:0] SW;
38
39     DE1_SoC dut (.HEX0, .HEX1, .HEX2, .HEX3, .HEX4, .HEX5, .KEY, .LEDR, .SW);
40
41     // Try all combinations of inputs.
42     integer i;
43     initial begin
44        SW[0] = 1'b0;
45        for(i = 0; i <8; i++) begin
46           SW[9:7] = i; #10;
47        end
48        SW[0] = 1'b1;
49        for(i = 0; i <8; i++) begin
50           SW[9:7] = i; #10;
51        end
52     end
53  endmodule
```