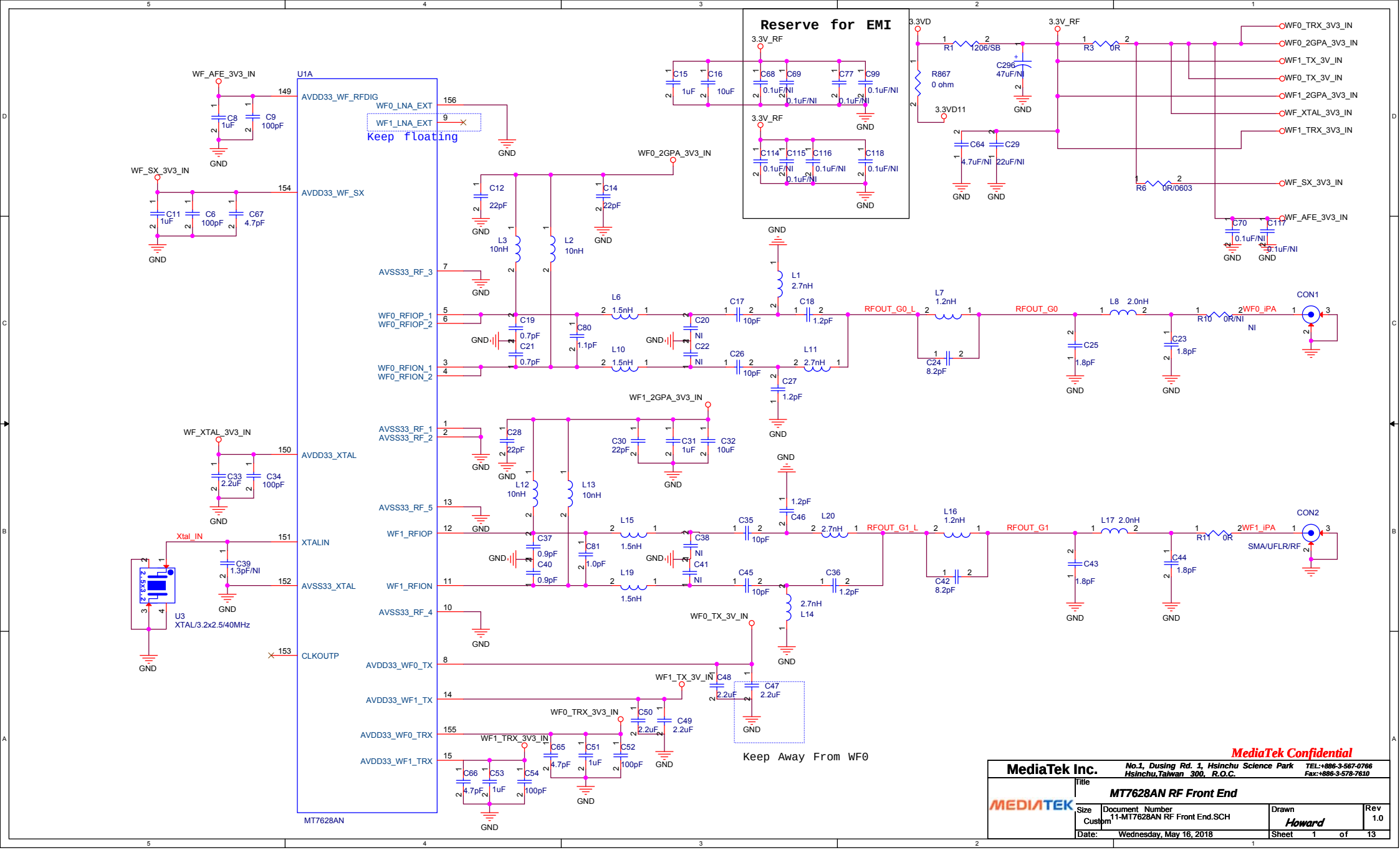
Reserve for EMI
U1A
MT7628AN
AVDD33_WF_RFDIG
AVDD33_WF_SX
AVDD33_XTAL
XTALIN
AVSS33_XTAL
CLKOUTP
WF0_LNA_EXT
WF1_LNA_EXT
Keep floating
AVSS33_RF_3
WF0_RFIOP_1
WF0_RFIOP_2
WF0_RFION_1
WF0_RFION_2
AVSS33_RF_1
AVSS33_RF_2
AVSS33_RF_5
WF1_RFIOP
WF1_RFION
AVSS33_RF_4
AVDD33_WF0_TX
AVDD33_WF1_TX
AVDD33_WF0_TRX
AVDD33_WF1_TRX
WF_AFE_3V3_IN
WF_SX_3V3_IN
WF_XTAL_3V3_IN
Xtal_IN
U3
XTAL/3.2x2.5/40MHz
WF0_2GPA_3V3_IN
WF1_2GPA_3V3_IN
WF0_TX_3V_IN
WF1_TX_3V_IN
WF0_TRX_3V3_IN
WF1_TRX_3V3_IN
RFOUT_G0_L
RFOUT_G0
RFOUT_G1_L
RFOUT_G1
CON1
CON2
WF0_iPA
WF1_iPA
SMA/UFLR/RF
Keep Away From WF0
3.3VD
3.3V_RF
3.3VD11
WF0_TRX_3V3_IN
WF0_2GPA_3V3_IN
WF1_2GPA_3V3_IN
WF1_TX_3V_IN
WF1_TRX_3V3_IN
WF_SX_3V3_IN
WF_AFE_3V3_IN
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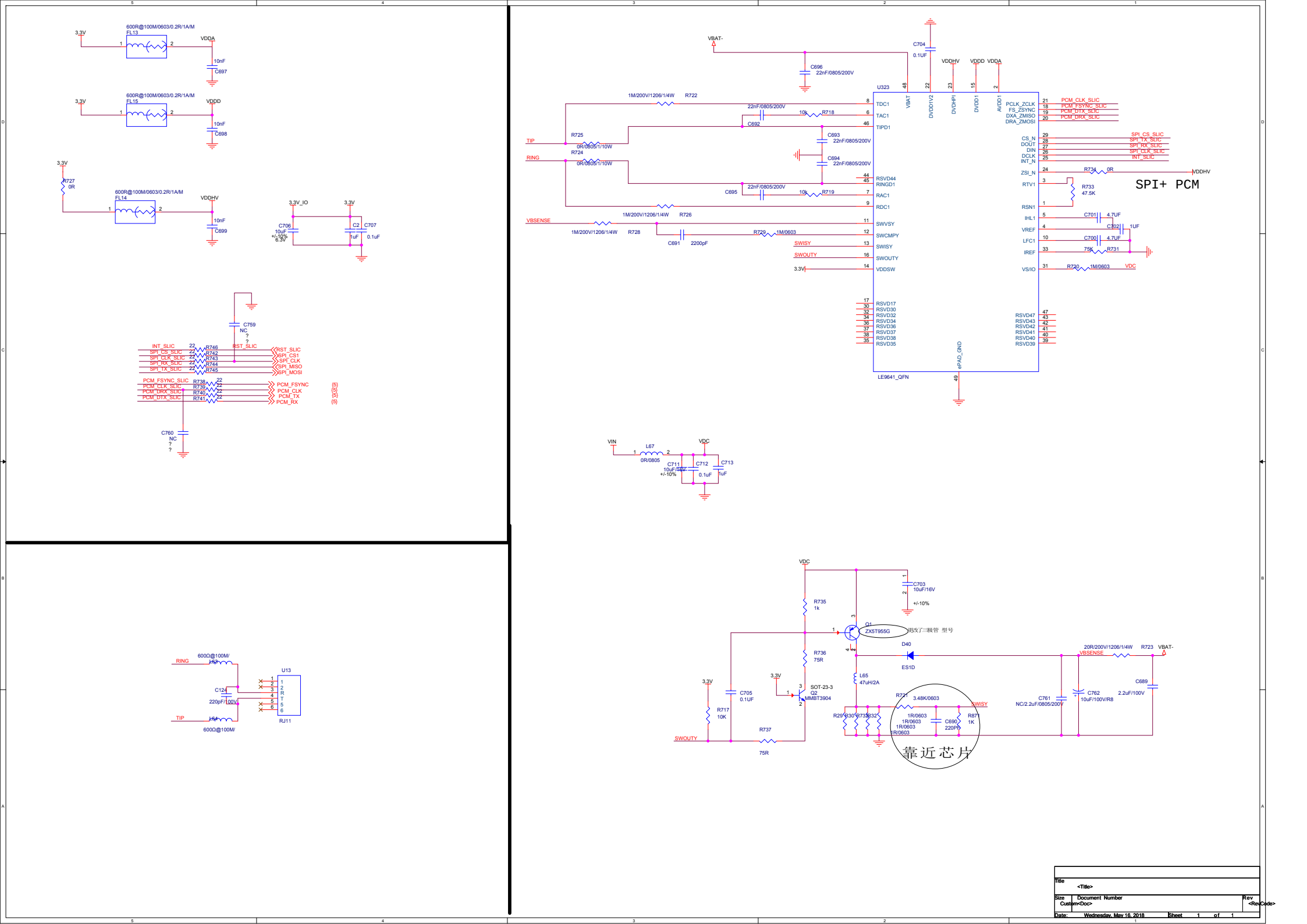
MT7628AN RF Front End
Size: Custom
Document Number: 11-MT7628AN RF Front End.SCH
Drawn: Howard
Rev: 1.0
Date: Wednesday, May 16, 2018
Sheet 1 of 13



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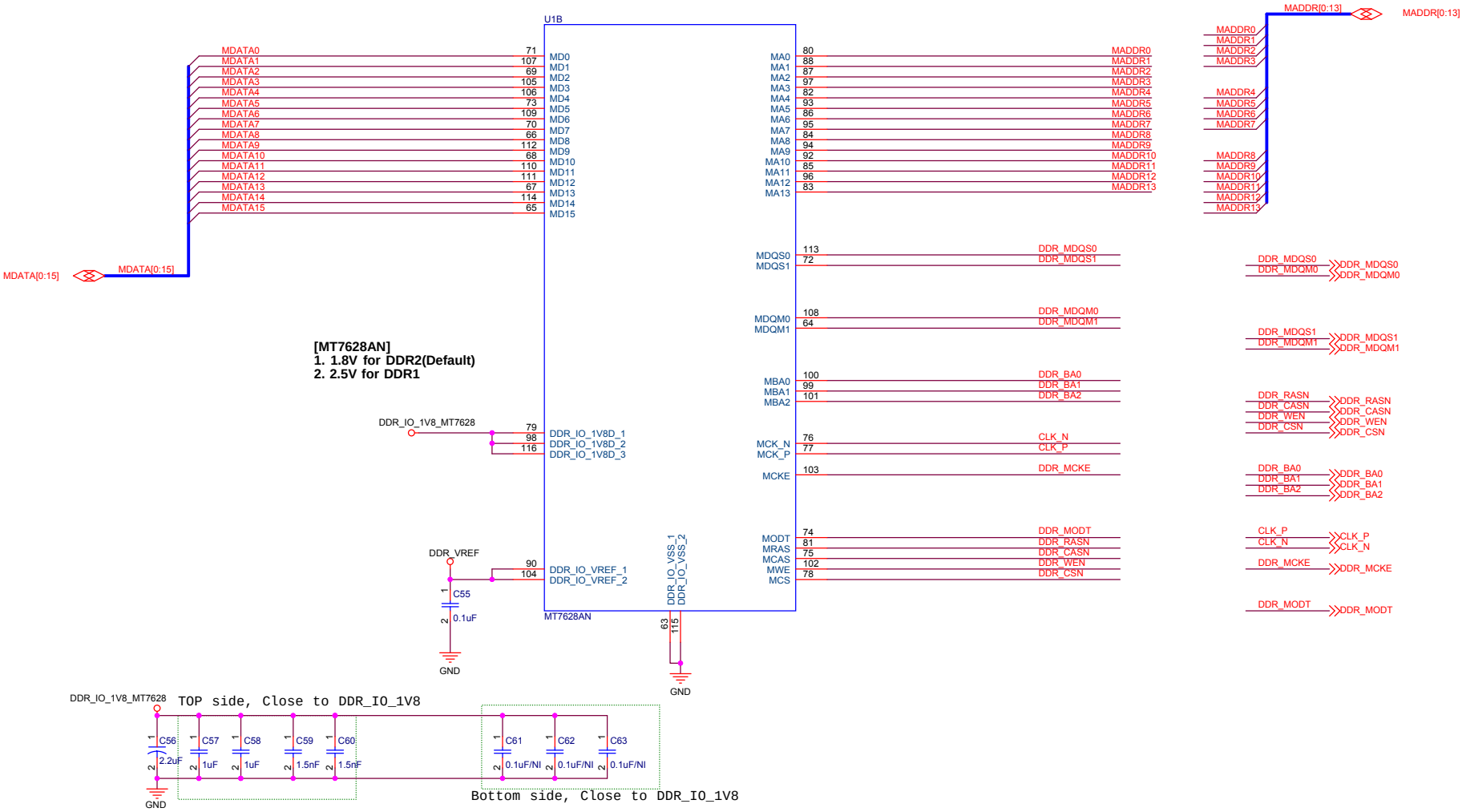
Date:	Wednesday, May 16, 2018
Sheet	1 of 1



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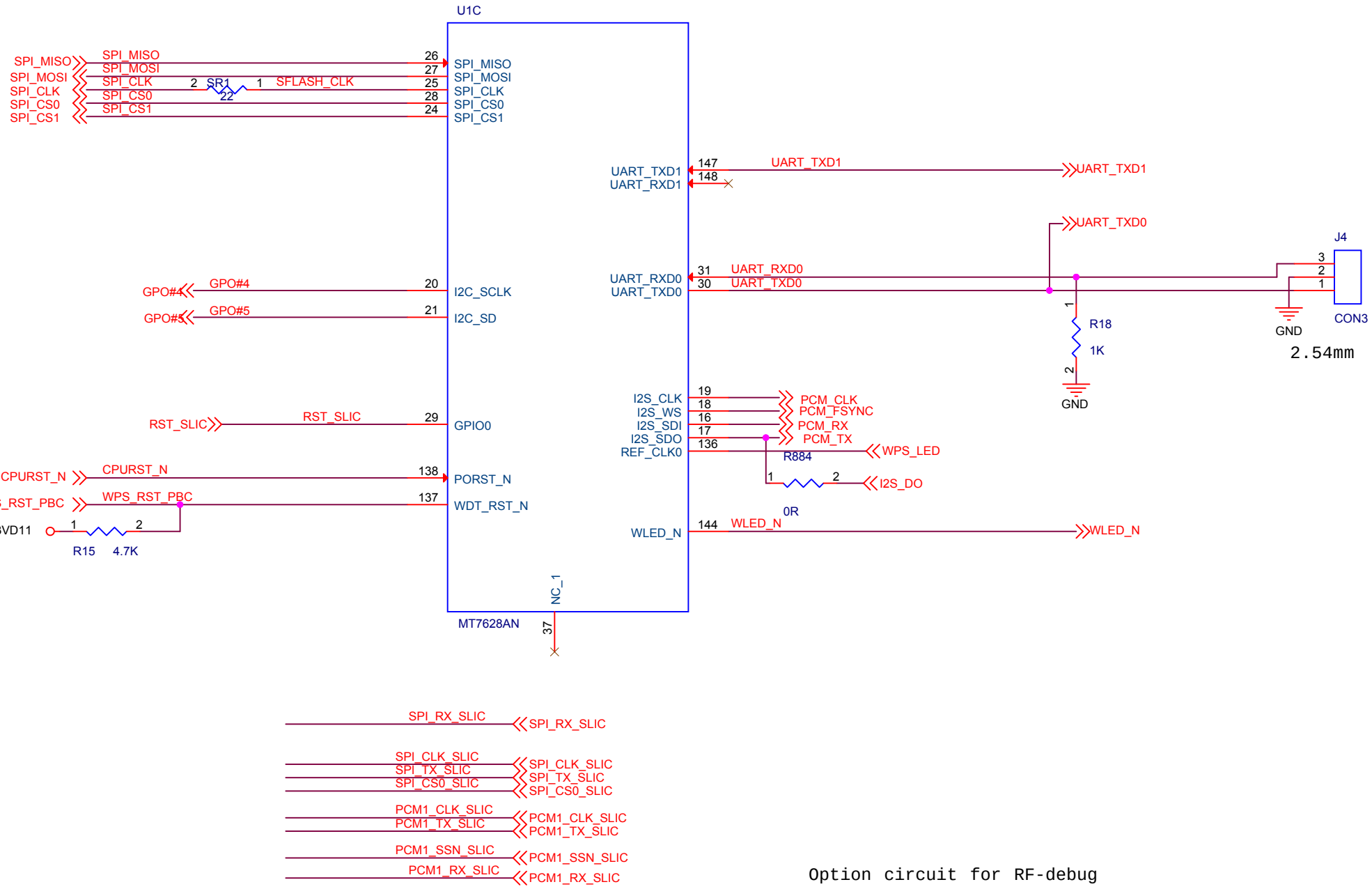
Title: MT7628AN DDR2 I/F			
Size: Custom	Document Number: 12-MT7628AN DDR2 I/F.SCH	Drawn: Howard	Rev: 1.0
Date: Wednesday, May 16, 2018		Sheet 2 of 13	



Option circuit for RF-debug

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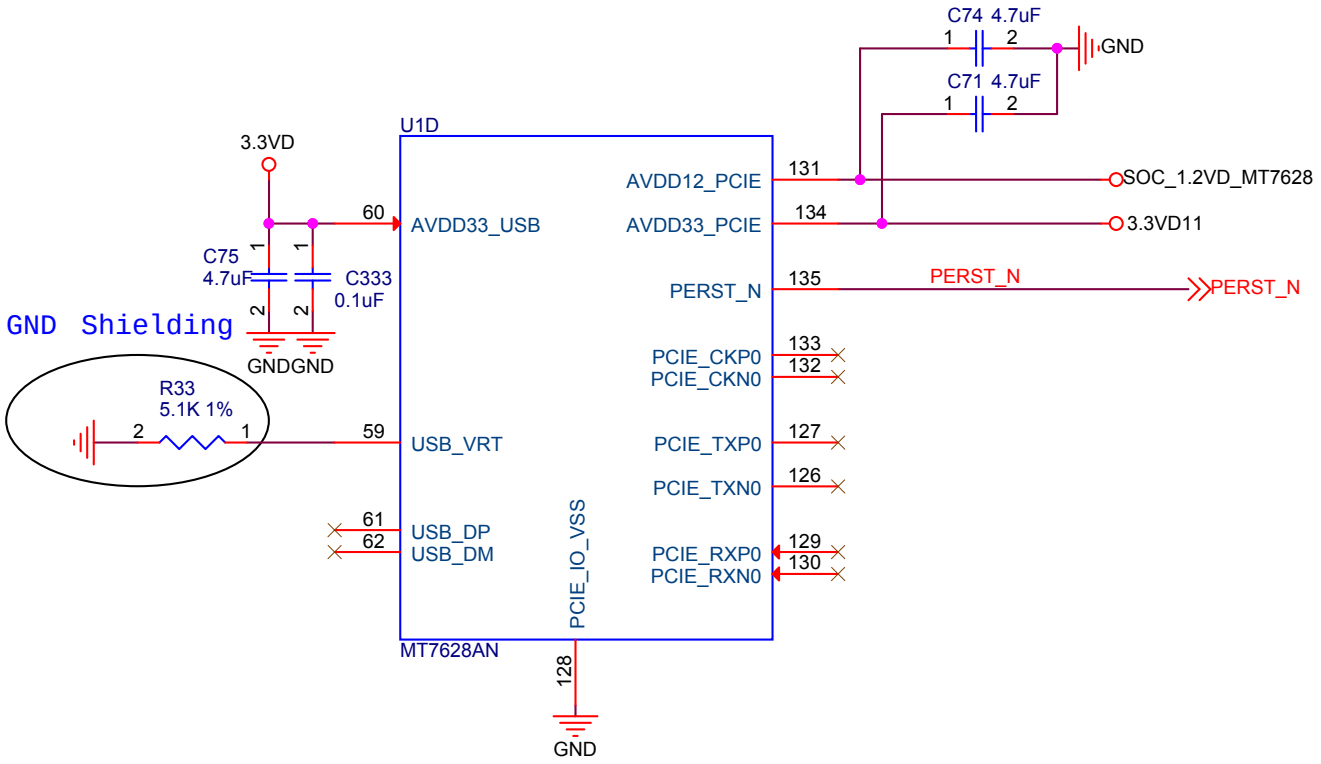
Title: MT7628AN Pheripheral			
Size: A4	Document Number: 13-MT7628AN Pheripheral-C.SCH	Drawn: Howard	Rev: 1.0
Date: Wednesday, May 16, 2018		Sheet 3 of 13	



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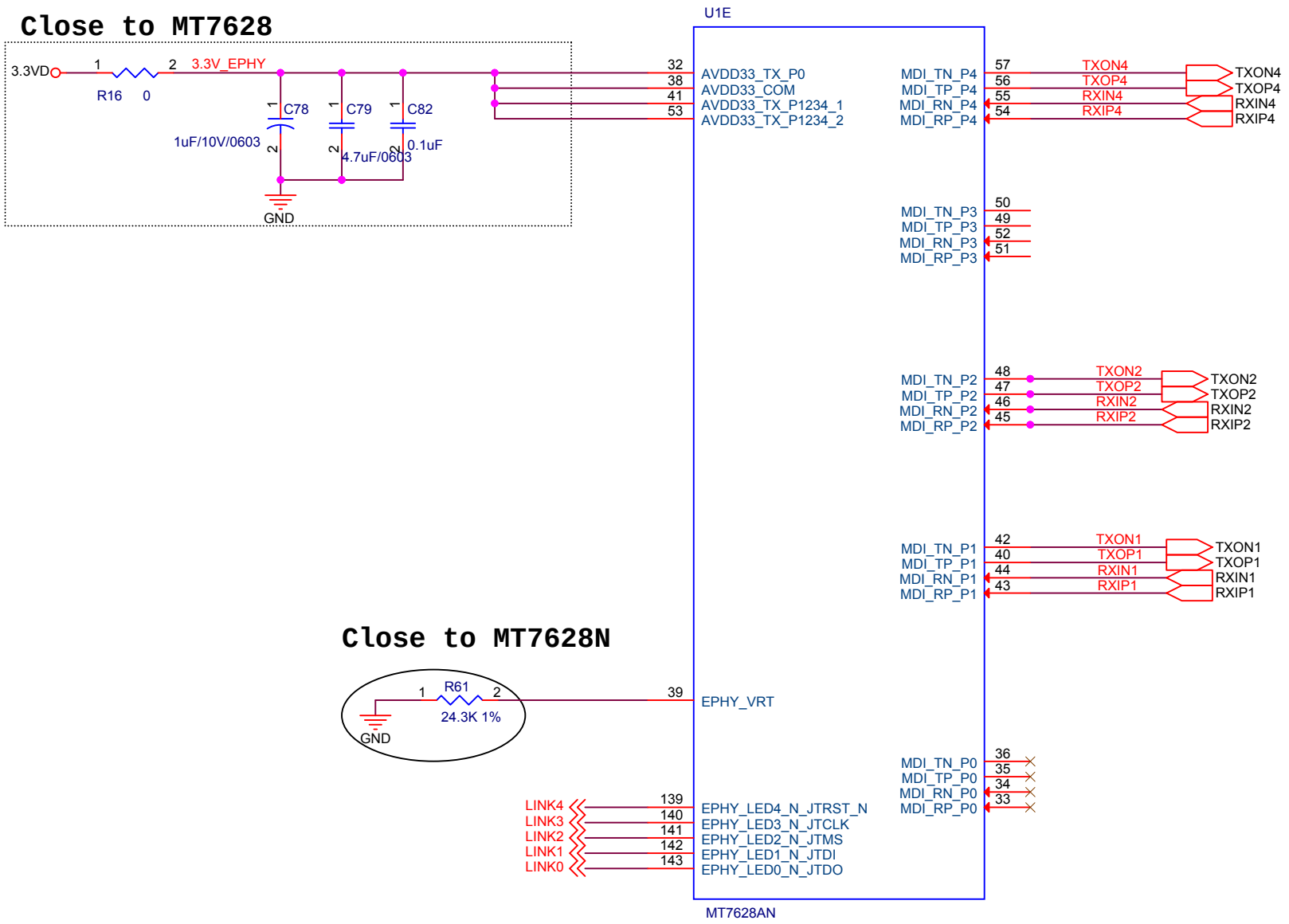
Title: MT7628AN USB-PCIe			
Size: Custom	Document Number: 14-MT7628AN USB-PCIe.sch	Drawn: Howard	Rev: 1.0
Date: Wednesday, May 16, 2018		Sheet 4 of 13	



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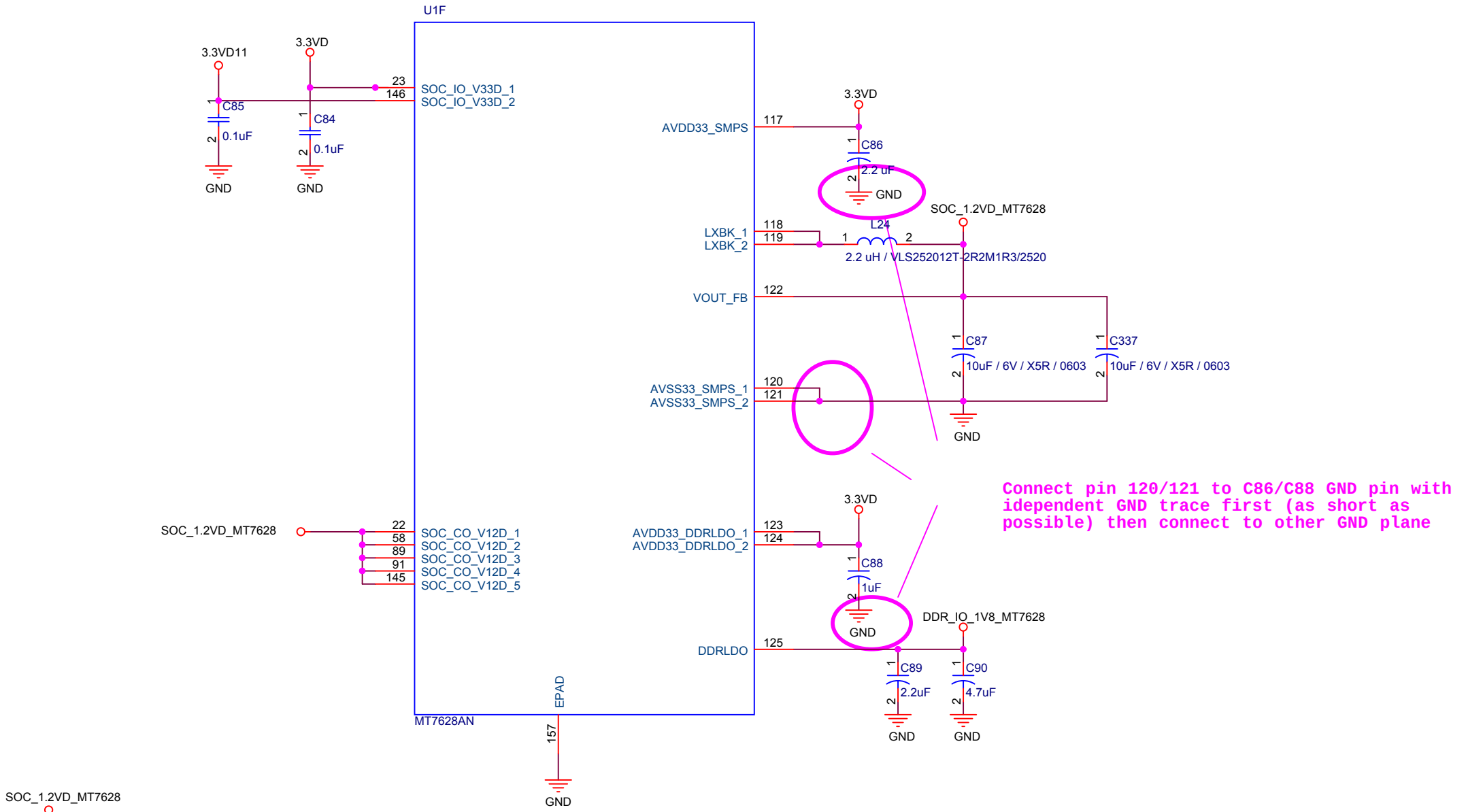
Title: MT7628AN Ethernet			
Size: A4	Document Number: 15-MT7628AN Ethernet-E.SCH	Drawn: Howard	Rev: 1.0
Date: Wednesday, May 16, 2018		Sheet 5 of 13	



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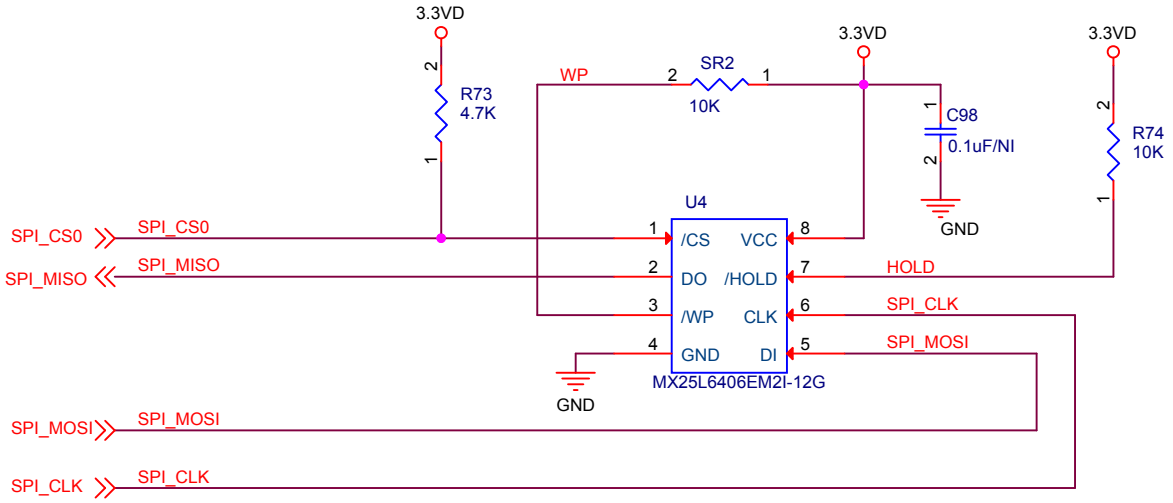
MEDIATEK	Title: MT7628AN Power		
	Size: A4	Document Number: 16-MT7628AN Power-F.SCH	Drawn: Howard
	Date: Wednesday, May 16, 2018	Sheet 6 of 13	Rev 1.0



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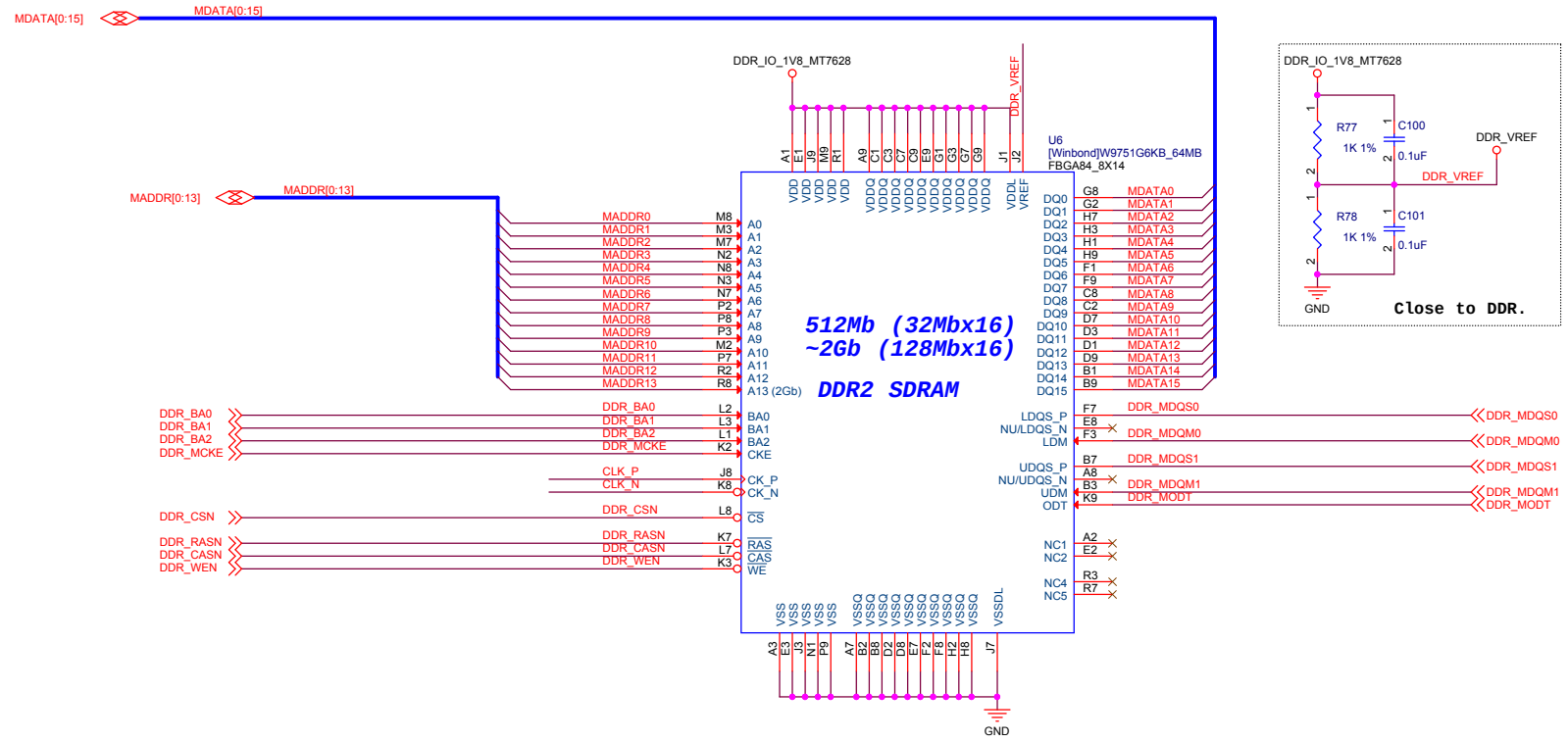
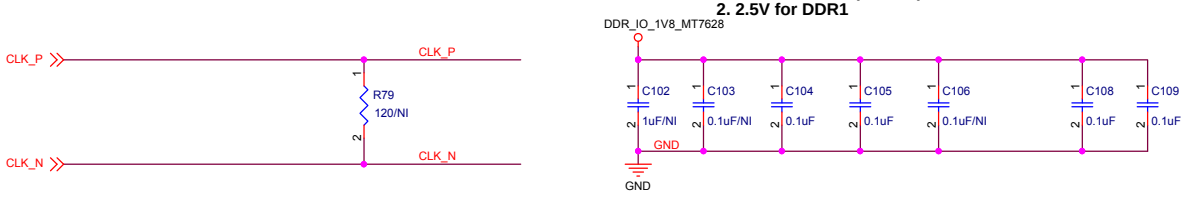
Title: SPI Flash			
Size: A4	Document Number: 17-SPI Flash.SCH	Drawn: Howard	Rev: 1.0
Date: Wednesday, May 16, 2018		Sheet 7 of 13	



1. 1.8V for DDR2 (Default)
2. 2.5V for DDR1



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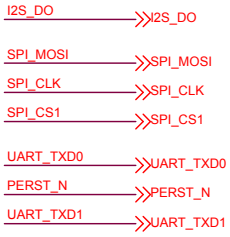
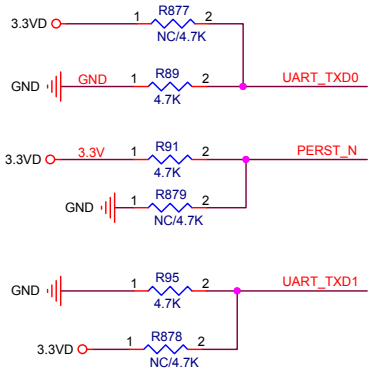
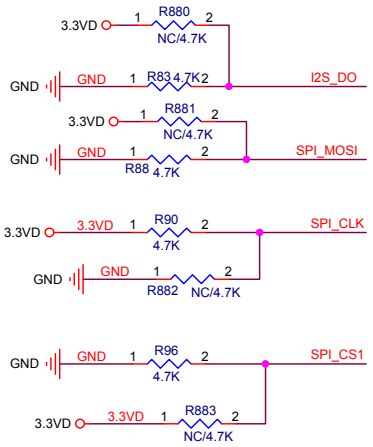
Title: DDR-CFG			
Size: Custom	Document Number: 18-DDR2-CFG.SCH	Drawn: Howard	Rev: 1.0
Date: Wednesday, May 16, 2018		Sheet 8 of 13	







Bootstrapping Pins Description

Pin Name	Boot Strapping Signal Name	Description
UART_TXD1	DBG_JTAG_MODE	0: JTAG_MODE 1: EPHY_LED (default)
PERST_N	XTAL_FREQ_SEL	0: 25 MHz DIP 1: 40 MHz SMD
I2S_SDO	DRAM_TYPE	1: DDR1 0: DDR2 [note] This pin is valid for MT7628AN only. It needs to be pull-low for 7628KN which only supports DDR1.
{SPI_MOSI SPI_CLK, SPI_CS1}	CHIP_MODE[2:0]	A vector to set chip function/test/debug modes. 000: Boot from PLL (boot from SPI 3-Byte Addr) 001: Boot from PLL (boot from SPI 4-Byte Addr) 010: Boot from XTAL (boot from SPI 3-Byte Addr) 011: Boot from XTAL (boot from SPI 4-Byte Addr)
PAD_TXD0	EXT_BGCK	1: Test Mode 0: Normal (default)

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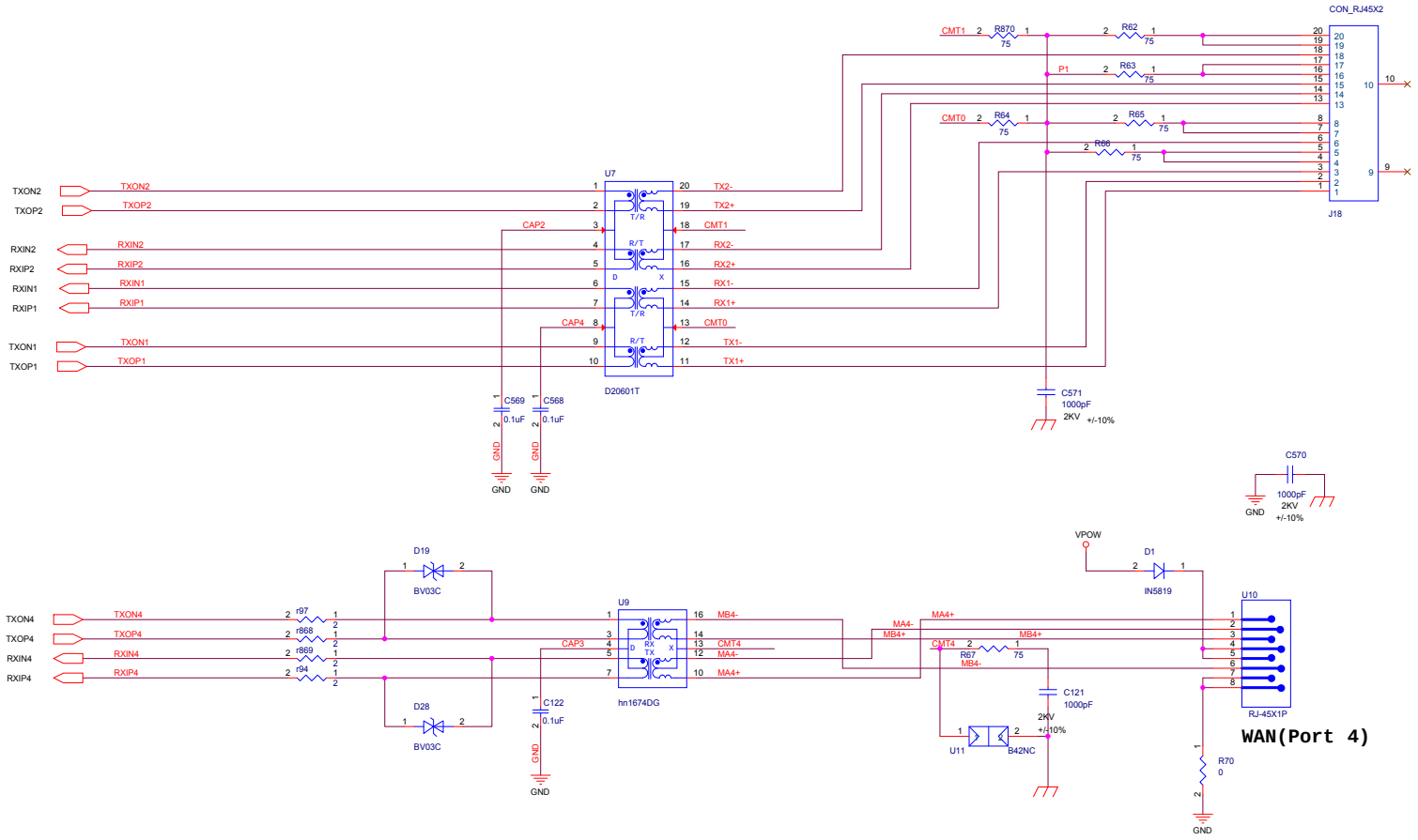
Title: Config			
Size: B	Document Number: 19-Config.SCH	Drawn: Howard	Rev: 1.0
Date: Wednesday, May 16, 2018		Sheet 9 of 13	



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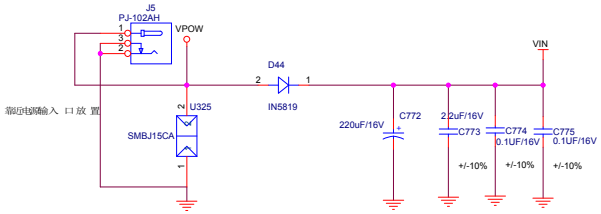
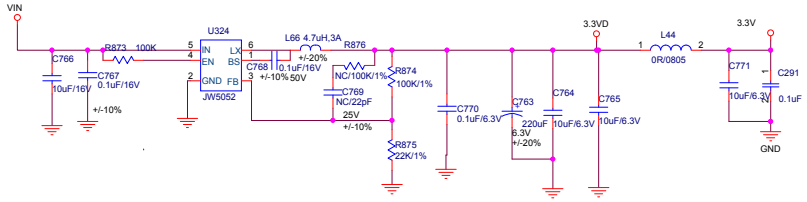
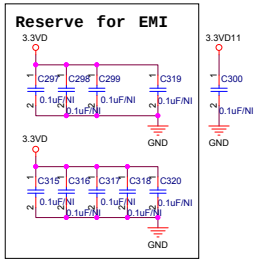
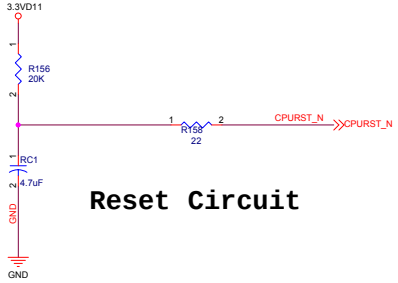
MEDIATEK	Title: XMER-RJ45		
	Size: C	Document Number: 21-XMER-RJ45.SCH	Drawn: Howard
	Date: Thursday, May 17, 2018	Sheet 11 of 13	Rev 1.0



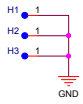
增加48V_POE电源







Reset Circuit



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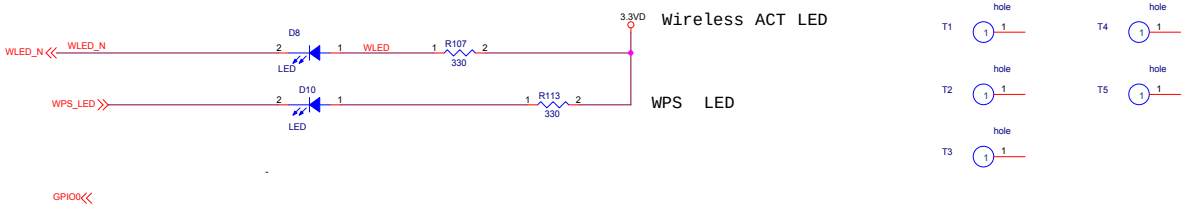
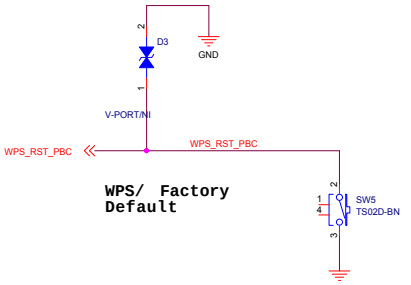
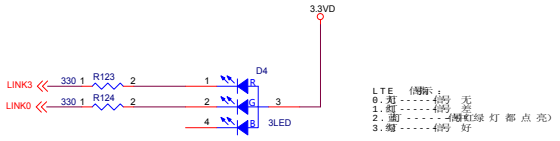
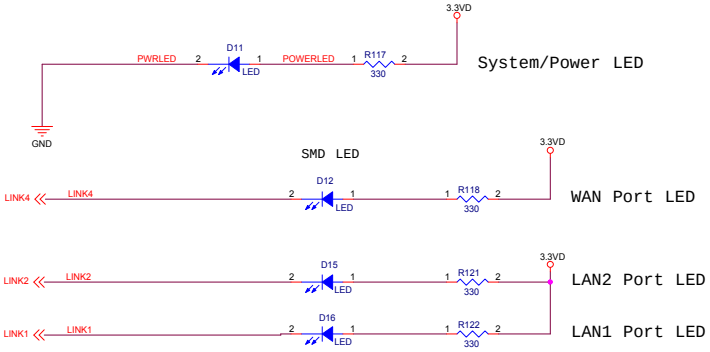
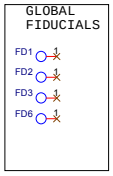
Title: Power & Reset			
Size: Custom	Document Number: 22-Power - Reset.SCH	Drawn: Howard	Rev: 1.0
Date: Wednesday, May 16, 2018		Sheet 12 of 13	











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MEDIATEK	Title: LED		
	Size: C	Document Number: 23-LED.SCH	Rev: 1.0
	Date: Wednesday, May 16, 2018	Drawn: Howard	Sheet 13 of 13