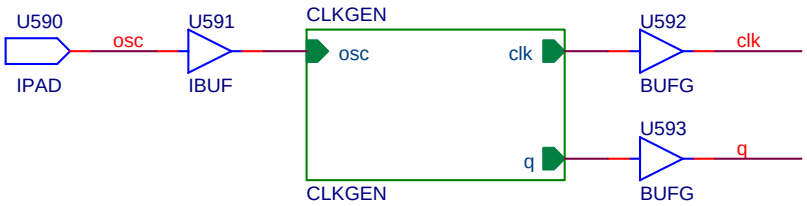
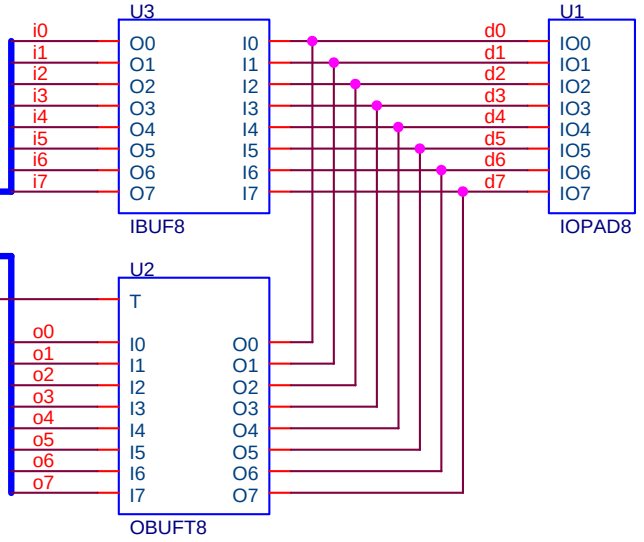
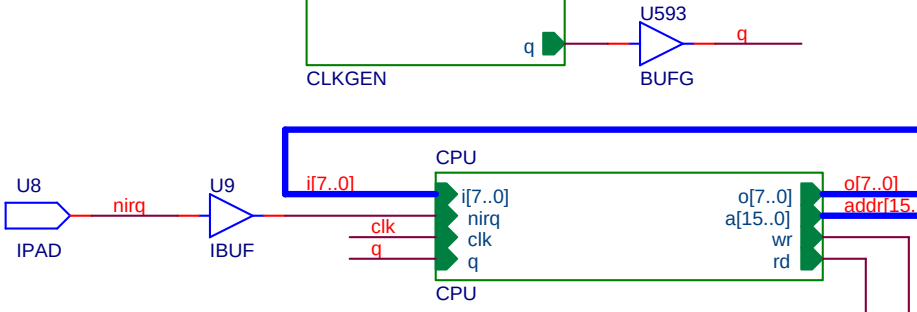
Two-phase clock generator

Q leads CLK by 90 degrees

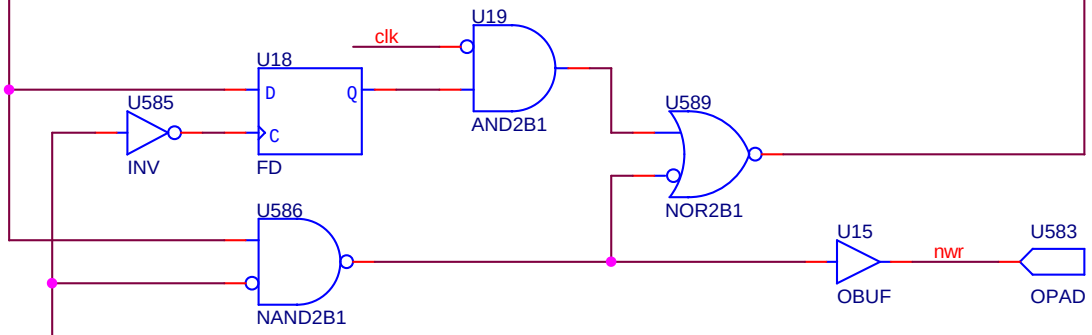


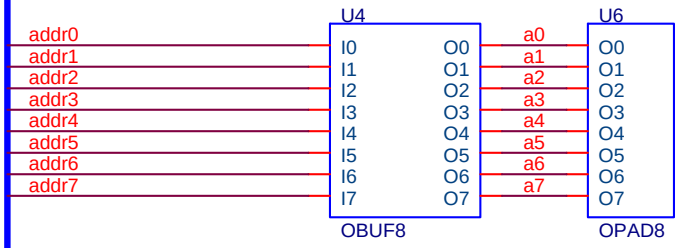
Bus buffers

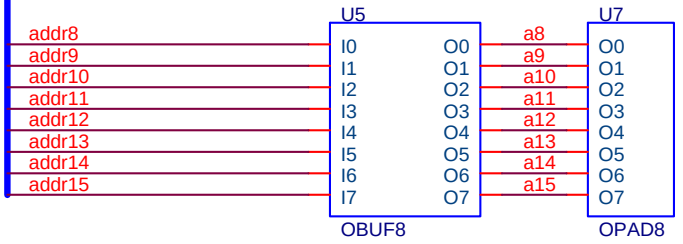




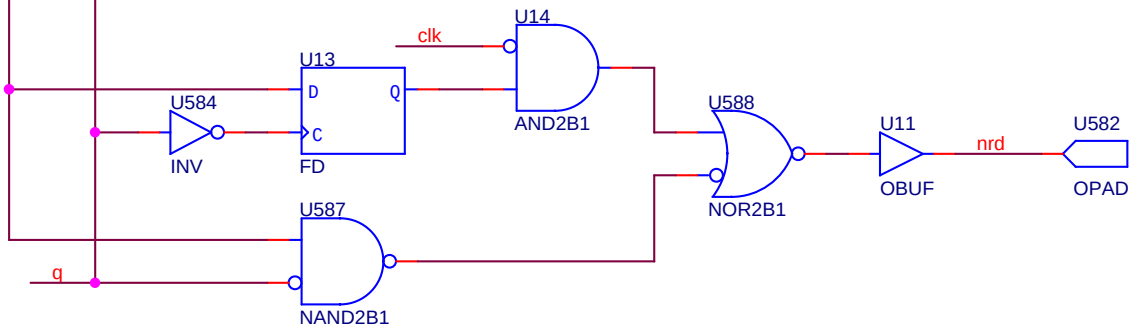
Write pulse generator







Read pulse generator



Joseph H. Allen		
Title: CPU Example Top Level		
Size: A	Document Number	Rev: 1
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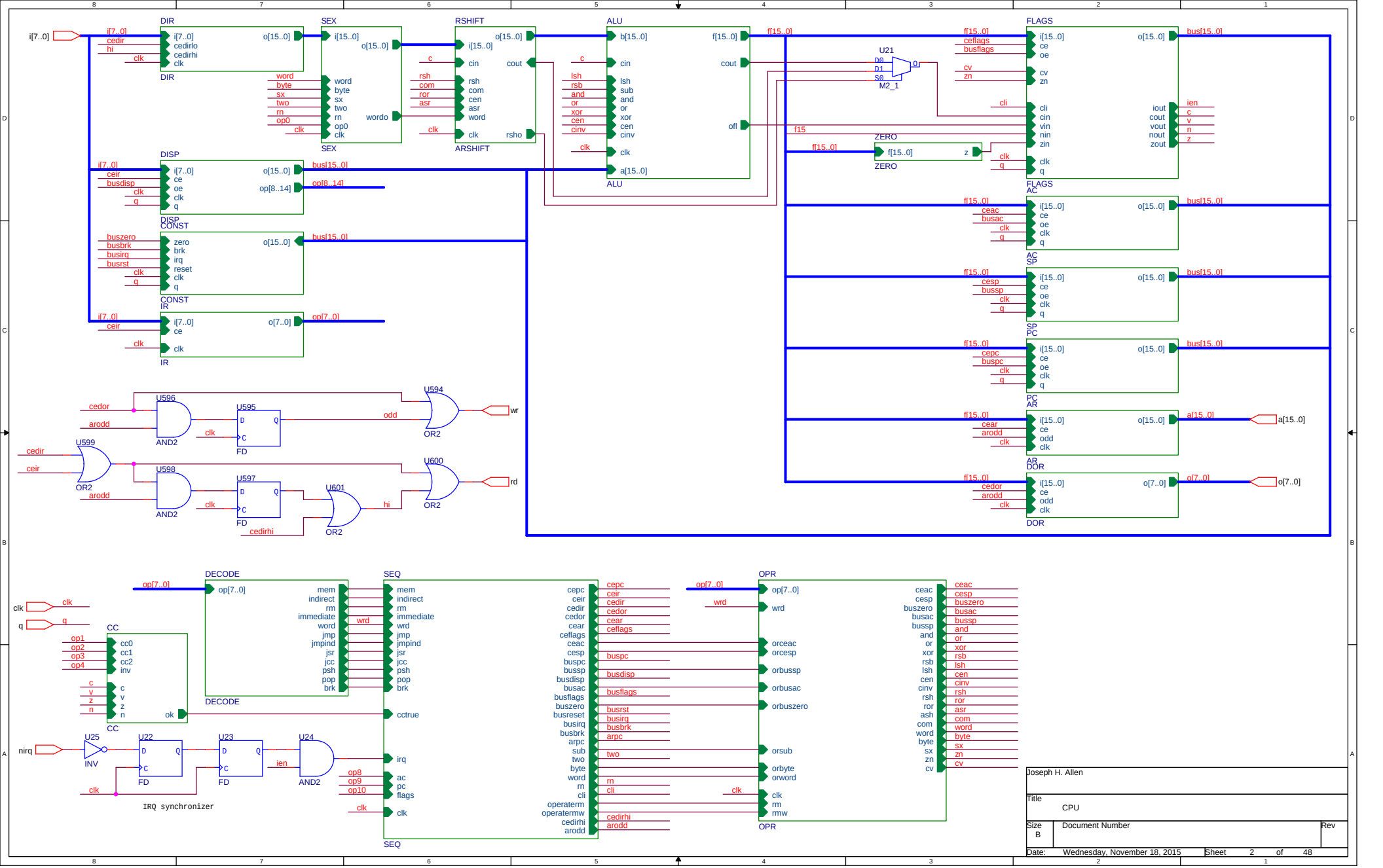
DIR
SEX
RSHIFT
ALU
FLAGS
U21
M2_1
ZERO
DISP
CONST
IR
FLAGS
AC
SP
PC
AR
DOR
U596
U595
U594
U599
U598
U597
U601
U600
AND2
FD
OR2
wr
rd
DECODE
SEQ
OPR
CC
U25
U22
U23
U24
INV
IRQ synchronizer
Joseph H. Allen
CPU
Size B
Document Number
Rev
Date: Wednesday, November 18, 2015
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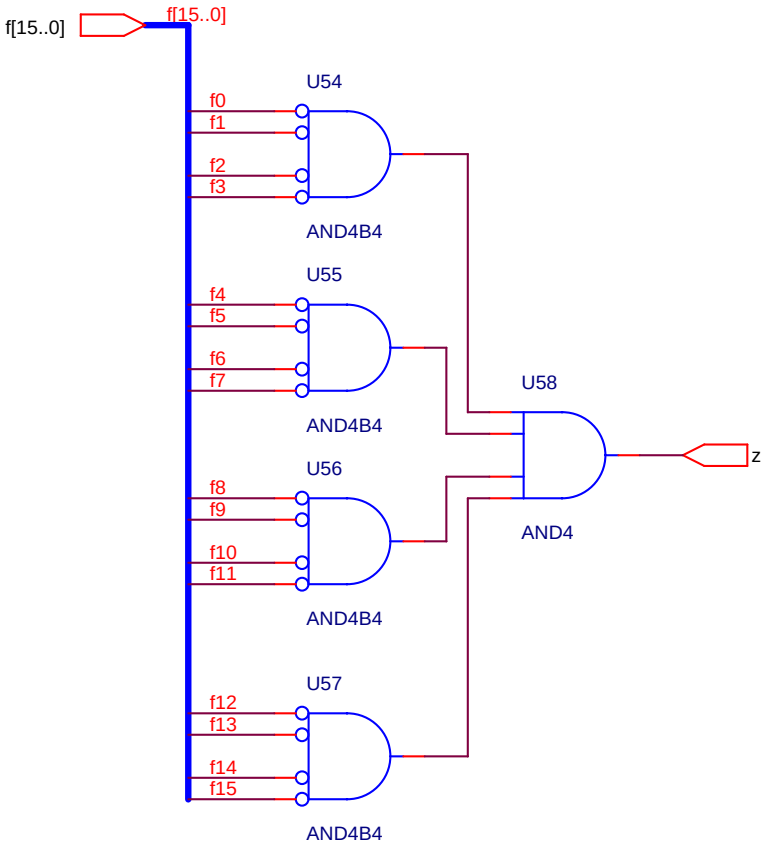
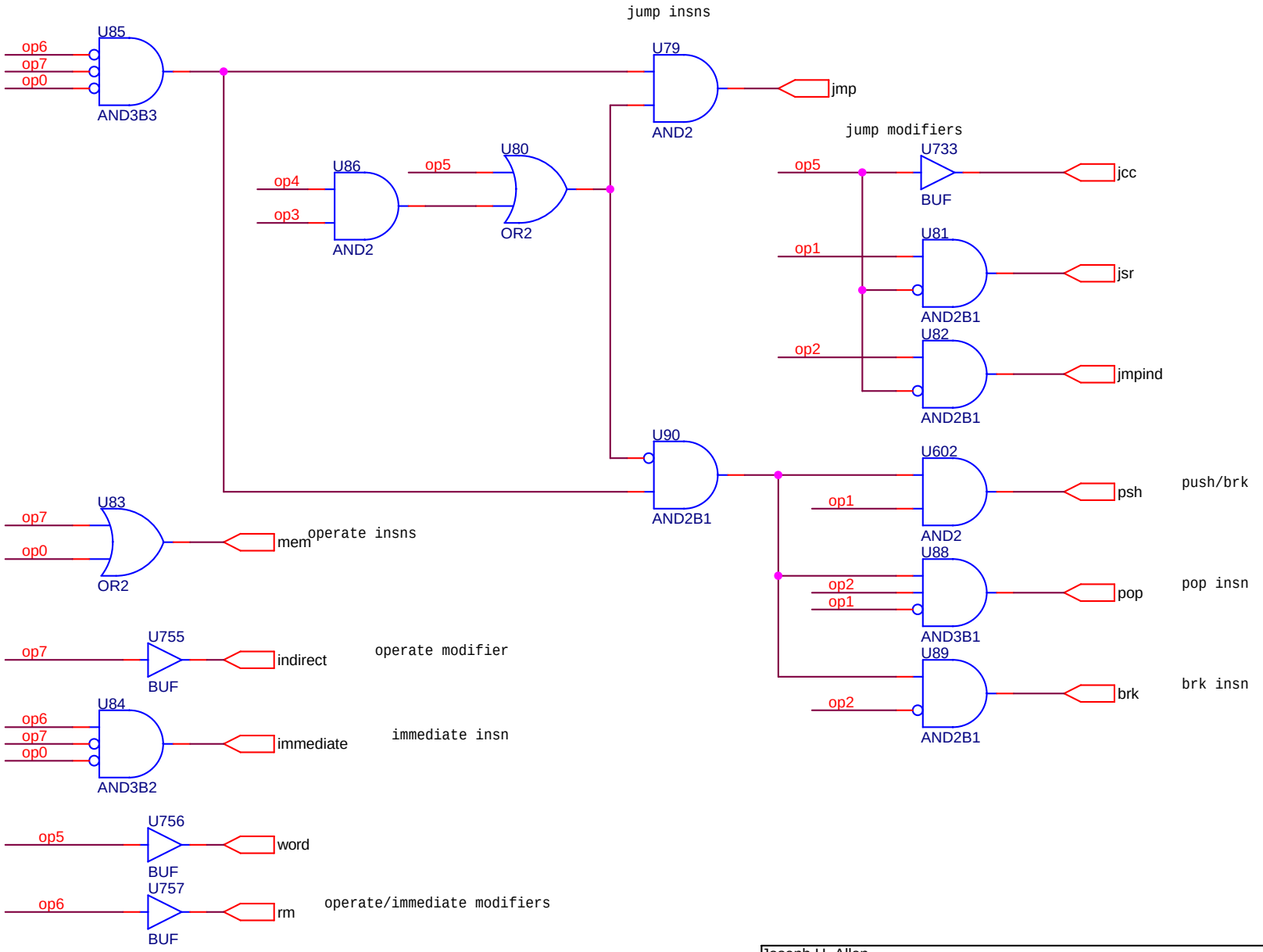
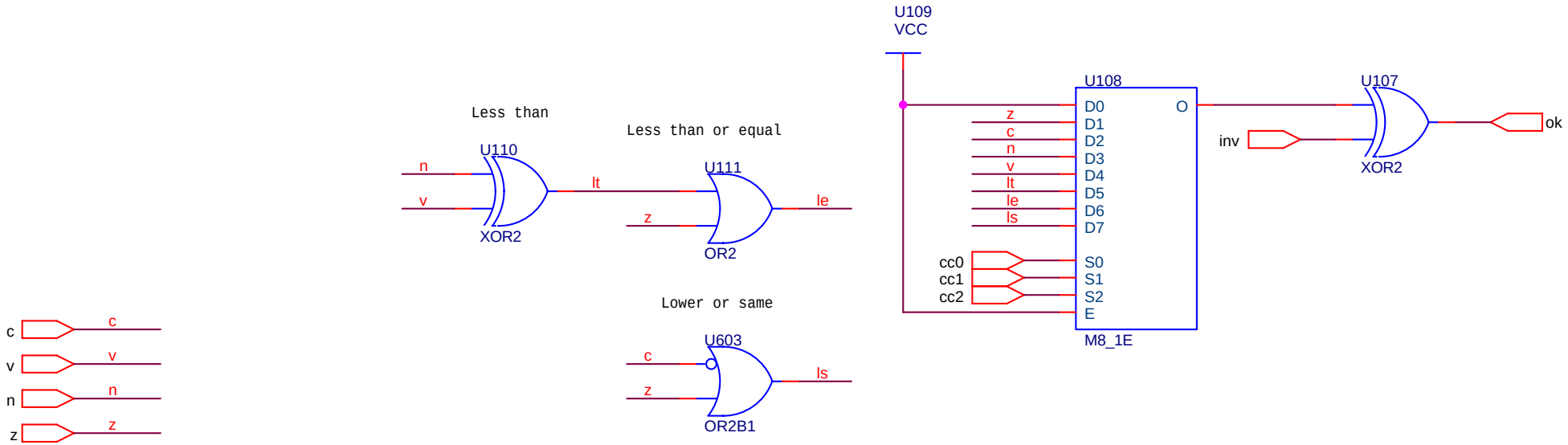


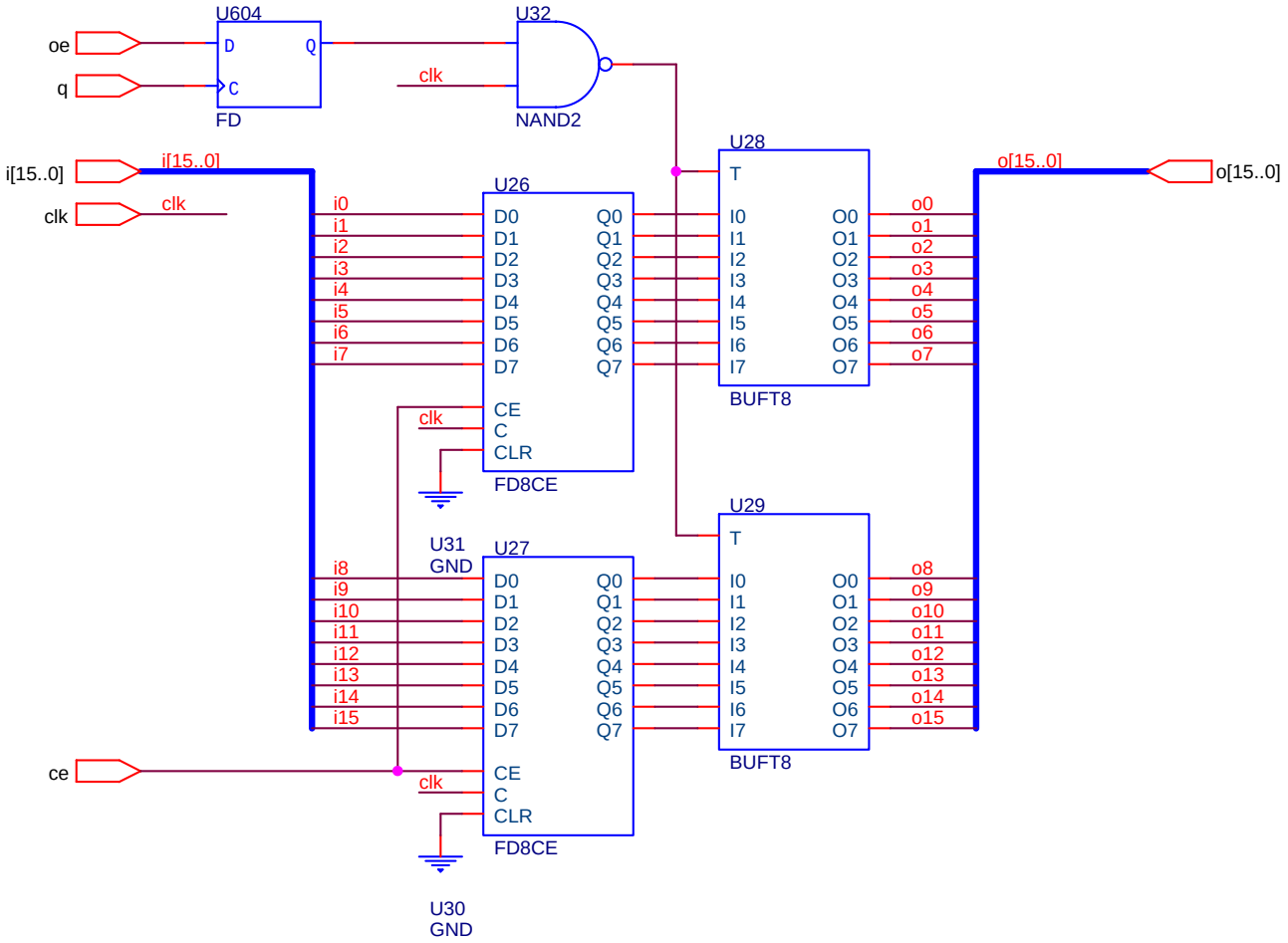
Joseph H. Allen		
Title: Zero detector		
Size: A	Document Number	Rev
Date: Wednesday, November 18, 2015	Sheet 3 of 48	



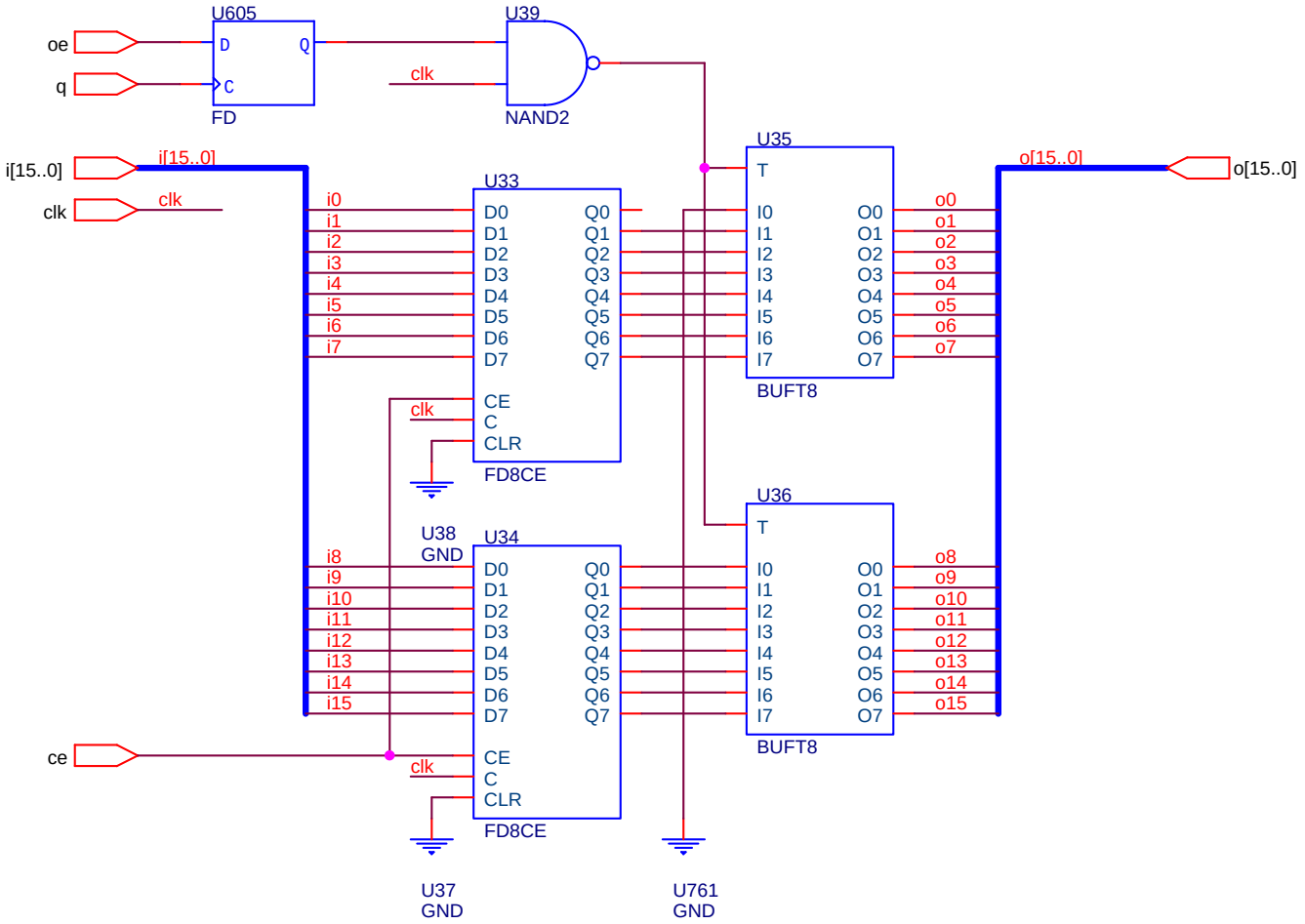
Joseph H. Allen		
Title: Instruction decoder		
Size: A	Document Number	Rev
Date: Wednesday, November 18, 2015	Sheet 4 of 48	



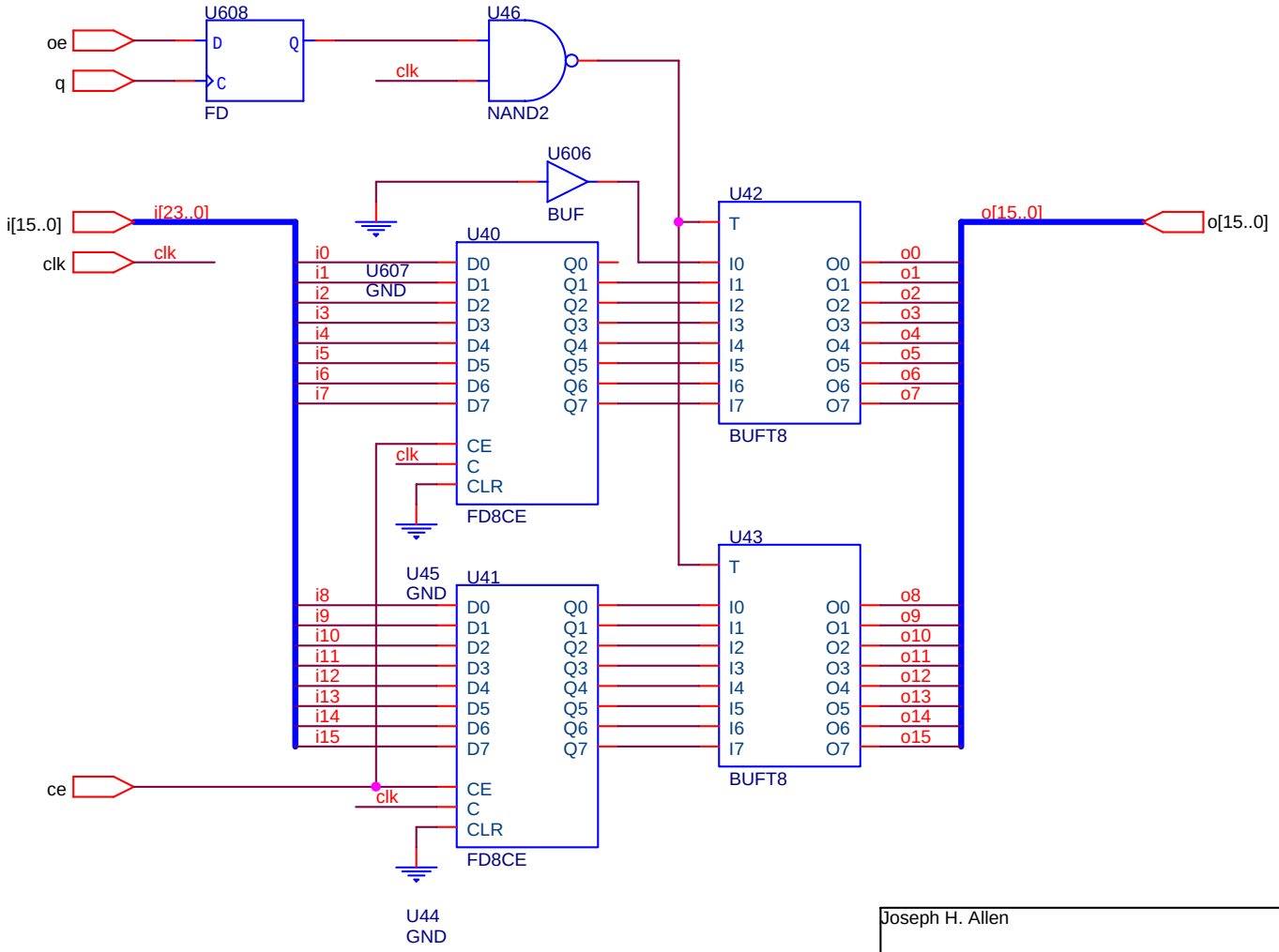
Joseph H. Allen		
Title: Condition test logic		
Size: A	Document Number	Rev
Date: Wednesday, November 18, 2015	Sheet 5 of 48	



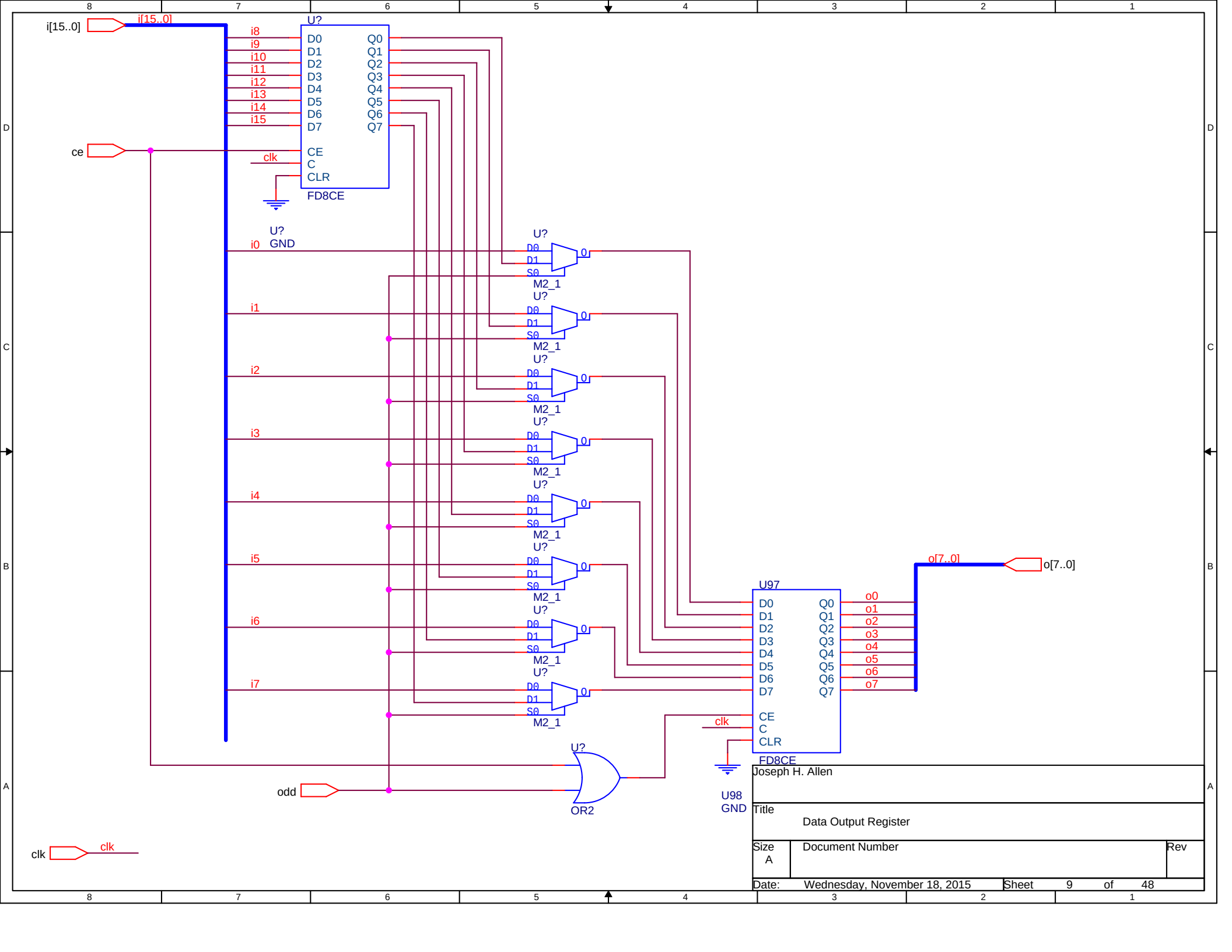
Joseph H. Allen		
Title: Accumulator		
Size: A	Document Number	Rev
Date: Wednesday, November 18, 2015	Sheet 6 of 48	



Joseph H. Allen		
Title: Stack Pointer		
Size: A	Document Number	Rev
Date: Wednesday, November 18, 2015	Sheet 7 of 48	



Joseph H. Allen		
Title: Program Counter		
Size: A	Document Number	Rev
Date: Wednesday, November 18, 2015	Sheet 8 of 48	


i[15..0]
i[15..0]
ce
clk
U?
D0
D1
D2
D3
D4
D5
D6
D7
CE
C
CLR
FD8CE
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
i8
i9
i10
i11
i12
i13
i14
i15
U?
GND
i0
M2_1
D0
D1
S0
0
i1
i2
i3
i4
i5
i6
i7
U97
o0
o1
o2
o3
o4
o5
o6
o7
o[7..0]
o[7..0]
odd
U?
OR2
U98
GND
clk
clk
Joseph H. Allen
Title
Data Output Register
Size
A
Document Number
Rev
Date:
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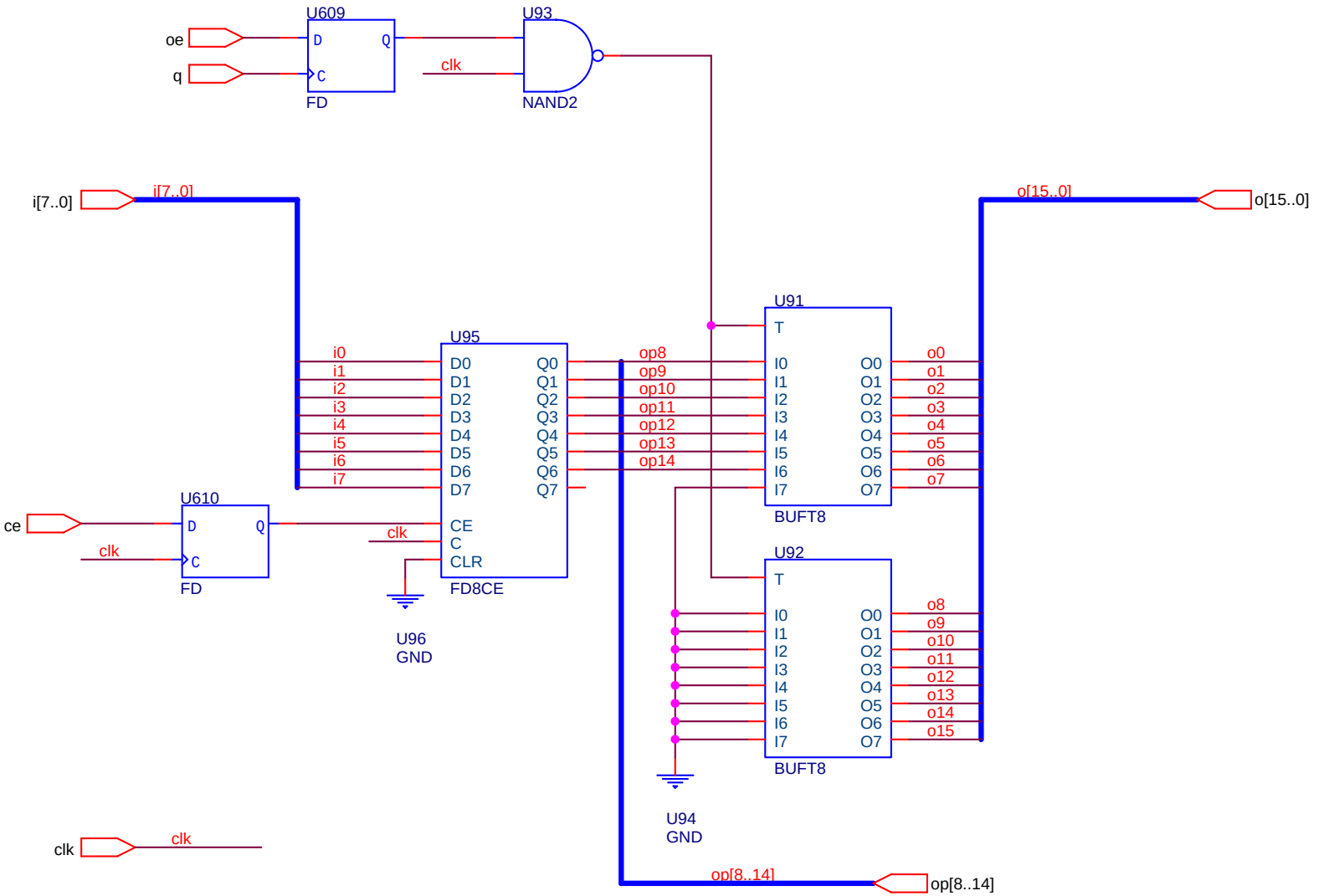
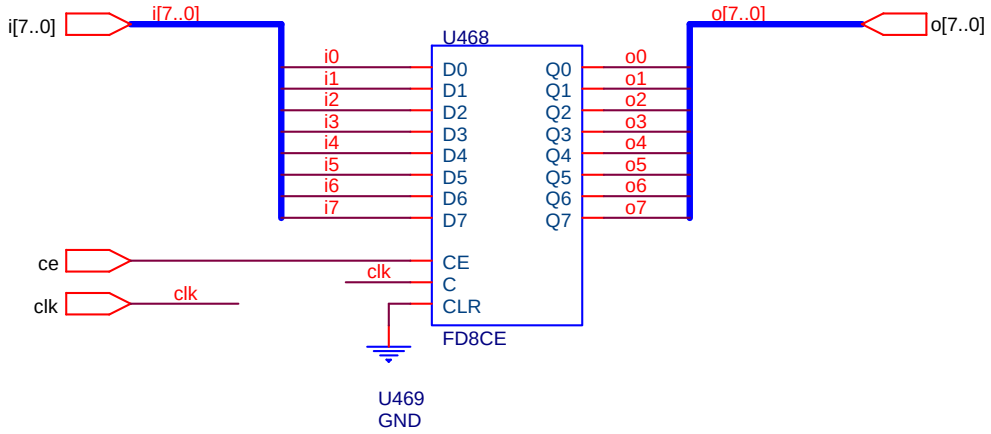
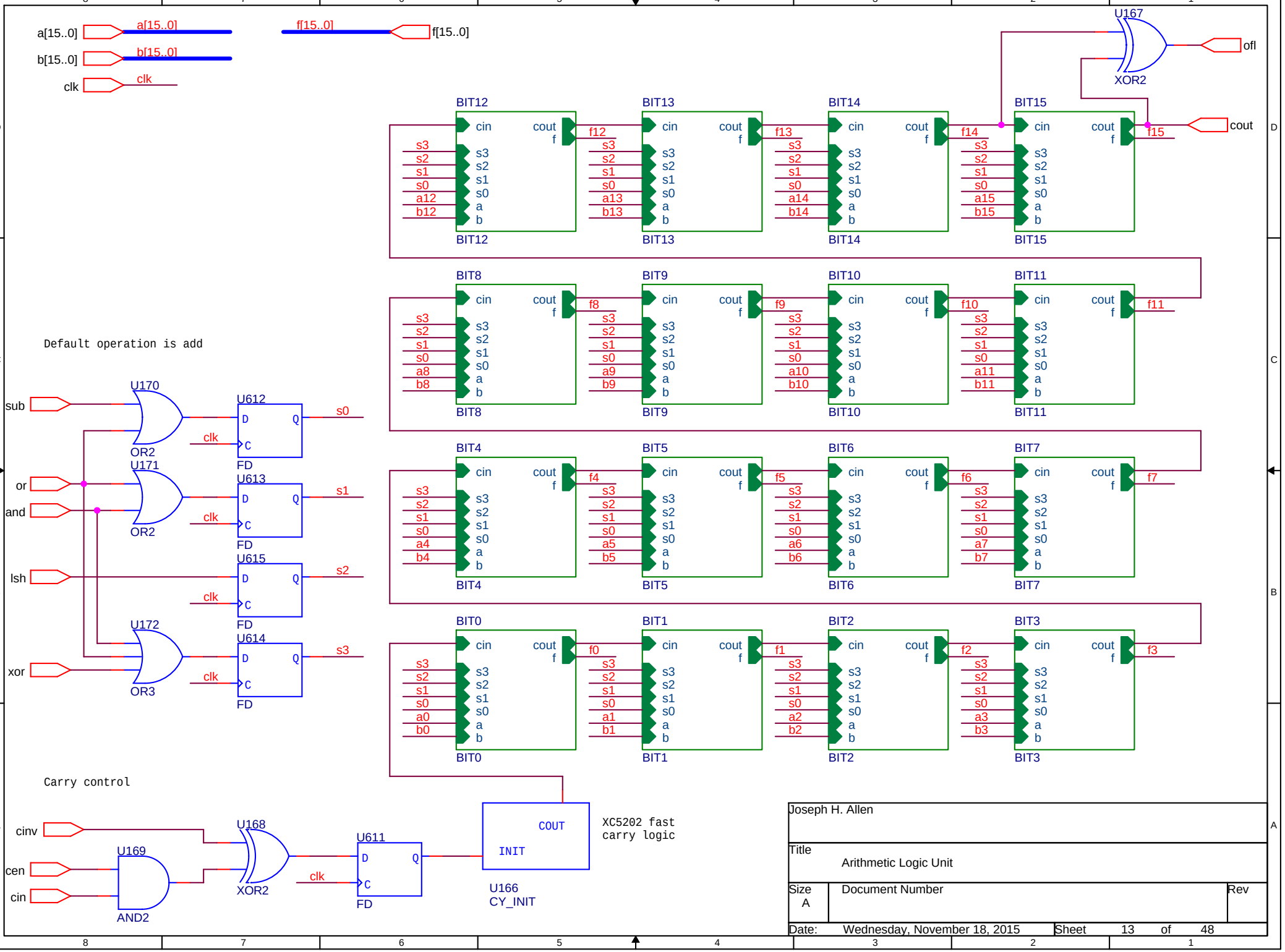
9
of
48



Joseph H. Allen		
Title: Displacement register		
Size: A	Document Number	Rev
Date: Wednesday, November 18, 2015	Sheet 11 of 48	



Joseph H. Allen		
Title: Instruction register		
Size: A	Document Number	Rev
Date: Wednesday, November 18, 2015	Sheet 12 of 48	


a[15..0]
b[15..0]
clk
f[15..0]
ofl
cout
U167
XOR2
BIT12
BIT13
BIT14
BIT15
BIT8
BIT9
BIT10
BIT11
BIT4
BIT5
BIT6
BIT7
BIT0
BIT1
BIT2
BIT3
cin
cout
f
s3
s2
s1
s0
a
b
Default operation is add
sub
or
and
lsh
xor
U170
U171
U172
OR2
OR3
U612
U613
U615
U614
FD
D
Q
C
s0
s1
s2
s3
Carry control
cinv
cen
cin
U169
AND2
U168
XOR2
U611
U166
CY_INIT
COUT
INIT
XC5202 fast
carry logic
Joseph H. Allen
Title
Arithmetic Logic Unit
Size
A
Document Number
Rev
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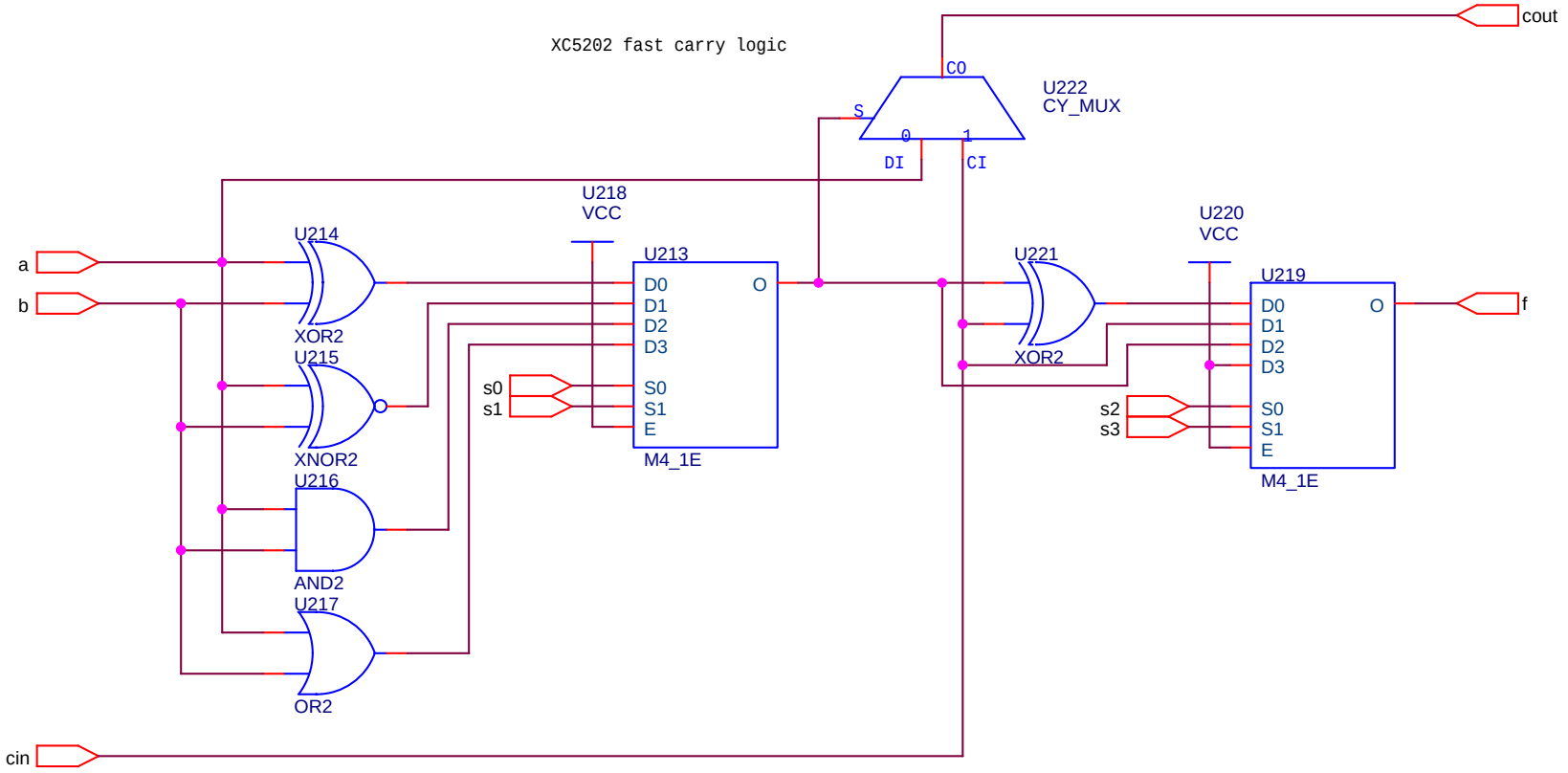

Joseph H. Allen		
Title: ALU BIT		
Size: A	Document Number	Rev
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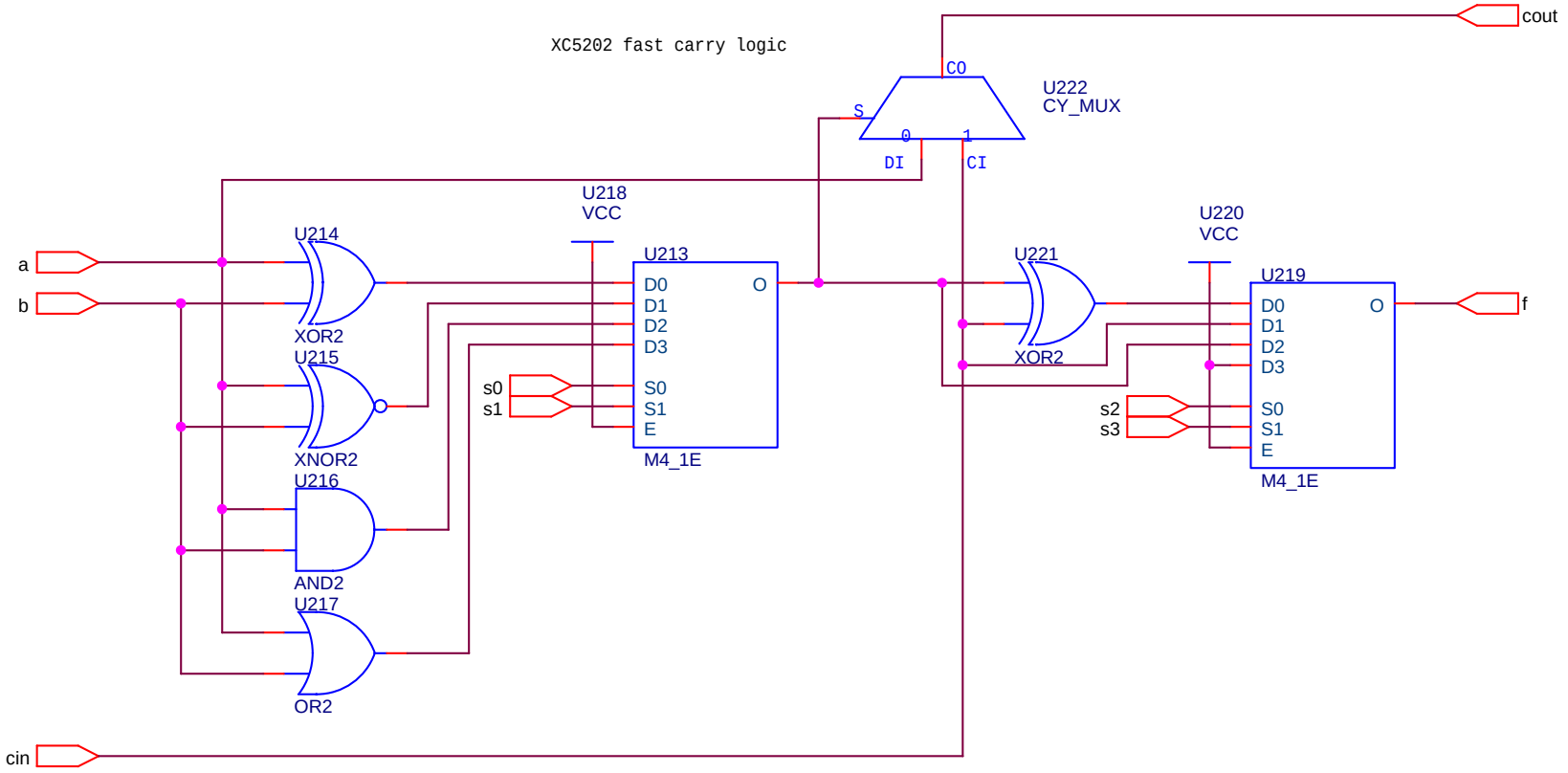
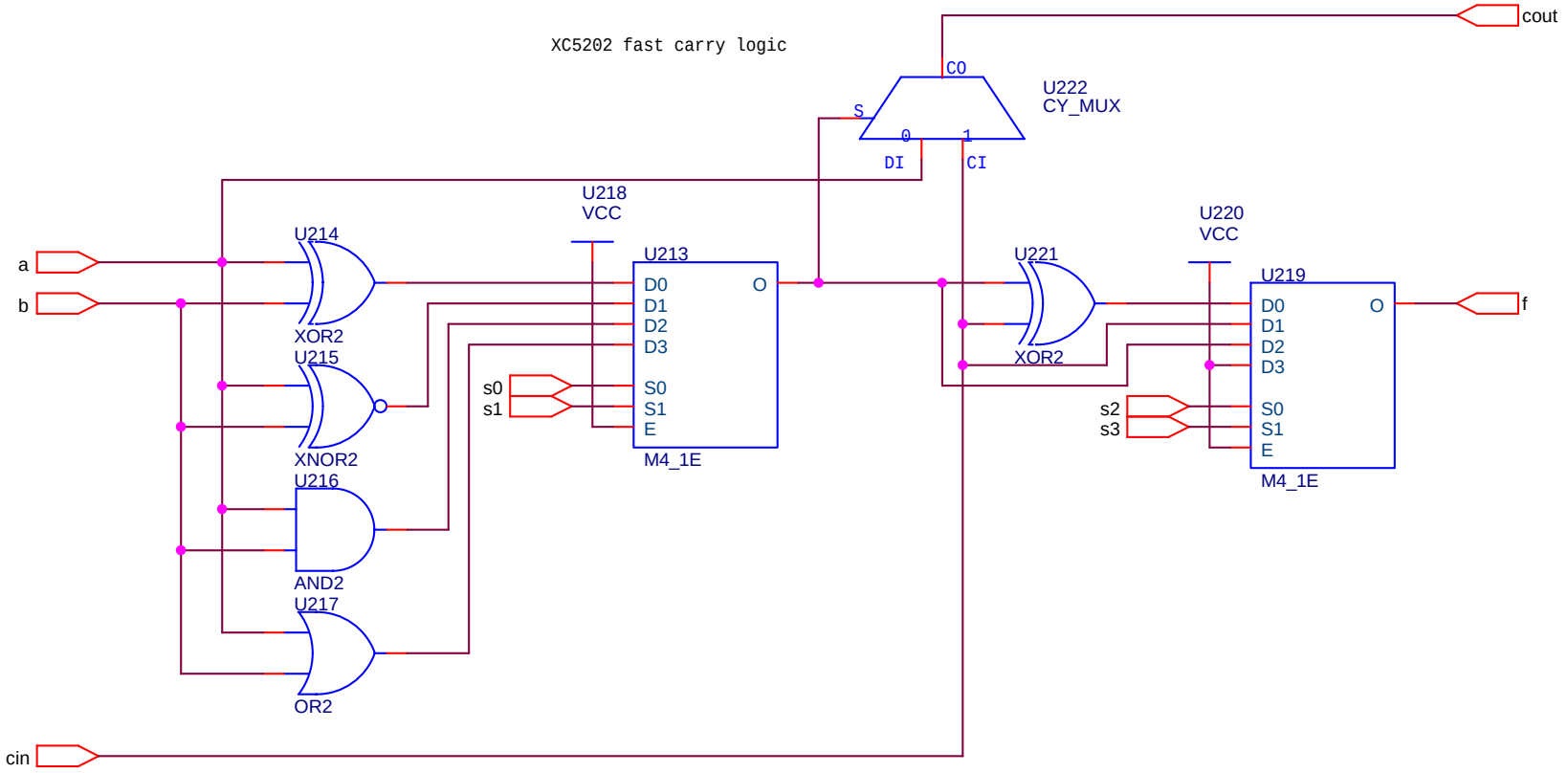
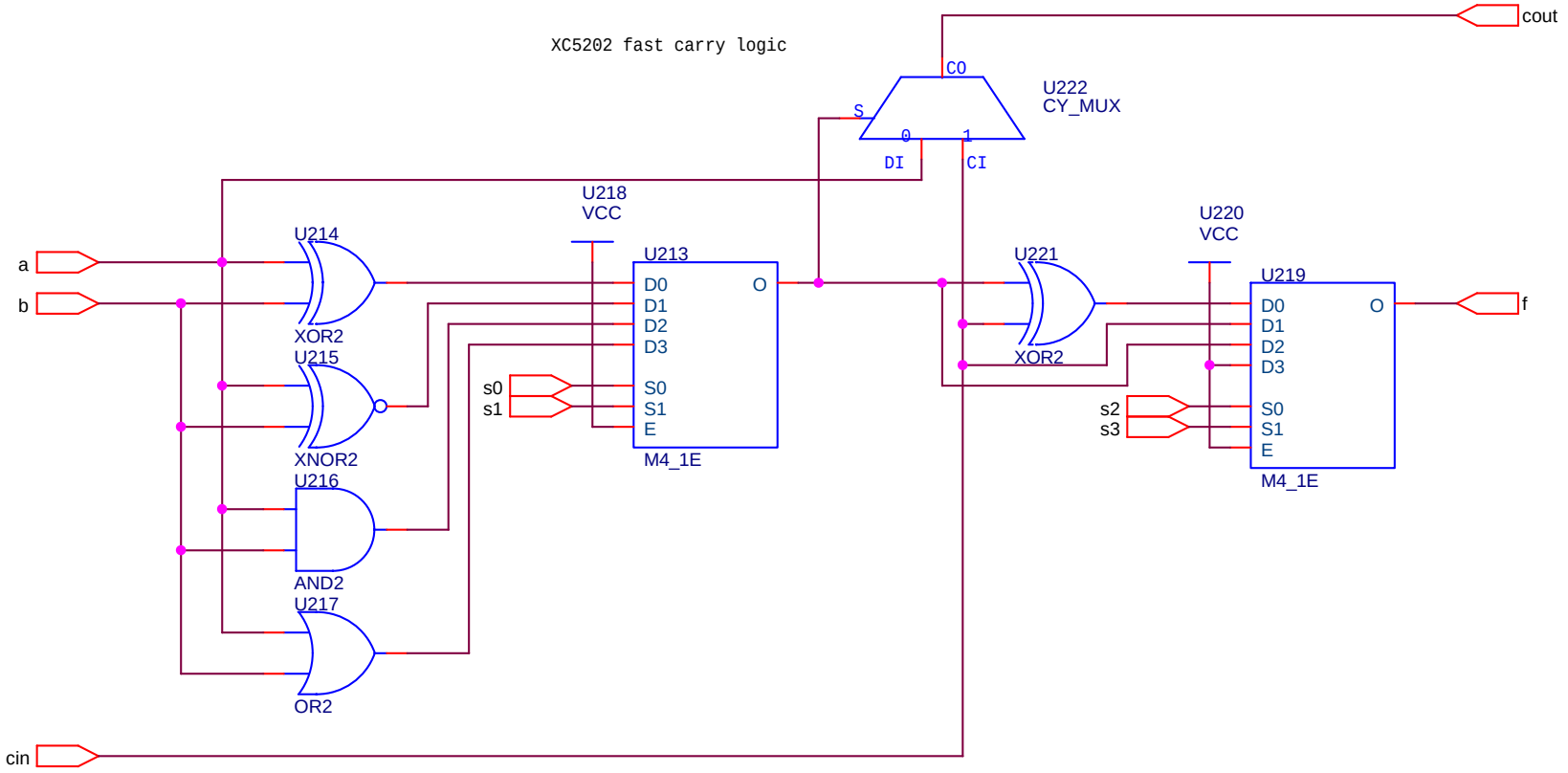


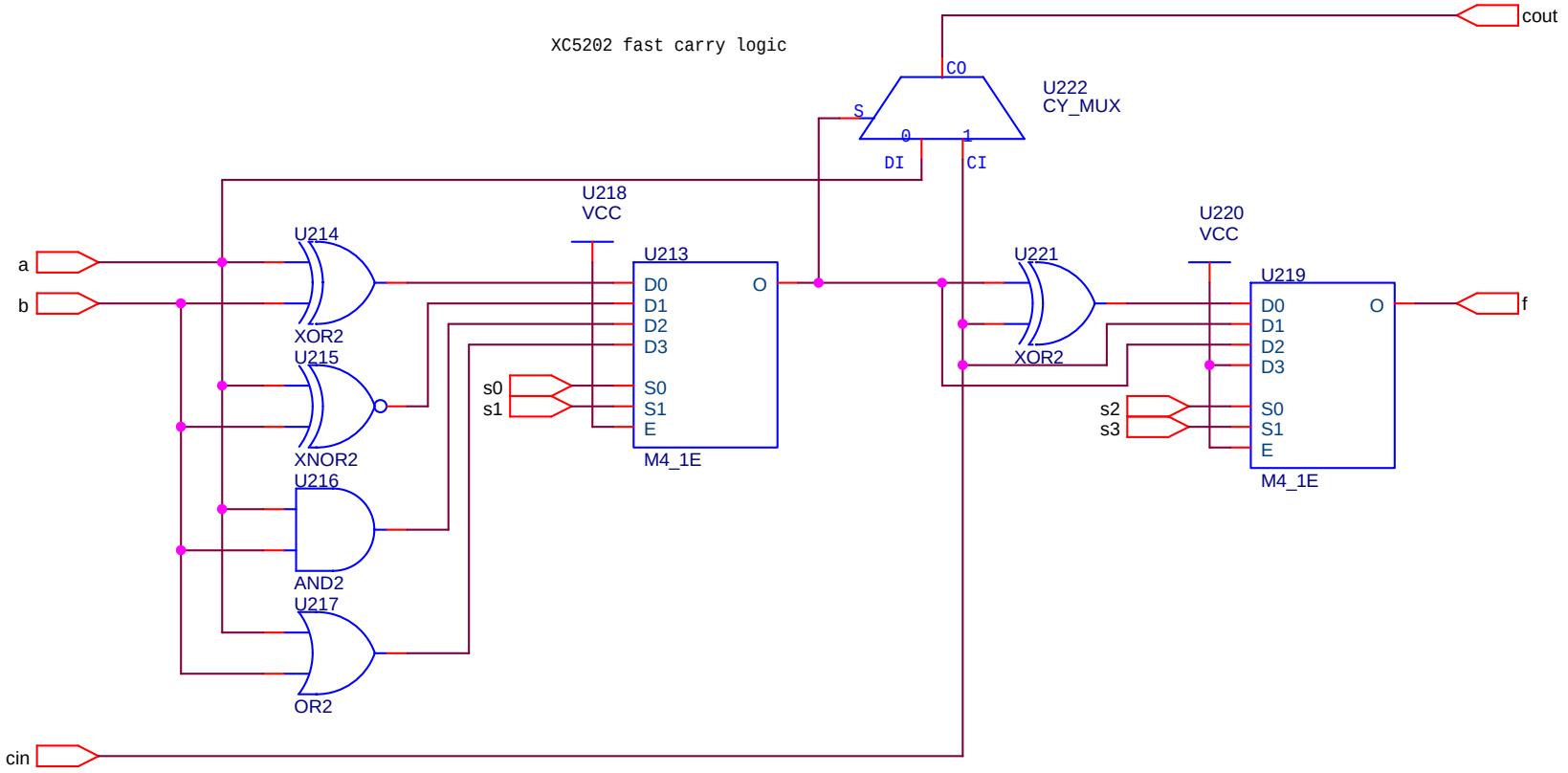
Joseph H. Allen		
Title: ALU BIT		
Size: A	Document Number	Rev
Date: Wednesday, November 18, 2015	Sheet 15 of 48	



Joseph H. Allen		
Title: ALU BIT		
Size: A	Document Number	Rev
Date: Wednesday, November 18, 2015	Sheet 16 of 48	



Joseph H. Allen		
Title: ALU BIT		
Size: A	Document Number	Rev
Date: Wednesday, November 18, 2015	Sheet 17 of 48	



Joseph H. Allen		
Title: ALU BIT		
Size: A	Document Number	Rev
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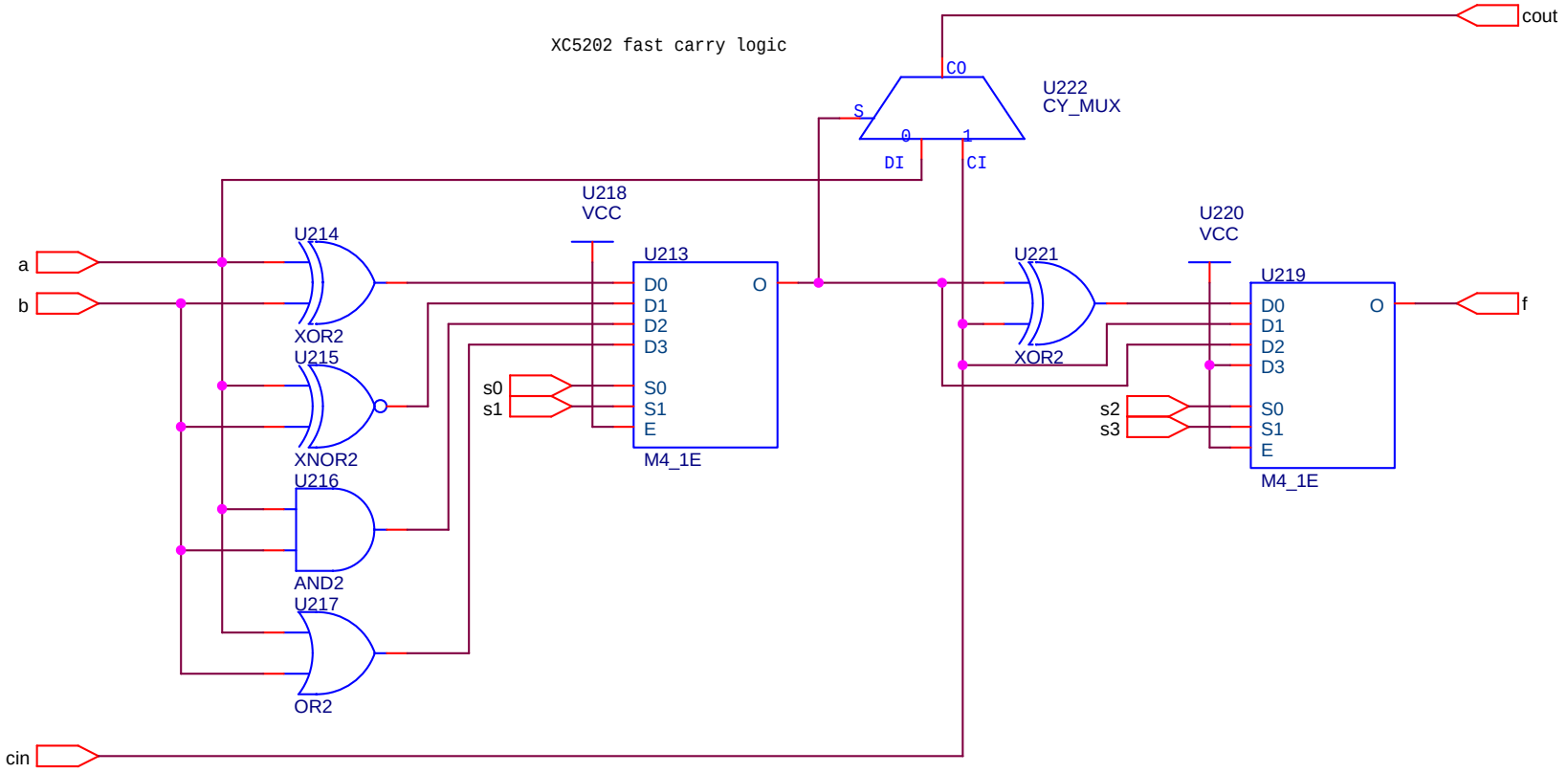
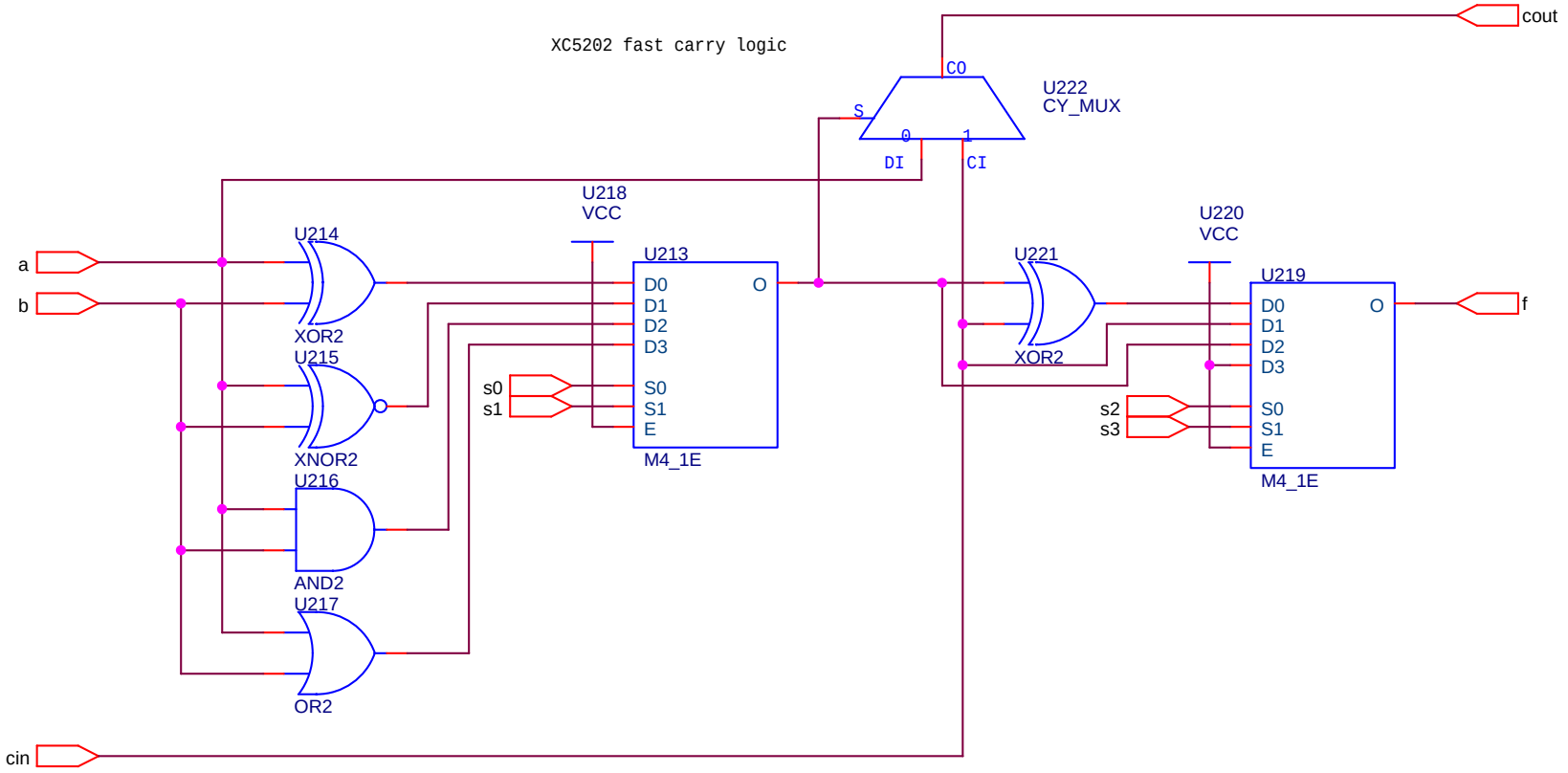
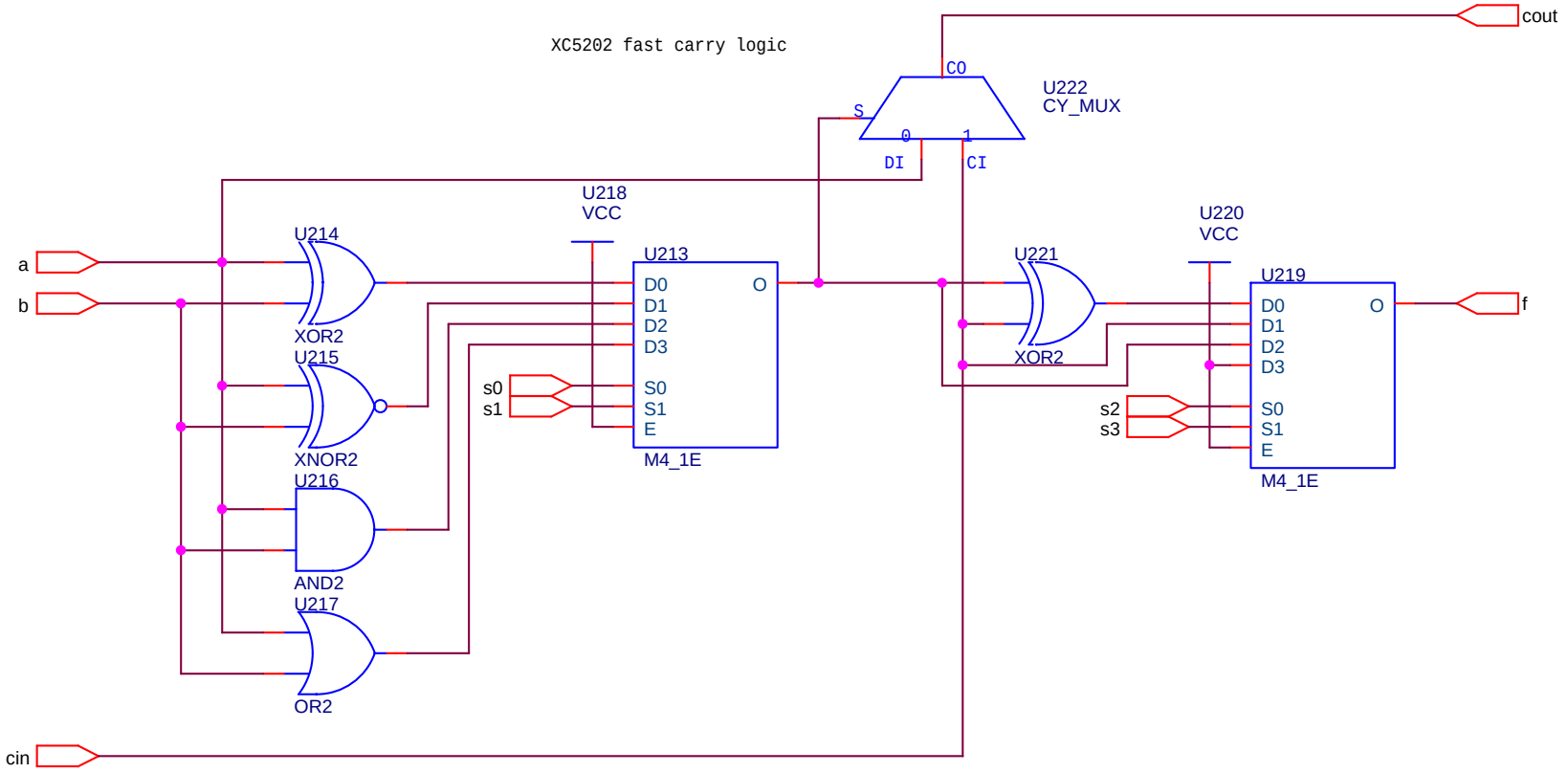


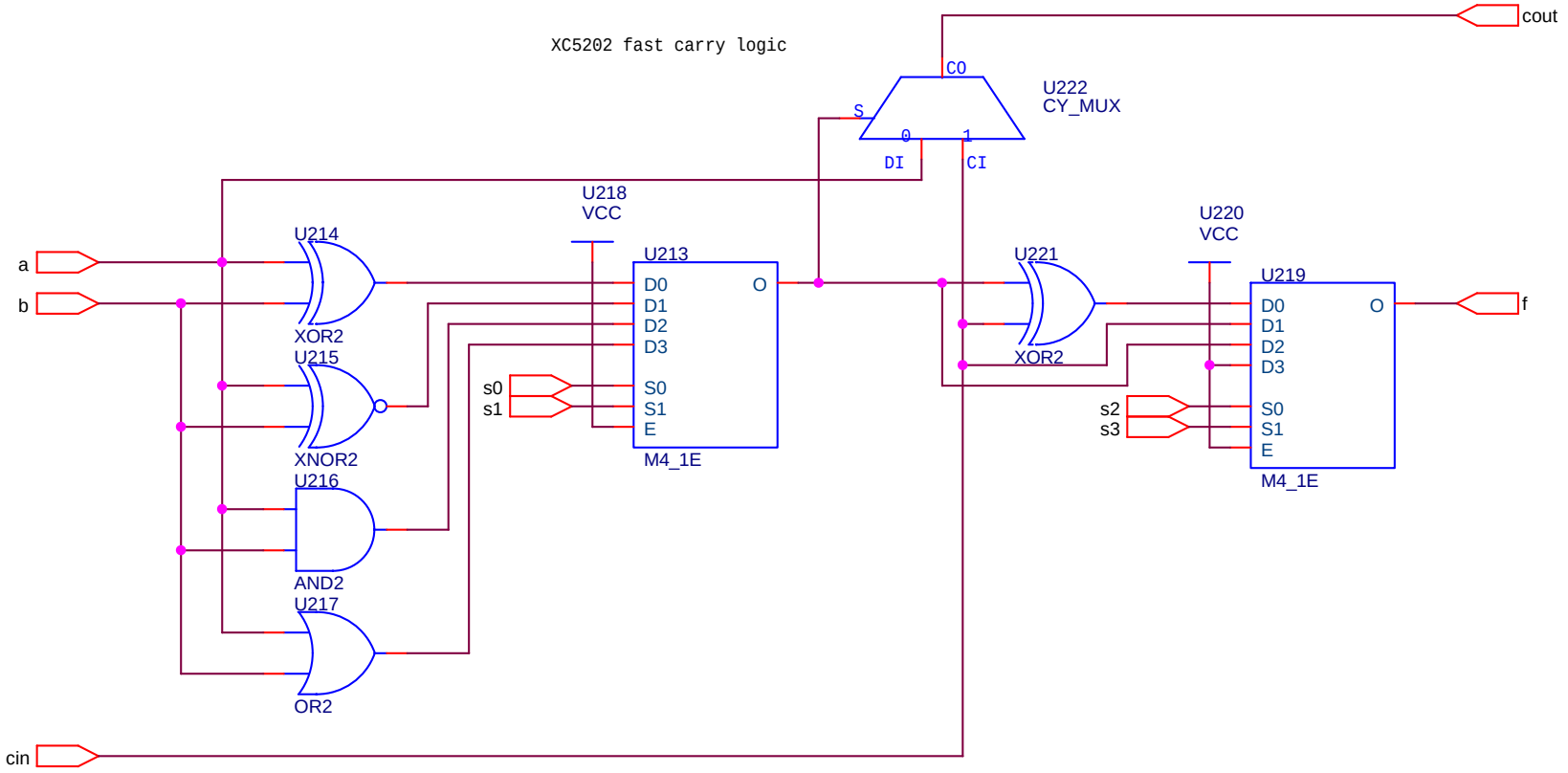
Joseph H. Allen		
Title: ALU BIT		
Size: A	Document Number	Rev
Date: Wednesday, November 18, 2015	Sheet 19 of 48	



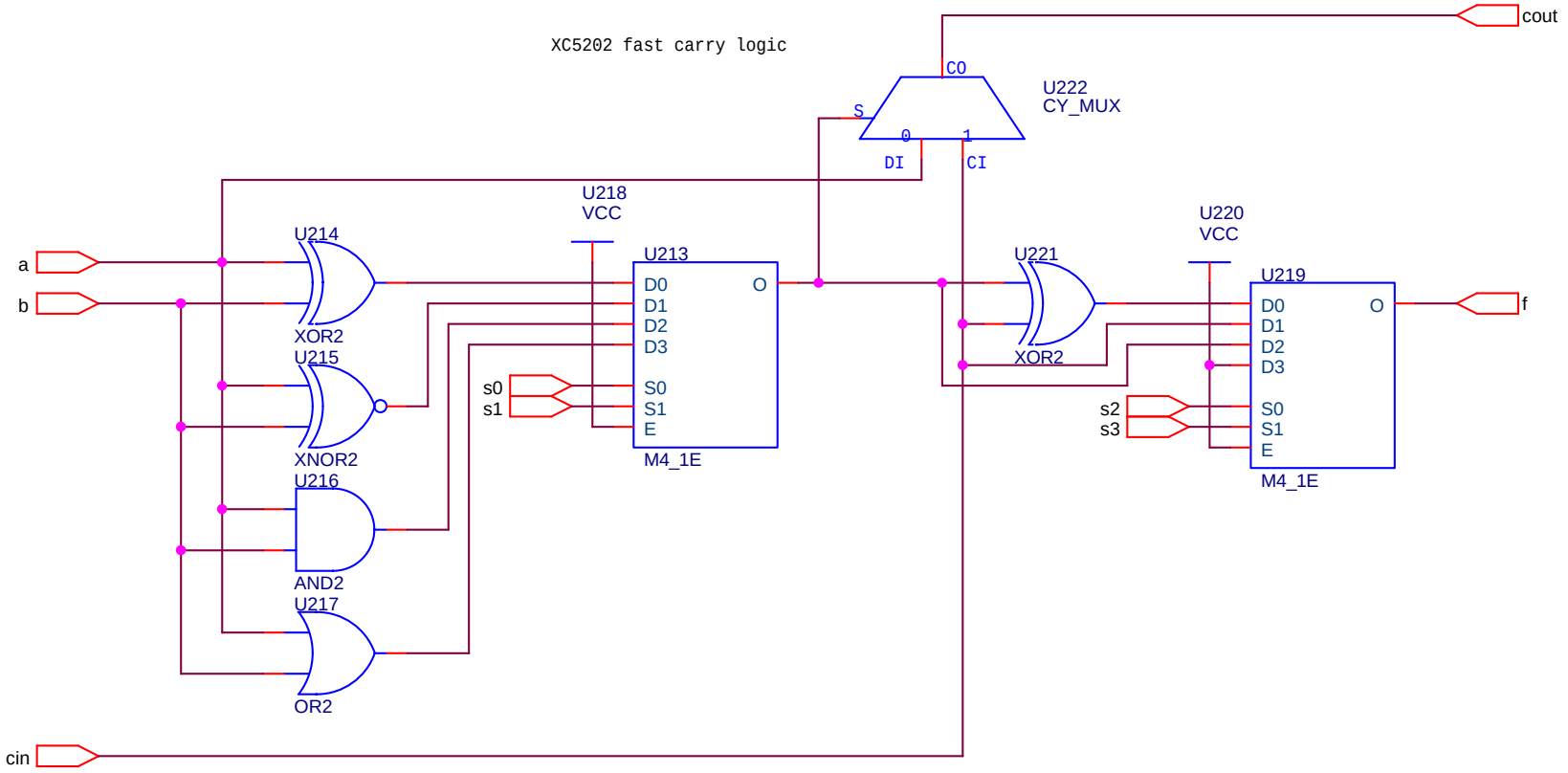
Joseph H. Allen		
Title: ALU BIT		
Size: A	Document Number	Rev
Date: Wednesday, November 18, 2015	Sheet 20 of 48	



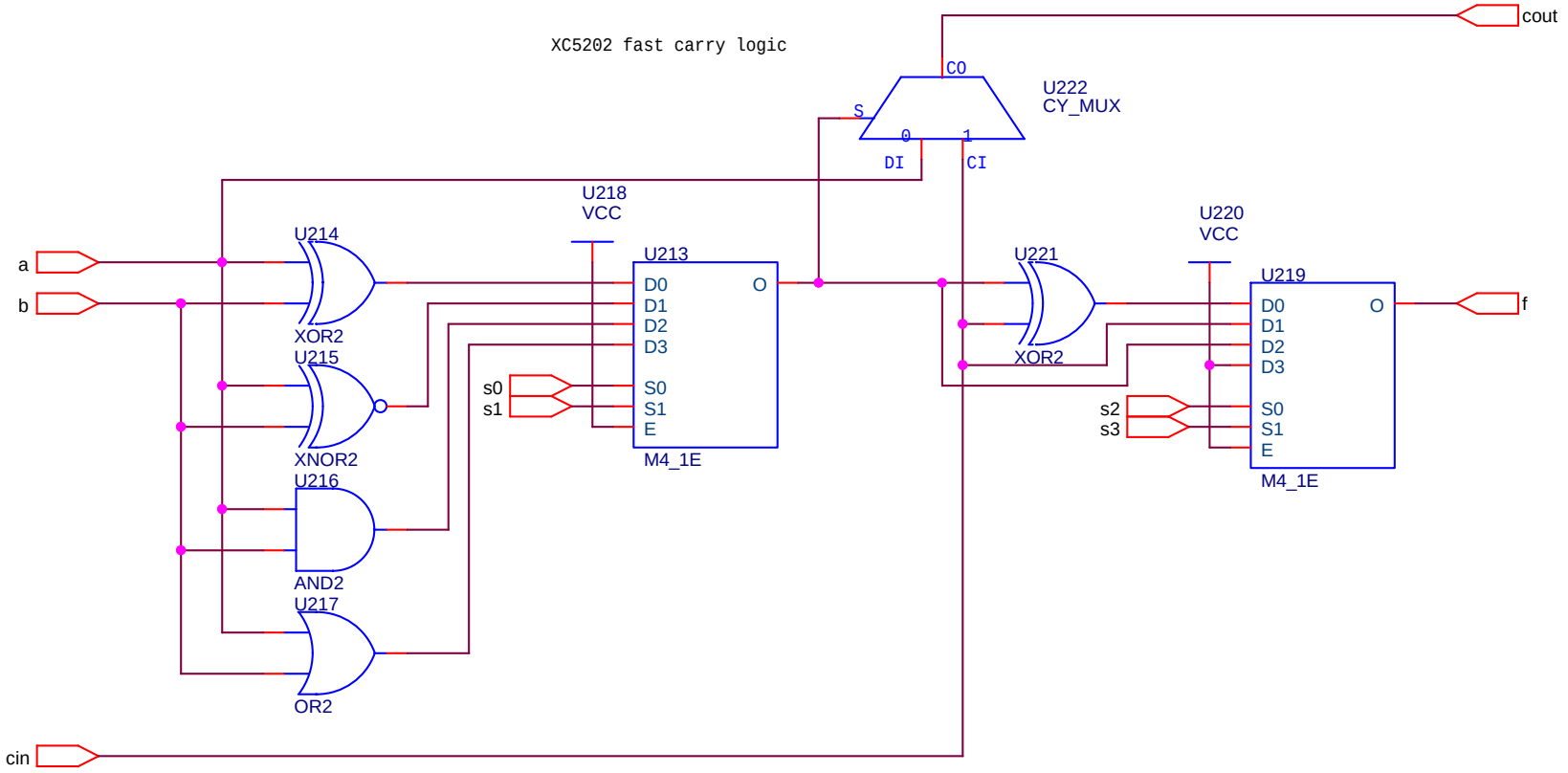
Joseph H. Allen		
Title: ALU BIT		
Size: A	Document Number	Rev
Date: Wednesday, November 18, 2015	Sheet 21 of 48	



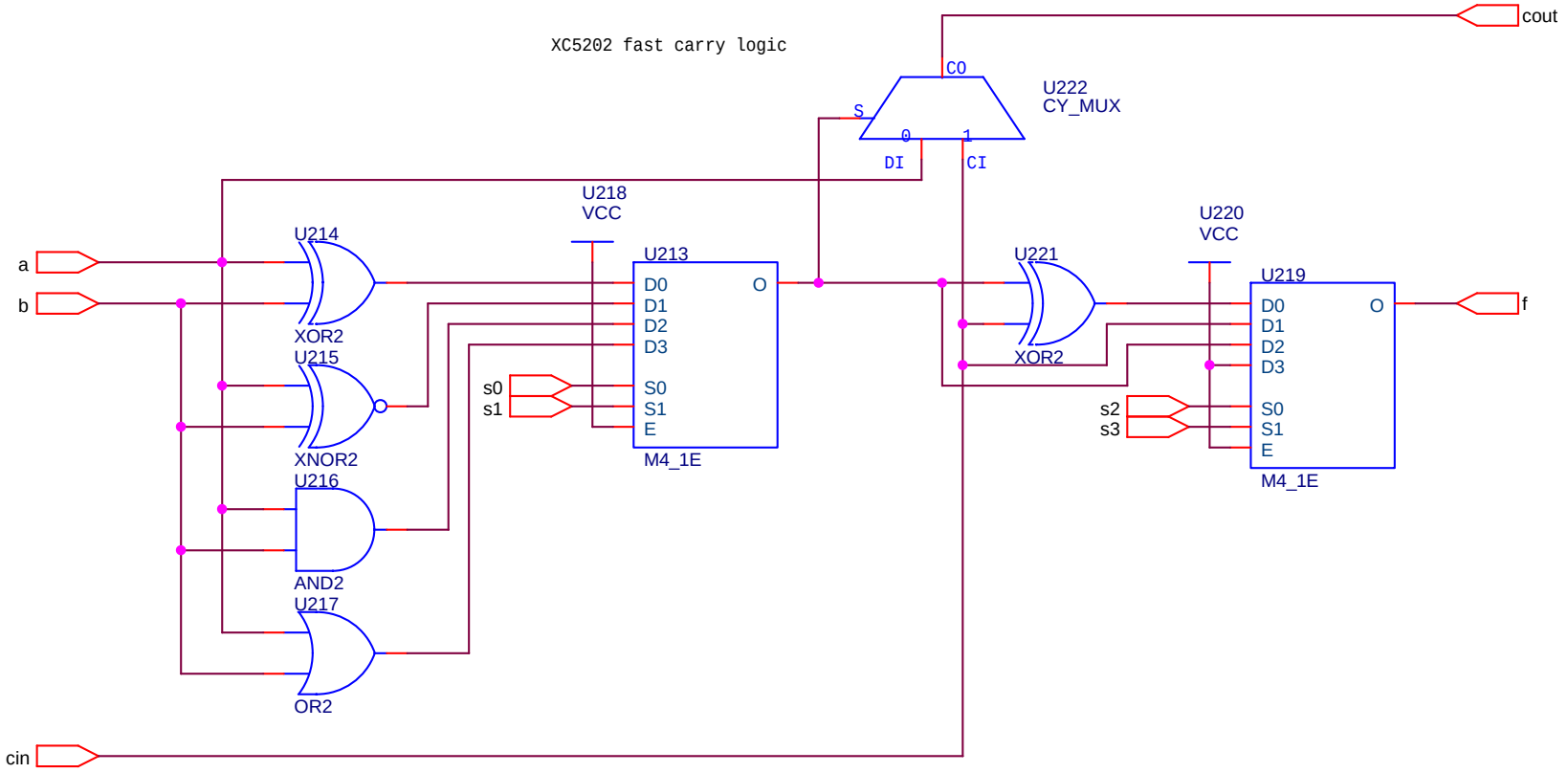
Joseph H. Allen		
Title: ALU BIT		
Size: A	Document Number	Rev
Date: Wednesday, November 18, 2015	Sheet 22 of 48	



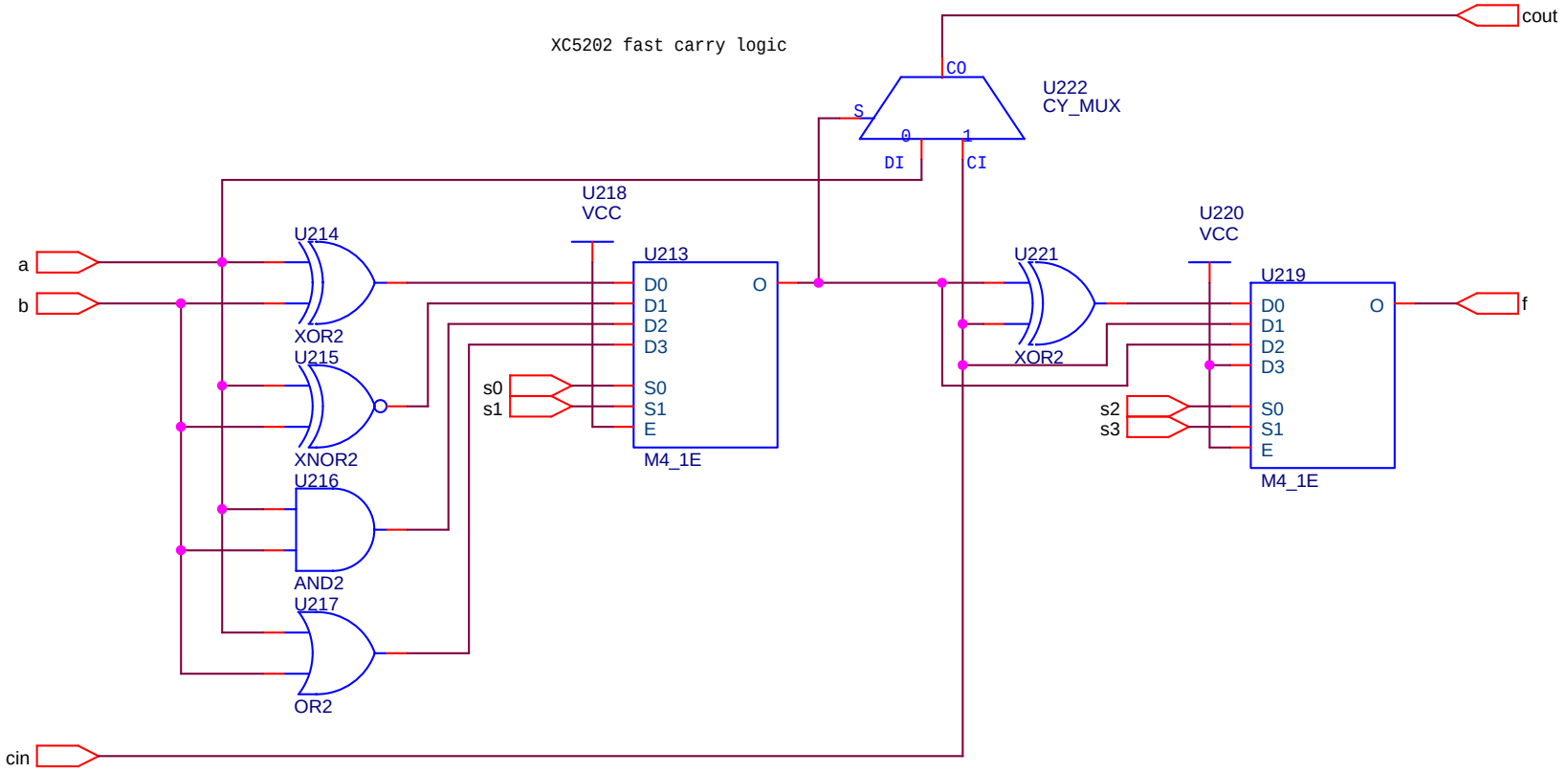
Joseph H. Allen		
Title: ALU BIT		
Size: A	Document Number	Rev
Date: Wednesday, November 18, 2015	Sheet 23 of 48	



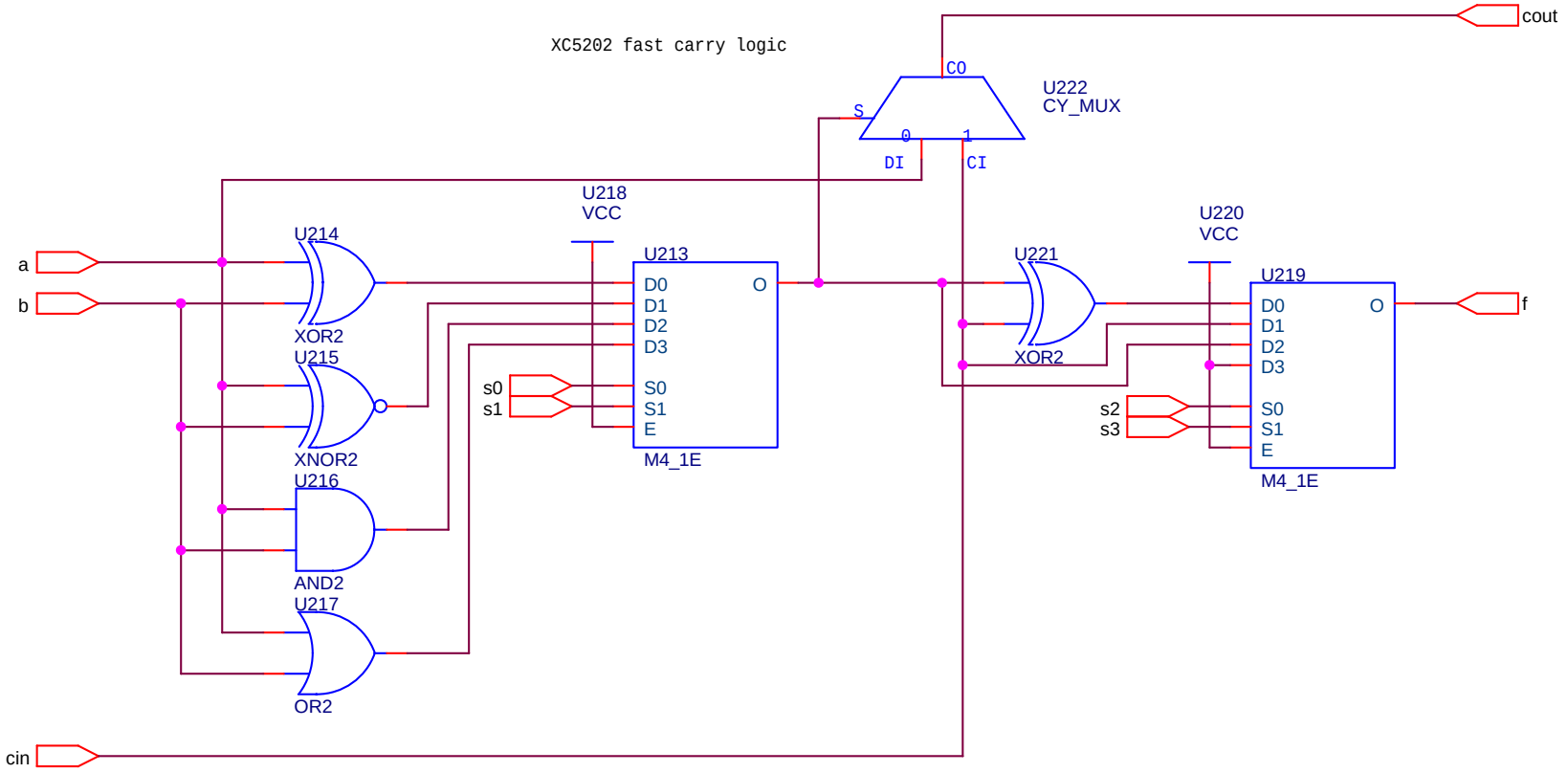
Joseph H. Allen		
Title: ALU BIT		
Size: A	Document Number	Rev
Date: Wednesday, November 18, 2015	Sheet 24 of 48	



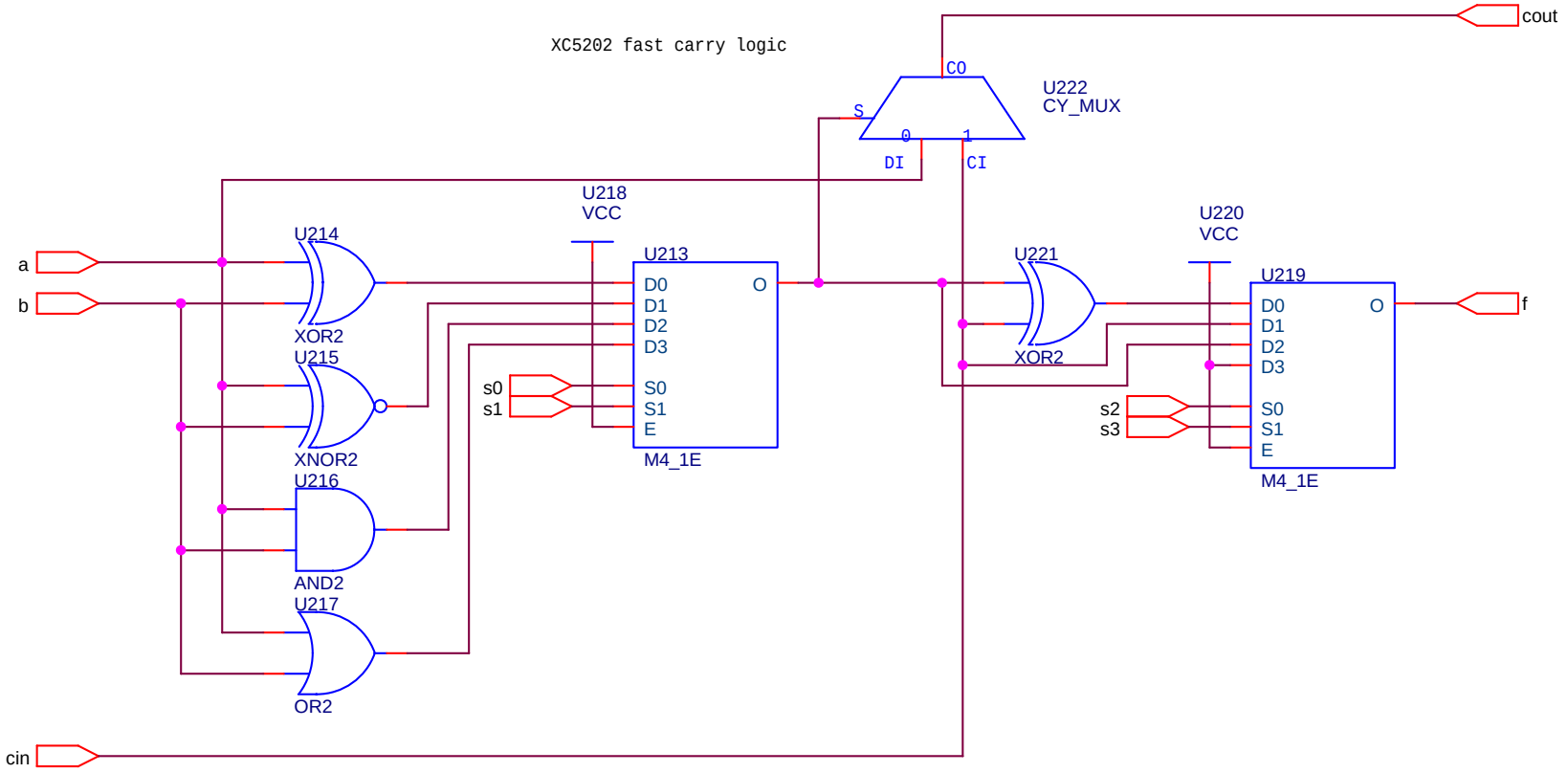
Joseph H. Allen		
Title: ALU BIT		
Size: A	Document Number	Rev
Date: Wednesday, November 18, 2015	Sheet 25 of 48	



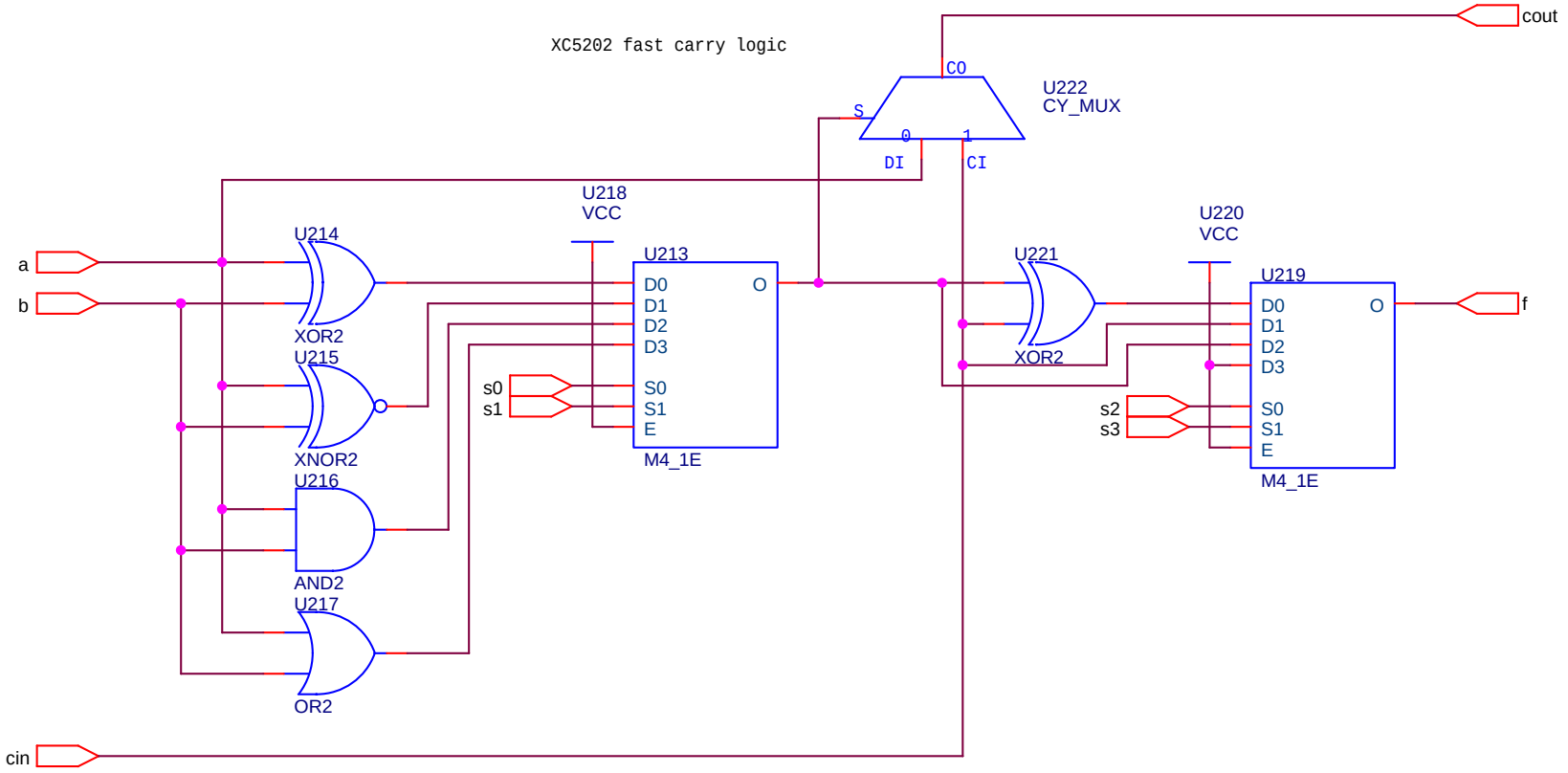
Joseph H. Allen		
Title: ALU BIT		
Size: A	Document Number	Rev
Date: Wednesday, November 18, 2015	Sheet 26 of 48	



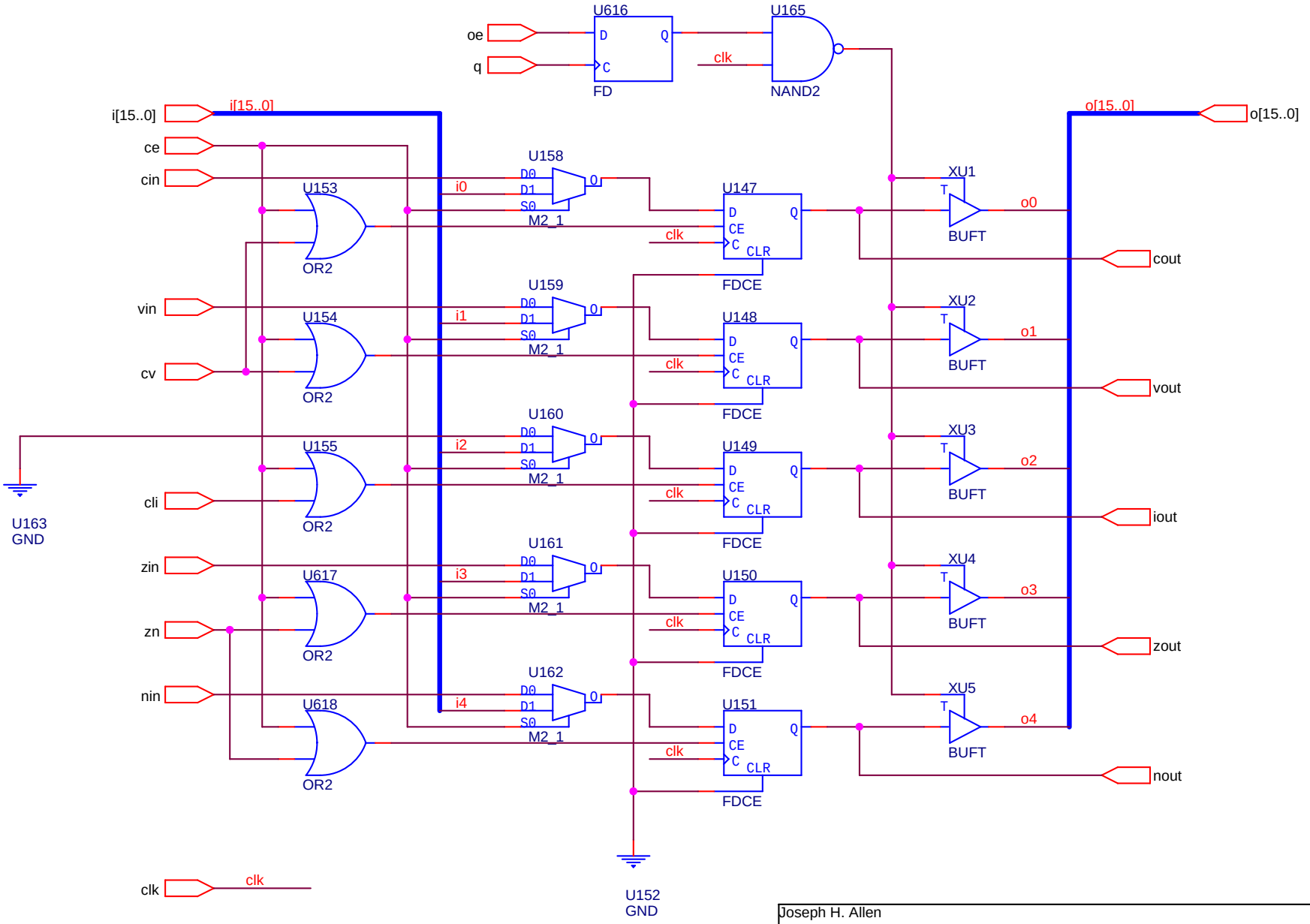
Joseph H. Allen		
Title: ALU BIT		
Size: A	Document Number	Rev
Date: Wednesday, November 18, 2015	Sheet 27 of 48	



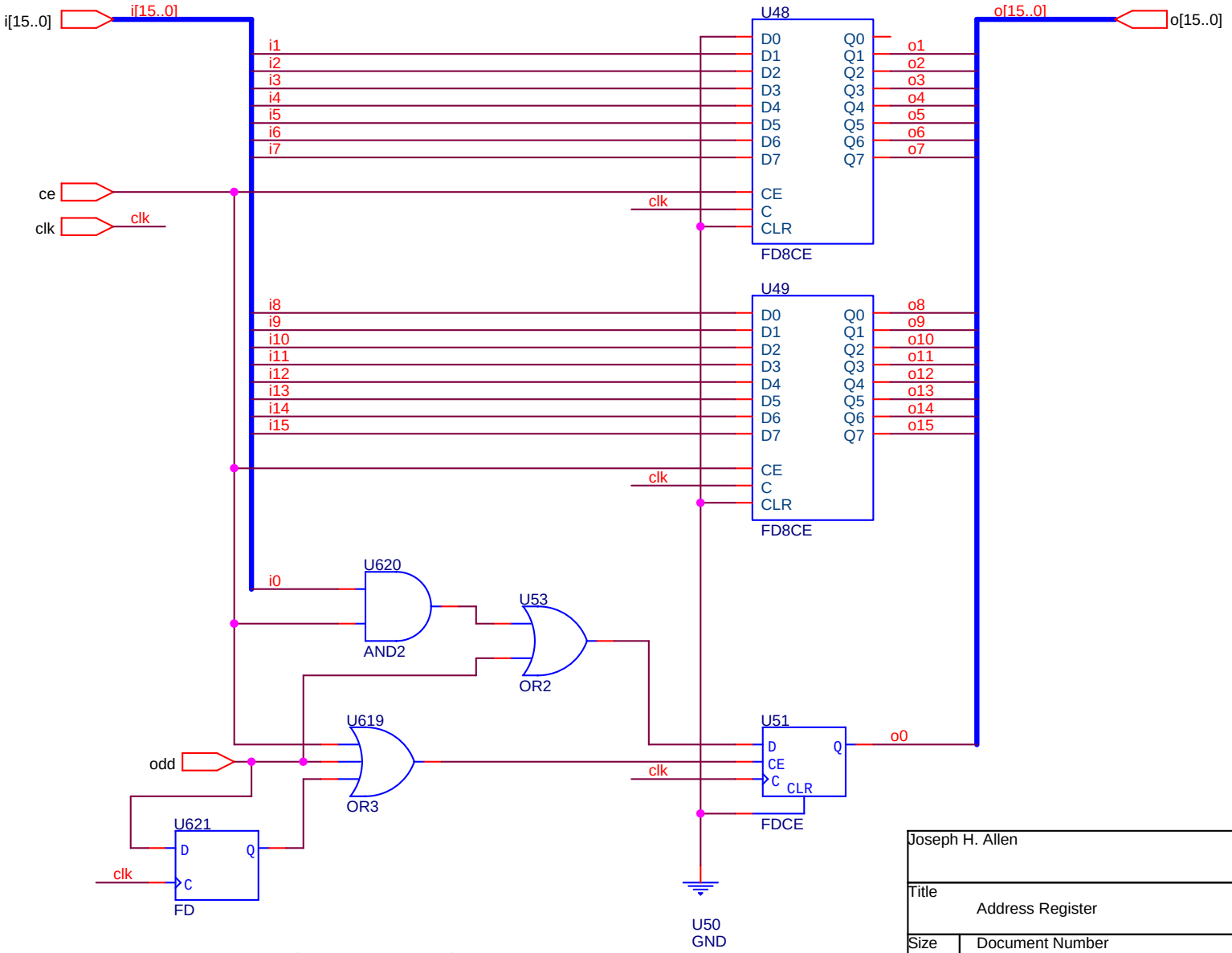
Joseph H. Allen		
Title: ALU BIT		
Size: A	Document Number	Rev
Date: Wednesday, November 18, 2015	Sheet 28 of 48	



Joseph H. Allen		
Title: ALU BIT		
Size: A	Document Number	Rev
Date: Wednesday, November 18, 2015	Sheet 29 of 48	



Joseph H. Allen		
Title: Status flags		
Size: A	Document Number	Rev
Date: Wednesday, November 18, 2015	Sheet 30 of 48	


i[15..0]
i[15..0]
i1
i2
i3
i4
i5
i6
i7
ce
clk
clk
clk
U48
D0
D1
D2
D3
D4
D5
D6
D7
CE
C
CLR
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
FD8CE
o1
o2
o3
o4
o5
o6
o7
o[15..0]
o[15..0]
i8
i9
i10
i11
i12
i13
i14
i15
clk
U49
FD8CE
o8
o9
o10
o11
o12
o13
o14
o15
i0
U620
AND2
U53
OR2
U619
OR3
odd
U621
D
Q
C
clk
FD
U51
D
Q
CE
C
CLR
FDCE
o0
clk
U50
GND
Odd causes LSB to be set and then cleared on next cycle
Joseph H. Allen
Title
Address Register
Size
A
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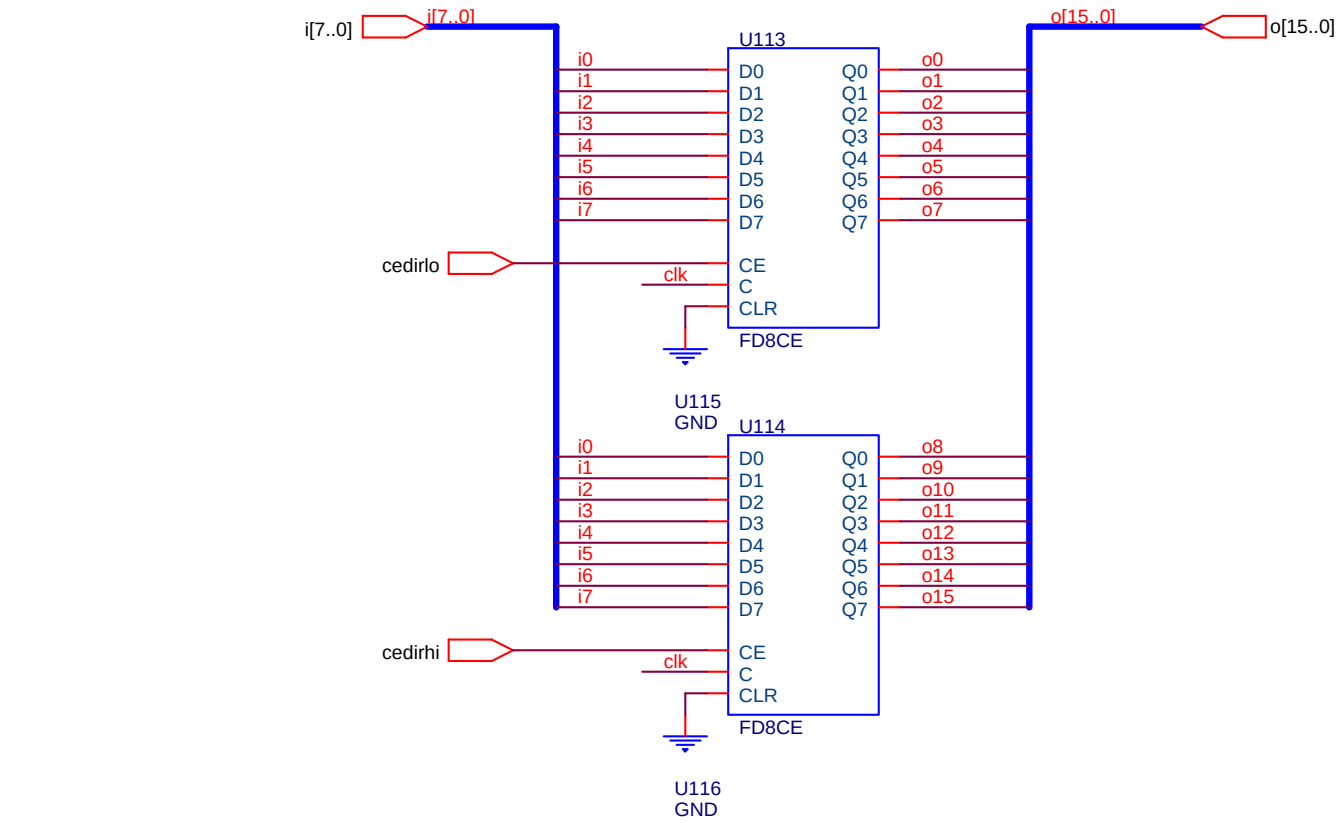

Joseph H. Allen		
Title: Data input register		
Size: A	Document Number	Rev: 1
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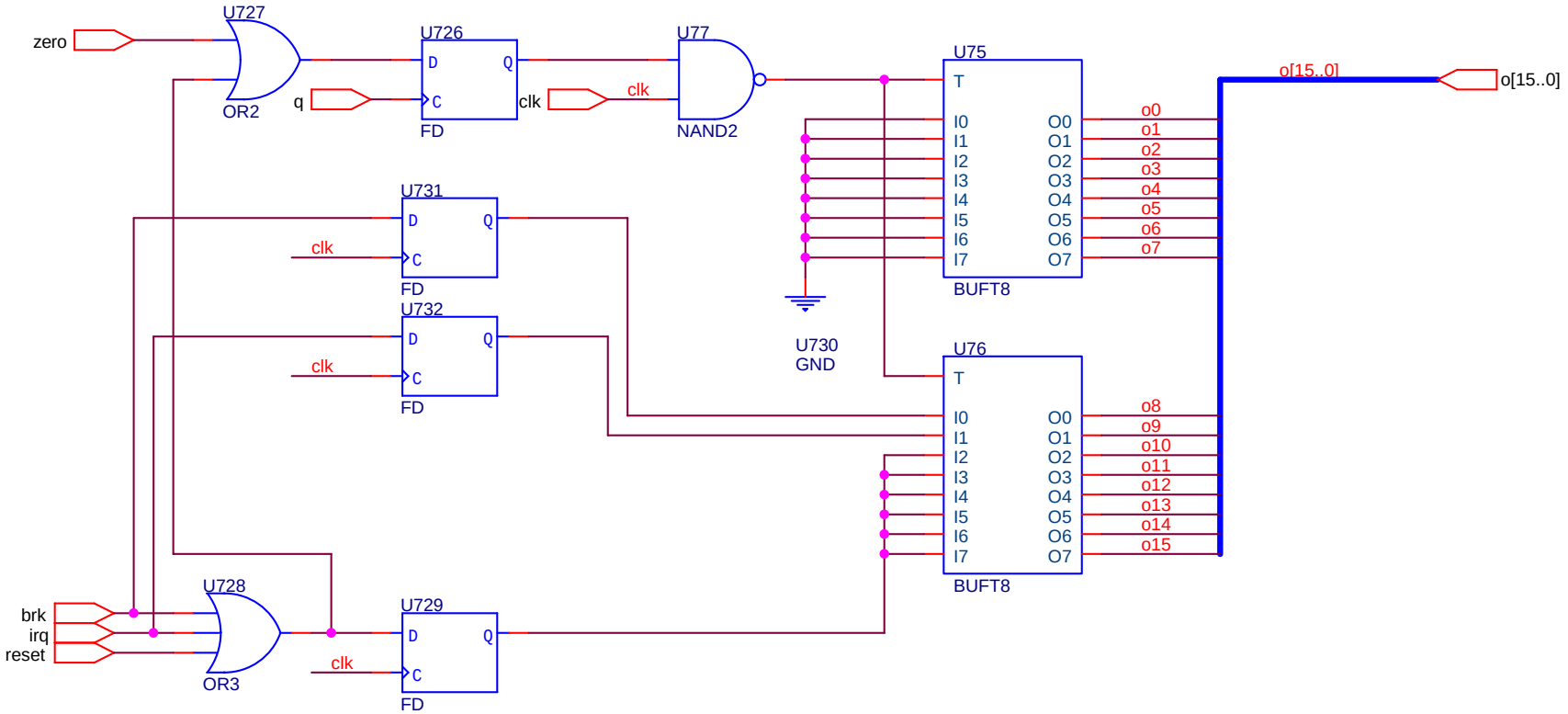

Joseph H. Allen		
Title: Constant generator		
Size: A	Document Number	Rev
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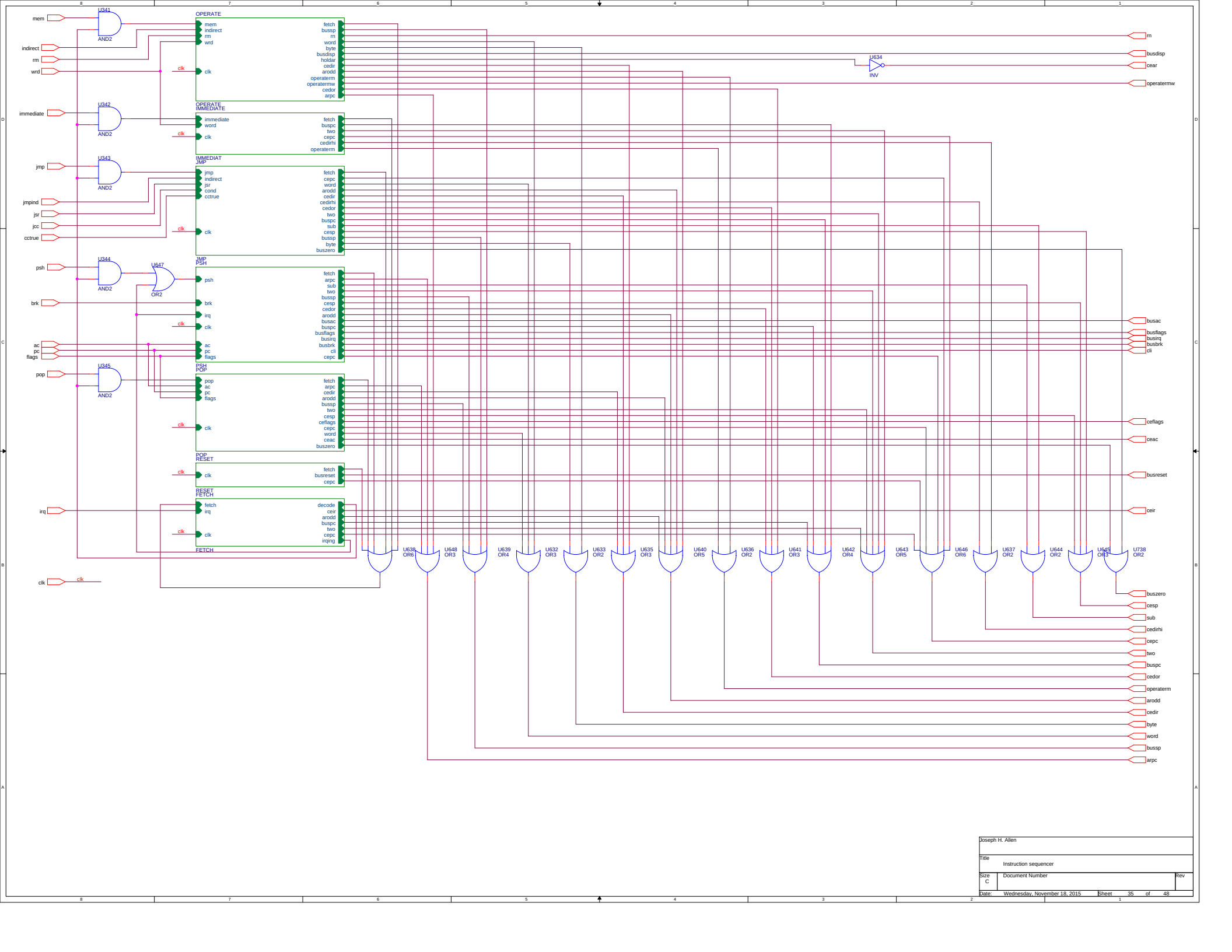

Joseph H. Allen		
Title: Instruction sequencer		
Size: C	Document Number	Rev
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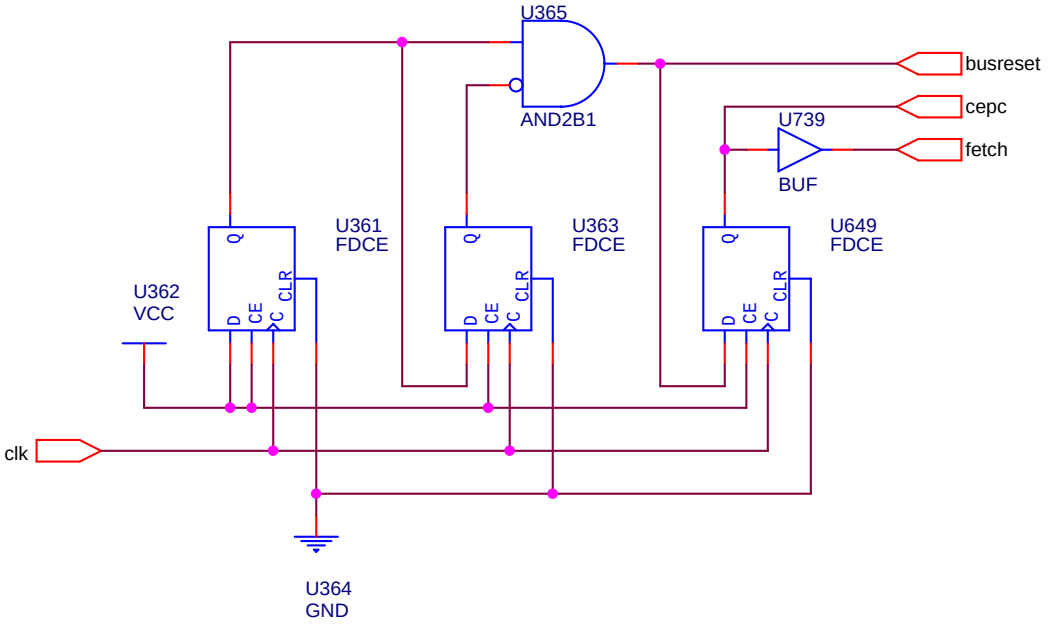
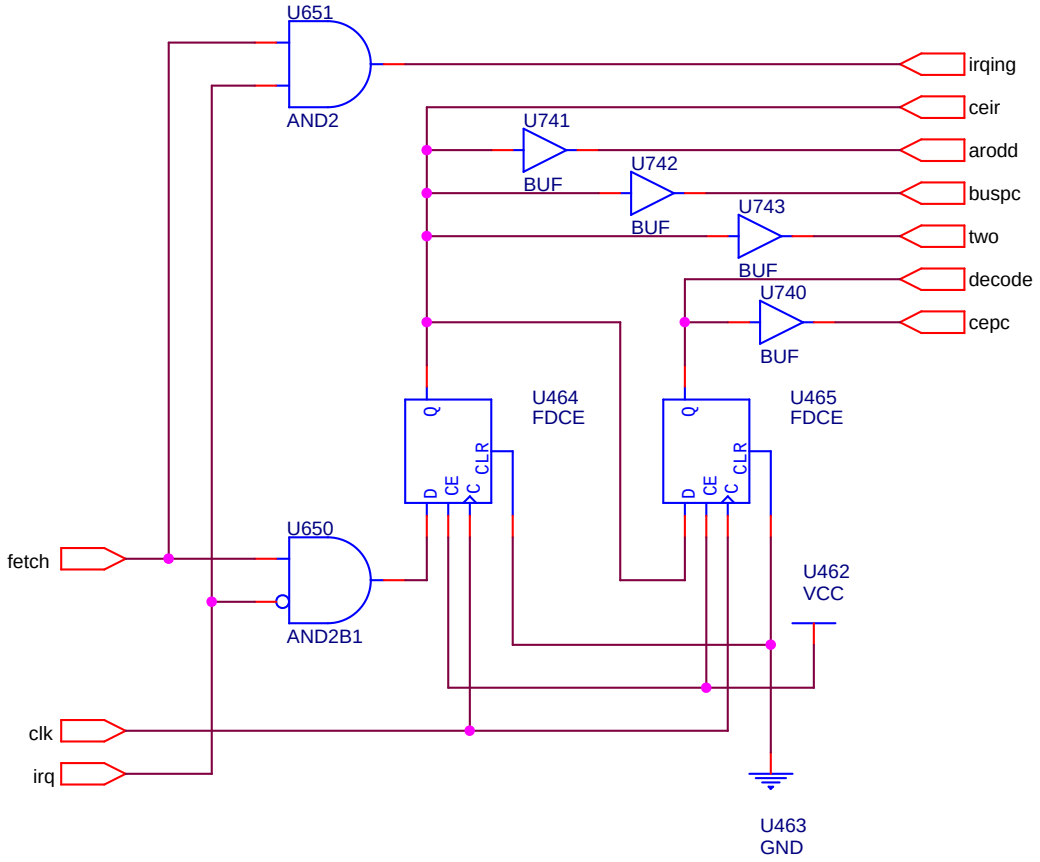


Joseph H. Allen		
Title: Reset sequence		
Size: A	Document Number	Rev
Date: Wednesday, November 18, 2015	Sheet 36 of 48	



Joseph H. Allen		
Title: Fetch sequence		
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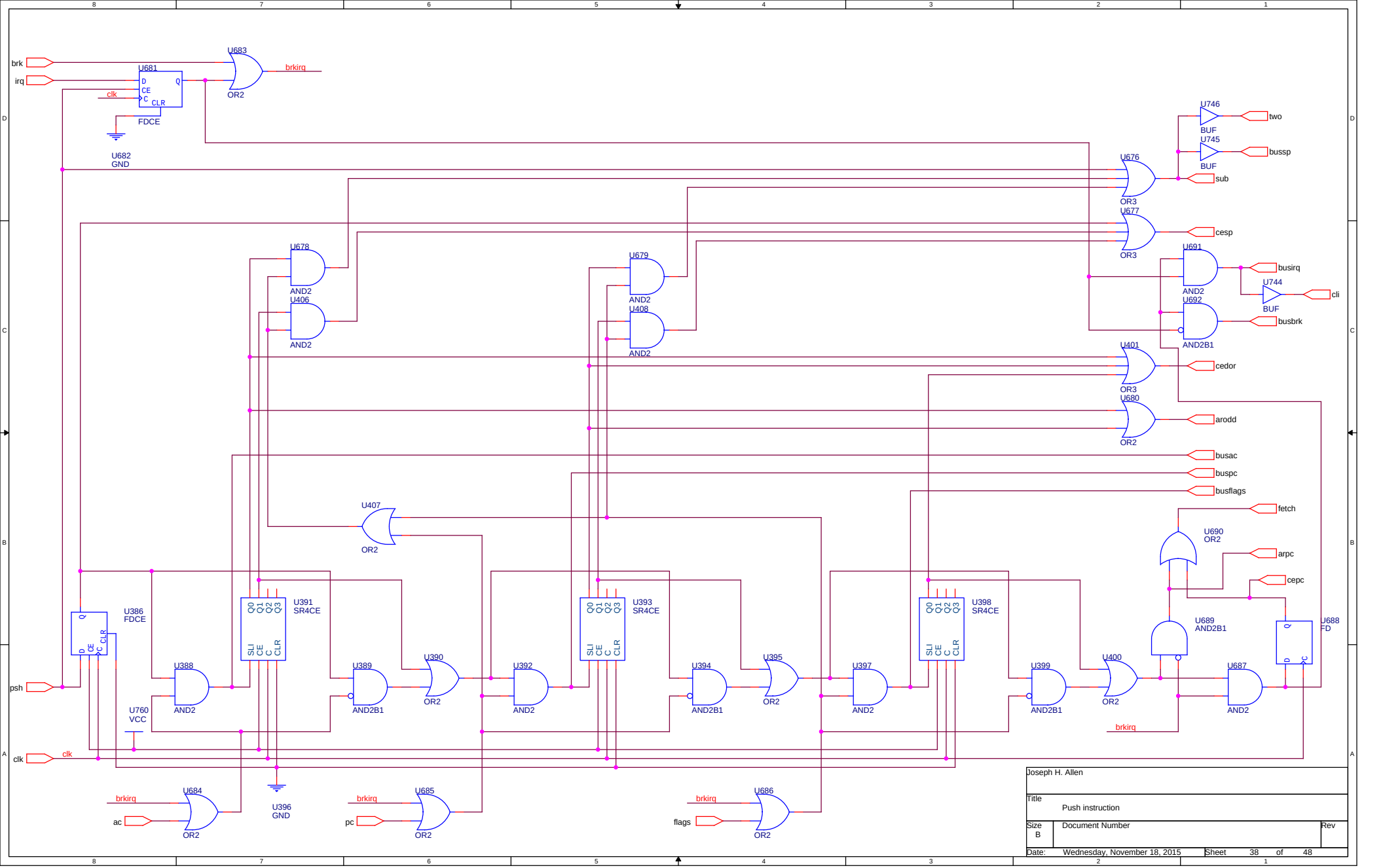
brk
irq
clk
U681
D
CE
C
CLR
Q
FDCE
U683
OR2
brkirq
U682
GND
U746
BUF
two
U745
BUF
bussp
sub
U676
OR3
U677
OR3
cesp
U678
AND2
U406
AND2
U679
AND2
U408
AND2
U691
AND2
busirq
U744
BUF
cli
U692
AND2B1
busbrk
U401
OR3
cedor
U680
OR2
arodd
busac
buspc
busflags
U407
OR2
fetch
U690
OR2
arpc
cepc
U386
FDCE
U391
SR4CE
U393
SR4CE
U398
SR4CE
U689
AND2B1
U688
FD
psh
U388
AND2
U389
AND2B1
U390
OR2
U392
AND2
U394
AND2B1
U395
OR2
U397
AND2
U399
AND2B1
U400
OR2
U687
AND2
U760
VCC
clk
brkirq
U684
OR2
ac
U396
GND
brkirq
U685
OR2
pc
brkirq
U686
OR2
flags
Joseph H. Allen
Title
Push instruction
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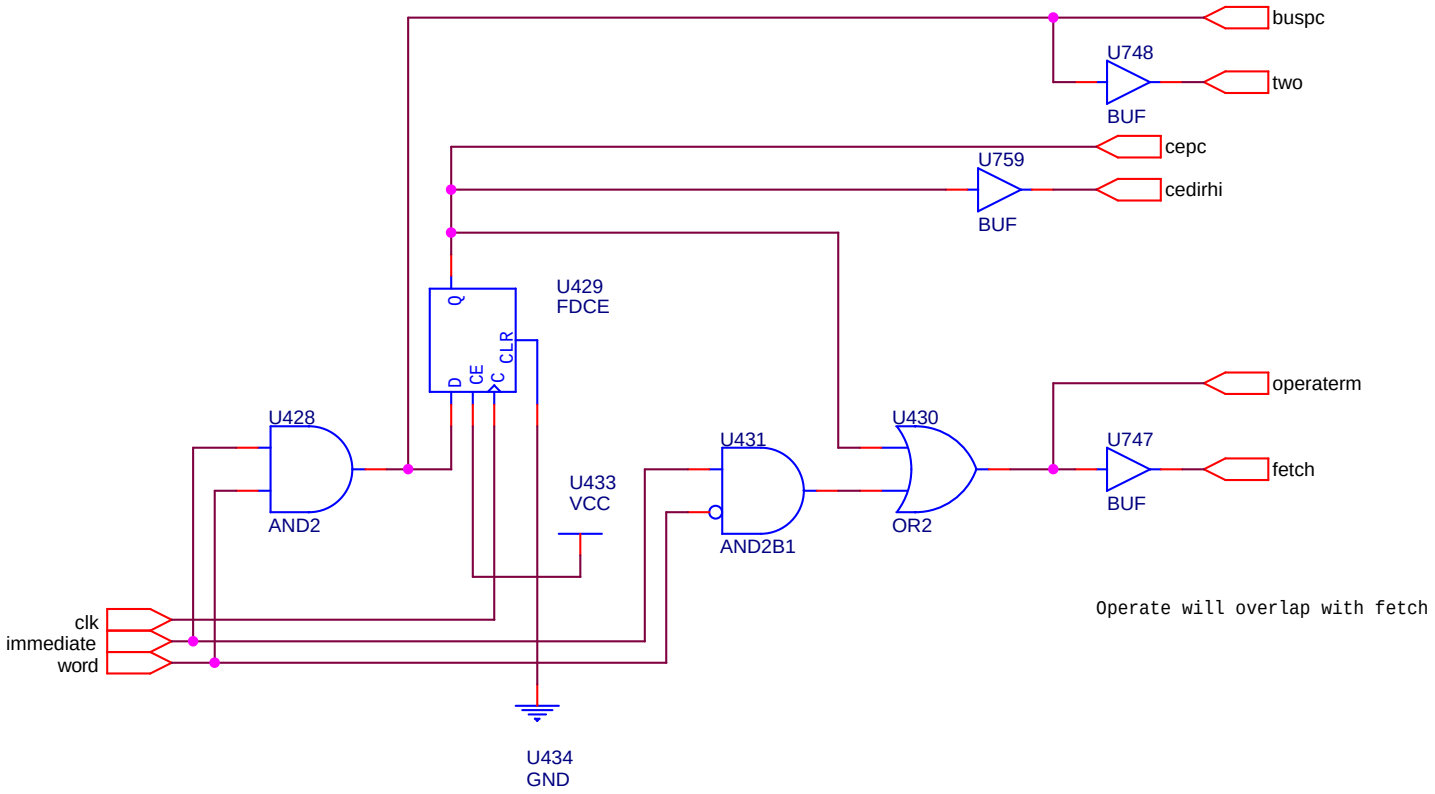

Joseph H. Allen		
Title: Immediate instructions		
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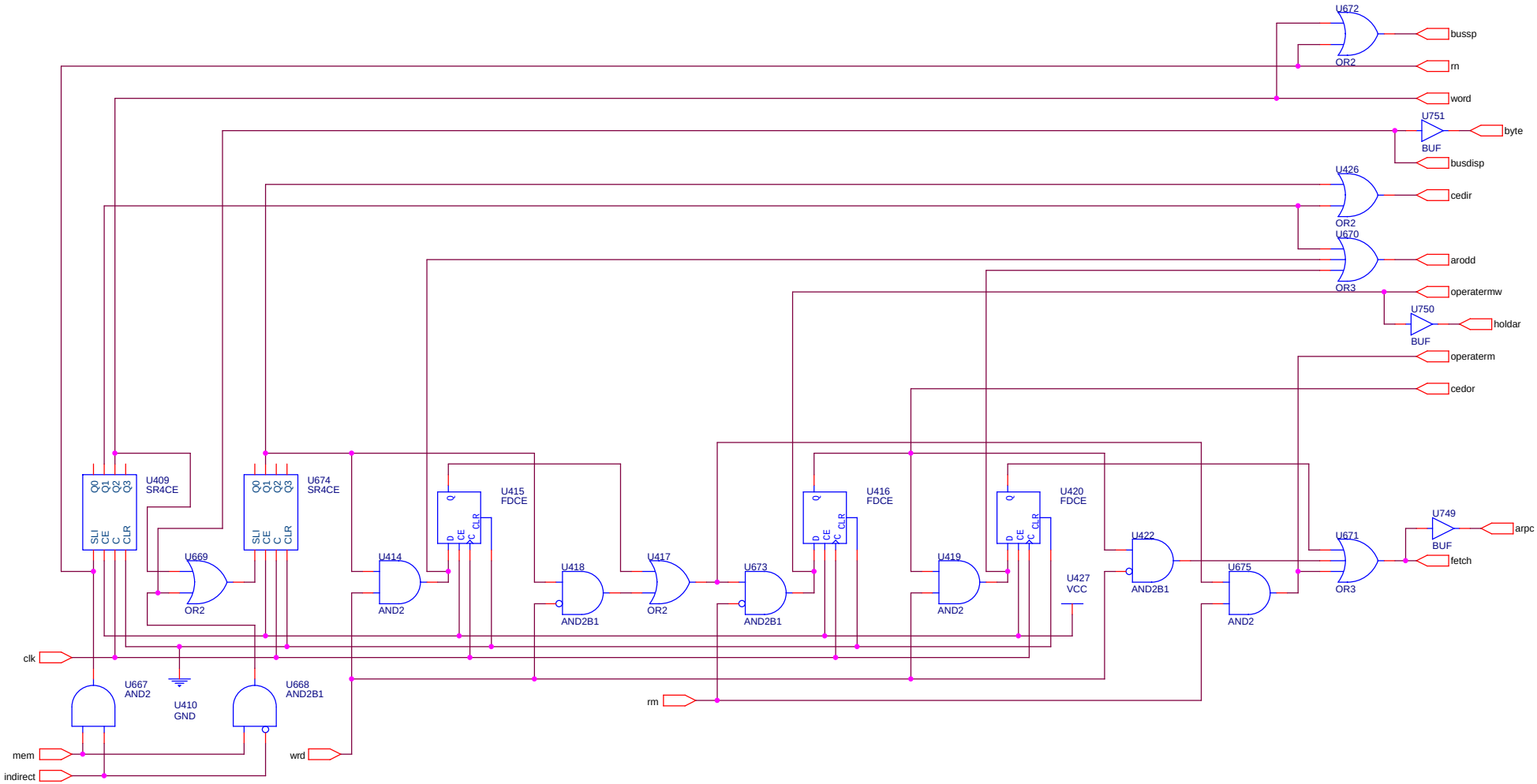

Joseph H. Allen		
Title: Operate insns		
Size: B	Document Number	Rev
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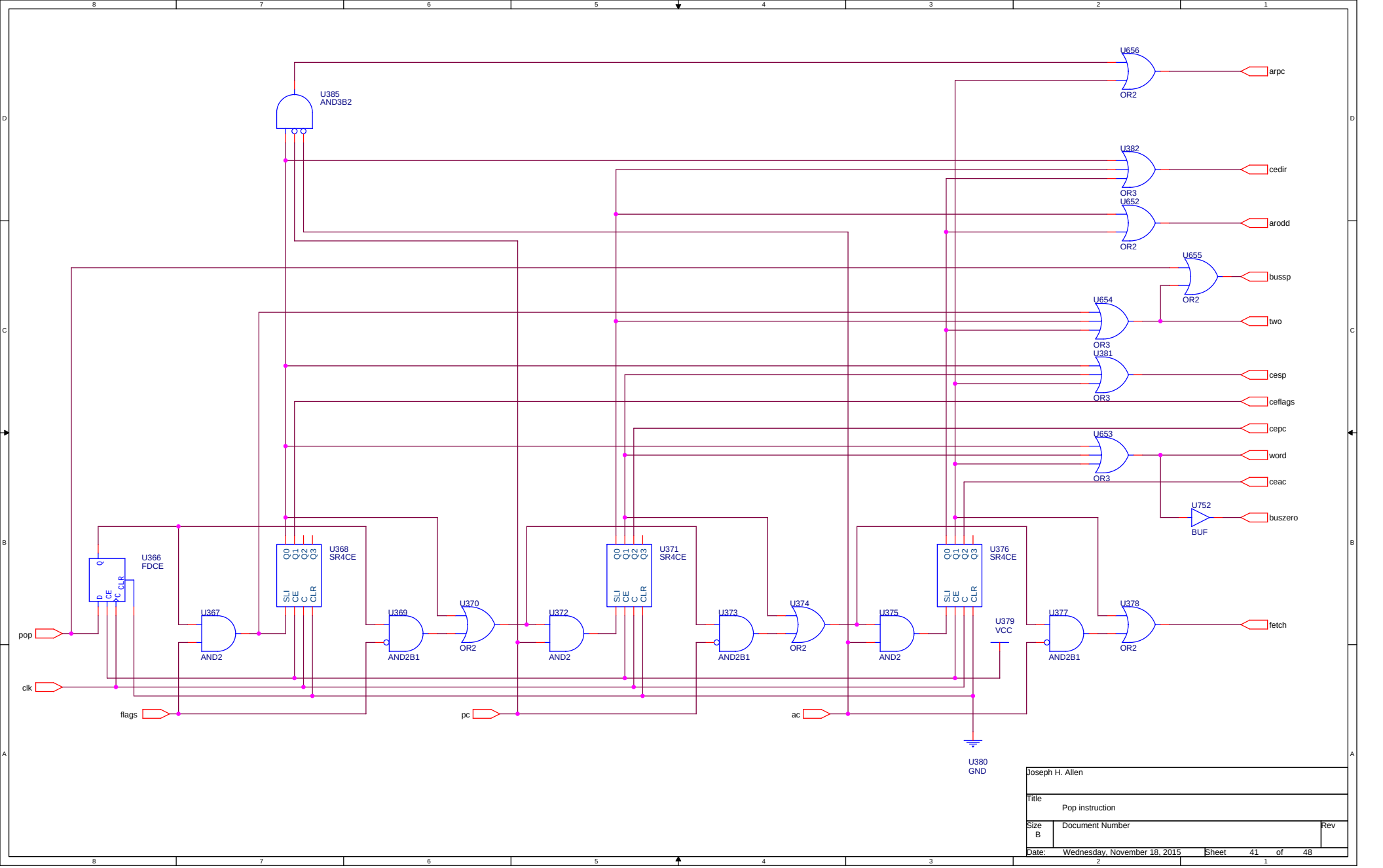

Joseph H. Allen		
Title: Pop instruction		
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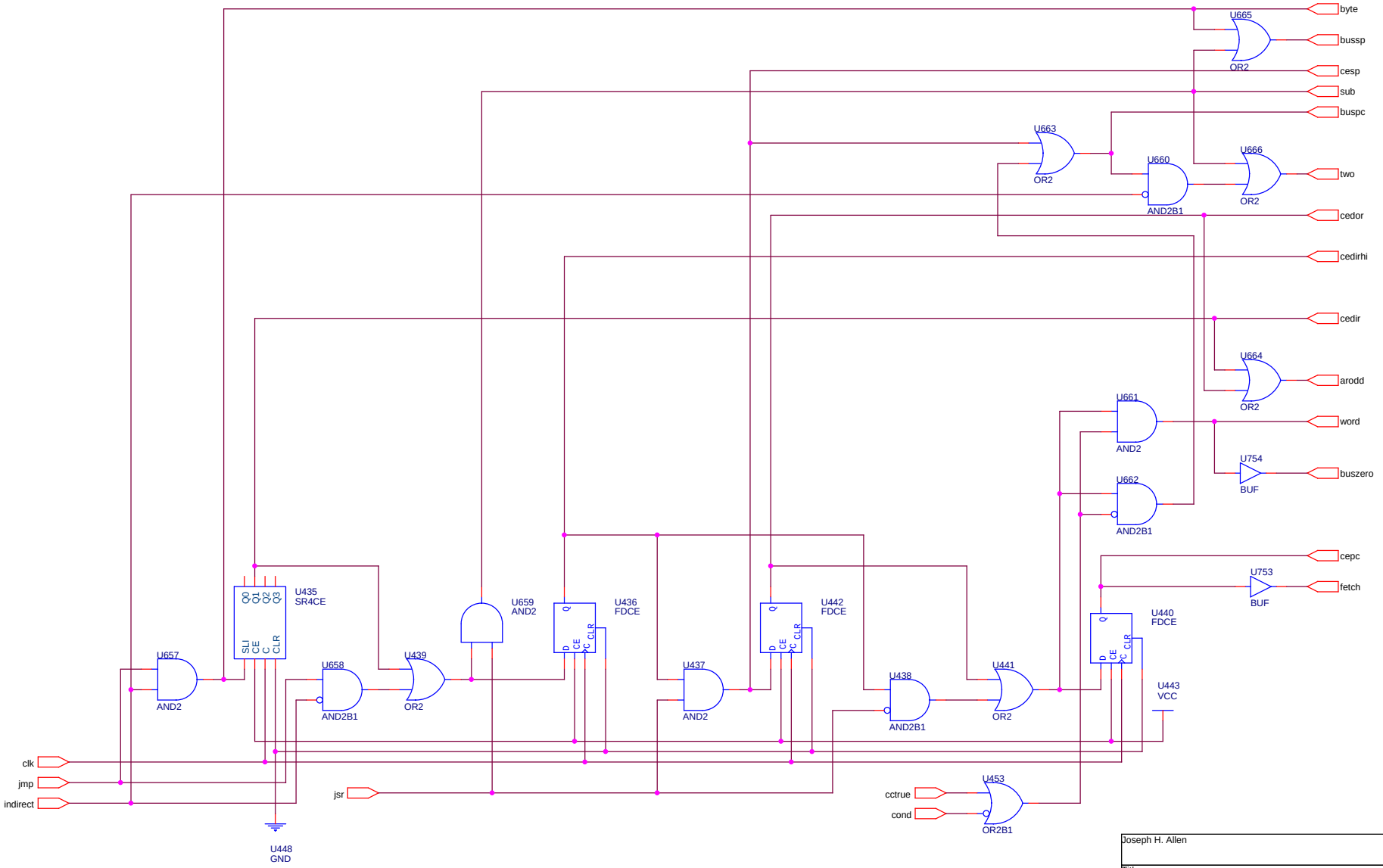

Joseph H. Allen		
Title: Jump instructions		
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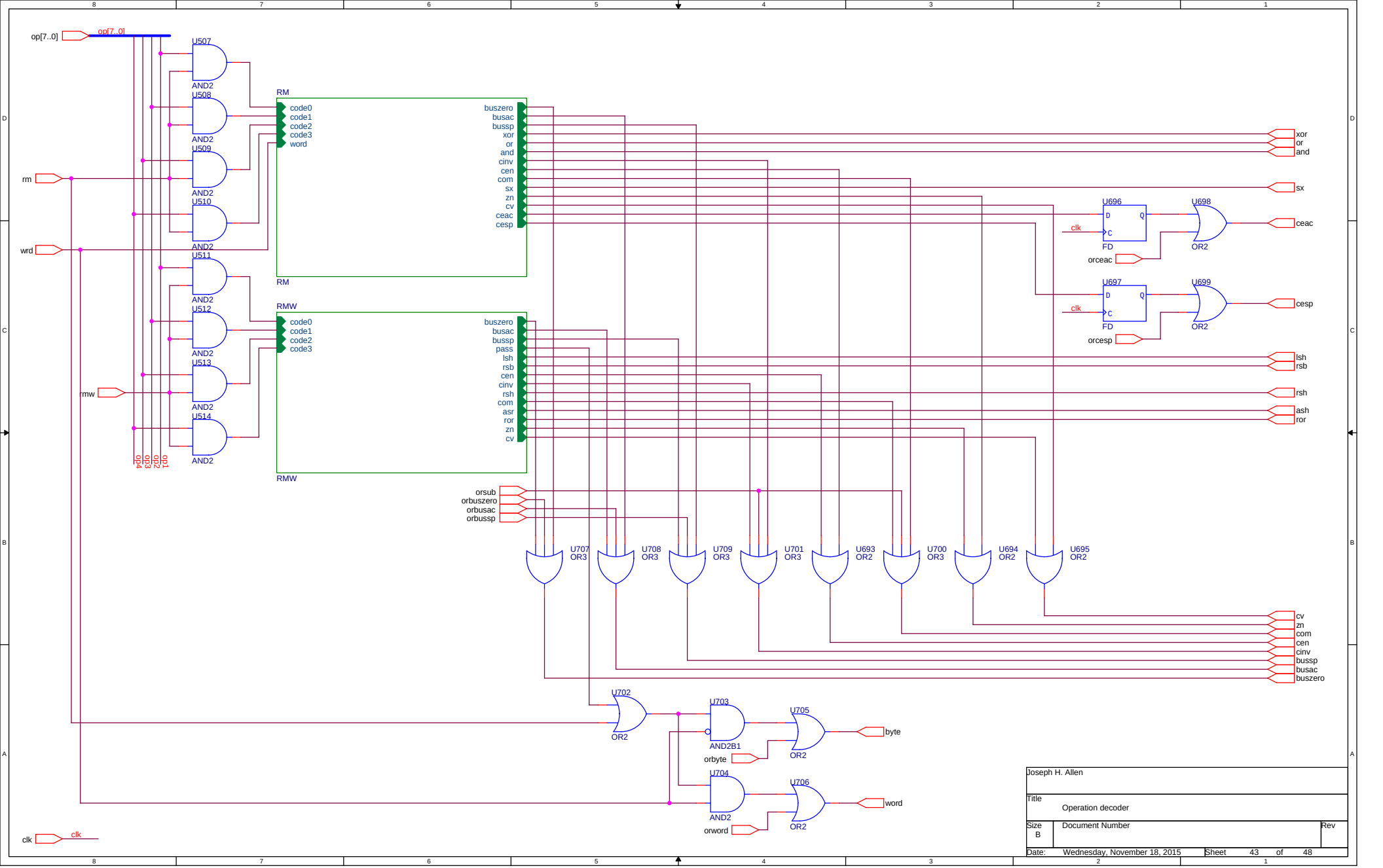

Joseph H. Allen		
Title: Operation decoder		
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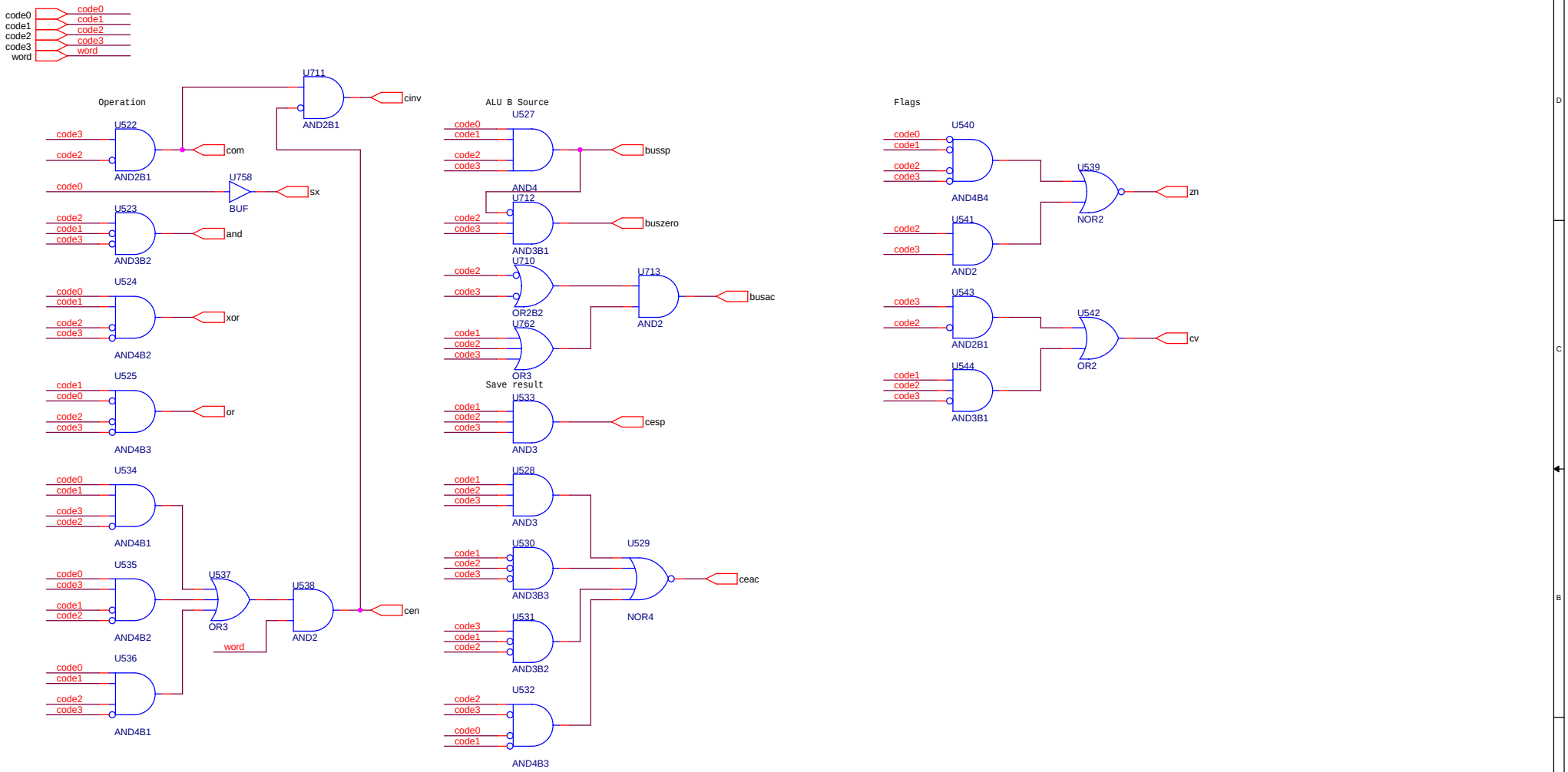

Joseph H. Allen		
Title: Register-Memory Operation Decoder		
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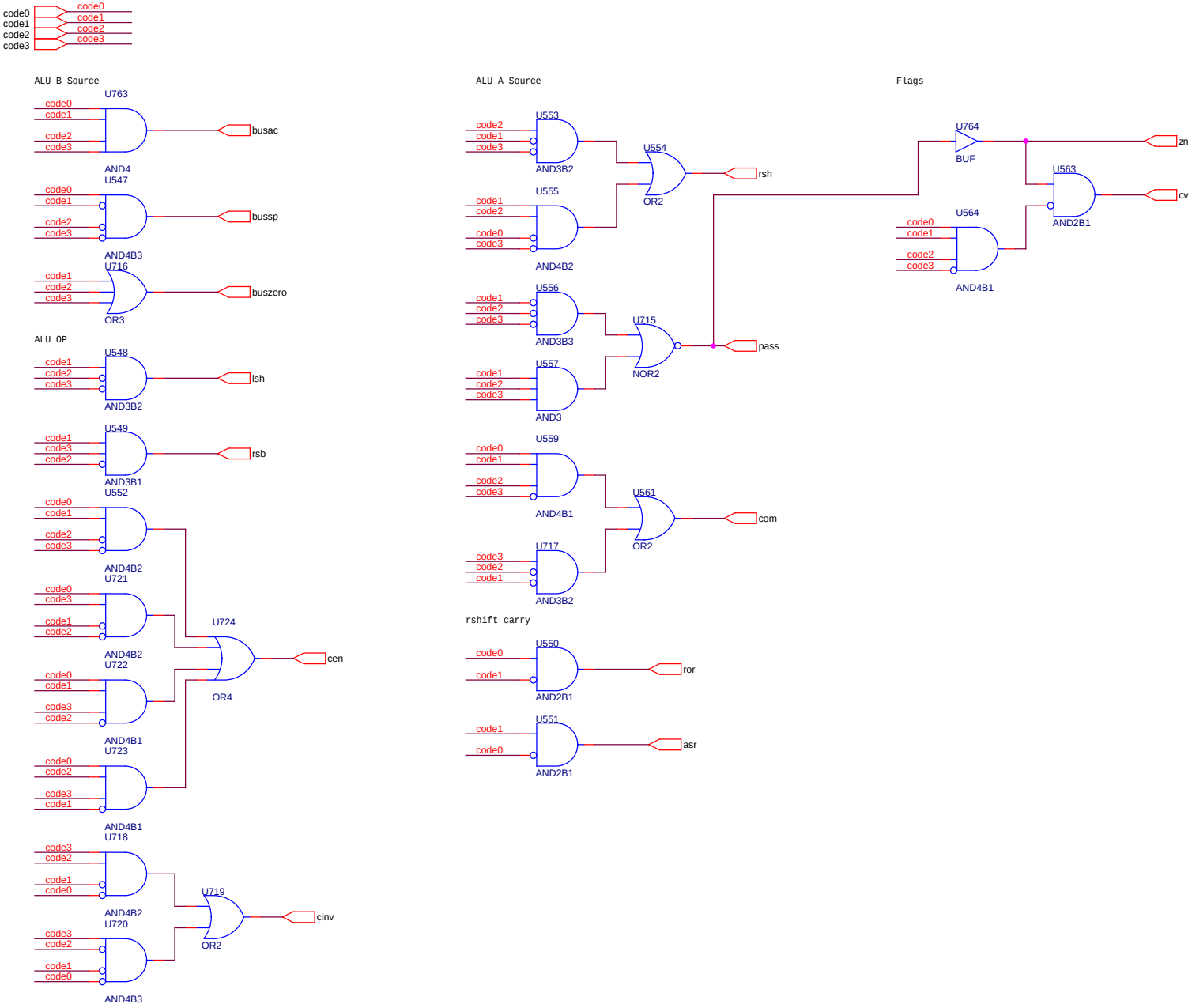

Joseph H. Allen		
Title: Read-Modify-Write Operation Decoder		
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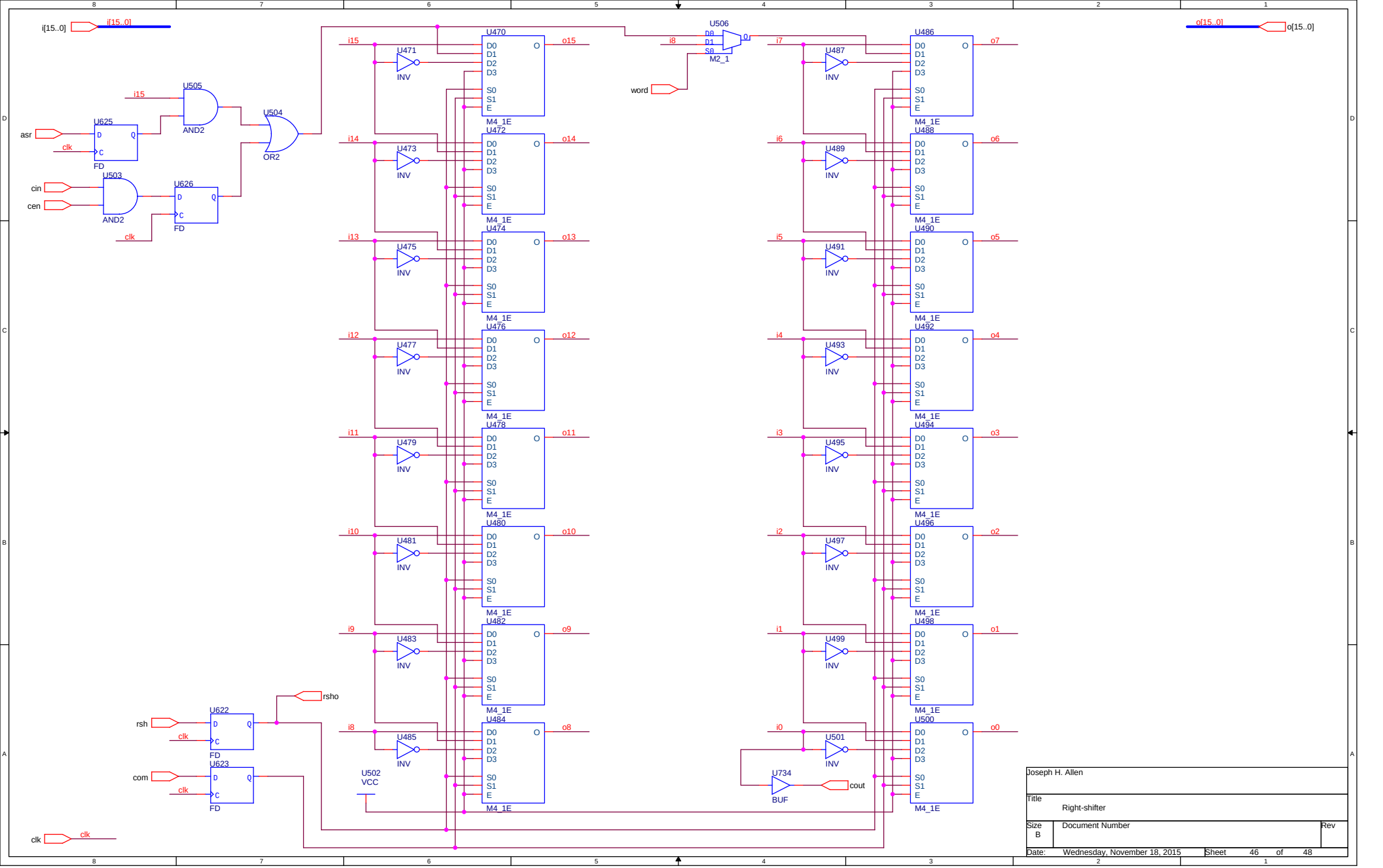
i[15..0]
o[15..0]
word
asr
clk
cin
cen
rsh
com
rsho
cout
U625
U626
U622
U623
U503
U504
U505
U506
U734
U501
U502
VCC
FD
AND2
OR2
M2_1
BUF
INV
M4_1E
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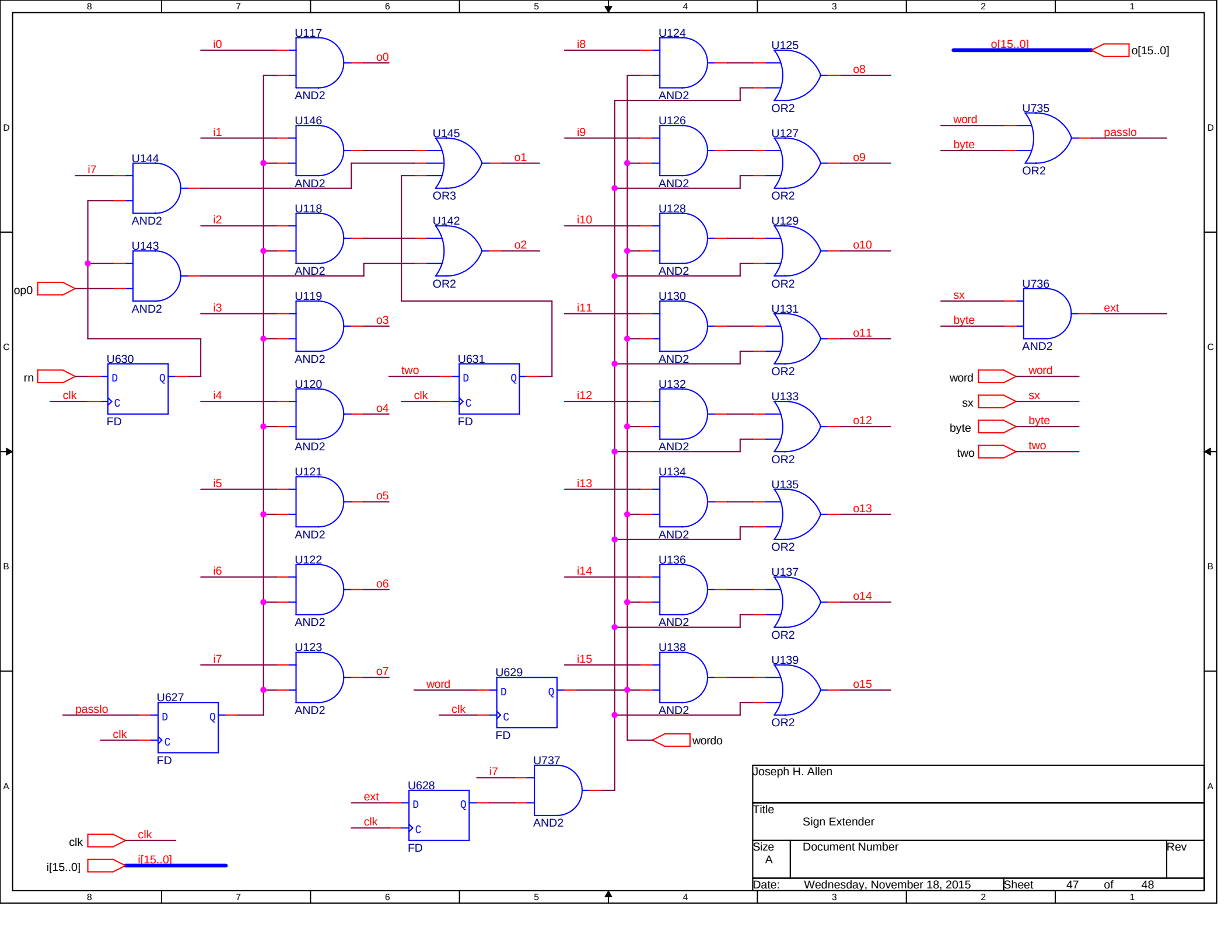
U117
AND2
i0
o0
U146
AND2
i1
U145
OR3
o1
U144
AND2
i7
U118
AND2
i2
U142
OR2
o2
U143
AND2
op0
U119
AND2
i3
o3
U630
FD
rn
clk
U631
FD
two
clk
U120
AND2
i4
o4
U121
AND2
i5
o5
U122
AND2
i6
o6
U123
AND2
i7
o7
U627
FD
passlo
clk
U629
FD
word
clk
U628
FD
ext
clk
U737
AND2
i7
clk
clk
i[15..0]
i[15..0]
U124
AND2
i8
U125
OR2
o8
U126
AND2
i9
U127
OR2
o9
U128
AND2
i10
U129
OR2
o10
U130
AND2
i11
U131
OR2
o11
U132
AND2
i12
U133
OR2
o12
U134
AND2
i13
U135
OR2
o13
U136
AND2
i14
U137
OR2
o14
U138
AND2
i15
U139
OR2
o15
wordo
o[15..0]
o[15..0]
U735
OR2
word
byte
passlo
U736
AND2
sx
byte
ext
word
word
sx
sx
byte
byte
two
two
Joseph H. Allen
Title
Sign Extender
Size
A
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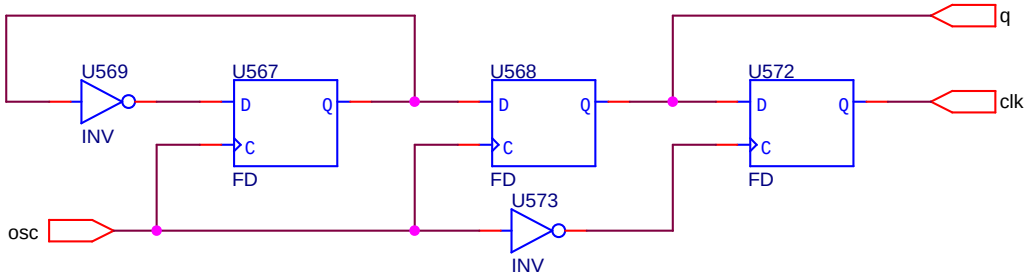

Q leads CLK by 90 degrees.

The first flip-flop is to ensure that the clock starts cleanly; remember that the fpga comes out of reset asynchronously with respect to osc.

This should be elaborated in the future: we need a ready line to stretch the clock when accessing slow devices.

Joseph H. Allen		
Title: Two-phase clock generator		
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