Part A

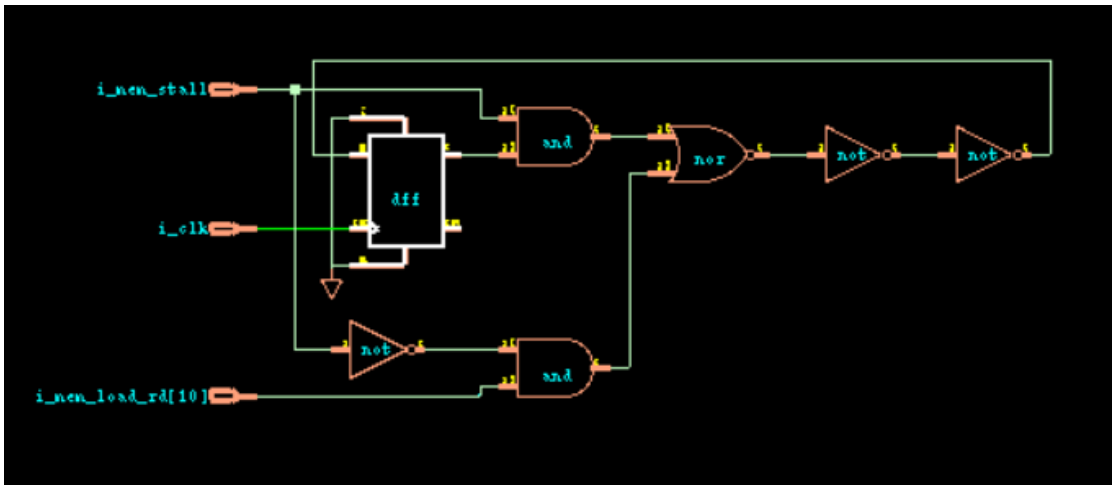
1.A brief report describing the netlist bugs and your resolution.

There are three netlist bugs:

The first one is

```
INVX1 U93 ( .A(n91), .Y(n880) );
INVX1 U930 (.A(n880), .Y(n88) );
```

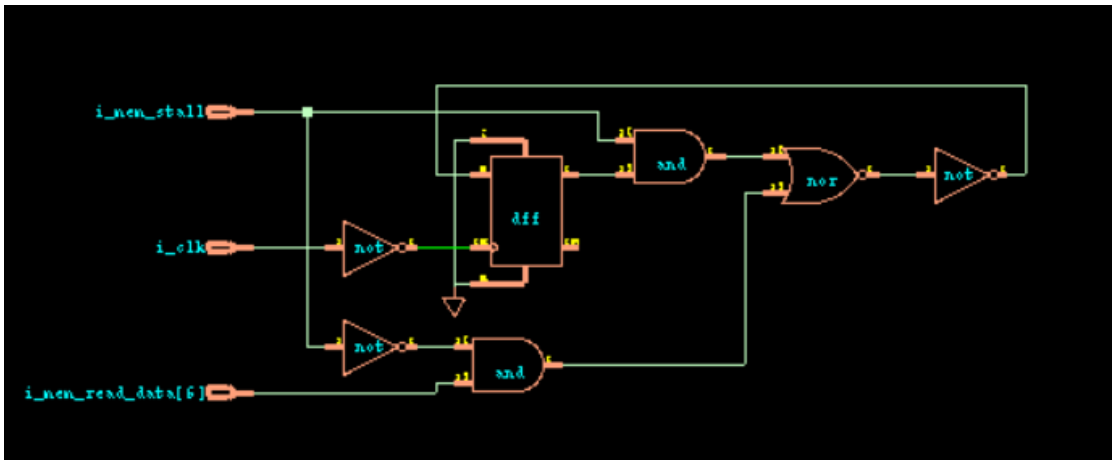
causing a duplicated inverter.



Solution: I delete the INVX1 U930 and reconnect the wire as INVX1 U93(.A(n91),.Y(n880)),

The second one is

```
DFFPOSX1 \mem_read_data_r_reg[7]   ( .D(n53), .CLK(i_clk), .Q(
      o_wb_read_data[7]) );
DFFNEGX1 \mem_read_data_r_reg[6]   ( .D(n52), .CLK(i_clk), .Q(
      o_wb_read_data[6]) );
```



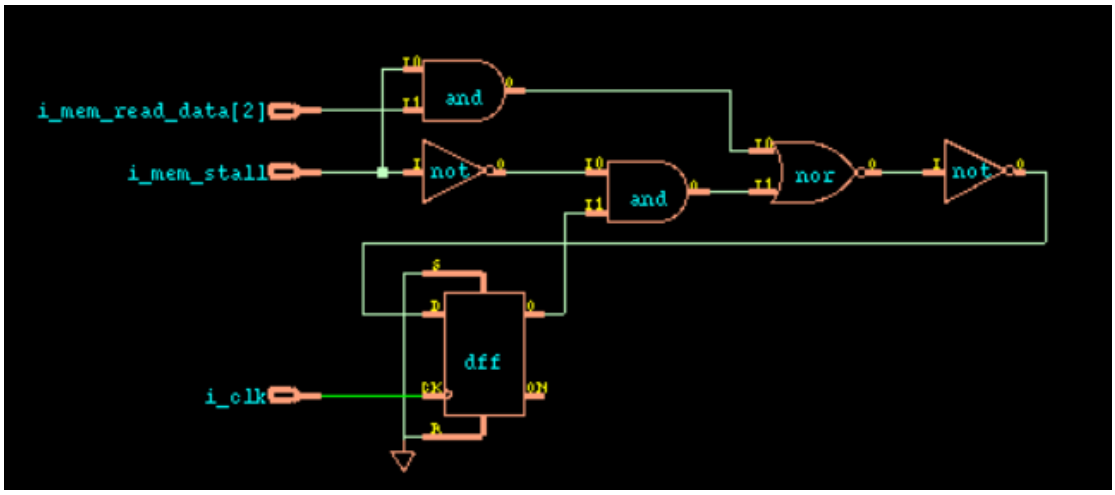
It should use a positive DFF as reg[7].

Solution: I correct the negative to positive as DFFPOSX1…

The third one is

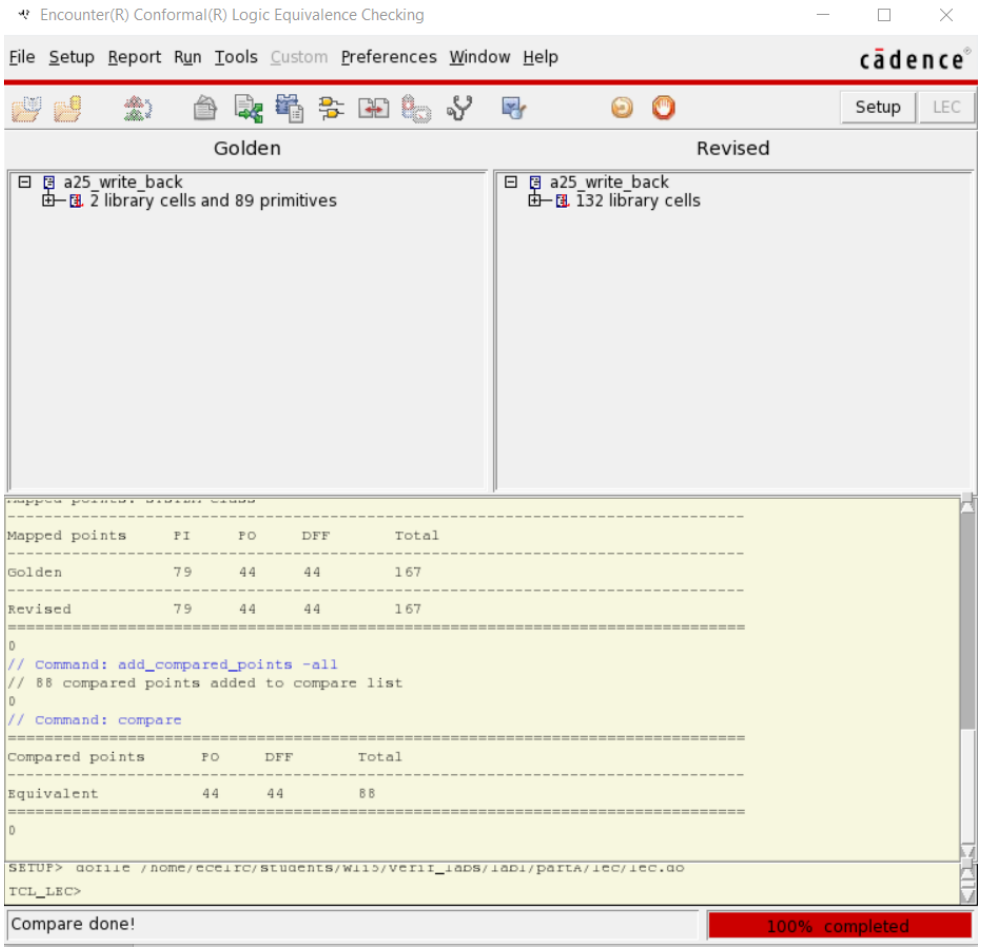
```
MUX2X1 U174 ( .B(o_wb_read_data[2]), .A(i_mem_read_data[2]), .S(i_mem_stall),
      .Y(n131) );
INVX1 U175 ( .A(n132), .Y(n47) );
```

The MUX2x1 U174 is wrong. The input wire is reversed.

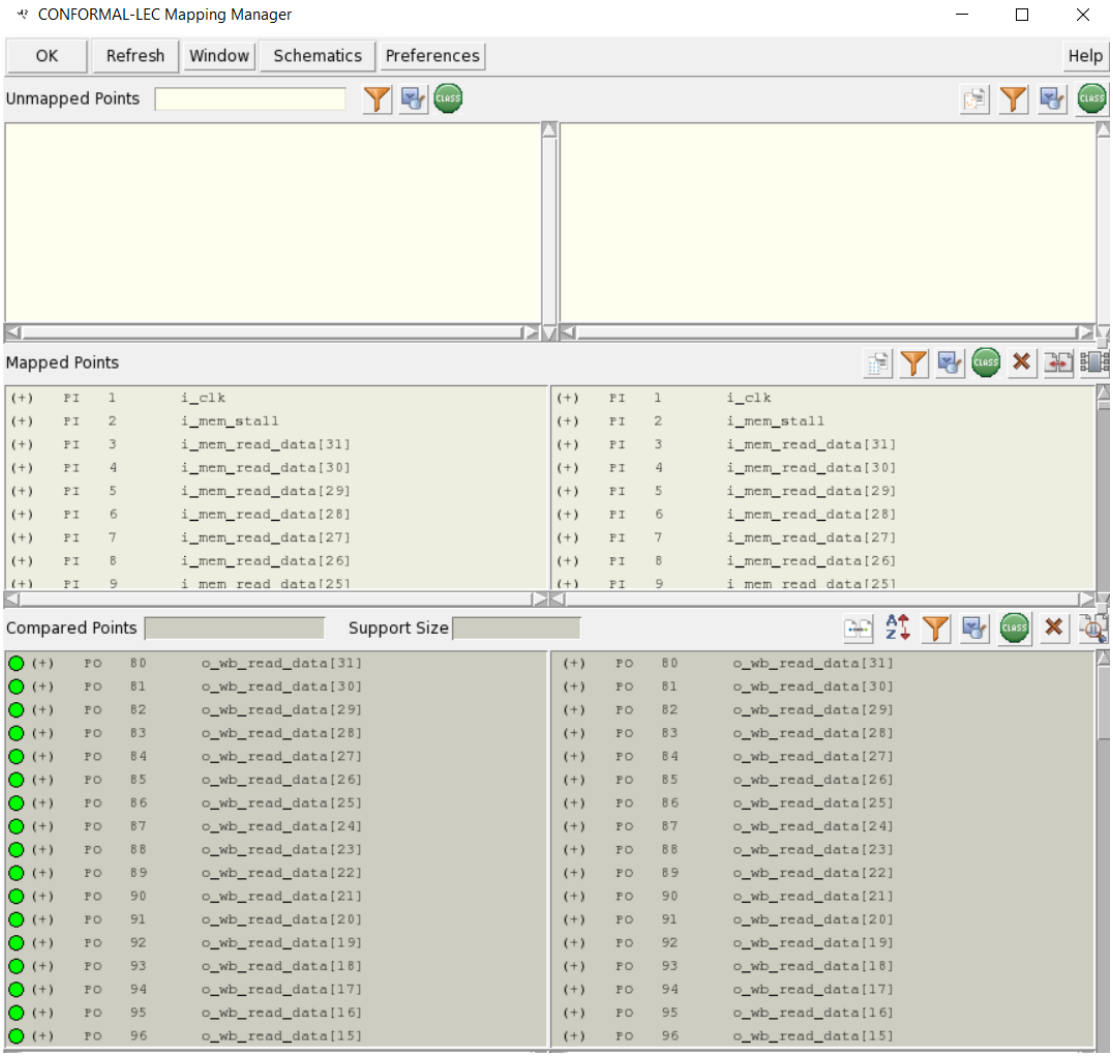


Solution: I change the order of .B and .A as MUX2X1 U174 (.B(i_mem_read_data[2]), .A(o_wb_read_data[2]), .S(i_mem_stall), .Y(n131));

2.Lec Console:



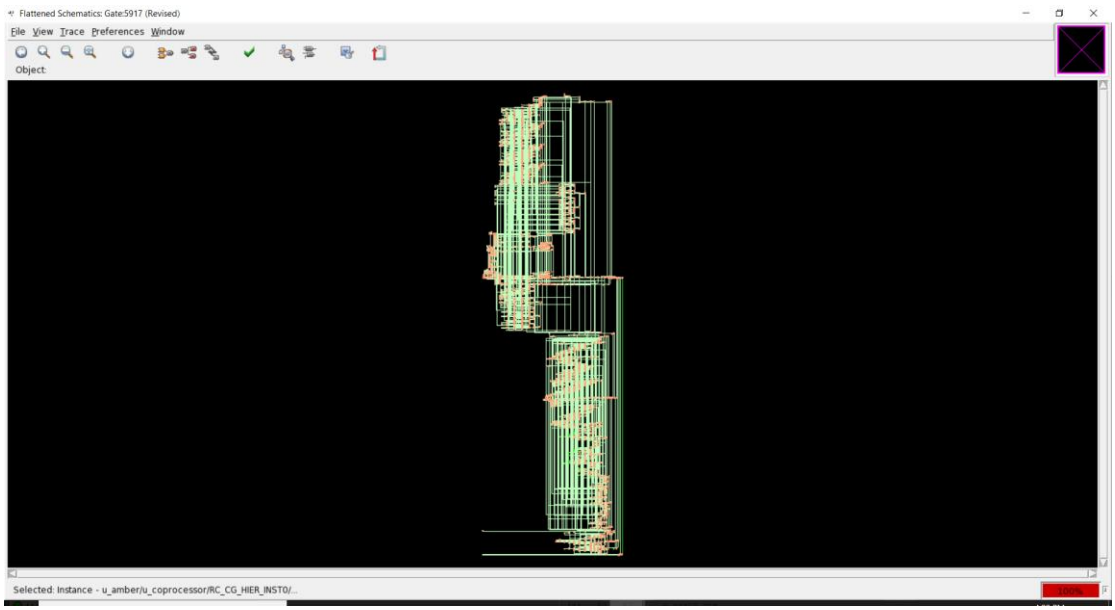
Mapping manager:

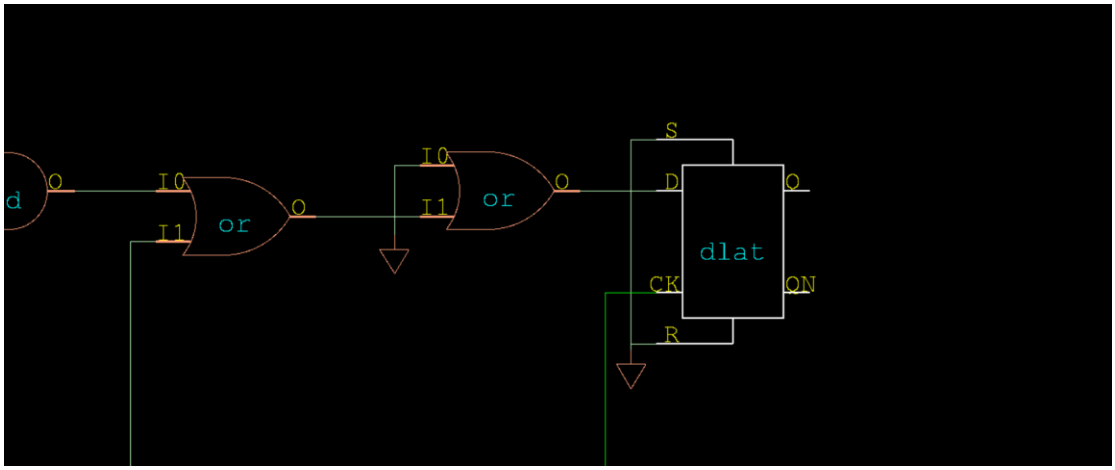


PartB:

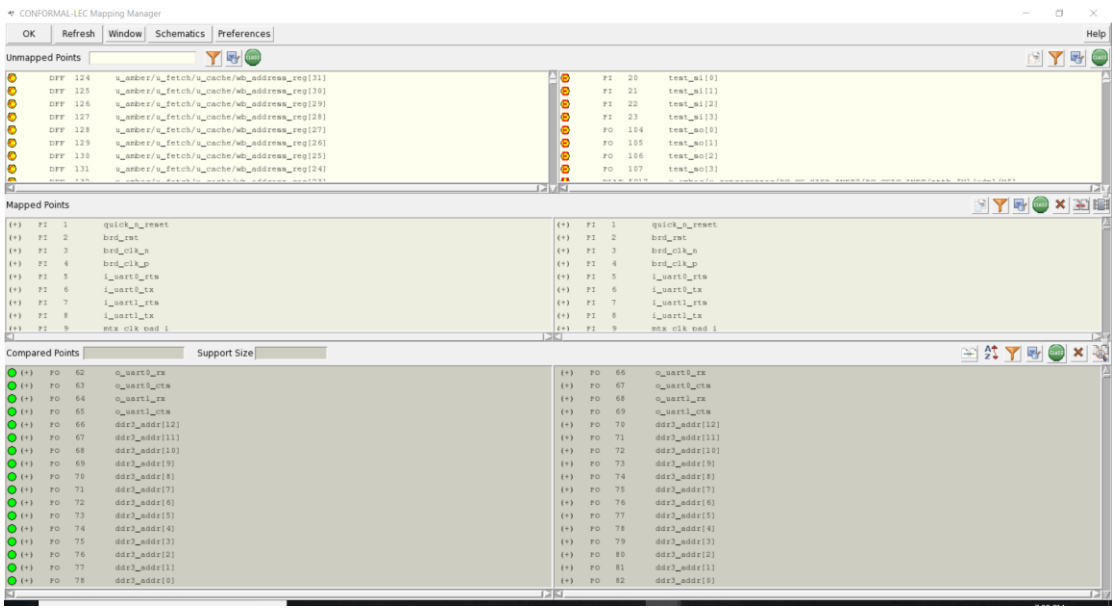
1.The scan style is muxed_scan which includes scan insertion and clock gating. Since they are not present in the RTL, so I have to add constraints to disable the clock gate and the added scan logic. And in the test signal objects, since they are all in high active, I set the constraint to 0 to disable the scan.

2.

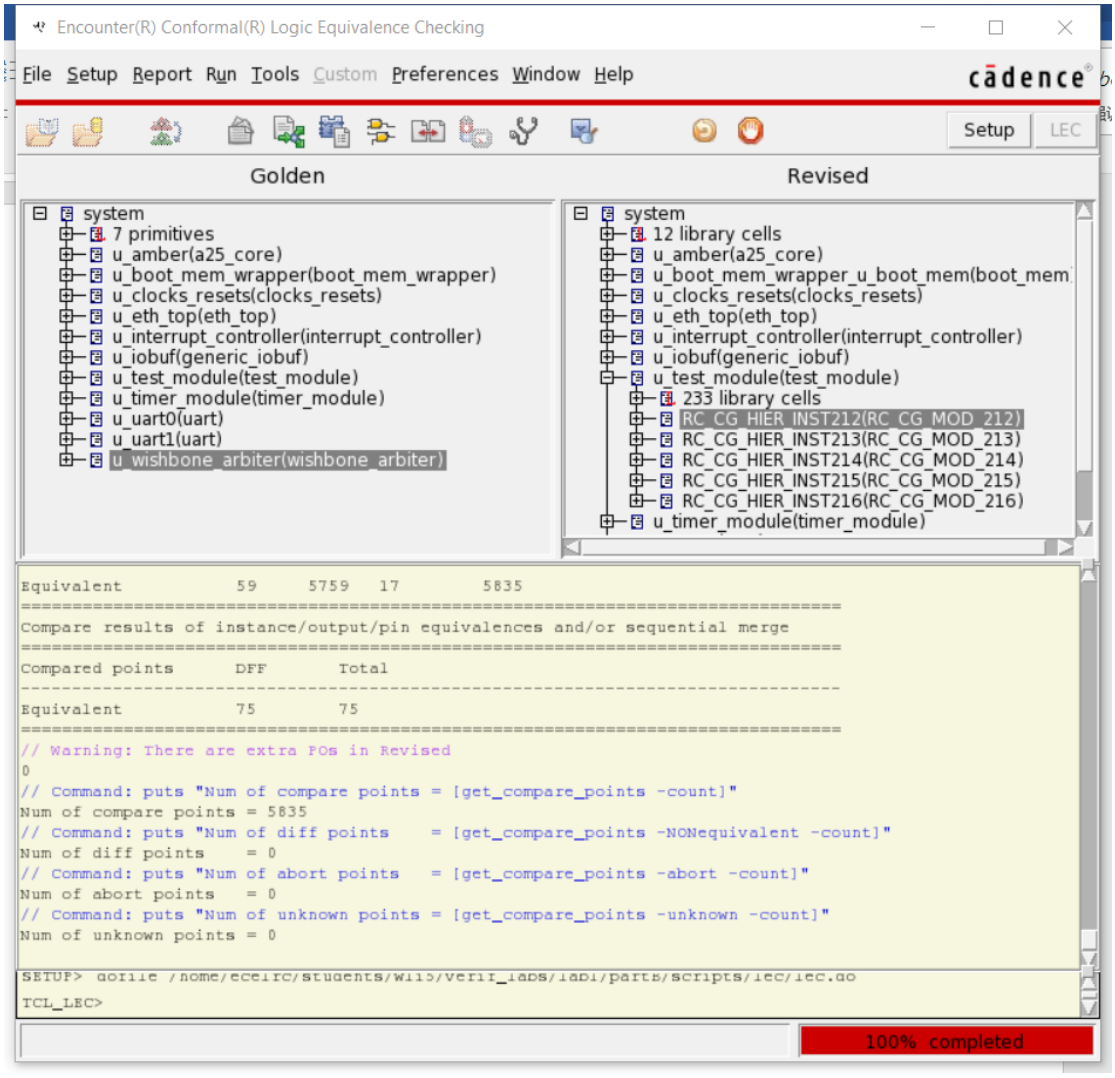




3. set_flatten_model -seq_constant -seq_constant_x_to 0
Remodel registers that also have feedback to constants.
Optimize the flip-flop to a constant zero when the flop is always in a don’t care (x) state.
set_flatten_model -gated_clock
Remodels the gated-clock logic of the clock port of a DFF.
set_analyze_option -auto
Determine the best place to run the ANALYZE SETUP command. Enable the automatic analysis.
4.mapping manager


CONFORMAL-LEC Mapping Manager
OK
Refresh
Window
Schematics
Preferences
Help
Unmapped Points
Mapped Points
Compared Points
Support Size

Lec console


Encounter(R) Conformal(R) Logic Equivalence Checking
File Setup Report Run Tools Custom Preferences Window Help
cadence
Setup
LEC
Golden
Revised
system
7 primitives
u_amber(a25_core)
u_boot_mem_wrapper(boot_mem_wrapper)
u_clocks_resets(clocks_resets)
u_eth_top(eth_top)
u_interrupt_controller(interrupt_controller)
u_iobuf(generic_iobuf)
u_test_module(test_module)
u_timer_module(timer_module)
u_uart0(uart)
u_uart1(uart)
u_wishbone_arbiter(wishbone_arbiter)
system
12 library cells
u_amber(a25_core)
u_boot_mem_wrapper_u_boot_mem(boot_mem
u_clocks_resets(clocks_resets)
u_eth_top(eth_top)
u_interrupt_controller(interrupt_controller)
u_iobuf(generic_iobuf)
u_test_module(test_module)
233 library cells
RC_CG_HIER_INST212(RC_CG_MOD_212)
RC_CG_HIER_INST213(RC_CG_MOD_213)
RC_CG_HIER_INST214(RC_CG_MOD_214)
RC_CG_HIER_INST215(RC_CG_MOD_215)
RC_CG_HIER_INST216(RC_CG_MOD_216)
u_timer_module(timer_module)
Equivalent 59 5759 17 5835
Compare results of instance/output/pin equivalences and/or sequential merge
Compared points DFF Total
Equivalent 75 75
// Warning: There are extra POs in Revised
0
// Command: puts "Num of compare points = [get_compare_points -count]"
Num of compare points = 5835
// Command: puts "Num of diff points = [get_compare_points -NONequivalent -count]"
Num of diff points = 0
// Command: puts "Num of abort points = [get_compare_points -abort -count]"
Num of abort points = 0
// Command: puts "Num of unknown points = [get_compare_points -unknown -count]"
Num of unknown points = 0
SETUP> dofile /home/eceirc/students/wil5/verif_labs/lab1/parts/scripts/lec/lec.do
TCL_LEC>
100% completed