Conformal LEC Tutorial

1 Introduction

This tutorial demonstrates the use of Conformal LEC from Cadence for checking the logical equivalence of an RTL design to its gate level netlist. All necessary files are in the zipped file 'lab1.tar.gz'. This tutorial is related to the part A of the lab.

2 Starting Conformal LEC

To start Conformal LEC tool in GUI mode, use the commands below on one of the ECE LRC 64-bit machines, luigi, wario, koopa or kamek. Please note that the tool is not available in any of the 32-bit machines.

```
module load cadence/2016

mkdir ~/verif_labs
cd ~/verif_labs
cp -rf ~sshaikh1/verif_labs/lab1.tar.gz .

tar -xvzf lab1.tar.gz
cd lab1/partA/lec/
lec -xl
```

The GUI should now be available to the user as shown in the snapshot below. LEC's window is split into two for loading the Golden and Revised models which will be discussed separately in the next section. In addition to that, there is a command line prompt available to the user as an alternative to the GUI menu options.

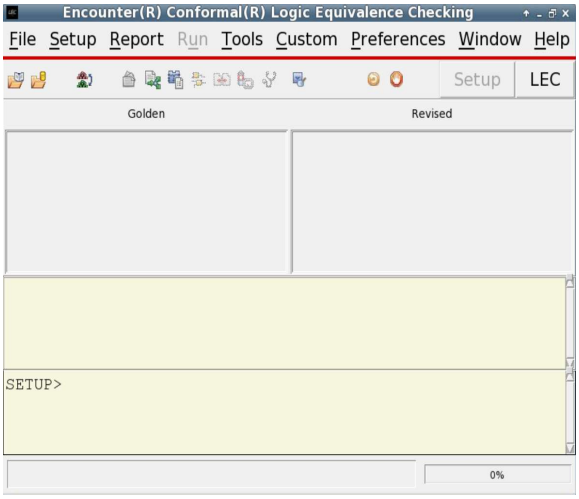

Figure 1: Conformal LEC GUI

Also, look at the mode change buttons on the top right corner just below the cadence logo. Setup mode is used to set up the environment and the LEC mode is used for the mapping between the two models. To switch between the two modes, these buttons can be used.

3 Setting up the environment

Before loading the RTL (aka the golden model) and gate netlist (aka the revised model), the library used for synthesis should be loaded using the Read Library button. For this tutorial gscl45nm.lib will be used because it was the library used during synthesis. Note that the library format should be Liberty. Once this is done, a message is displayed in the output pane that the library was read successfully.

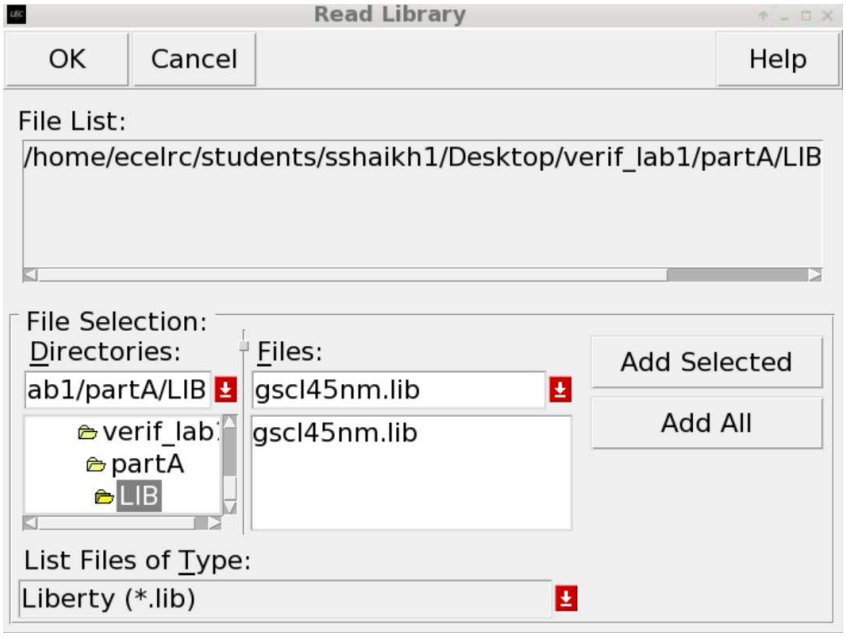

Figure 2: Load the library

Then use the Read Design button to load the golden and revised designs. First load the RTL as the golden model and then load the netlist as the revised model. A message is displayed in the output pane after reading each model successfully. Once these two designs are loaded, the environment is set up and we can proceed to LEC mode.

Snapshots in Figures 3, 4 and 5 can be used as references while in setup mode for loading the two designs.

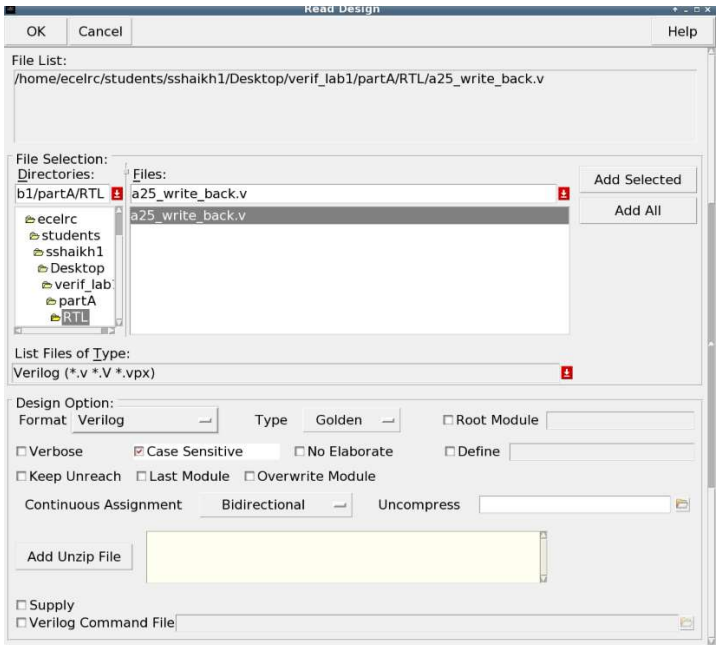

Figure 3: Load the golden model

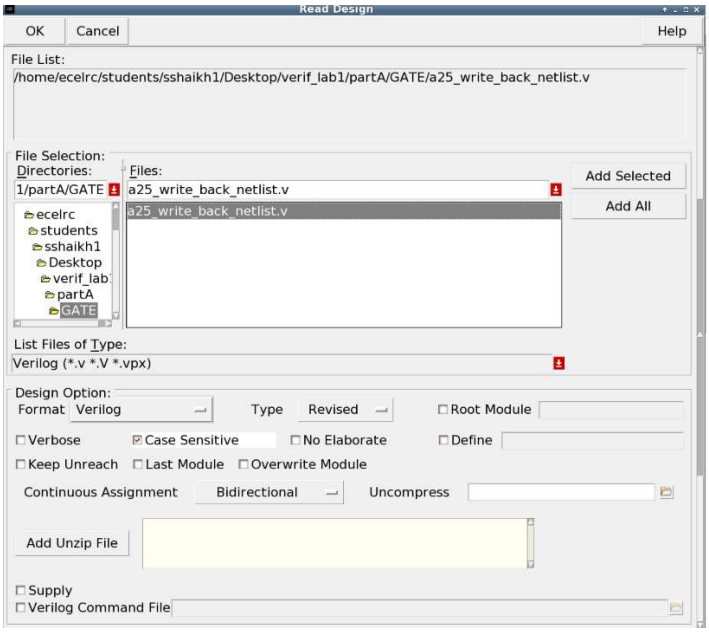

Figure 4: Load the revised model

```
SETUP> read design /home/ecelrc/students/sshaikh1/Desktop/verif_lab1/partA/RTL/a25_wr
ite_back.v -Verilog -Golden   -sensitive         -continuousassignment Bidirectional
 -nokeep_unreach   -nosupply
// Command: read design /home/ecelrc/students/sshaikh1/Desktop/verif_lab1/partA/RTL/a
25_write_back.v -Verilog -Golden   -sensitive         -continuousassignment Bidirecti
onal   -nokeep_unreach   -nosupply
// Parsing file /home/ecelrc/students/sshaikh1/Desktop/verif_lab1/partA/RTL/a25_write
_back.v ...
// Golden root module is set to 'a25_write_back'
// Warning: (DIR3.1) synthesis/translate/compile on/off directive is detected (occurr
ence:2)
// Warning: (DIR4.2) HDL directive/pragma is supported (occurrence:2)
// Warning: (IGN1.1) Initial assignment is ignored (occurrence:3)
// Warning: (HRC3.10a) An input port is declared, but it is not completely used in th
e module (occurrence:33)
// Note: Read VERILOG design successfully
SETUP> read design /home/ecelrc/students/sshaikh1/Desktop/verif_lab1/partA/GATE/a25_w
rite_back_netlist.v -Verilog -Revised   -sensitive         -continuousassignment Bidi
rectional   -nokeep_unreach   -nosupply
// Command: read design /home/ecelrc/students/sshaikh1/Desktop/verif_lab1/partA/GATE/
a25_write_back_netlist.v -Verilog -Revised   -sensitive         -continuousassignment
Bidirectional   -nokeep_unreach   -nosupply
// Parsing file /home/ecelrc/students/sshaikh1/Desktop/verif_lab1/partA/GATE/a25_writ
e_back_netlist.v ...
// Revised root module is set to 'a25_write_back'
// Warning: (HRC3.10a) An input port is declared, but it is not completely used in th
e module (occurrence:33)
// Note: Read VERILOG design successfully
```

Figure 5: LEC console while loading golden and revised designs

4 Using the LEC mode

Switch from Setup mode to LEC mode using the GUI or the command line.

set system mode lec

Notice that the prompt changes from SETUP to LEC. Also note that the tool does the following things,

- Analyzes the golden and revised models
- Identifies key points in each model
- Produces a mapping between each model's key points
- Summarizes mapped input, output ports and D flip flops
- For part A. make sure that there are no unmapped on unreachable points in the design. If there are, you will have to fix them. For part A, you should get the window exactly as shown in Figure 6. However, for the rest of the parts, do not proceed with the next steps till you have no "unmapped or unreachable" points.

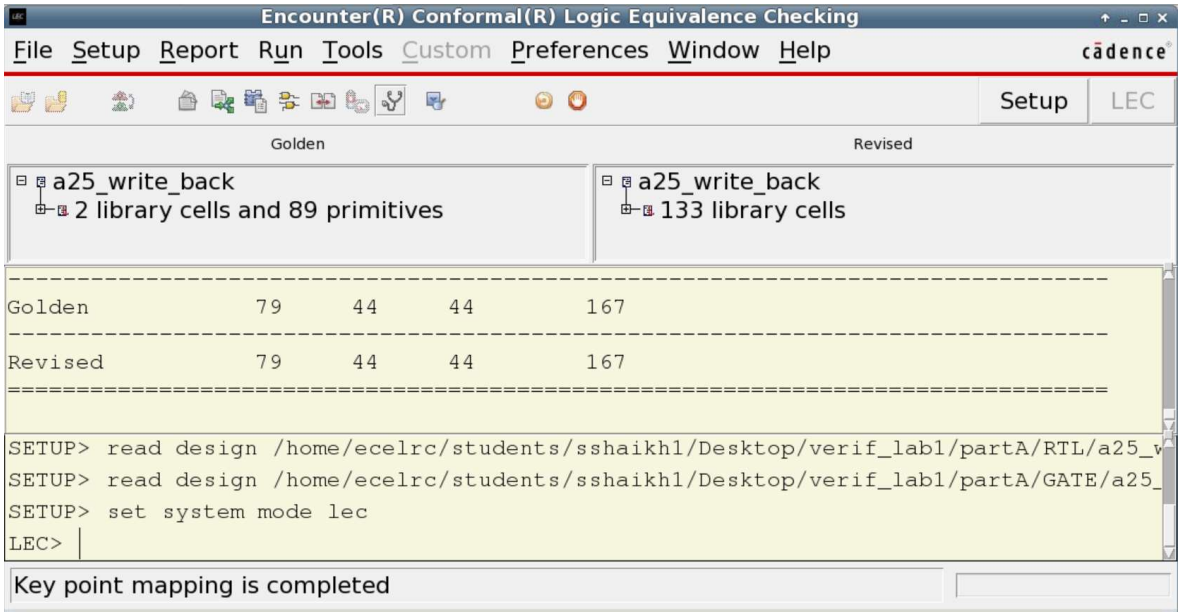

Figure 6: Change mode to LEC

In LEC mode, select **Run -> Compare** and then click on **Compare** after ensuring only **Add All Compare Points** is selected.

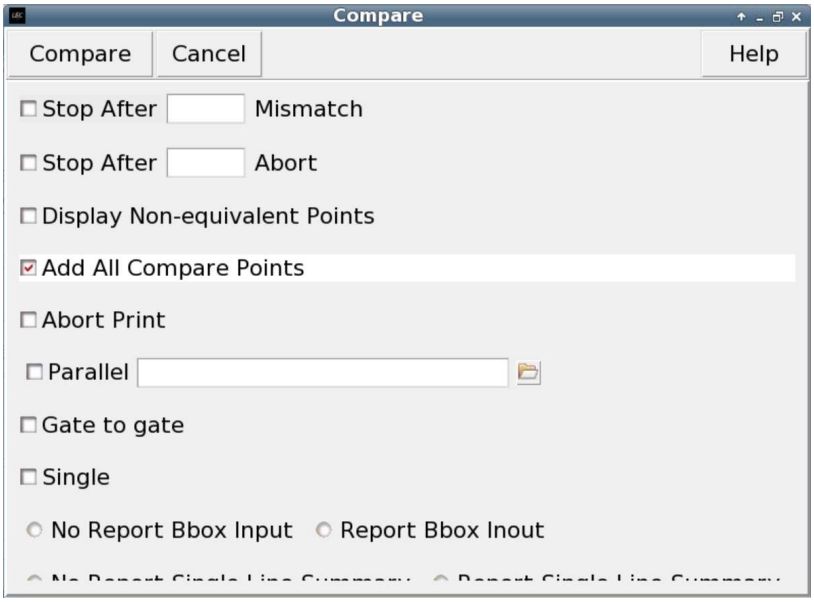

Figure 7: Compare Options

After the comparison has completed, you should get the results as shown in Figure 8. You will observe that there are non-equivalent points in the design. You will have to fix these errors till no non-equivalent points remain.

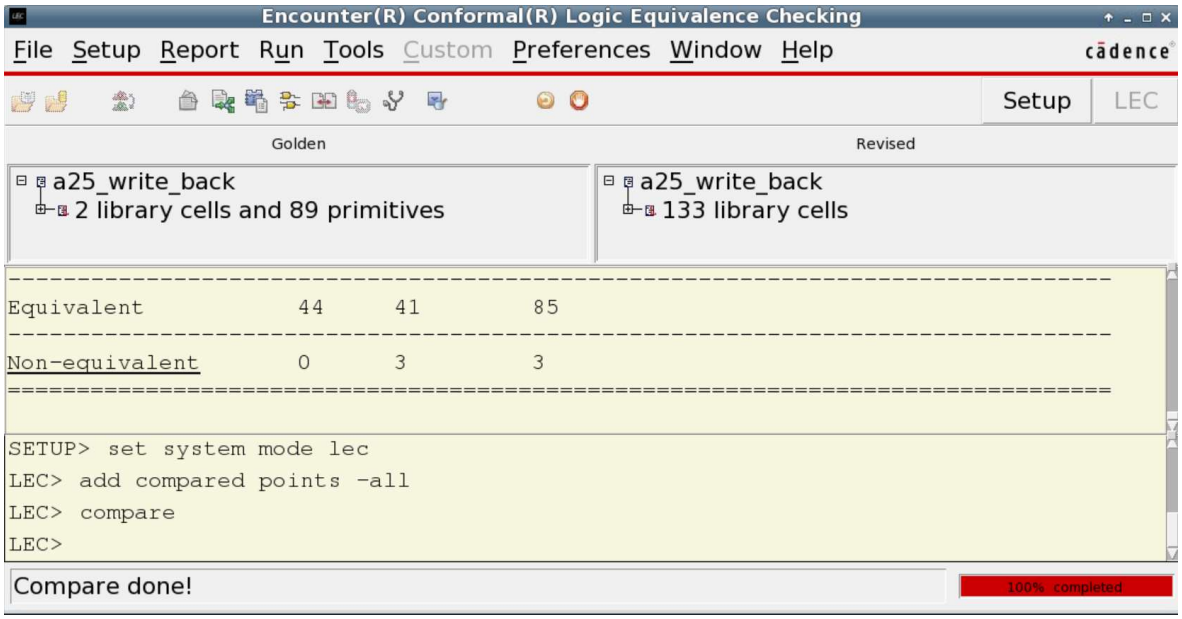

Figure 8: Result

To start debugging the design, you can use the Mapping Manager. It is accessible though Tools Mapping Manager. This opens a window where you can analyze the points which do not match with the RTL description. You can also click on "Non-equivalent points" in the main window.

In the Compare Points pane, use the class button to select only the non-equivalent points. Each point can be looked up on the schematic and input and output cones can be traced either through the schematic or the netlist or the RTL. Try to open the schematics by right clicking on the first DFF and selecting Schematics. This opens two schematic windows, one each for the Golden and the Revised models. You can use this to debug the errors in the netlist. Fix the netlist so that all points become equivalent.

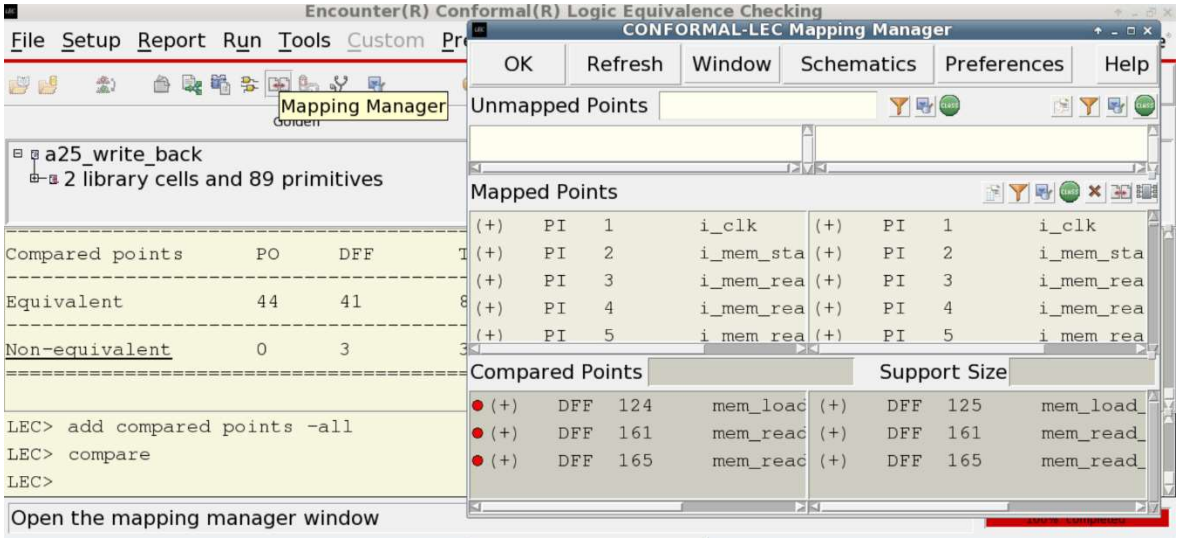

Figure 9: Mapping Manager Window

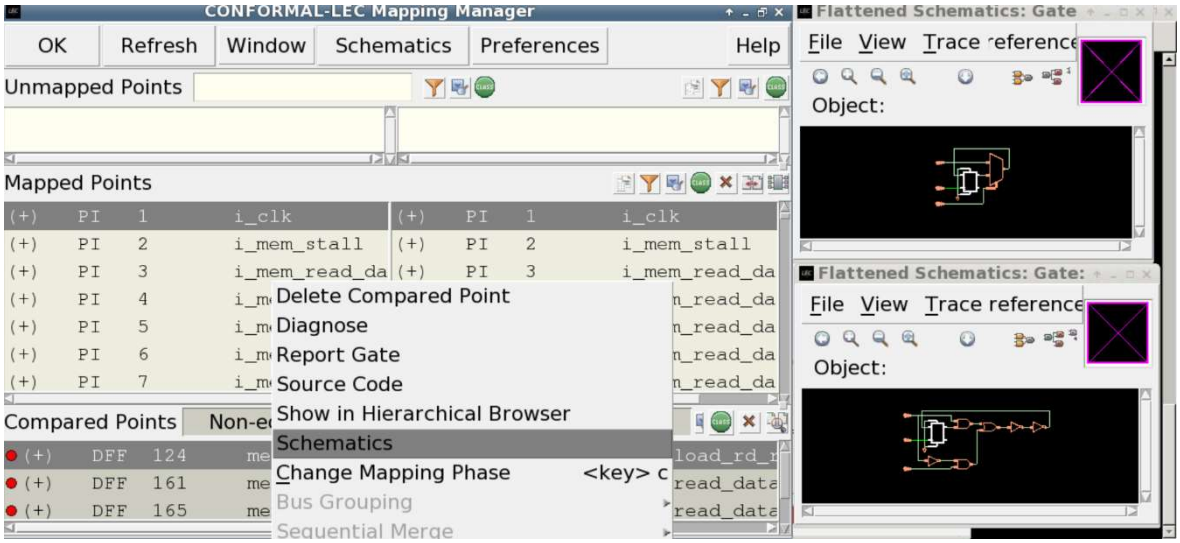

Figure 10: Golden and Revised non-equivalent point schematic comparison

5 Conformal LEC help

For information on the usage of the commands click on 'Help -> Commands'. Browse through the list to find the necessary commands as shown in the Figure 11.

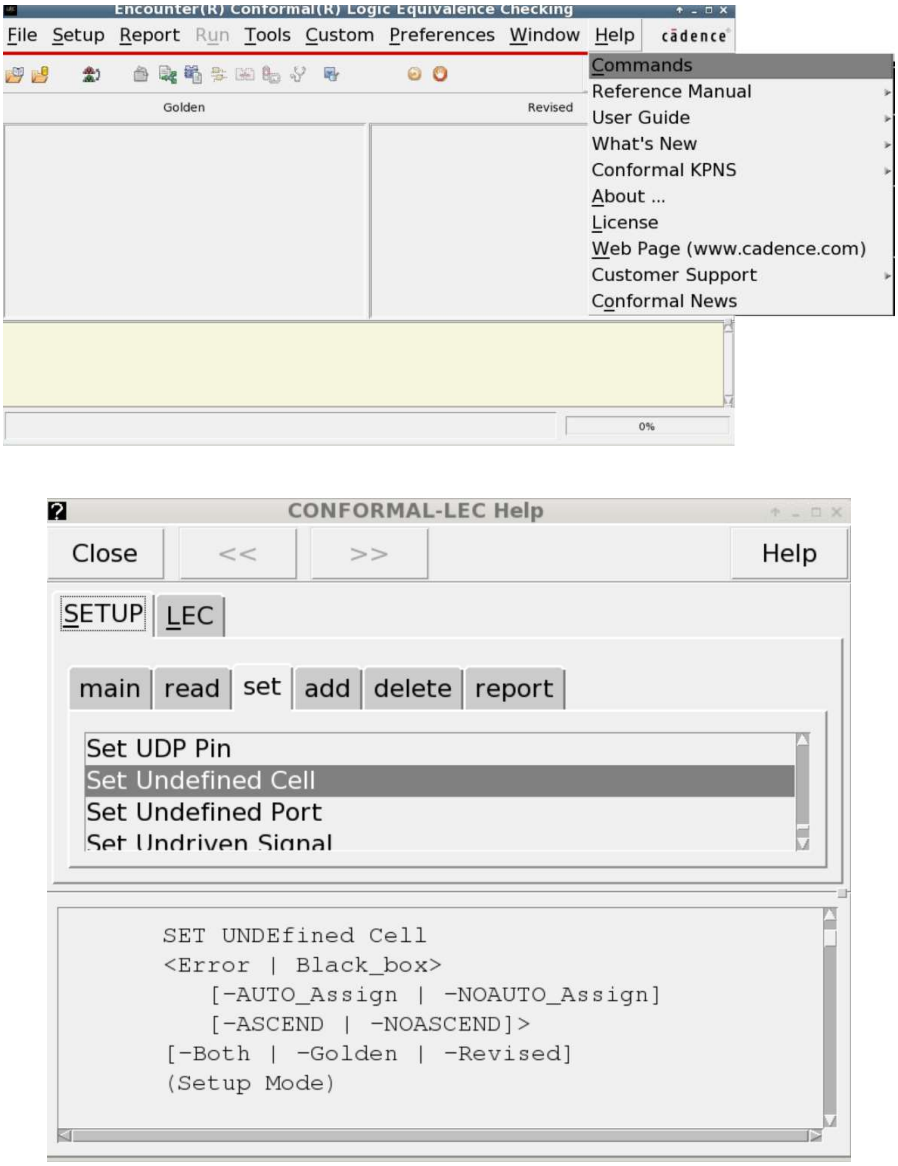

Figure 11: Command reference manual

6 LEC dofile

When a command is executed in conformal LEC GUI, such as, reading the library as shown in the Figure 2, the LEC console prints the 'read library' command as shown in the figure below.

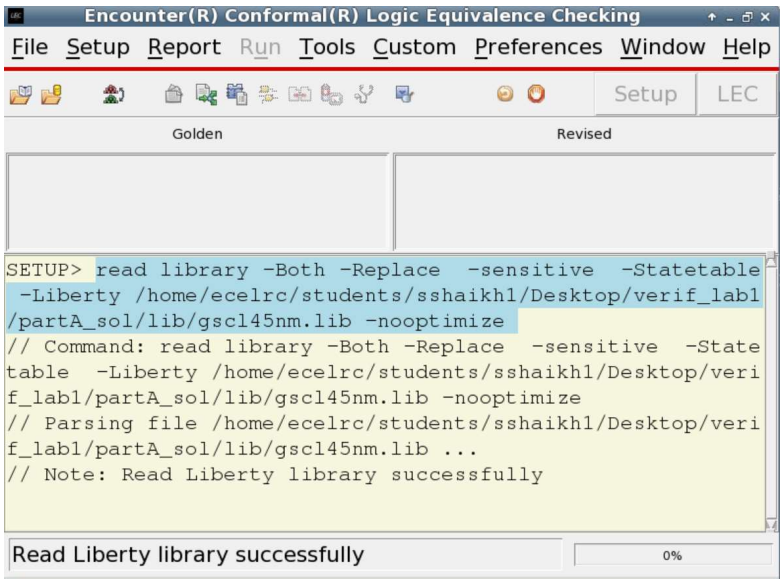

Figure 12: LEC console

We can paste this 'highlighted' command directly into the lec.do file and execute the dofile. Below is the lec.do file written in 'vpxmode' (which is by default).

```
// Load the library
read library -Both -Replace  -sensitive  -Statetable  -Liberty ../lib/gscl45nm.lib -nooptimize

// Load the golden design: RTL
read design ../rtl/a25_write_back.v -Verilog -Golden   -sensitive -continuousassignment Bidirectional   -nokeep_unreach   -nosupply

// Load the revised design: Netlist
read design ../gate/a25_write_back_netlist_rectified.v -Verilog -Revised -sensitive  -continuousassignment Bidirectional -nokeep_unreach -nosupply

// Change the mode to LEC
set system mode lec

// Add compare points and compare
add compared points -all
compare
```

To write the dofile in TCL mode, add the command 'tclmode' at the start of the dofile and concatenate the words in the command by underscores as shown in the snippet below.

```
// The dofile must be in 'tclmode'
tclmode

// Load the library
read_library -Both -Replace  -sensitive  -Statetable  -Liberty ../lib/gscl45nm.lib -nooptimize

// Load the golden design: RTL
read_design ../rtl/a25_write_back.v -Verilog -Golden   -sensitive -continuousassignment Bidirectional   -nokeep_unreach   -nosupply

// Load the revised design: Netlist
read_design ../gate/a25_write_back_netlist_rectified.v -Verilog -Revised   -sensitive  -continuousassignment Bidirectional -nokeep_unreach -nosupply

// Change the mode to LEC
set_system_mode lec

// Add compare points and compare
add_compared_points -all
compare
```

To execute the dofile, click on 'File -> Do Dofile' and select the 'lec.do' file in the browsing window as shown in the Figure 13.

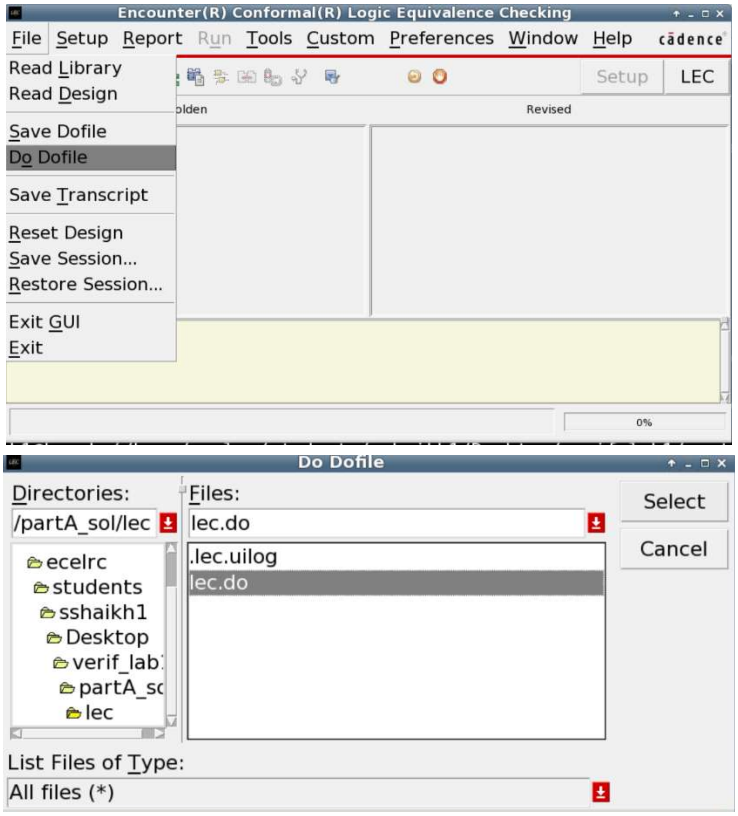

Figure 13: Execution of dofile.