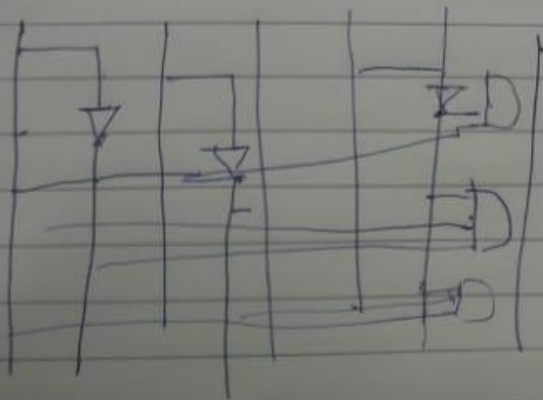
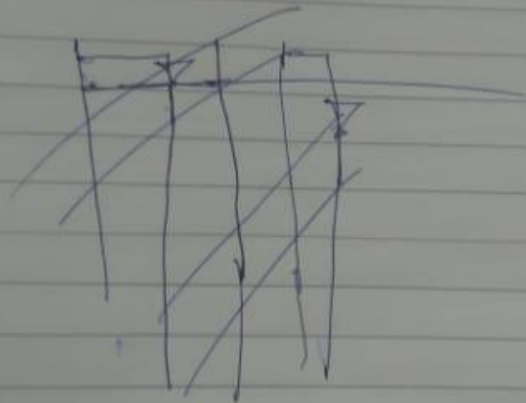
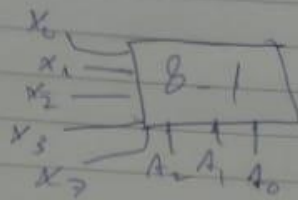


Phasenfaktor essen A_0
 sec 24

b3

$z=1 \rightarrow$ use B-1 Mod mult



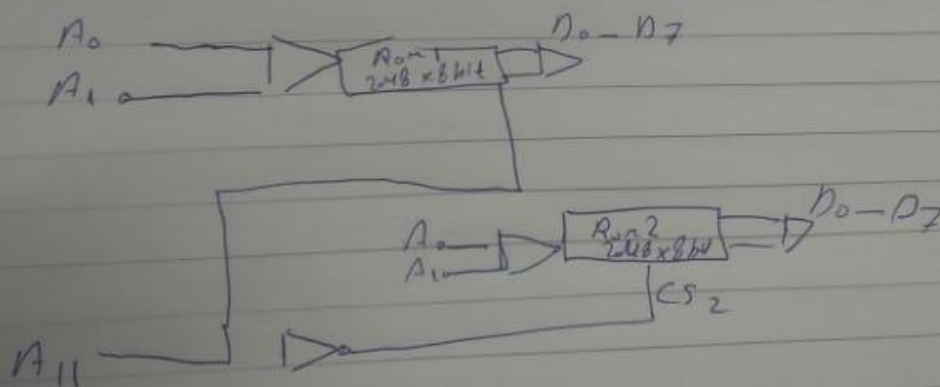
Abbildungsschema

Sec: 4

$$(1024 * 16 \text{ bit}) \quad \text{---} \quad 4096 * 16 \text{ bit}$$

no of required add = 12

no of available add = 12

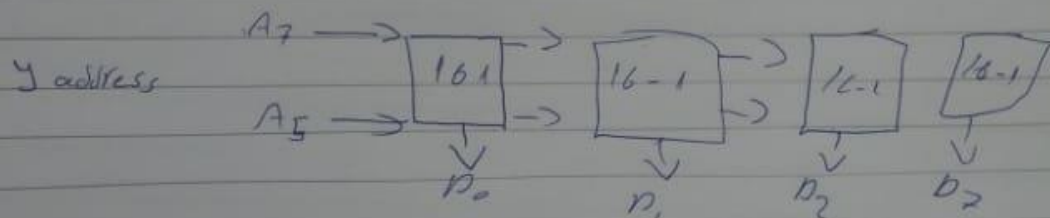
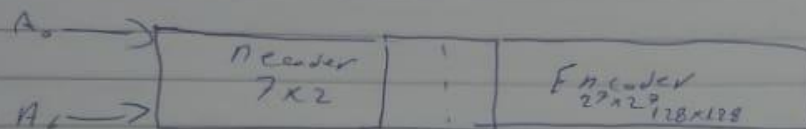


Abdelrahman Essam Ali
sec 4

$$\text{total address} = 2 = 2^{10} \times 2^4 = 2^7 \times 2^2$$

$$\text{data line} = 4 \text{ bit}$$

Address line =



$$\text{Number of x-address} = 2$$

$$\text{Number of y-address} = 2$$

$$\text{Number of NAND gate} = 2^7 [(16 \times 1) \times 8] = 264$$

$$\text{Number of Transistor} = 2^7 = 128$$

$$\text{Number of emitter} = 2^7 = 128$$