# EE2003: Computer Organisation

## Assignment # 3

*By :*

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Question 19

Plot the Miss Rate for any 2 replacement policies and 4-way associativity for L3 while varying the number of cores (1, 2, 4, 8).

*Date:*
19tht October 2023

# Contents

## 0.1 Cache Configuration of My System

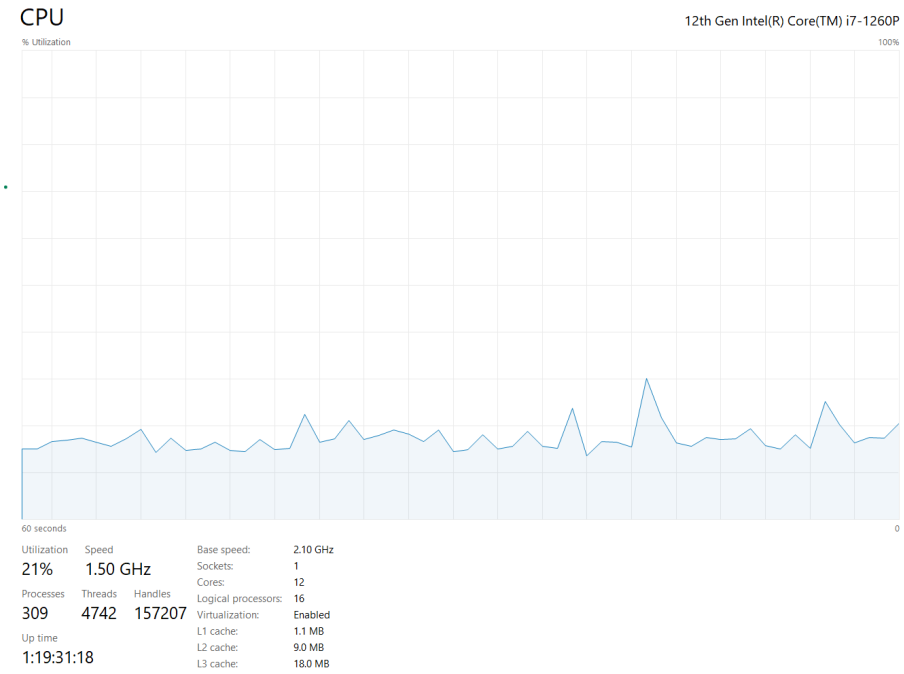


Figure 1: Cache Configuration of My System in task manager performance

```
PS C:\Users\iitms> Get-WmiObject -Class Win32_Processor | Select-Object Name, L1CacheSize, L2CacheSize, L3CacheSize

Name                                 L1CacheSize L2CacheSize L3CacheSize
----                                 ----------- ----------- -----------
12th Gen Intel(R) Core(TM) i7-1260P                    9216       18432
```

Figure 2: Cache Configuration of My System using get-winObject

```
C:\Users\iitms>wmic memcache list brief
BlockSize  CacheSpeed  CacheType  DeviceID        InstalledSize  Level  MaxCacheSize  NumberOfBlocks  Status
1024                   4          Cache Memory 0  192            3      192           192             OK
1024                   3          Cache Memory 1  128            3      128           128             OK
1024                   5          Cache Memory 2  5120           4      5120          5120            OK
1024                   5          Cache Memory 3  18432          5      18432         18432           OK
1024                   4          Cache Memory 4  256            3      256           256             OK
1024                   3          Cache Memory 5  512            3      512           512             OK
1024                   5          Cache Memory 6  4096           4      4096          4096            OK
1024                   5          Cache Memory 7  18432          5      18432         18432           OK
```

Figure 3: All Cache Configuration of My System using wmic memcache list brief

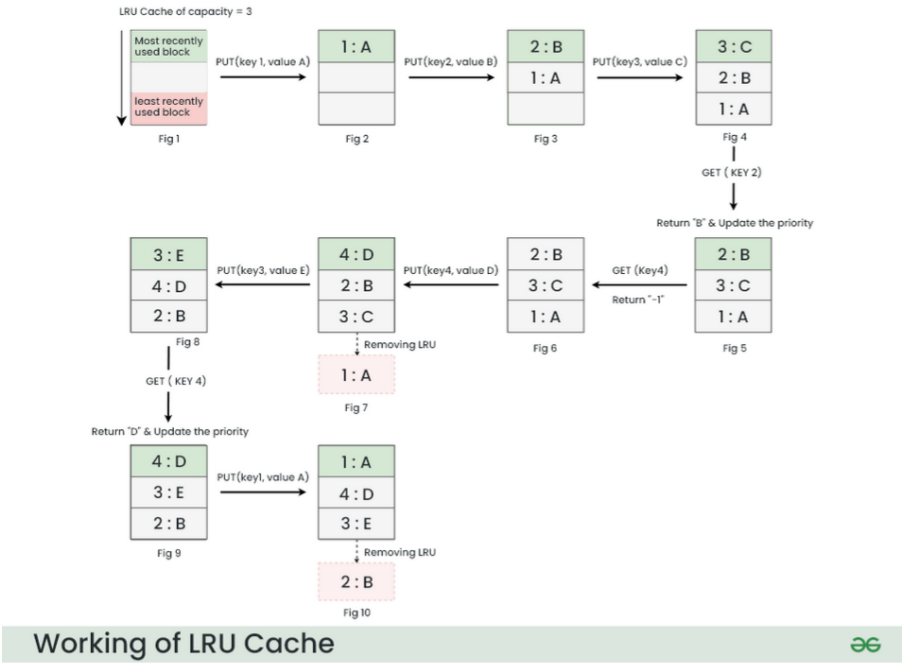


Figure 4: Least Replacement Policy

# 1 Replacement Policy

### 1.0.1 About LRU

Cache replacement algorithms are efficiently designed to replace the cache when the space is full. The Least Recently Used (LRU) is one of those algorithms. As the name suggests when the cache memory is full, LRU picks the data that is least recently used and removes it in order to make space for the new data. The priority of the data in the cache changes according to the need of that data i.e. if some data is fetched or updated recently then the priority of that data would be changed and assigned it to highest priority, and the priority of the data de-

creases if it remains unused operations after operations.

### 1.0.2 About SHIP

Most replacement policies attempt to learn the re-reference in- terval of cache lines by always making the same re-reference pre- diction for all cache insertions. Instead of making the same re- reference predictions for all cache insertions, we associate each cache reference with a distinct signature. We show that cache re- placement policies can be significantly improved by dynamically learning the re-reference interval of each signature and applying the information learned at cache insertion time. The goal of signature-based cache replacement is to predict whether the insertions by a given signature will receive future cache hits. The intuition is that if cache insertions by a given signature are re-referenced, then future cache insertions by the same signa- ture will again be re-referenced. Conversely, if cache insertions by a given signature do not receive subsequent hits, then future inser- tions by the same signature will again not receive any subsequent hits. To explicitly correlate the re-reference behavior of a signature, we propose a Signature-based Hit Predictor (SHiP)

## 2 Simulation Results

```
1 Core 1
2 LRU
3
4 LLC TOTAL        ACCESS:    8167612 HIT:     265315 MISS:
      7902297
5 LLC LOAD         ACCESS:    2390511 HIT:       4520 MISS:
      2385991
```

```
LLC RFO          ACCESS:    1874911 HIT:       8385 MISS:
    1866526
LLC PREFETCH     ACCESS:          0 HIT:          0 MISS:
    0
LLC WRITE        ACCESS:    2798352 HIT:     249843 MISS:
    2548509
LLC TRANSLATION  ACCESS:    1103838 HIT:       2567 MISS:
    1101271
LLC PREFETCH REQUESTED:          0 ISSUED:          0 USEFUL:
        0 USELESS:          0
LLC AVERAGE MISS LATENCY: 495.9 cycles

SHIP

LLC TOTAL        ACCESS:    8166107 HIT:     253843 MISS:
    7912264
LLC LOAD         ACCESS:    2390279 HIT:       4445 MISS:
    2385834
LLC RFO          ACCESS:    1874896 HIT:      12821 MISS:
    1862075
LLC PREFETCH     ACCESS:          0 HIT:          0 MISS:
    0
LLC WRITE        ACCESS:    2798289 HIT:     233000 MISS:
    2565289
LLC TRANSLATION  ACCESS:    1102643 HIT:       3577 MISS:
    1099066
LLC PREFETCH REQUESTED:          0 ISSUED:          0 USEFUL:
        0 USELESS:          0
LLC AVERAGE MISS LATENCY: 493.5 cycles

Core 2
LRU

LLC TOTAL        ACCESS:    8033099 HIT:      92356 MISS:
    7940743
LLC LOAD         ACCESS:    2389368 HIT:       2614 MISS:
    2386754
LLC RFO          ACCESS:    1807866 HIT:       6945 MISS:
    1800921
LLC PREFETCH     ACCESS:          0 HIT:          0 MISS:
    0
LLC WRITE        ACCESS:    2734562 HIT:      82385 MISS:
    2652177
LLC TRANSLATION  ACCESS:    1101303 HIT:        412 MISS:
    1100891
LLC PREFETCH REQUESTED:          0 ISSUED:          0 USEFUL:
        0 USELESS:          0
LLC AVERAGE MISS LATENCY: 580.3 cycles
LLC TOTAL        ACCESS:    8181877 HIT:      97346 MISS:
    8084531
LLC LOAD         ACCESS:    2398300 HIT:       2432 MISS:
    2395868
LLC RFO          ACCESS:    1874812 HIT:       6823 MISS:
    1867989
LLC PREFETCH     ACCESS:          0 HIT:          0 MISS:
    0
```

```
39 LLC WRITE        ACCESS:    2801774 HIT:      87744 MISS:
       2714030
40 LLC TRANSLATION  ACCESS:    1106991 HIT:        347 MISS:
       1106644
41 LLC PREFETCH REQUESTED:          0 ISSUED:          0 USEFUL:
         0 USELESS:          0
42 LLC AVERAGE MISS LATENCY: 580.3 cycles
43
44 SHIP
45
46 LLC TOTAL        ACCESS:    8033169 HIT:      99733 MISS:
       7933436
47 LLC LOAD         ACCESS:    2389383 HIT:       2723 MISS:
       2386660
48 LLC RFO          ACCESS:    1807836 HIT:       9713 MISS:
       1798123
49 LLC PREFETCH     ACCESS:          0 HIT:          0 MISS:
       0
50 LLC WRITE        ACCESS:    2734579 HIT:      86030 MISS:
       2648549
51 LLC TRANSLATION  ACCESS:    1101371 HIT:       1267 MISS:
       1100104
52 LLC PREFETCH REQUESTED:          0 ISSUED:          0 USEFUL:
         0 USELESS:          0
53 LLC AVERAGE MISS LATENCY: 580.8 cycles
54 LLC TOTAL        ACCESS:    8181696 HIT:     108809 MISS:
       8072887
55 LLC LOAD         ACCESS:    2398307 HIT:       2870 MISS:
       2395437
56 LLC RFO          ACCESS:    1874721 HIT:       8218 MISS:
       1866503
57 LLC PREFETCH     ACCESS:          0 HIT:          0 MISS:
       0
58 LLC WRITE        ACCESS:    2801450 HIT:      96864 MISS:
       2704586
59 LLC TRANSLATION  ACCESS:    1107218 HIT:        857 MISS:
       1106361
60 LLC PREFETCH REQUESTED:          0 ISSUED:          0 USEFUL:
         0 USELESS:          0
61 LLC AVERAGE MISS LATENCY: 580.8 cycles
62
63 Core 4
64
65 LRU
66
67 LLC TOTAL        ACCESS:    8332090 HIT:      47277 MISS:
       8284813
68 LLC LOAD         ACCESS:    2401279 HIT:       2034 MISS:
       2399245
69 LLC RFO          ACCESS:    1942255 HIT:       5297 MISS:
       1936958
70 LLC PREFETCH     ACCESS:          0 HIT:          0 MISS:
       0
71 LLC WRITE        ACCESS:    2866679 HIT:      39838 MISS:
       2826841
72 LLC TRANSLATION  ACCESS:    1121877 HIT:        108 MISS:
       1121769
```

```
LLC PREFETCH REQUESTED:          0 ISSUED:          0 USEFUL:
        0 USELESS:          0
LLC AVERAGE MISS LATENCY: 812.7 cycles
LLC TOTAL        ACCESS:    8337626 HIT:      49674 MISS:
    8287952
LLC LOAD         ACCESS:    2400925 HIT:       2280 MISS:
    2398645
LLC RFO          ACCESS:    1941970 HIT:       5613 MISS:
    1936357
LLC PREFETCH     ACCESS:          0 HIT:          0 MISS:
    0
LLC WRITE        ACCESS:    2863499 HIT:      41656 MISS:
    2821843
LLC TRANSLATION  ACCESS:    1131232 HIT:        125 MISS:
    1131107
LLC PREFETCH REQUESTED:          0 ISSUED:          0 USEFUL:
        0 USELESS:          0
LLC AVERAGE MISS LATENCY: 812.7 cycles
LLC TOTAL        ACCESS:    8322573 HIT:      47787 MISS:
    8274786
LLC LOAD         ACCESS:    2397291 HIT:       2192 MISS:
    2395099
LLC RFO          ACCESS:    1941708 HIT:       5600 MISS:
    1936108
LLC PREFETCH     ACCESS:          0 HIT:          0 MISS:
    0
LLC WRITE        ACCESS:    2861352 HIT:      39858 MISS:
    2821494
LLC TRANSLATION  ACCESS:    1122222 HIT:        137 MISS:
    1122085
LLC PREFETCH REQUESTED:          0 ISSUED:          0 USEFUL:
        0 USELESS:          0
LLC AVERAGE MISS LATENCY: 812.7 cycles
LLC TOTAL        ACCESS:    8166696 HIT:      49909 MISS:
    8116787
LLC LOAD         ACCESS:    2390339 HIT:       2065 MISS:
    2388274
LLC RFO          ACCESS:    1874811 HIT:       5594 MISS:
    1869217
LLC PREFETCH     ACCESS:          0 HIT:          0 MISS:
    0
LLC WRITE        ACCESS:    2798181 HIT:      42070 MISS:
    2756111
LLC TRANSLATION  ACCESS:    1103365 HIT:        180 MISS:
    1103185
LLC PREFETCH REQUESTED:          0 ISSUED:          0 USEFUL:
        0 USELESS:          0
LLC AVERAGE MISS LATENCY: 812.7 cycles

SHIP

LLC TOTAL        ACCESS:    8336359 HIT:      58856 MISS:
    8277503
LLC LOAD         ACCESS:    2403715 HIT:       1971 MISS:
    2401744
LLC RFO          ACCESS:    1942203 HIT:       5569 MISS:
    1936634
```

```
105 LLC PREFETCH     ACCESS:          0 HIT:          0 MISS:
        0
106 LLC WRITE        ACCESS:    2867646 HIT:      51105 MISS:
        2816541
107 LLC TRANSLATION  ACCESS:    1122795 HIT:        211 MISS:
        1122584
108 LLC PREFETCH REQUESTED:          0 ISSUED:          0 USEFUL:
            0 USELESS:          0
109 LLC AVERAGE MISS LATENCY: 813.7 cycles
110 LLC TOTAL        ACCESS:    8340332 HIT:      58208 MISS:
        8282124
111 LLC LOAD         ACCESS:    2402671 HIT:       2359 MISS:
        2400312
112 LLC RFO          ACCESS:    1941984 HIT:       6063 MISS:
        1935921
113 LLC PREFETCH     ACCESS:          0 HIT:          0 MISS:
        0
114 LLC WRITE        ACCESS:    2864757 HIT:      49621 MISS:
        2815136
115 LLC TRANSLATION  ACCESS:    1130920 HIT:        165 MISS:
        1130755
116 LLC PREFETCH REQUESTED:          0 ISSUED:          0 USEFUL:
            0 USELESS:          0
117 LLC AVERAGE MISS LATENCY: 813.7 cycles
118 LLC TOTAL        ACCESS:    8327945 HIT:      57688 MISS:
        8270257
119 LLC LOAD         ACCESS:    2398149 HIT:       2291 MISS:
        2395858
120 LLC RFO          ACCESS:    1943412 HIT:       6374 MISS:
        1937038
121 LLC PREFETCH     ACCESS:          0 HIT:          0 MISS:
        0
122 LLC WRITE        ACCESS:    2863620 HIT:      48788 MISS:
        2814832
123 LLC TRANSLATION  ACCESS:    1122764 HIT:        235 MISS:
        1122529
124 LLC PREFETCH REQUESTED:          0 ISSUED:          0 USEFUL:
            0 USELESS:          0
125 LLC AVERAGE MISS LATENCY: 813.7 cycles
126 LLC TOTAL        ACCESS:    8166897 HIT:      59794 MISS:
        8107103
127 LLC LOAD         ACCESS:    2390489 HIT:       2267 MISS:
        2388222
128 LLC RFO          ACCESS:    1874938 HIT:       6309 MISS:
        1868629
129 LLC PREFETCH     ACCESS:          0 HIT:          0 MISS:
        0
130 LLC WRITE        ACCESS:    2798367 HIT:      51040 MISS:
        2747327
131 LLC TRANSLATION  ACCESS:    1103103 HIT:        178 MISS:
        1102925
132 LLC PREFETCH REQUESTED:          0 ISSUED:          0 USEFUL:
            0 USELESS:          0
133 LLC AVERAGE MISS LATENCY: 813.7 cycles
134
135 core 8
136
```

```
137
138 I tried simulating it for thrice it took 11 hours 1st time then 9
        hours but no proper simulation result I could get.
139  Here are some snippets of the simulation when I ran for Warmup
        Instructions: 2000000 Simulation Instructions: 10000000, when I
         simulated for  Warmup Instructions: 200000 Simulation
        Instructions: 1000000 it was running for 9 hour when I aborted.
140
141
142  LRU
143
144 Heartbeat CPU 2 instructions: 1130000000 cycles: 502516720
        heartbeat IPC: 3.125 cumulative IPC: 2.249 (Simulation time: 11
         hr 03 min 27 sec)
145 Heartbeat CPU 3 instructions: 770000003 cycles: 503259489 heartbeat
         IPC: 2.298 cumulative IPC: 1.53 (Simulation time: 11 hr 04 min
         27 sec)
146 Heartbeat CPU 1 instructions: 1560000001 cycles: 503791083
        heartbeat IPC: 3.669 cumulative IPC: 3.097 (Simulation time: 11
         hr 05 min 27 sec)
147 Heartbeat CPU 4 instructions: 450000003 cycles: 504961826 heartbeat
         IPC: 1.457 cumulative IPC: 0.8912 (Simulation time: 11 hr 07
        min 12 sec)
148 20:00:0020:00:00Heartbeat CPU 2 instructions: 1140000000 cycles:
        505967796 heartbeat IPC: 2.898 cumulative IPC: 2.253 (
        Simulation time: 11 hr 09 min 20 sec)Heartbeat CPU 1
        instructions: 1570000003 cycles: 506516336 heartbeat IPC: 3.669
         cumulative IPC: 3.1 (Simulation time: 11 hr 10 min 22 sec)
149 Heartbeat CPU 3 instructions: 780000002 cycles: 508107924 heartbeat
         IPC: 2.063 cumulative IPC: 1.535 (Simulation time: 11 hr 12
        min 33 sec)
150 Heartbeat CPU 2 instructions: 1150000003 cycles: 509029019
        heartbeat IPC: 3.267 cumulative IPC: 2.259 (Simulation time: 11
         hr 13 min 53 sec)
151
152  SHIP
153 Heartbeat CPU 4 instructions: 450000003 cycles: 504961826 heartbeat
         IPC: 1.457 cumulative IPC: 0.8912 (Simulation time: 11 hr 03
        min 47 sec)
154 20:00:0020:00:00Heartbeat CPU 2 instructions: 1140000000 cycles:
        505967796 heartbeat IPC: 2.898 cumulative IPC: 2.253 (
        Simulation time: 11 hr 05 min 48 sec)
155 Heartbeat CPU 1 instructions: 1570000003 cycles: 506516336
        heartbeat IPC: 3.669 cumulative IPC: 3.1 (Simulation time: 11
        hr 06 min 45 sec)
156 Heartbeat CPU 3 instructions: 780000002 cycles: 508107924 heartbeat
         IPC: 2.063 cumulative IPC: 1.535 (Simulation time: 11 hr 08
        min 55 sec)
157 Heartbeat CPU 2 instructions: 1150000003 cycles: 509029019
        heartbeat IPC: 3.267 cumulative IPC: 2.259 (Simulation time: 11
         hr 10 min 15 sec)
158 Heartbeat CPU 1 instructions: 1580000001 cycles: 509241636
        heartbeat IPC: 3.669 cumulative IPC: 3.103 (Simulation time: 11
         hr 10 min 33 sec)
159
160
```

Listing 1: 1st problem code

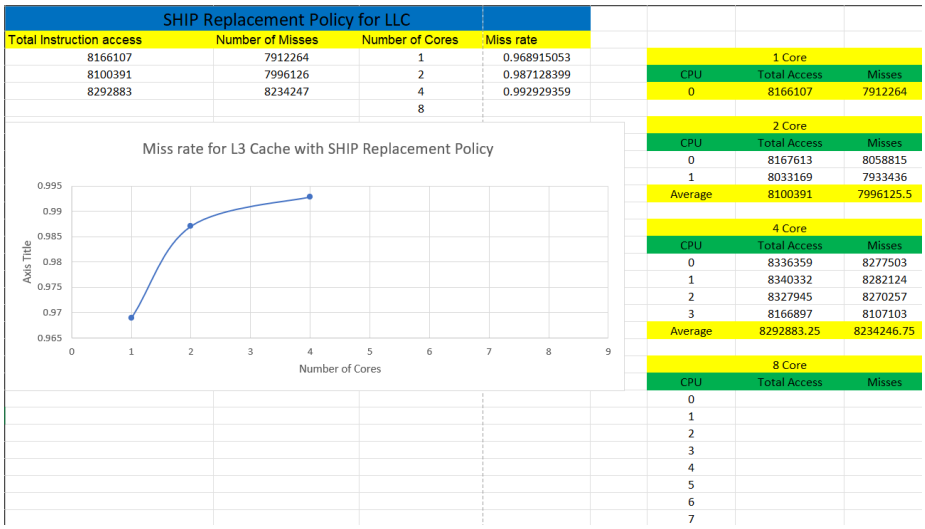


Figure 5: SHIP Replacement Policy

# 3 Outputs

The outputs of simulating are:-

Here we can see that miss rate is quite high and is increasing with increase in number of core. The relationship between the L3 cache miss rate and the number of processor cores in a multi-core system is complex and depends on several factors. It's not always the case that the miss rate increases with the number of cores; it can vary depending on the architecture, workload, and cache design. However, there are several reasons why you might observe an increase in L3 cache miss rate with an increasing number of cores in some scenarios:

Cache Contention: As the number of cores increases, there is greater contention for the shared L3 cache. Multiple cores may simultaneously access the cache, leading to increased cache contention, which can result in higher cache miss rates.

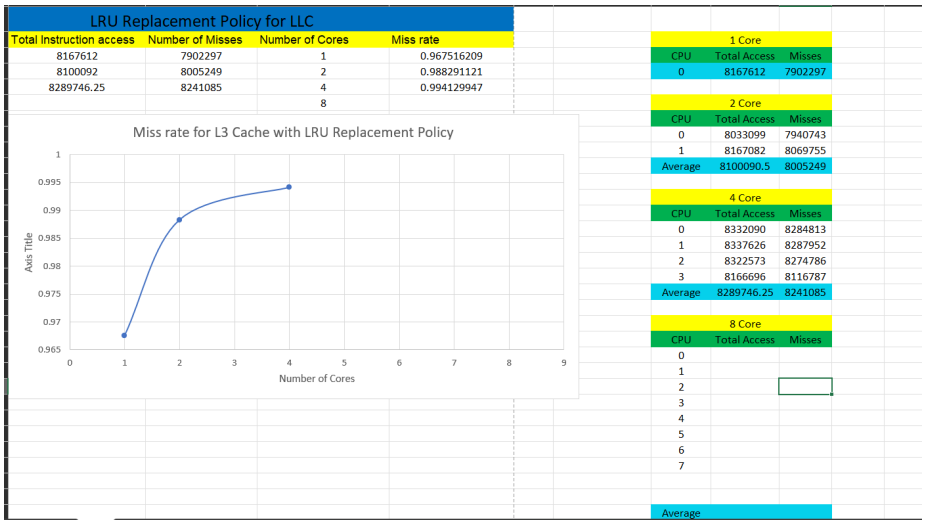


Figure 6: Least Replacement Policy

Cache Thrashing: With more cores, there is a higher likelihood of cache thrashing, where data is frequently evicted from the cache to make room for data from other cores. This can increase cache miss rates as data needed by a core is more likely to be evicted before it's reused.

Increased Memory Traffic: Multi-core systems tend to generate more memory traffic due to the simultaneous execution of multiple threads or processes. This increased memory traffic can lead to a higher rate of cache misses in the L3 cache as it struggles to keep up with the demand.

Scalability Issues: Some cache designs may not scale well with the number of cores. If the cache architecture was not designed to handle a large number of cores efficiently, it may experience diminishing returns and increased cache contention as more cores are added.

Non-Uniform Access: In some multi-core architectures,

the L3 cache may be non-uniformly accessed, meaning that some cores have faster access to the cache than others. This non-uniformity can lead to cores experiencing higher cache miss rates.