

Assignment 6

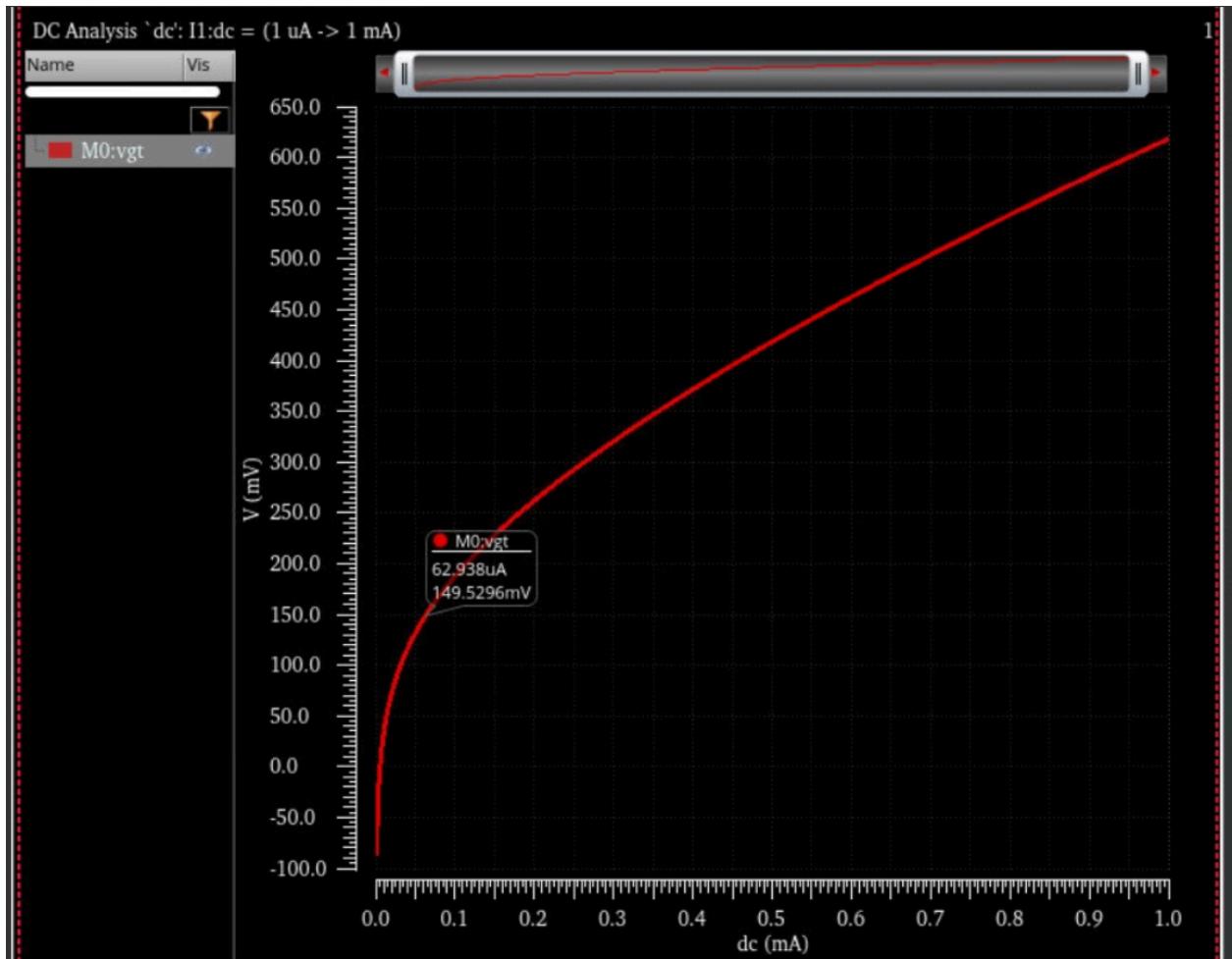
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EE21B017

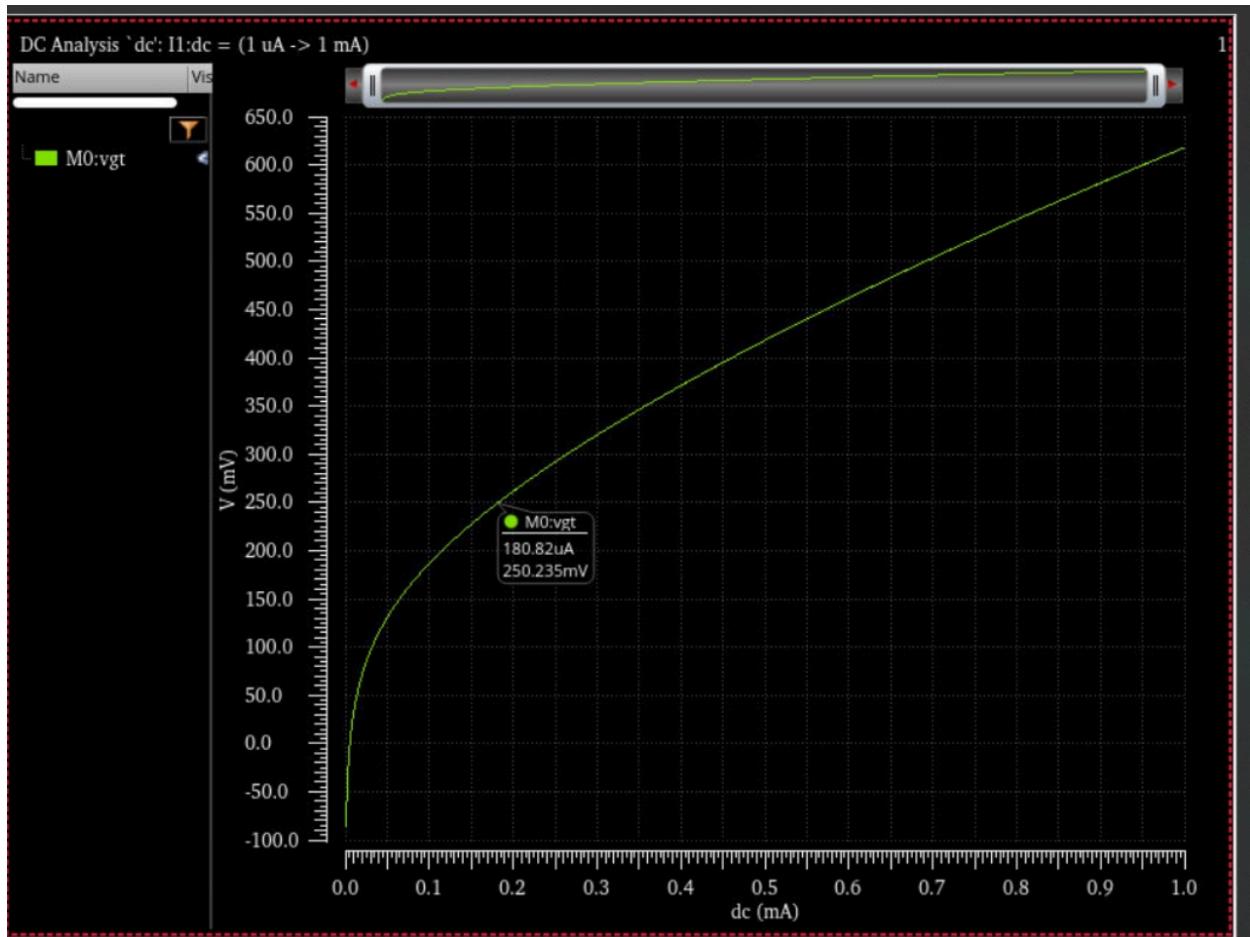
Simulation Results

Name of Parameter	Value
Supply Voltage (Vdd)	1.8 V
Vss	0 V
Common mode-bias (Vcm)	0.9
Length of all transistors (L)	0.3um
Unit-width (w)	1um
m00	2
m0	40
m1=m2=m5=m6	56
m3=m4=m7=m8	16
m11	24
m12	91
Bias Current (I00)	9.55u
Vb56	665mV
Vb78	830mV
Simulation Temperature	100
gm1	1.052 mS
gm11	3.63 mS
Cc	1PF
RL	1.88348K Ohms
CL	13 PF
k	13

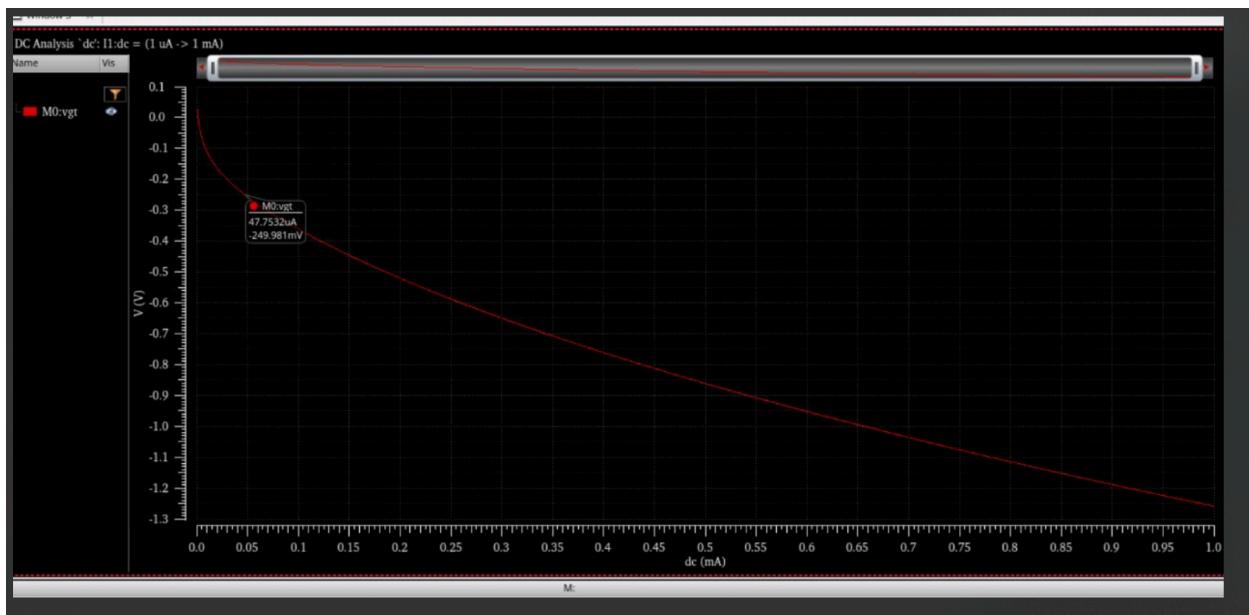
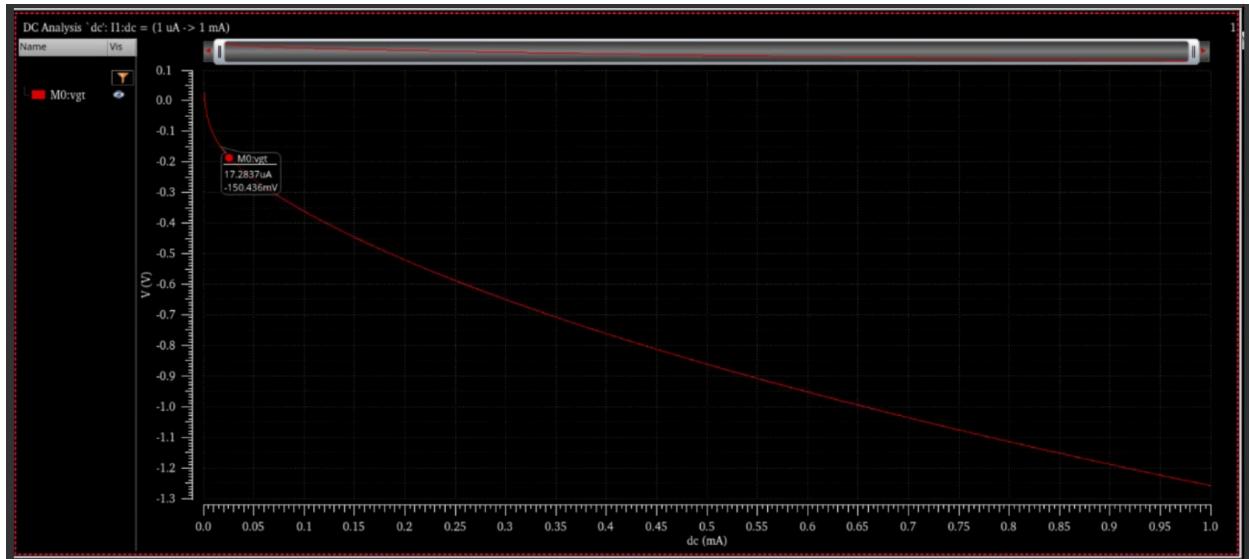
Ad	360f
As	360f
Dd	2.72u
i00	9.55u
I	300n
m0	40
m00	2
m11	24
m12	91
mn	16
mp	56
Sd	2.72u
Vb56	665m
Vb78	830m
w	1u

ADEL Parameters

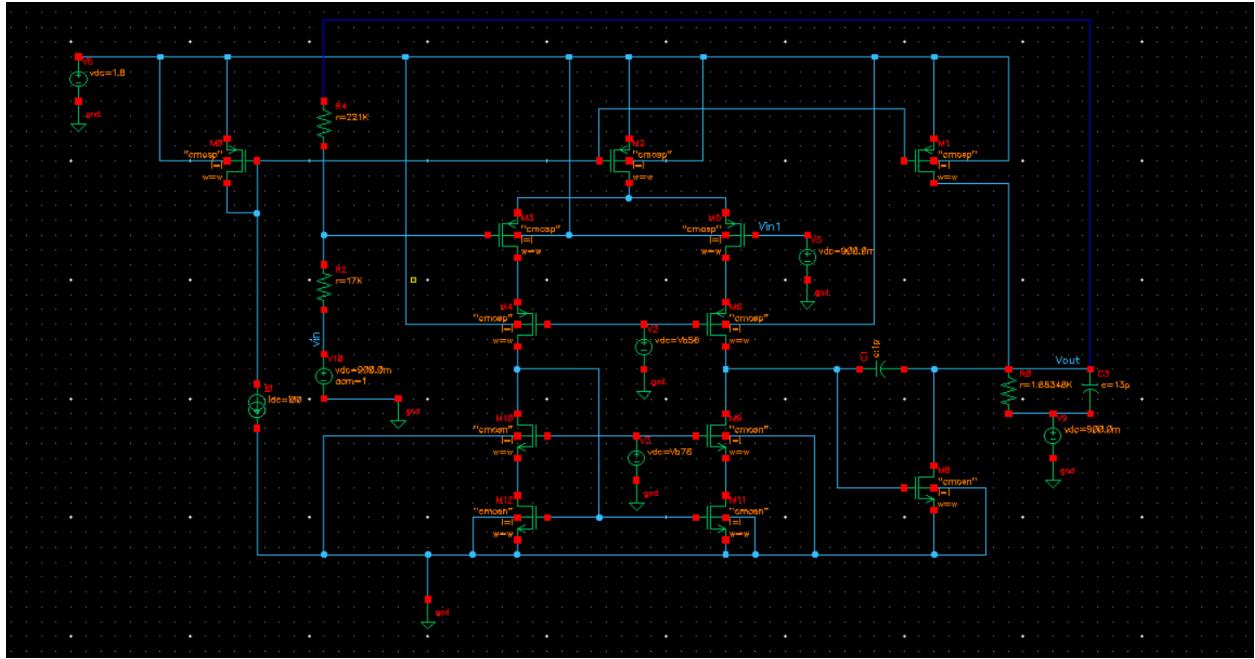




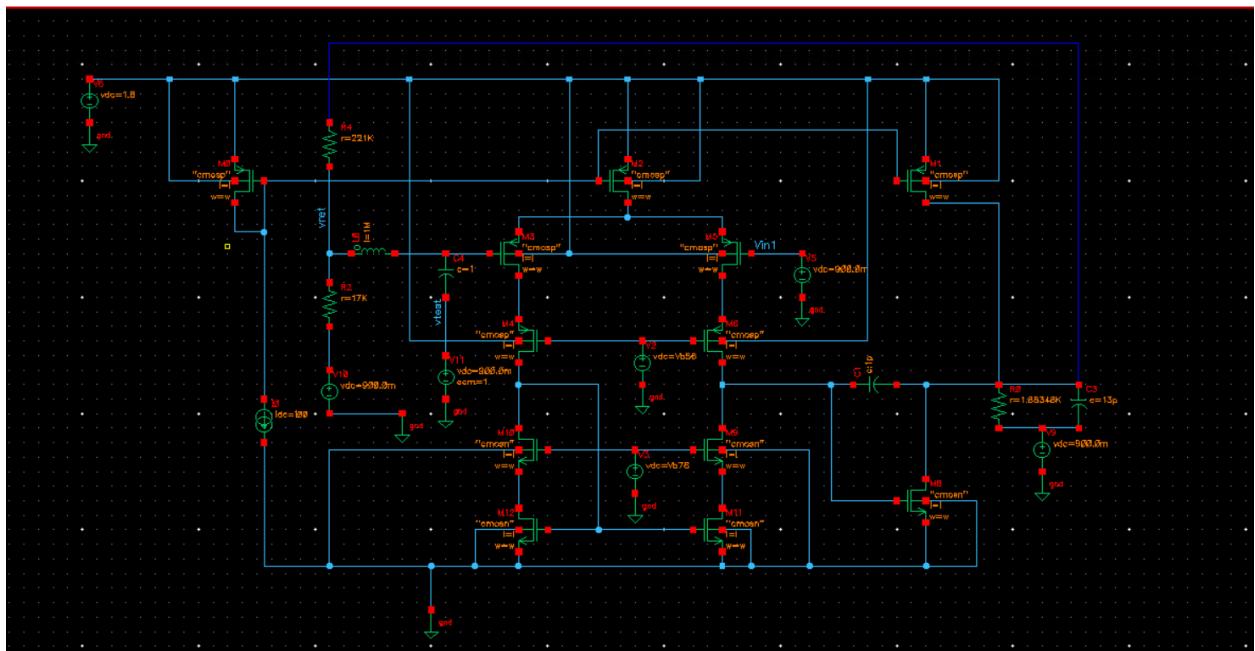
NMOS $10 \times I_{perw}$ for $V_{Dsat} = 150\text{mV}$ and 250mV



PMOS 10*Iperw for VDsat=150m V and 250m V



Closed Loop Circuit



Loop Gain Circuit

Simulation Results

Name of Parameter	Obtained Value
Closed Loop DC gain	12.955 (desired 13)
Closed Loop 3-dB Bandwidth	14.9624MHz (desired 13 MHz)
Unity Loop Gain Frequency	8.97429MHz
Phase Margin	75.023 degree
Integrated RMS Output Noise	1.221m
Opamp open-loop DC gain	290.78
Positive Slew rate	19.359M
Negative Slew rate	76.83M
Positive Swing Limit (at output)	1.5999 V
Negative Swing Limit (at output)	127.789mV
HD3	222.42 dB
Supply voltage	1.8
Current Consumption	0.6219mA

Device	Param	Noise Contribution	% Of Total
/R2	rn	9.86342e-07	66.16
/M11	fn	1.1756e-07	7.89
/M12	fn	1.17375e-07	7.87
/R4	rn	7.57934e-08	5.08
/M12	id	4.92905e-08	3.31
/M11	id	4.92622e-08	3.30
/M3	id	4.59355e-08	3.08
/M5	id	4.34531e-08	2.91
/M3	fn	1.31337e-09	0.09
/M5	fn	1.31026e-09	0.09
/M0	id	9.39051e-10	0.06
/M2	id	6.38456e-10	0.04
/M10	fn	2.52854e-10	0.02
/M9	fn	2.5044e-10	0.02
/M4	id	2.3984e-10	0.02
/M8	id	1.94638e-10	0.01
/M8	fn	1.82118e-10	0.01
/M1	id	1.74782e-10	0.01
/M10	id	8.23676e-11	0.01
/M9	id	7.93427e-11	0.01
/M6	id	7.28774e-11	0.00
/R0	rn	4.59084e-11	0.00
/M0	fn	6.6145e-12	0.00
/M2	fn	5.23379e-12	0.00
/M4	fn	2.27443e-12	0.00
/M6	fn	1.97584e-12	0.00
/M1	fn	1.64777e-12	0.00
/M0	rs	0	0.00
/M0	rd	0	0.00
/M1	rs	0	0.00
/M1	rd	0	0.00
/M10	rs	0	0.00
/M10	rd	0	0.00

Noise Contribution from different Sources

Maximum noise contribution is from R2 i.e. $R_i=17K$, The contribution from 2nd stage is about 0.07 percent, while that of 1st stage is 28.69 percent.

VDsat of the Transistors

MOSFET	Observed VDsat (in mV)	Required VDsat (in mV)
M1	-144.1	-150
M2	-144.3	-150
M3	144.8	150
M4	144.8	150
M5	-133.8	-150
M6	-134.7	-150
M7	133.7	150
M8	132.5	150
M0	-248	-250
M00	-249.5	-250
M11	251.6m	250
M12	-250.2	-250

< assignment06

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Assignment 6

$$Gm_1 = 1.06m_{M_1}$$

$$Gm_2 = 363 \text{ m}$$

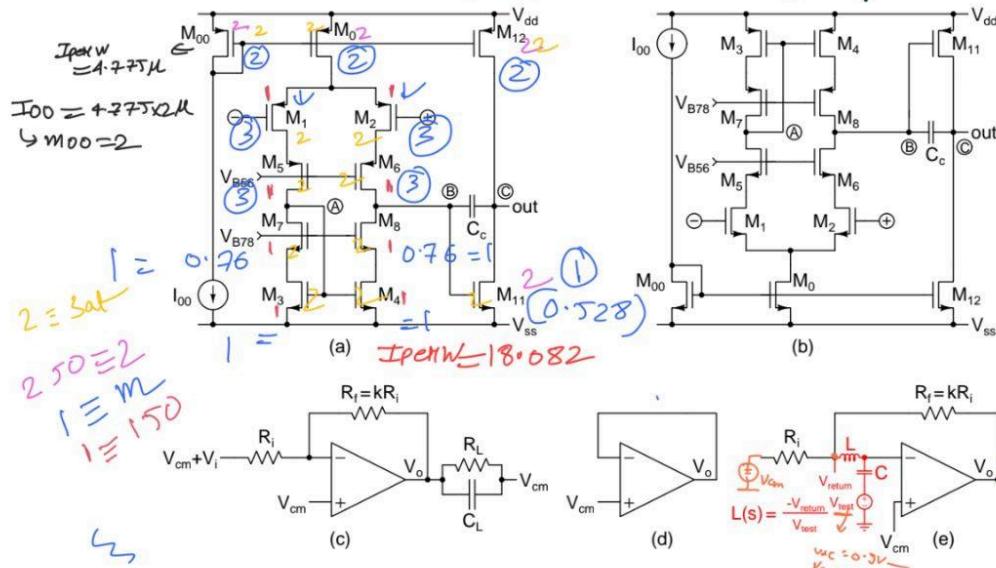


Figure 6.1: Problem 6.1.

- 6.1. Fig. 6.1 shows two-stage opamps. The first stage is a telescopic cascode stage. (a) uses a pMOS differential pair in the first stage and an nMOS common-source amplifier in the second stage. (b) uses an nMOS differential pair in the first stage and a pMOS common-source amplifier in the second stage.

Realize the inverting amplifier (Fig. 6.1(c)) that you designed in assignment 4 using these opamps. You will be using the same component values here. You will also need the results of MOS characterization to determine the current density.

For simulating the operating point, place the opamp in unity negative feedback as shown in Fig. 6.1(d) or simulate it in open loop with nodes A, B, and C shorted to each other and both inputs at V_{cm} .

- $V_{dd} = 1.8 \text{ V}$, $V_{ss} = 0 \text{ V}$, $V_{cm} = 0.9 \text{ V}$.
 - Simulation temperature: 100°C .
 - Odd roll numbers: pMOS input pair; Even roll numbers: nMOS input pair.
 - $L = 0.3 \mu\text{m}$ for all transistors.
 - Use¹ $V_{DSAT} = 0.15 \text{ V}$ for the first stage transistors except M_0 . Use $V_{DSAT} = 0.25 \text{ V}$ for the second stage transistors, M_0 , and M_{00} .
 - Choosing the V_{DSAT} value fixes the g_m and I_D per $1 \mu\text{m}/0.3 \mu\text{m}$ finger. Choose the multiplier m for each transistor to set its g_m or I_D as required.

¹Choose the current density that sets the V_{DSAT} to within 10mV of the specified values. Do not aim for microvolt precision.

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- For M_{00} , use $m = 2$ and choose I_{00} (integer μA) that sets the desired bias in the first and the second stages.
- All nMOS bulk terminals should be connected to V_{ss} . All pMOS bulk terminals should be connected to V_{dd} .
- Adjust V_{B56} such that the V_{DS} of $M_{1,2}$ is 50 mV above their V_{DSAT} . Similarly, Adjust V_{B78} such that the V_{DS} of $M_{3,4}$ is 50 mV above their V_{DSAT} . i.e., M_{1-4} must be in saturation region with 50 mV margin.

Verify that the operating point (bias currents, voltages, transconductances) are correctly set up before simulating the amplifier.

Present the following results.

Tables:

- Specification table with your specific values and all the component values.
- Table showing simulation results: closed loop dc gain, closed loop 3-dB bandwidth, unity loop gain frequency, phase margin, rms output noise (integrated from 10 kHz to 100 MHz), fraction of noise variance (integrated from 10 kHz to 100 MHz) contributed by R_i , R_f , first stage, second stage, and R_L , Opamp open loop dc gain, positive and negative slew rates, positive and negative swing limits, HD_3 , supply voltage, current consumption. To find the opamp slew rates apply a large input step (from V_{cm} to $V_{cm} + V_{step}$) such that the first stage current is completely switched to one side.

To find HD_3 , apply a sinusoidal input that results in a 1 V peak-peak output at a frequency that is 1/4th the bandwidth. Report HD_3 , the ratio of the third harmonic to the fundamental (in dB).

Plots:

- Loop gain magnitude (dB) and phase (degrees). The unity loop gain frequency and phase margin must be marked. Break the loop as shown in Fig. 6.1(e) to simulate the loop gain. Use large L , C , e.g., $L = 10^6 \text{ H}$, $C = 1 \text{ F}$. The frequency range should be from $\sim 0.1 \times$ dominant pole to where the loop gain is $\sim -20 \text{ dB}$.
- Closed loop transfer function magnitude on a log-y scale showing the dc gain and the 3-dB bandwidth.
- Closed loop dc transfer curve. Vary V_i from $V_{cm} - 0.5 \text{ V}$ to $V_{cm} + 0.5 \text{ V}$
- Small-signal step response: Output should step from $V_{cm} - 0.05 \text{ V}$ to $V_{cm} + 0.05 \text{ V}$ and back. Use a short rise time $\sim 100 \text{ ps}$.
- Large-signal step response: Output should step from $V_{cm} - 0.5 \text{ V}$ to $V_{cm} + 0.5 \text{ V}$ and back. Use a short rise time $\sim 100 \text{ ps}$. Check to see that the current is completely switched to one side in the first stage.
- Output noise PSD and the input referred noise PSD of the closed loop amplifier from 10 kHz to 100 MHz.
- Input referred noise PSD of the opamp from 10 kHz to 100 MHz.

(Not for submission):

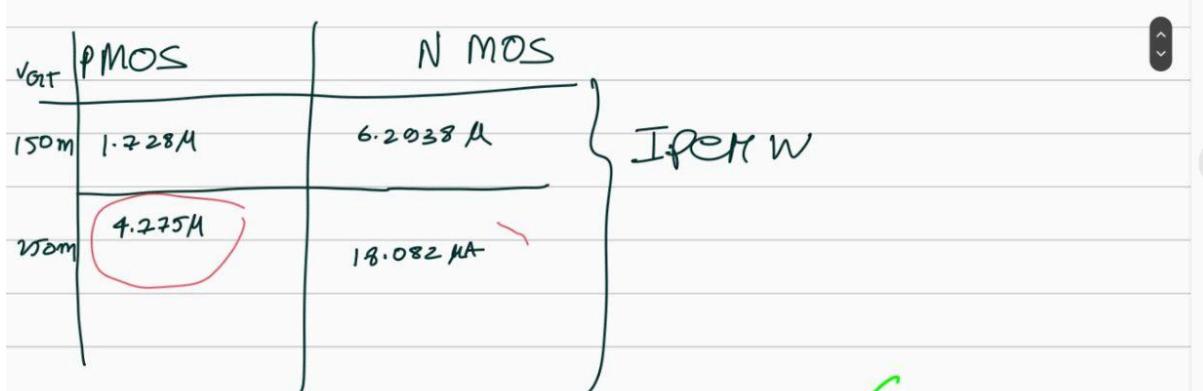
- Remove the cascodes from the first stage, run the simulations and find out the differences
- Connect C_c to the drain of M_2 or M_4 instead of the drains of $M_{6,8}$. See if there is a difference in phase margin. You can also try connecting $C_c/2$ each to the drains of M_2 and M_4 .

slew
HD3
noise

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< assignment06

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$$m_1 = m_2 = m_6 = m_5 \Rightarrow \checkmark$$

$$m_7 = m_8 = m_3 = m_4 = 1 \checkmark$$

$$m_{11} = 1 \quad m_{12} = 2 = m_0$$

$$m_{00} = 2$$

$$= 0.00363$$

$$Gm_1 = 1.06 m$$

affected
by m_1

$$Gm_2 = 3.63 m$$

affected by
 m_{11}

$$\alpha m_1 = 63.81 \mu$$

$$D\mu \quad 63.83 \mu$$

$$1.06 \times 10^{-3} = 63.83 \times 10^{-6} \times \mu_4$$

$$\mu = 16.606$$

$$\alpha m_2 = 128.9 \mu$$

$$3.63 \times 10^{-3} = 128.9 \mu_2$$

$$\mu_2 = 28.16$$

$$m_{11} = 14.86$$

$$\approx 15$$

$$m_{00} = 2 \approx 24$$

$$m_1 = m_2 = m_6 = m_5$$

$$= 45.88$$

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$$m_1 = m_2 = m_6 = m_5 \\ = 45.88 \\ \approx 46 \quad \approx 56$$

$$\text{mod} = 2 \approx 24$$

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$$m_3 = m_4 = m_7 = m_8 \\ \approx 13 \quad \approx 16$$

$$m_{12} \\ = 56.32 \\ \approx 57$$

$$M_D = 33.212 \\ \approx 34 \\ \approx 33 \\ \approx 40$$

$$\approx 91$$

$$\begin{aligned} V_{BJ6} &= 665 \text{ m} \\ V_{B78} &= 830 \text{ m} \end{aligned}$$

$$\begin{aligned} \text{dib} &\rightarrow 1-2 \quad 0.52 \text{ m} \\ \text{dib} &\rightarrow 3-4 \quad 0.53 \text{ m} \end{aligned}$$

$$\begin{aligned} M_1 \Rightarrow V_{\text{sat}} &= -144.1 \text{ m} \\ M_2 \Rightarrow V_{\text{sat}} &= -144.3 \text{ m} \end{aligned}$$

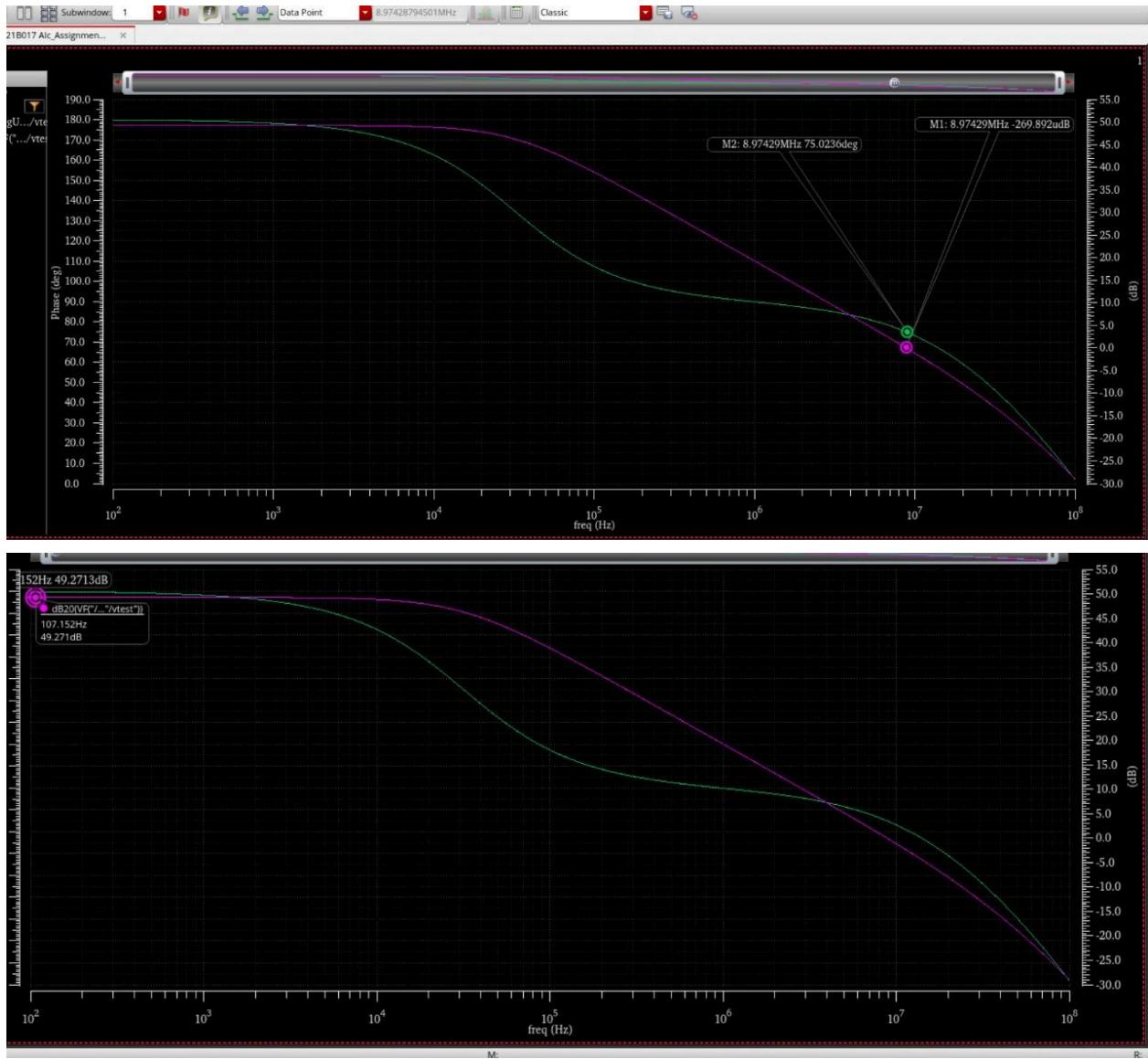
$$\begin{aligned} M_5 \Rightarrow V_{\text{sat}} &= -133.8 \text{ m} \\ M_6 \Rightarrow V_{\text{sat}} &= -134.9 \text{ m} \end{aligned}$$

$$M_7 \Rightarrow V_{\text{sat}} = 133.7 \text{ m}$$

$$M_8 \Rightarrow V_{\text{sat}} = 132.5 \text{ m}$$

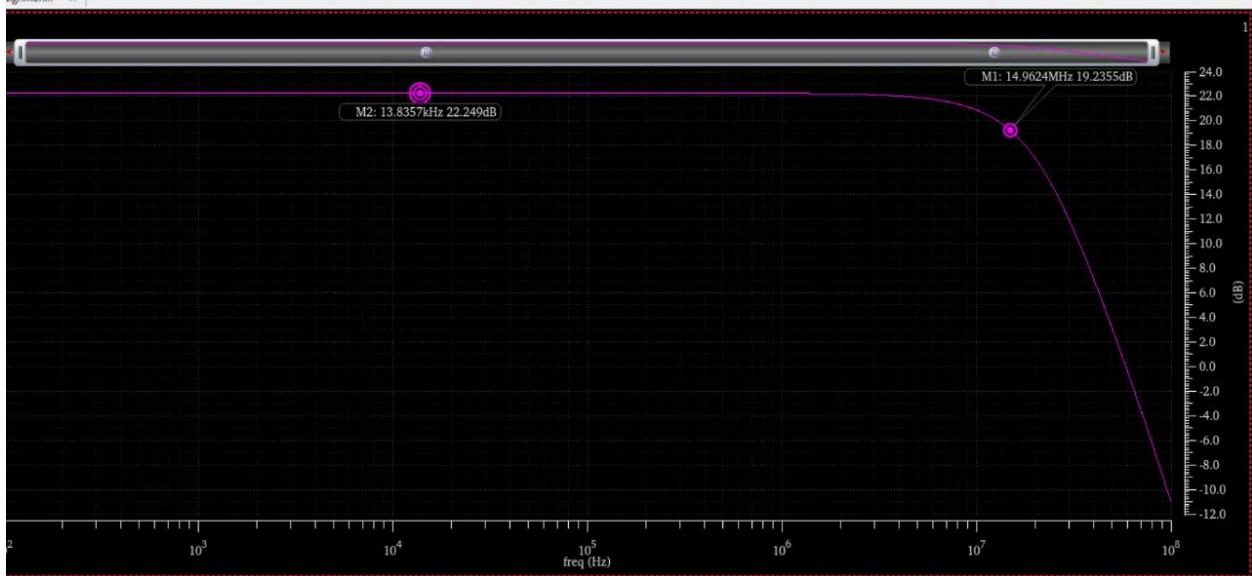
Plots

Loop gain Magnitude and phase



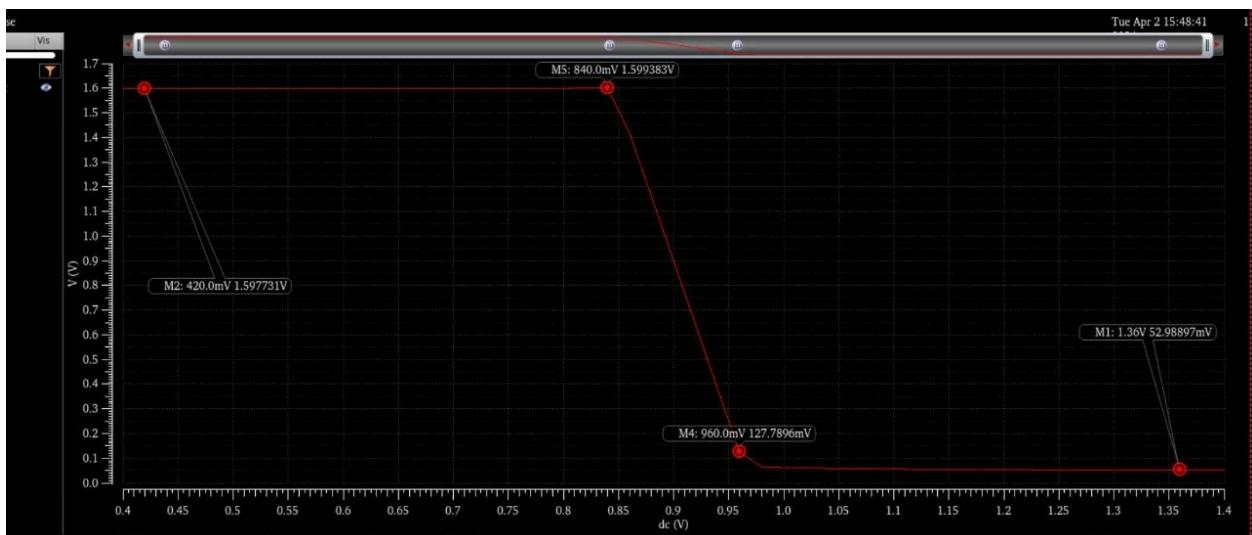
The observed unity loop gain frequency is close to 8.974MHz and the phase margin is 75 degree and the loop gain magnitude is 49.27 dB.

Closed Loop DC gain and Bandwidth



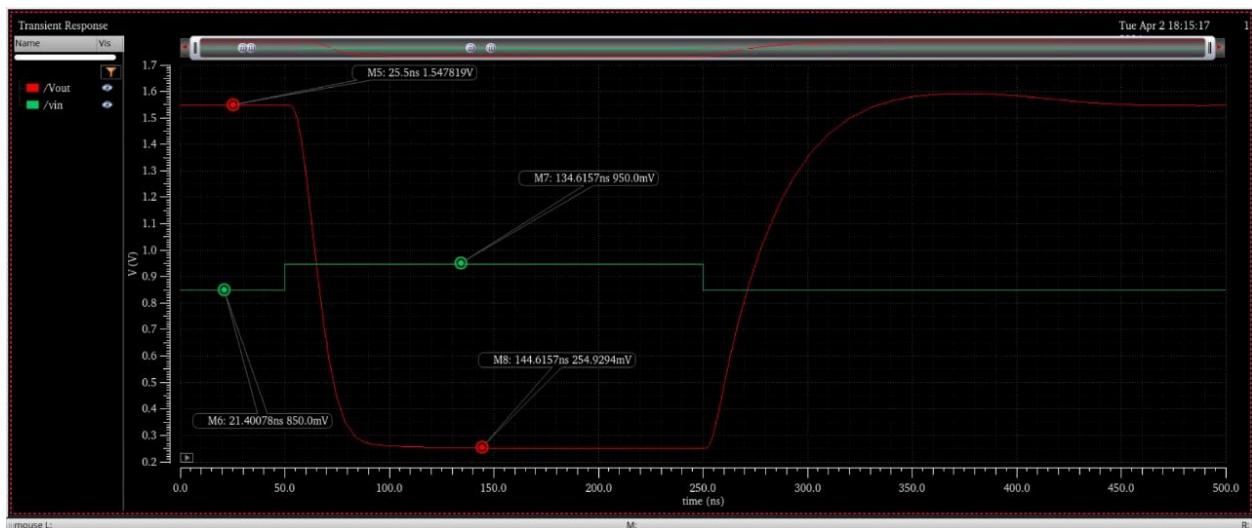
The DC gain observed over here is 22.249 dB, while the calculated gain is 22.27 dB, and the observed 3-dB bandwidth gain is 14.96 MHz which is quite off from the desired value of 13 MHz.

Closed Loop DC Transfer Curve



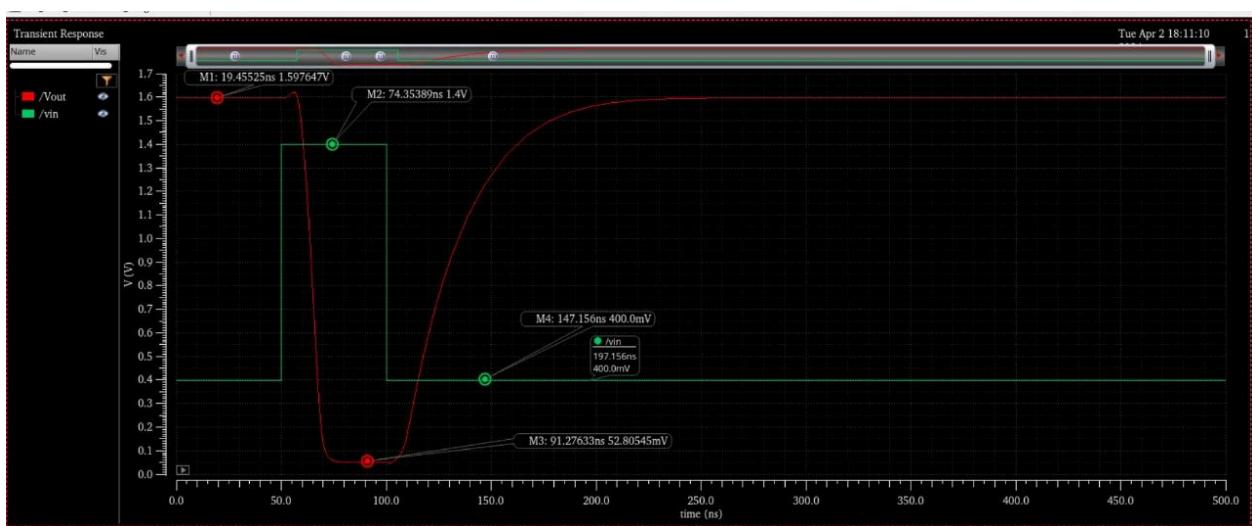
The x-axis represents the large-signal input voltage (V_i) which varies from $V_{cm}-0.5V=0.4$ V to $V_{cm}+0.5$ V=1.4 V. The y-axis shows the large signal output voltage which is observed to be in the range of 0.0529 V to 1.599 V (i.e., approximately from V_{ss} to V_{dd}). So, the opamp is observed to be linear in the range of small signal V_i equal to (840-900) to (960-900) mV i.e., from -60 mV to +60 mV. (As V_{cm} is equal to 900 mV).

Small Signal Step response



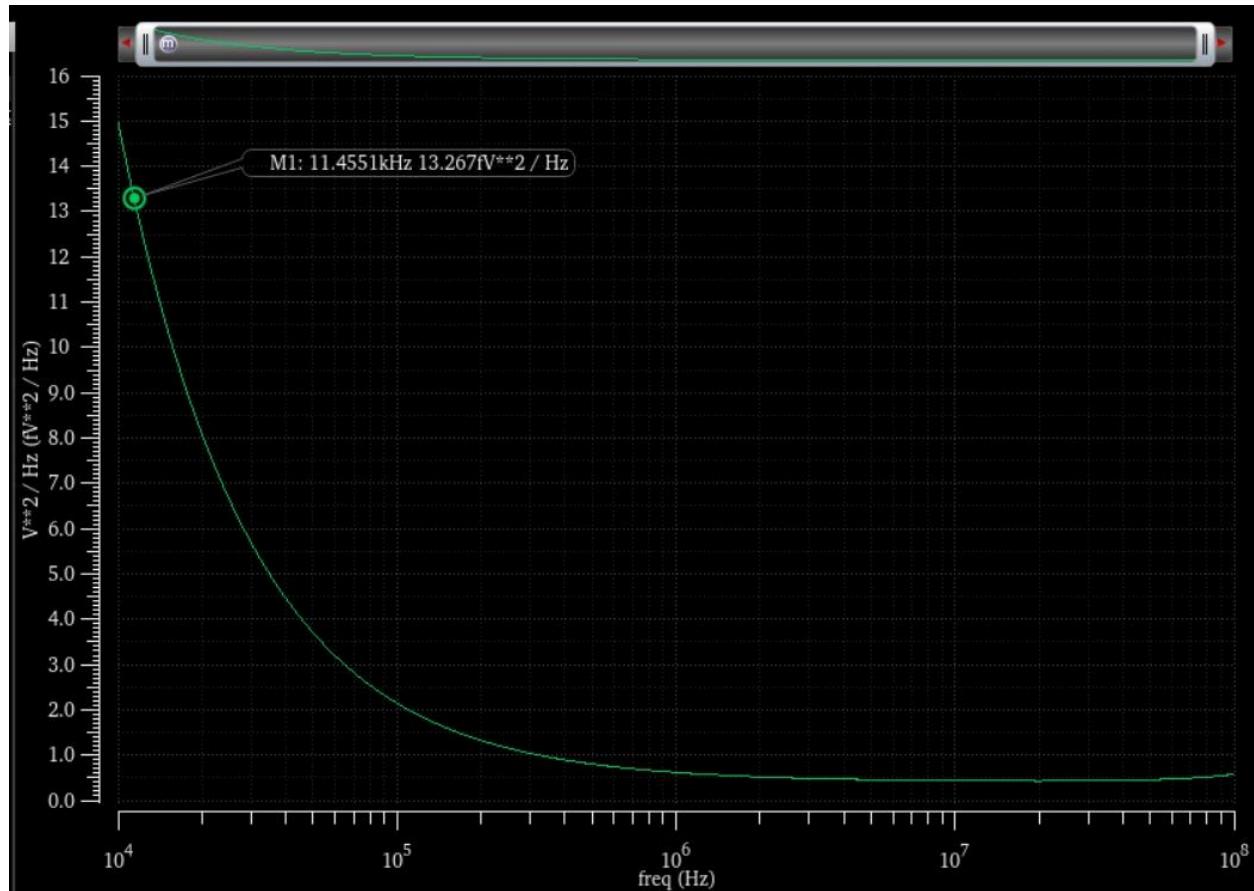
The small-signal step-response for input stepping from $(V_{cm}-0.05) = 0.85$ volts to $(V_{cm}+0.05) = 0.95$ volts . The rise time used for the step input is 100 ps.

Large Signal Step Response

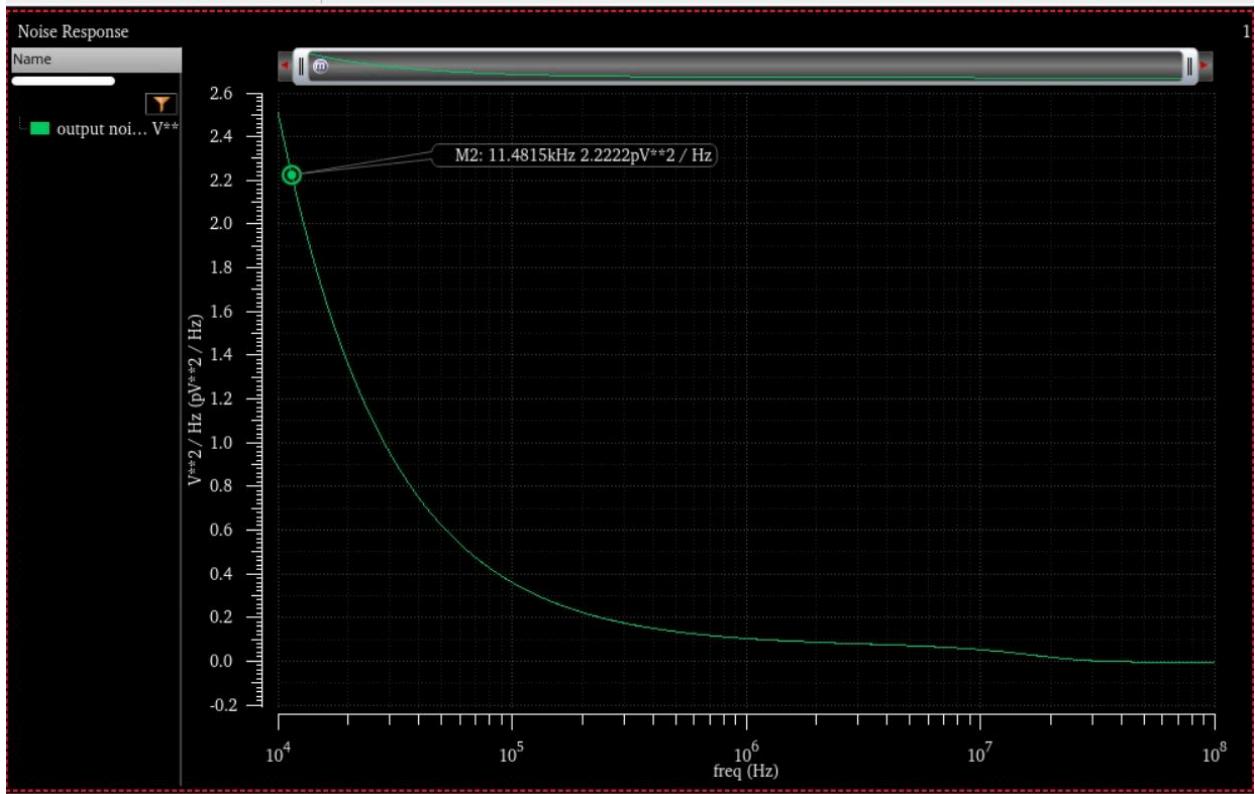


The large-signal step-response for input stepping from $(V_{cm}-0.5) = 0.4$ volts to $(V_{cm}+0.5) = 1.4$ volts . Here also the rise time used for the step input is equal to 100 ps.

Output Noise PSD and Input Noise PSD of the closed loop amplifier

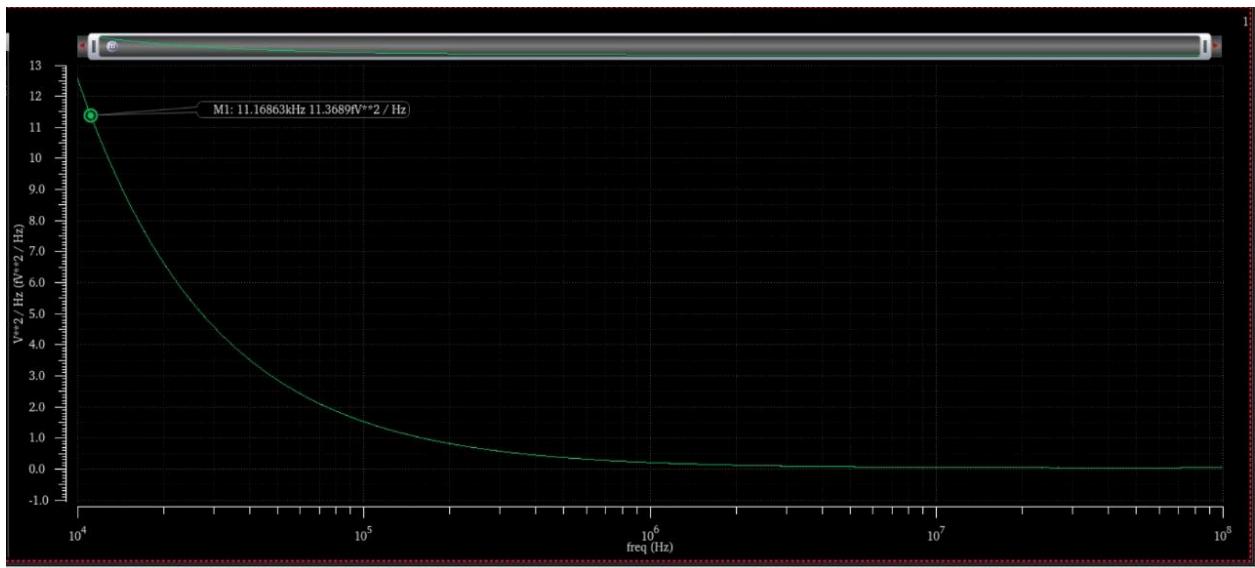


Input noise of the amplifier

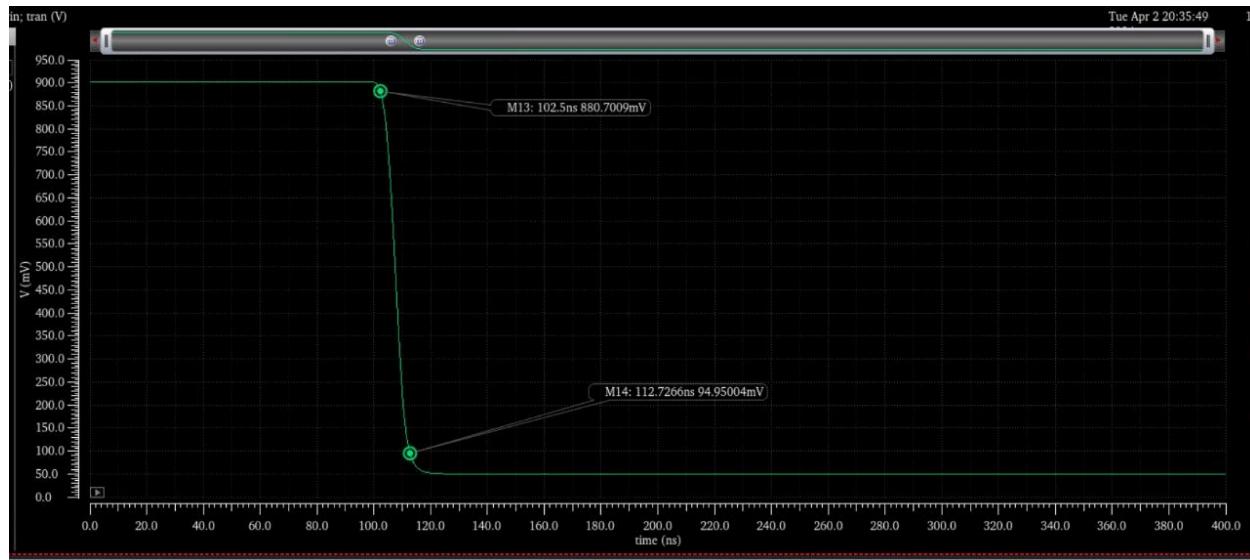


Output noise of amplifier

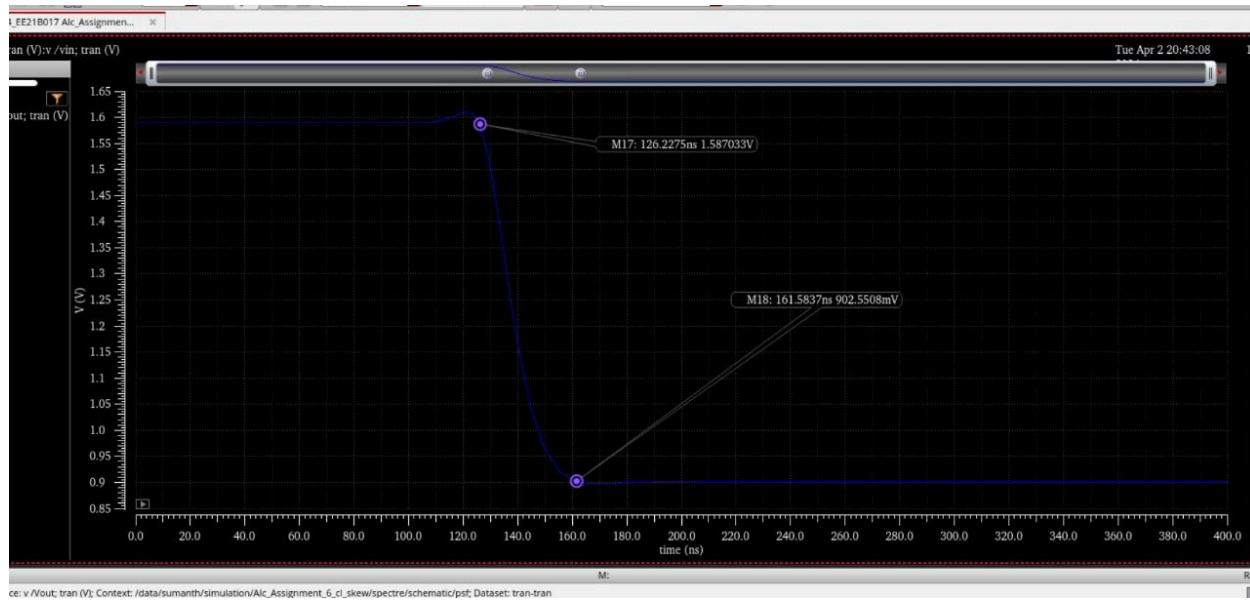
Input referred Noise PSD of the opamp



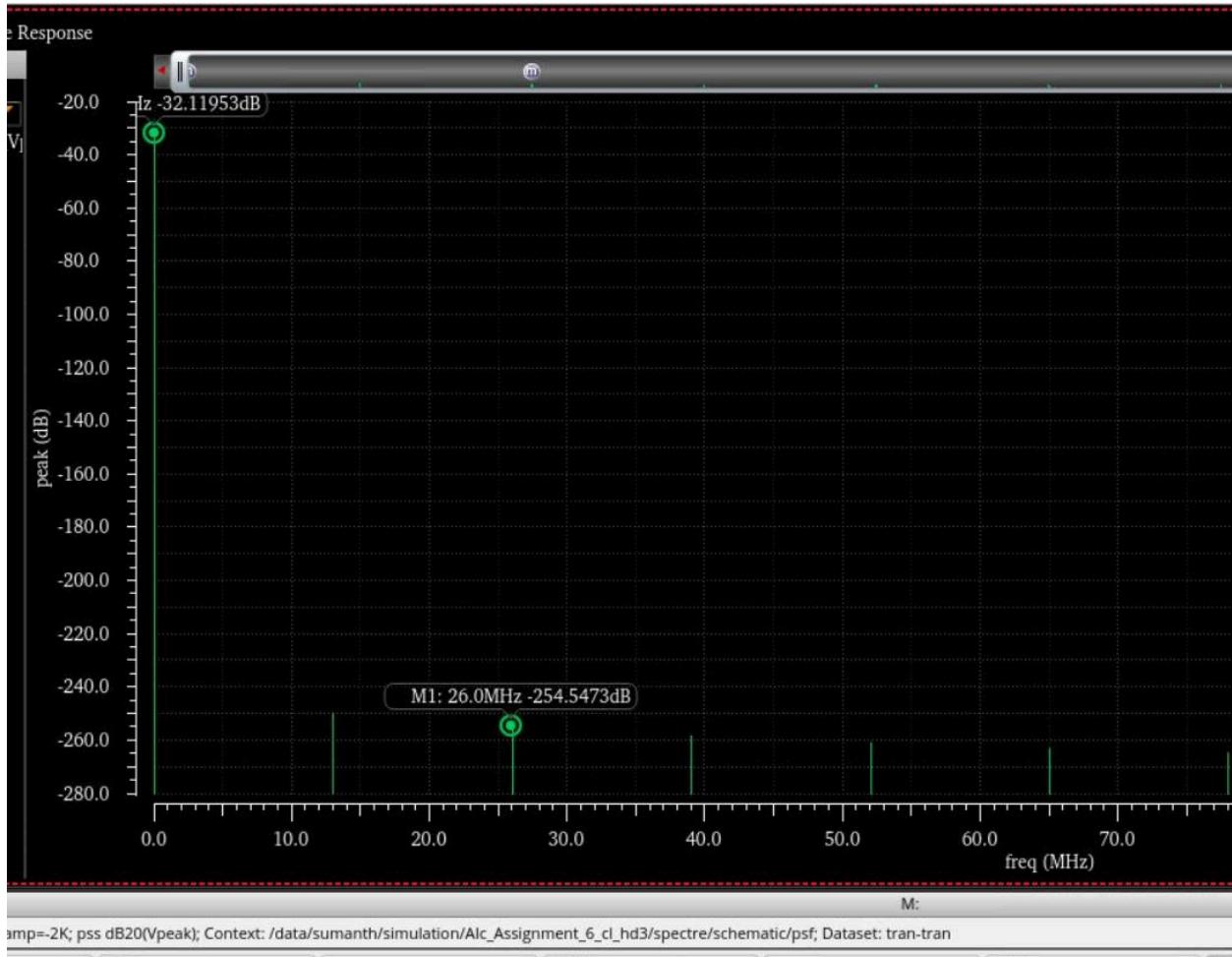
Negative Slew Rate Calculation (at Vstep=0.6 V)



Positive Slew Rate Calculation (at Vstep= -0.5 V)



HD3 Simulation



PSS Analysis for HD3