1. Description

1.1. Project

Project Name	ThBOT_Mainboard
Board Name	NUCLEO-F446ZE
Generated with:	STM32CubeMX 4.23.0
Date	11/20/2017

1.2. MCU

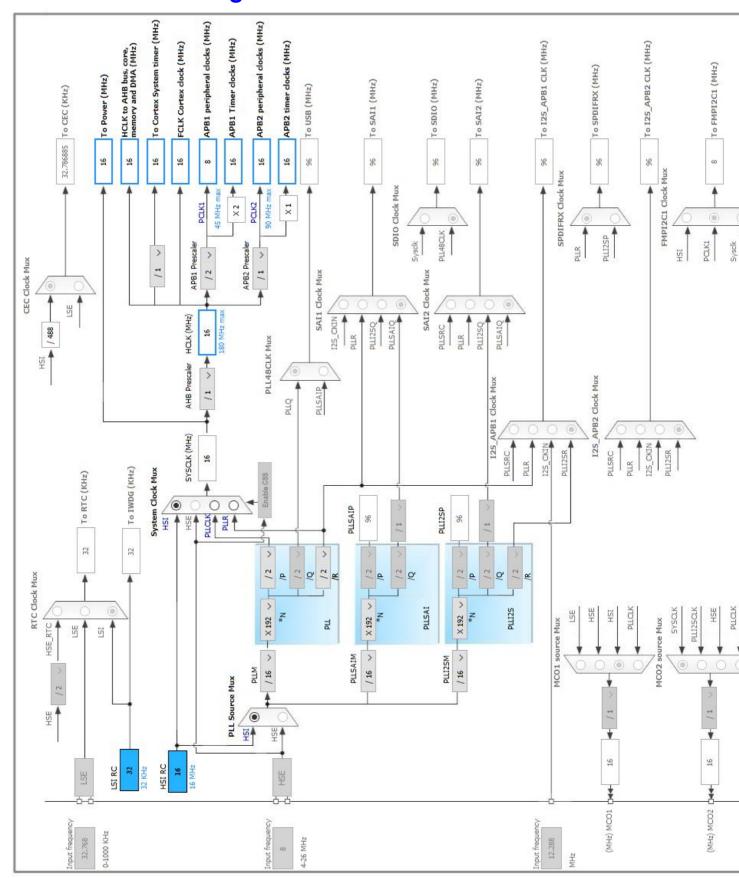|	
MCU Series	STM32F4
MCU Line	STM32F446
MCU name	STM32F446ZETx
MCU Package	LQFP144
MCU Pin number	144

2. Pinout Configuration

3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
7	PC13	I/O	GPIO_EXTI13	USER_Btn [B1]
8	PC14-OSC32_IN *	I/O	RCC_OSC32_IN	
9	PC15-OSC32_OUT *	I/O	RCC_OSC32_OUT	
16	VSS	Power		
17	VDD	Power		
23	PH0-OSC_IN *	I/O	RCC_OSC_IN	MCO [STM32F103CBT6_PA8]
24	PH1-OSC_OUT *	I/O	RCC_OSC_OUT	
25	NRST	Reset		
30	VDD	Power		
31	VSSA	Power		
32	VREF+	Power		
33	VDDA	Power		
34	PA0-WKUP	I/O	TIM5_CH1	ENCA_R
35	PA1	I/O	TIM5_CH2	ENCB_R
38	VSS	Power		
39	VDD	Power		
41	PA5	I/O	TIM2_CH1	ENCA_L
42	PA6	I/O	TIM3_CH1	PWM_L
46	PB0 **	I/O	GPIO_Output	LD1 [Green]
51	VSS	Power		
52	VDD	Power		
61	VSS	Power		
62	VDD	Power		
71	VCAP_1	Power		
72	VDD	Power		
75	PB14 **	I/O	GPIO_Output	LD3 [Red]
77	PD8 *	I/O	USART3_TX	STLK_RX [STM32F103CBT6_PA3]
78	PD9 *	I/O	USART3_RX	STLK_TX [STM32F103CBT6_PA2]
81	PD12	I/O	TIM4_CH1	PWM_R
83	VSS	Power		
84	VDD	Power		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
91	PG6 **	I/O	GPIO_Output	USB_PowerSwitchOn [STMPS2151STR_EN]
92	PG7 **	I/O	GPIO_Input	USB_OverCurrent [STMPS2151STR_FAULT]
94	VSS	Power		
95	VDDUSB	Power		
100	PA8 *	I/O	USB_OTG_FS_SOF	USB_SOF [TP1]
101	PA9 *	I/O	USB_OTG_FS_VBUS	USB_VBUS
102	PA10 *	I/O	USB_OTG_FS_ID	USB_ID
103	PA11 *	I/O	USB_OTG_FS_DM	USB_DM
104	PA12 *	I/O	USB_OTG_FS_DP	USB_DP
105	PA13 *	I/O	SYS_JTMS-SWDIO	TMS
106	VCAP_2	Power		
107	VSS	Power		
108	VDD	Power		
109	PA14 *	I/O	SYS_JTCK-SWCLK	TCK
120	VSS	Power		
121	VDD	Power		
130	VSS	Power		
131	VDD	Power		
133	PB3	I/O	TIM2_CH2	ENCB_L
137	PB7 **	I/O	GPIO_Output	LD2 [Blue]
138	BOOT0	Boot		
143	PDR_ON	Reset		
144	VDD	Power		

** The pin is affected with an I/O function

 * The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration

5. IPs and Middleware Configuration

5.1. SYS

Timebase Source: TIM1

5.2. TIM2

Combined Channels: Encoder Mode

5.2.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**4294967295 ***
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	Encoder Mode TI1
_____ Parameters for Channel 1 _____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
_____ Parameters for Channel 2 _____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

5.3. TIM3

Channel1: PWM Generation CH1

5.3.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**65535 ***
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	**1 ***
Fast Mode	Disable
CH Polarity	High

5.4. TIM4

Channel1: PWM Generation CH1

5.4.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**65535 ***
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	**1 ***
Fast Mode	Disable
CH Polarity	High

5.5. TIM5

Combined Channels: Encoder Mode

5.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**4294967295 ***
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	Encoder Mode TI1
_____ Parameters for Channel 1 _____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
_____ Parameters for Channel 2 _____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

5.6. FREERTOS

mode: Enabled

5.6.1. Config parameters:

Versions:

FreeRTOS version	9.0.0
CMSIS-RTOS version	1.02

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	**100 ***
MAX_PRIORITIES	7

MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Disabled
USE_COUNTING_SEMAPHORES	Disabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Enabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled

Memory management settings:

Memory Allocation	Dynamic
TOTAL_HEAP_SIZE	15360
Memory Management scheme	heap_4

Hook function related definitions:

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Disabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Disabled

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

5.6.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled

vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	Disabled
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Disabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Disabled
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	Disabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Disabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled

* User modified value

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
TIM2	PA5	TIM2_CH1	Alternate Function Push Pull	**Pull-up ***	Low	ENCA_L
	PB3	TIM2_CH2	Alternate Function Push Pull	**Pull-up ***	Low	ENCB_L
TIM3	PA6	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM_L
TIM4	PD12	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM_R
TIM5	PA0-WKUP	TIM5_CH1	Alternate Function Push Pull	**Pull-up ***	Low	ENCA_R
	PA1	TIM5_CH2	Alternate Function Push Pull	**Pull-up ***	Low	ENCB_R
Single Mapped Signals	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	MCO [STM32F103CBT6_PA8]
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
	PD8	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	STLK_RX [STM32F103CBT6_PA3]
	PD9	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	STLK_TX [STM32F103CBT6_PA2]
	PA8	USB_OTG_FS_SOF	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	USB_SOF [TP1]
	PA9	USB_OTG_FS_VBUS	Input mode	No pull-up and no pull-down	**n/a**	USB_VBUS
	PA10	USB_OTG_FS_ID	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	USB_ID
	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	USB_DM
	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	USB_DP
	PA13	SYS_JTMS-SWDIO	n/a	n/a	**n/a**	TMS
	PA14	SYS_JTCK-SWCLK	n/a	n/a	**n/a**	TCK
GPIO	PC13	GPIO_EXTI13	External Interrupt Mode with	No pull-up and no pull-down	n/a	USER_Btn [B1]

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
			Rising edge trigger detection			
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD1 [Green]
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD3 [Red]
	PG6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	USB_PowerSwitchOn [STMPS2151STR_EN]
	PG7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	USB_OverCurrent [STMPS2151STR_FAULT]
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD2 [Blue]

6.2. DMA configuration

nothing configured in DMA service

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
TIM1 update interrupt and TIM10 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM2 global interrupt	unused		
TIM3 global interrupt	unused		
TIM4 global interrupt	unused		
EXTI line[15:10] interrupts	unused		
TIM5 global interrupt	unused		
FPU global interrupt	unused		

* User modified value

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F4
Line	STM32F446
MCU	STM32F446ZETx
Datasheet	027107_Rev6

7.2. Parameter Selection

Temperature	25
Vdd	3.6

8. Software Project

8.1. Project Settings

Name	Value
Project Name	ThBOT_Mainboard
Project Folder	C:\CBot\workspace\ThBOT_Mainboard
Toolchain / IDE	SW4STM32
Firmware Package Name and Version	STM32Cube FW_F4 V1.17.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No