**Digital IC Design Project 01**

Design of 4:16 Decoder for Speed

**In this project we will design a 4:16 decoder similar to the one described in the “Logical Effort for Paths”**

**lecture and in Section 4.5.3 in the textbook (Weste and Harris).**

# Specifications

1. Use static CMOS logic.
2. A unit size transistor is defined as 𝑊 = 𝑊𝑚𝑖𝑛 and 𝐿 = 𝐿𝑚𝑖𝑛. For 45nm PDK, use Wmin = 120nm and Lmin = 45nm.
3. True and complementary address inputs A]3:0[ are considered.
4. Each input may drive 10 unit-sized transistors.
5. **The target is to maximize the speed (minimum propagation delay).**

# Design: NAND4-INV

2

# Logical Effort: G =

GBH = 153.61

# Path Effort: F =

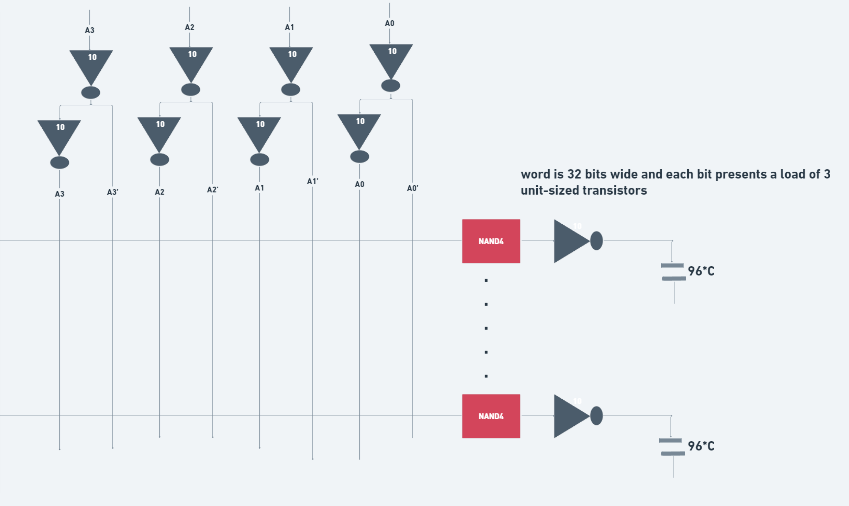
# Branching Effort: B = 8

# Stage Effort:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Design | N | G | P | D | 𝒇𝒐𝒑𝒕 |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| NAND4-INV | 2 | 2 | 5 | 29.8 | 12.39 |

# Path Delay: *D* 



# Design: INV-NAND4-INV

3

# Logical Effort: G =

GBH = 154

# Path Effort: F =

# Branching Effort: B = 8

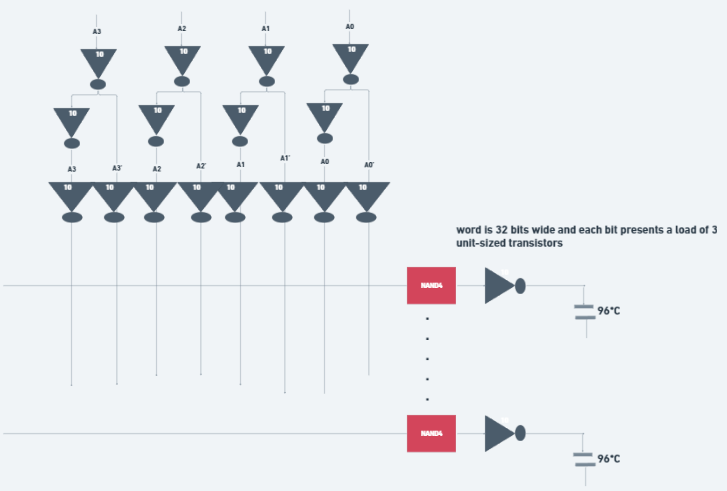
# Stage Effort:

3*f*ˆ  1 +4+1= 22.1

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Design | N | G | P | D | 𝒇𝒐𝒑𝒕 |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| INV -NAND4-INV | 3 | 3 | 6 | 22.1 | 5.36 |

# Path Delay: *D* 



# Design: NOR4

1

# Logical Effort: G =

GBH = 230.4

# Path Effort: F =

# Branching Effort: B = 8

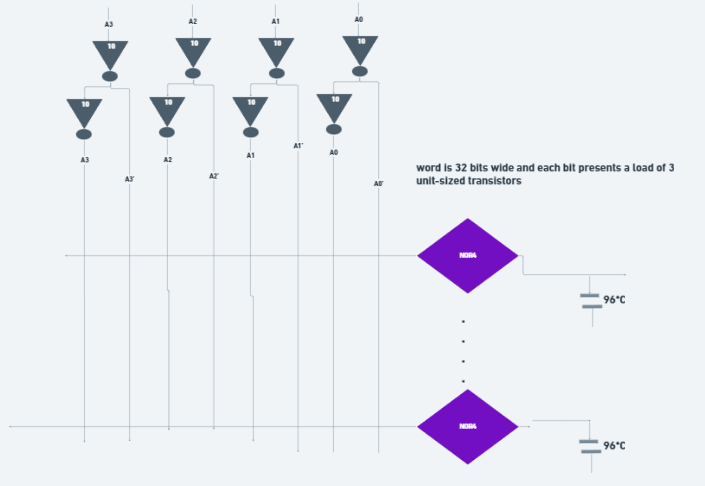
# Stage Effort:

234.4

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Design | N | G | P | D | 𝒇𝒐𝒑𝒕 |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| NOR4 | 1 | 3 | 4 | 234.4 | 230.4 |

# Path Delay: *D* 



# Design: NAND2-INV-NAND2-INV

16/9

# Logical Effort: G =

GBH = 136.53

# Path Effort: F =

# Branching Effort: B = 8

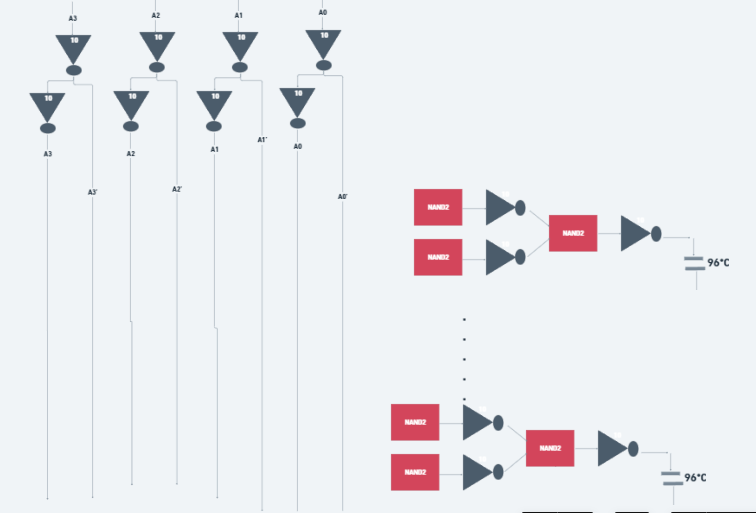
# Stage Effort:

19.7

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Design | N | G | P | D | 𝒇𝒐𝒑𝒕 |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| NAND2-INV-NAND2-INV | 4 | 16/9 | 6 | 19.7 | 3.42 |

# Path Delay: *D* 



# Design: NAND4-INV-INV-INV

2

# Logical Effort: G =

GBH = 153.6

# Path Effort: F =

# Branching Effort: B = 8

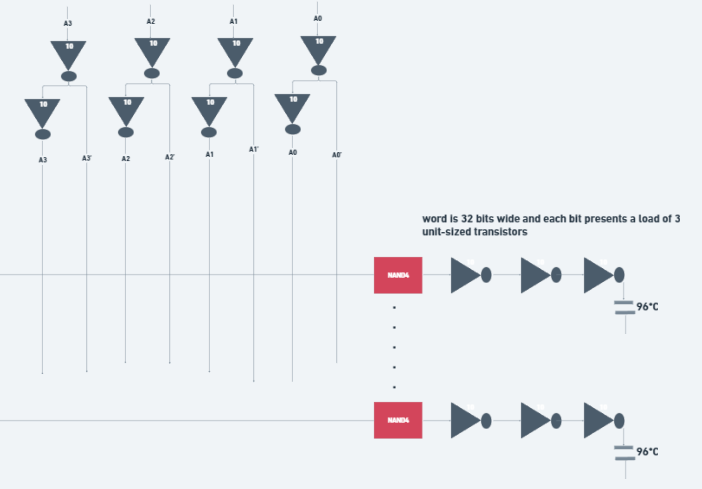
# Stage Effort:

21.1

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Design | N | G | P | D | 𝒇𝒐𝒑𝒕 |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| NAND4-INV-INV-INV | 4 | 2 | 7 | 21.1 | 3.52 |

# Path Delay: *D* 



# Design: INV-NAND4-INV-INV-INV

16/9

# Logical Effort: G =

GBH = 136.53

# Path Effort: F =

# Branching Effort: B = 8

# Stage Effort:

20.4

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Design | N | G | P | D | 𝒇𝒐𝒑𝒕 |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| NAND4-INV-INV-INV | 5 | 16/9 | 7 | 20.4 | 2.67 |

# Path Delay: *D* 

# So

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Design** | **N** | **G** | **P** | **D** | 𝒇𝒐𝒑𝒕 |
| NOR4 | 1 | 3 | 4 | 234 | 230.40 |
| NAND4-INV | 2 | 2 | 5 | 29.8 | 12.39 |
| NAND2-NOR2 | 2 | 20/9 | 4 | 30.1 | 13.06 |
| INV-NAND4-INV | 3 | 2 | 6 | 22.1 | 5.36 |
| NAND4-INV-INV-INV | 4 | 2 | 7 | 21.1 | 3.52 |
| NAND2-NOR2-INV-INV | 4 | 20/9 | 6 | 20.5 | 3.61 |
| NAND2-INV-NAND2-INV (Best Speed Design) | 4 | 16/9 | 6 | 19.7 | 3.42 |
| INV-NAND2-INV-NAND2-INV | 5 | 16/9 | 7 | 20.4 | 2.67 |
| NAND2-INV-NAND2-INV-INV-INV | 6 | 16/9 | 8 | 21.6 | 2.27 |

Select the fastest design and size the gates appropriately. Explain your sizing method.

# NAND2-INV-NAND2-INV is the best design for speed but have large area and power consumption since the 4 stages. Our sizing method is to increase the speed of each gate in the whole design by make them hold the highest driving strength as much as it can by increase the width but increase it by fingers so we reduce the diffusion and parasitic capacitance and increase the current so we expect high speed design therefore the maximum possible width is Kn=5, Kp=10.

Schematics of each stage (gate) showing sizing of transistors. Explain your sizing method.

# Schematic of the NAND2-INV-NAND2-INV block as NAND4 but highly optimized

# Schematic of the inverter

# PMOS device properties:

# Minimum Length used = 45n M

# Minimum Width used as a reference as a unit inverter = 120n M

# User FP as parameter for the fingers of PMOS.

# NMOS device properties:

# Minimum Length used = 45n M

# Minimum Width used as a reference as a unit inverter = 120n M

# Used FN as parameter for the fingers of NMOS.

# Inverter Symbol

# NAND2 Schematic & Symbol

# 

# 

# So FP=10, FN=5

# 

# 

# Therefore NAND2-INV-NAND2-INV ‘s Symbol:

# Schematic of the whole decoder (cell-based)

# 

# Symbol of the whole decoder:

# If we test this design without wordline load so:

# Add Vpulse of properties for each input:

# 

# So: First test case: 0010 >> M2 = 1

# 

# If we try to calculate the propagation delay:

# Deliverables

|  |  |  |
| --- | --- | --- |
| **Index** | **Deliverable** | **Points** |
| 1 | **Normalized** delay vs h plot for each of the following gates (INV, NAND2, NAND4, NOR2, NOR4). Consider ONLY the worst-case input of the gate. Justify your  selection. | 5 |
| 2 | 𝑝 for each gate extracted from the plot (INV, NAND2, NAND4, NOR2, NOR4) | 5 |
| 3 | 𝑔 for each gate extracted from the plot (INV, NAND2, NAND4, NOR2, NOR4) | 5 |
| 6 |  | 4 |
| 7 |  | 4 |
| 8 | Schematic of your testbench. The design should be in a single cell. Use two FO4  inverters to shape each input and load each output of the design. Do NOT include the power and delay of these FO4 inverters. | 4 |
| 9 | Transient simulation showing the operation of the decoder for all different input  combinations (define your inputs as clocks with binary weighted periods) | 20 |
| 10 | Try to identify the path and **input transition** that has the worst-case delay. Justify  your answer. Note that input ordering may affect the delay. | 4 |
| 11 | Transient simulation showing the worst-case delay. | 4 |
| 12 | Compare the worst-case delay simulation result with the hand analysis result  estimated by logical effort. Comment on the result. | 2 |
| 13 | Transient simulation showing transient power consumption and average power  consumption. | 2 |
| 14 | [**Optional**] Estimate the dynamic power consumption analytically. Assume activity factor for all inputs is 0.5. Draw the logic diagram indicating the activity factor after each stage.  Hint: You may get a rough estimate of 𝐶𝑔𝑔 and 𝐶𝑑𝑑 from operating point (OP)  simulation (a more accurate method can be found in Section 8.4.3 in the textbook). | 0 |
| 15 | [**Optional**] Compare the power consumption simulation result with the hand analysis result. Comment on the comparison result. What should be the overall  effective activity factor such that the two results match? Comment. | 0 |
| 16 | Estimate the area of the design. Just consider the area of the transistors for  simplicity: ∑ 𝑊 ∗ (2 ∗ 𝐿𝐷 + 𝐿). | 4 |
| 17 | Summarize the key performance metrics of your design in a table. Include the following in the table: Delay (delay in ps and in units of FO4), Max Speed, Power, Area, Power-Delay Product (PDP) (i.e., Energy), Energy-Delay Product (EDP), and  Area-Delay Product. | 4 |
| 18 | [**Optional**] The layout of the whole decoder. Snapshots showing that the layout is  DRC clean and LVS clean. | 0 |
| Total | | 80 |

Thanks to all who contributed to these labs. If you find any errors or have suggestions concerning these labs, please contact [Hesham.omran@eng.asu.edu.eg.](mailto:Hesham.omran@eng.asu.edu.eg)

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