Cairo University
Faculty of Engineering

Department of Electronics and
Communications Engineering

Project deadline: Wednesday May 15th , 2024

For the 3 tasks, use the PDK of a UMC 0.13µm technology:

Task #1 (10 marks):

For an NMOS with Drain and Gate connected to VDD = 1.2V and Source connected to a current source $IREF$ = 200μA to GND and Bulk connected to GND. Fix L=Lmin and sweep W from W=L to W=100L. Plot the following for N_12_HS_L130E (high-speed NMOS) and N_LV_12_HS_L130E (Low-Vth high-speed NMOS) transistors:

1. VTH versus W/L (1 mark)

2. Vov (VGS-VTH) versus W/L & VDSAT versus W/L, is VDSAT=VGS-VTH? (2 marks)

3. gm.ro versus W/L (1 mark)

4. Repeat for L=2Lmin, L=4Lmin , L=8Lmin and L=16Lmin (plot the 5 curves for different values of L for each of the required parameters mentioned above in the same figure). (2 marks)

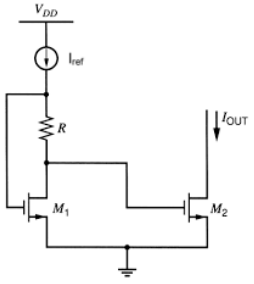
5. Mention the long channel equation for each of the above simulated parameters. Is the trend of the simulations similar to the equations? (1 mark)

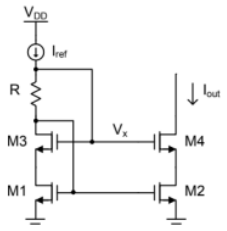
6. Mention one advantage and one disadvantage for N_LV_12_HS_L130E compared to N_12_HS_L130E. What do you recommend to be used in a high-gain amplifier? (3 mark)

Task #2 (10 marks): Use the NMOS core high speed HS transistor (N_12_HS_L130E) and the poly resistor (RNPPO_MML130E) to design the two following current mirrors to compare between them (according to the architecture shown) operating at VDD = 1.2V with the following specifications:

$Iout$ = 2$IREF$ = 200μA, with error < 1% @Vout=500mV

- $Vcomp$ ≤ 350mV (defined as the minimum output voltage required for all devices to operate in saturation)
- $Rout$ ≥ 500kΩ @ $Vout$ = 500mV





The documentation of your design must include the following:

1. Schematic diagram with dimensions and component values annotated for both circuits. (1 mark)

2. Schematic diagram with DC operating point annotated at Vout=350mV to verify the Vcomp specification for both circuits. (2 marks)

3. Simulation results to verify Iout and $Rout$ specifications for both circuits.(2 marks)

4. An estimate of this mirror's area for both circuits. (1 mark)

5. If your manager told you the area you ended up with is too large and you need to sacrifice one of the specs to have reasonable area, suggest a modification and comment on what you'll gain and lose from it (Discuss this point for both designs separately). (1 mark)

6- Compare both designs in a table by adding the analyzed results with the simulated results for both designs.(1 mark)

7- Discuss the circuits at which each circuit is more suitable to be used. (1 mark)

8- Draw and estimate the noise of both circuits and define which devices are more dominant in the total noise. (1 mark)

Task #3 (10 marks): Use the NMOS core high voltage RF transistor (N_33_RF), an ideal current source, and an ideal DC blocking cap of 1µF to design a class A Power Amplifier (according to the architecture shown) operating at VDD = 3.3V with the following specifications:

▪ Vin,DC = 2.3V

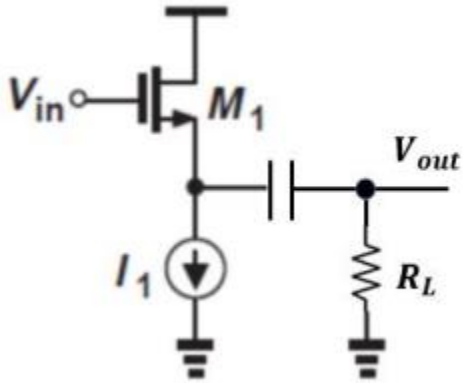
▪ Vin,AC = A sin(2πft) , f = 60MHz, A = 0.8V

▪ RL = 50Ω ▪ $|Vout,peak|$ > 600mV

▪ Output signal linearity is characterized as

$|Vout,max|-|Vout,min|$ $Vout,max$ < 2.5%

The documentation of your design must include the following:



1. Schematic diagram with dimensions and component values annotated. (1 mark)

2. Schematic diagram with DC operating point annotated. (1 mark)

3. Transient simulation results to verify the required specifications:

   a. Plot a complete period of Vout vs time at the given frequency. (1 mark)

   b.Plot a complete period of the current flowing in the main device to make sure the device doesn't turn off. (1 mark)

4. Calculation of the efficiency using simulations and compare it with the theoretical equation. (2 marks) 5. Replace the ideal current source with a current mirror with $IREF$ = 10mA using N_33_RF device, design the mirror using a suitable topology of your choice, and plot $Vout$ and $Imain\ device$. Did the linearity degrade? Why/why not? (4 marks)

Assessment:

- The total grade of this project is 30 points.
- Maximum number of students per group is 3.
- You are required to deliver a pdf report that clearly describes your work, including all the required items.
- Any missing requirement from the final report will be penalized in the final grading.
- Every day late = (-10%) from the assignment points.
- Any copied report will take ZERO.