EECE - Faculty of Engineering

Cairo University

Electronics Project (Cadence)
ELC2060_PROJECT

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Task #1

For an NMOS with Drain and Gate connected to VDD = 1.2V and Source connected to a current source IREF =
200µA to GND and Bulk connected to GND. Fix L=LMIN and sweep W from W=L to W=100L. Plot the following for
N_12_HS_L130E (high-speed NMOS) and N_LV_12_HS_L130E (Low-Vth high-speed NMOS) transistors:

1. VTH versus W/L

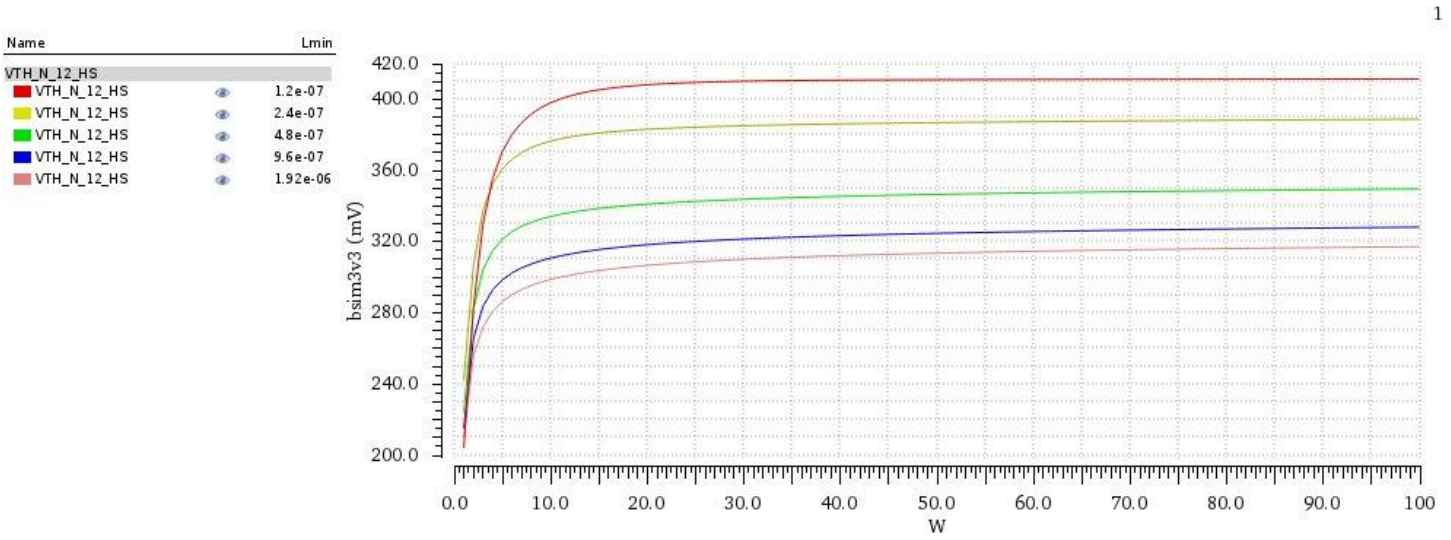


Figure 1: VTH versus W/L using N_12_HS_L130E

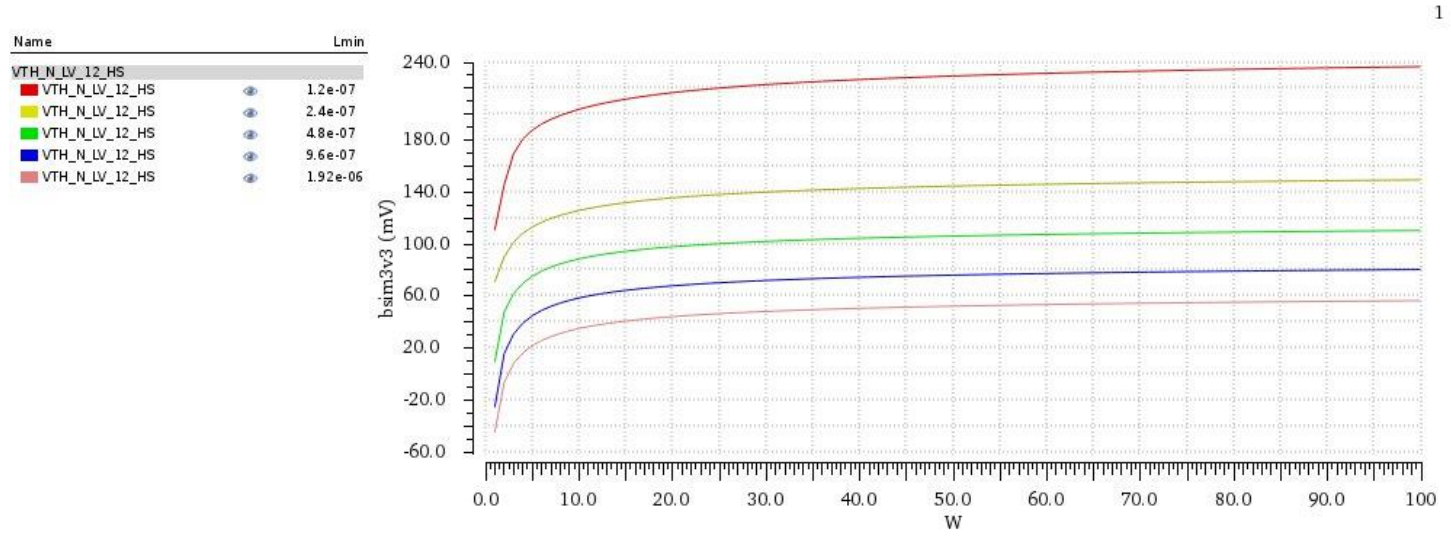


Figure 2: VTH versus W/L using N_LV_12_HS_L130E

2. Vov (VGS-VTH) versus W/L

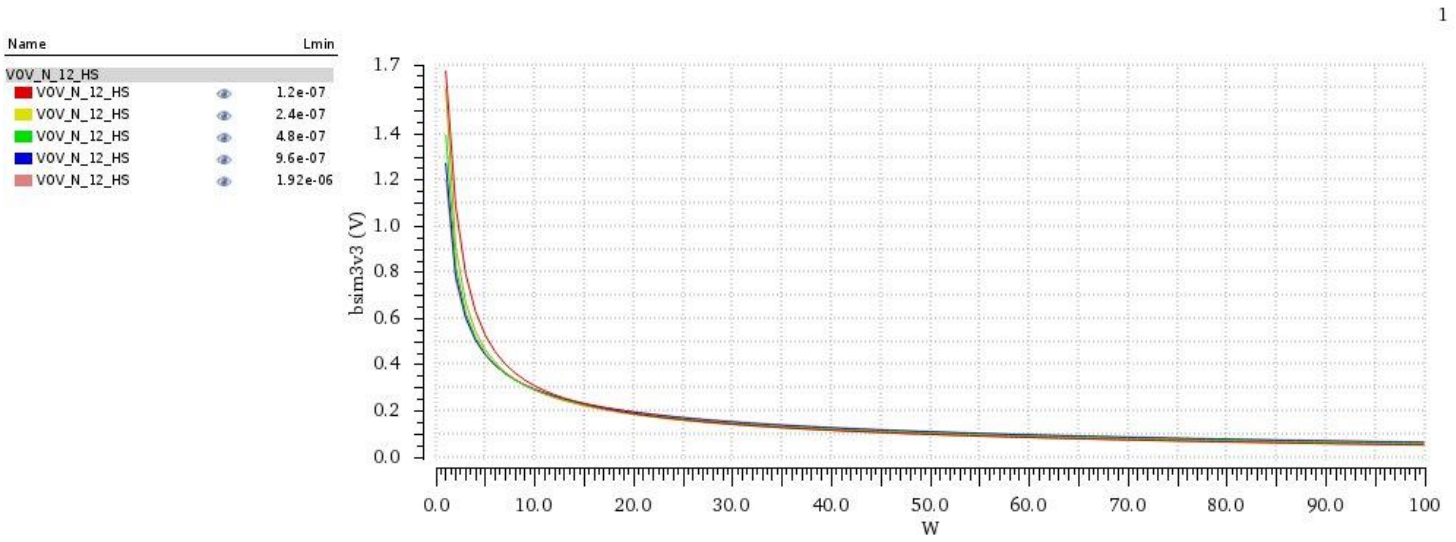


Figure 3: Vov versus W/L using N_12_HS_L130E

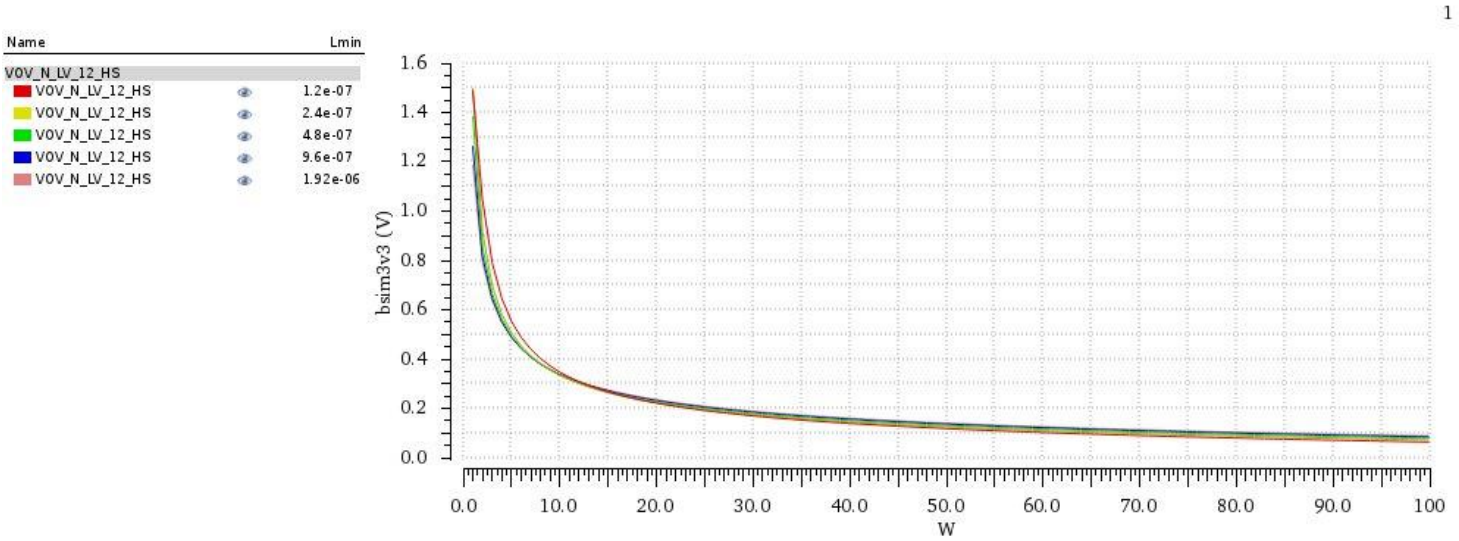
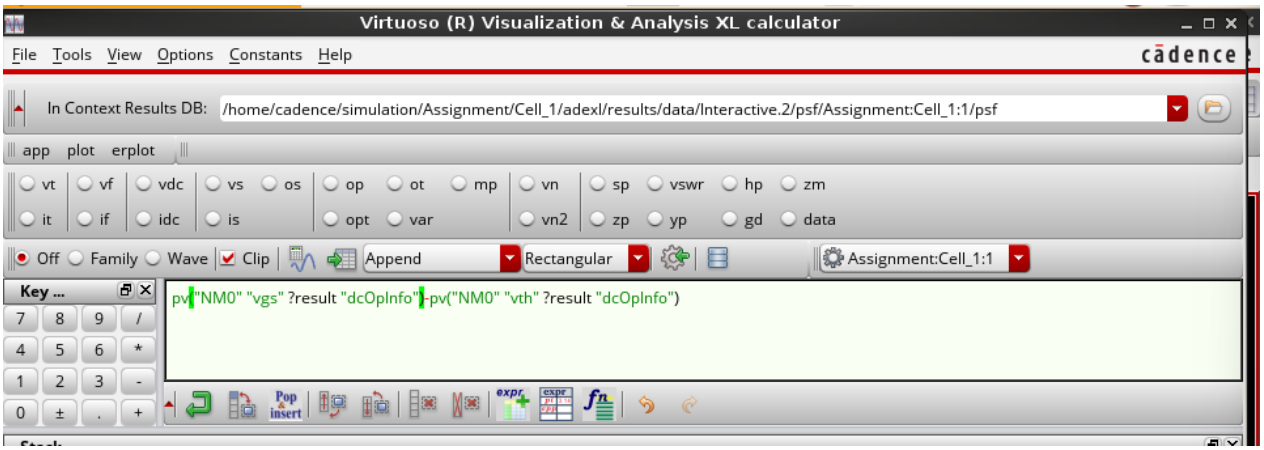


Figure 4: Vov versus W/L using N_LV_12_HS_L130E



Equation of Vov

VDSAT (VGS-VTH) versus W/L

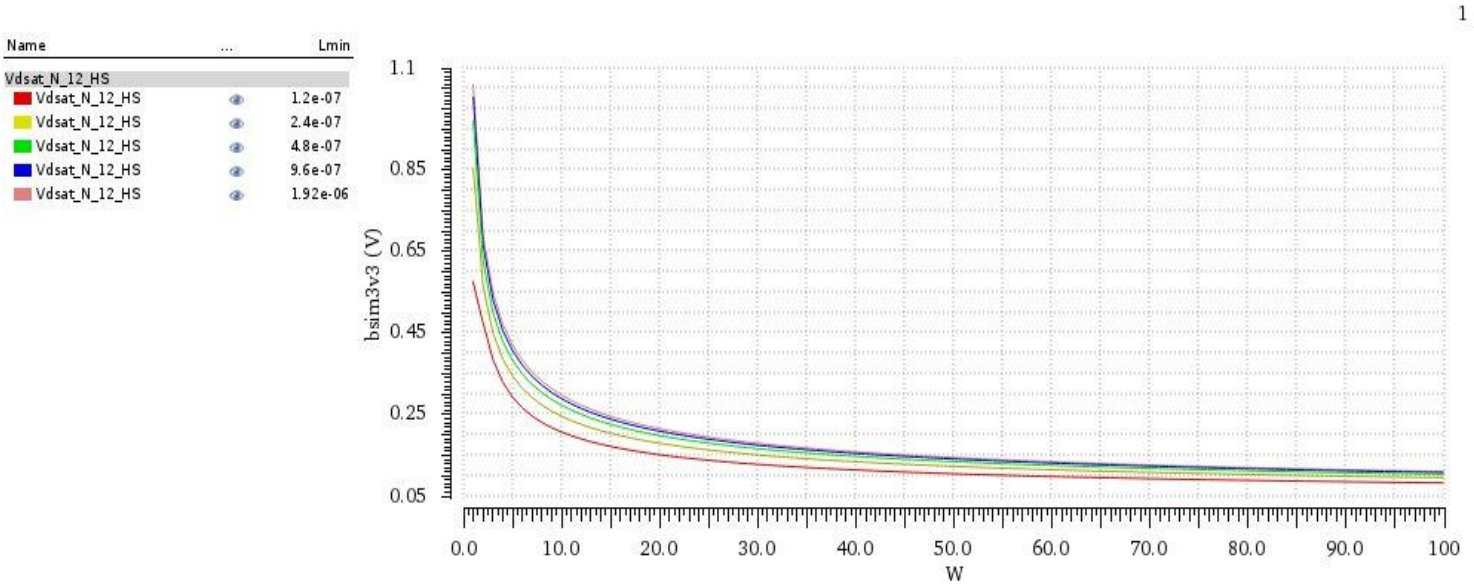


Figure 6: VDSAT versus W/L using N_12_HS_L130E

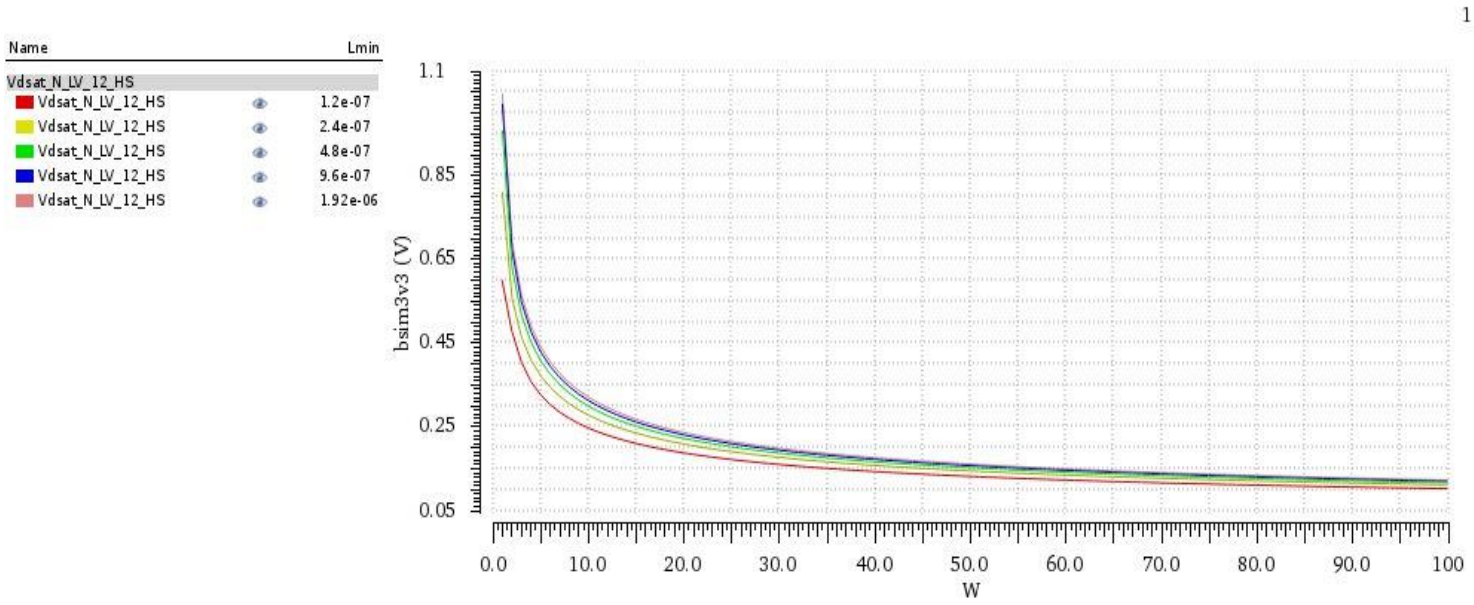


Figure 5: VDSAT versus W/L using N_LV_12_HS_L130E

- **Is VDSAT=VGS-VTH?**

No, because square law isn't correct 100% because there is approximations
and also there are many other reasons like modeling complexity, Tempreature effects, simulation conditions, and Model accuracy

3. gm.ro versus W/L

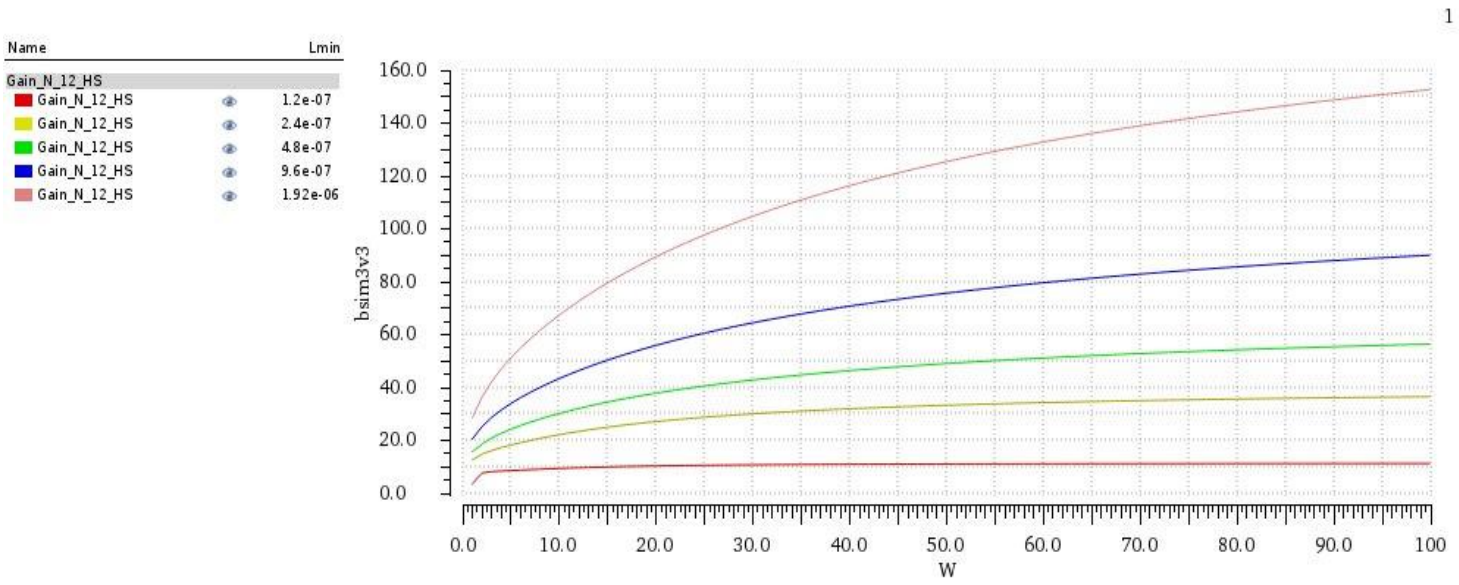


Figure 7: Gain versus W/L using N_12_HS_L130E

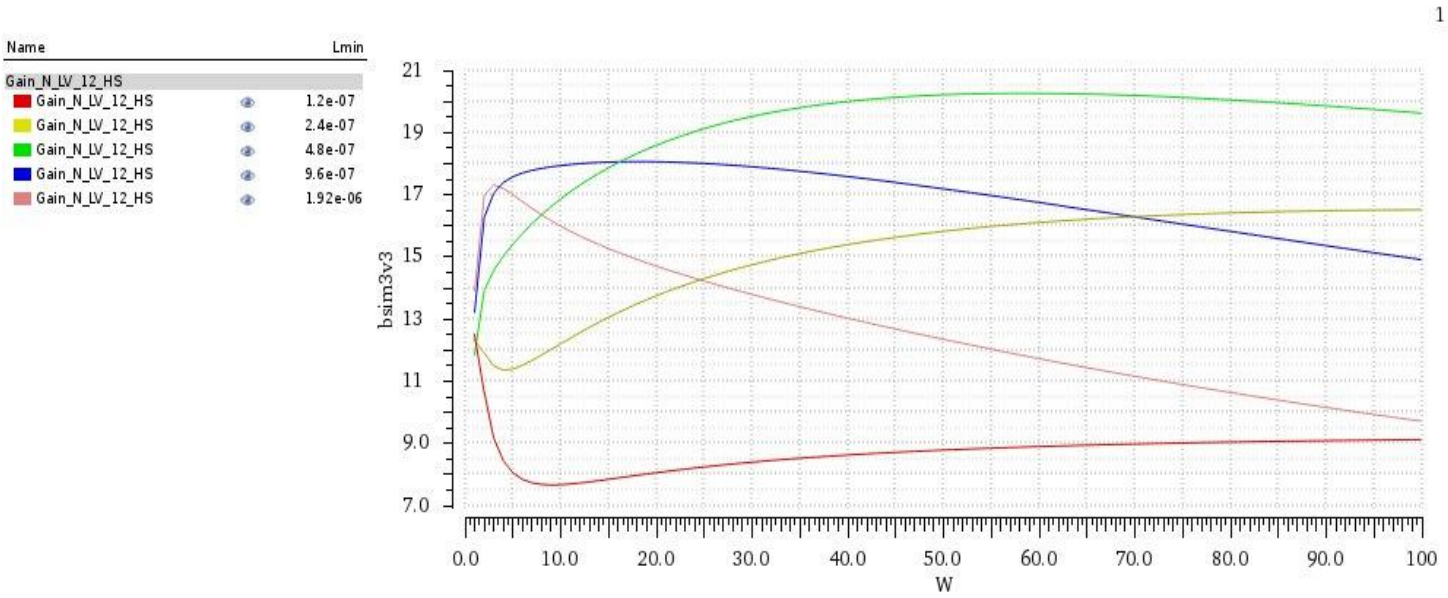
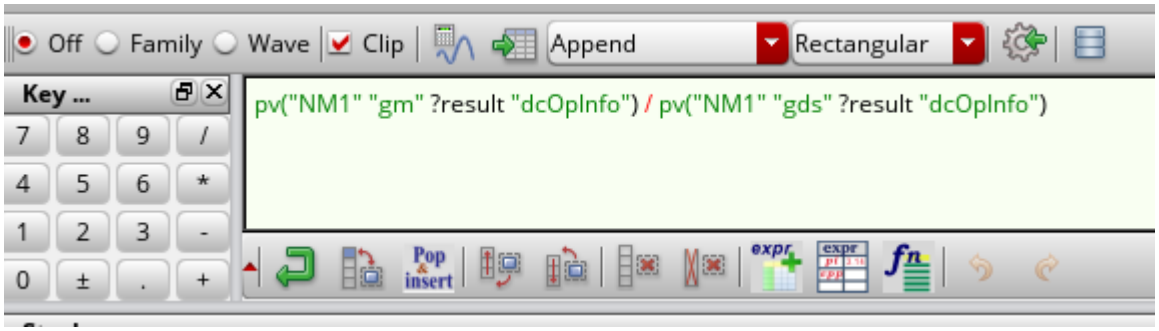


Figure 8: Gain versus W/L using N_LV_12_HS_L130E



equation of gmro

gm versus W/L

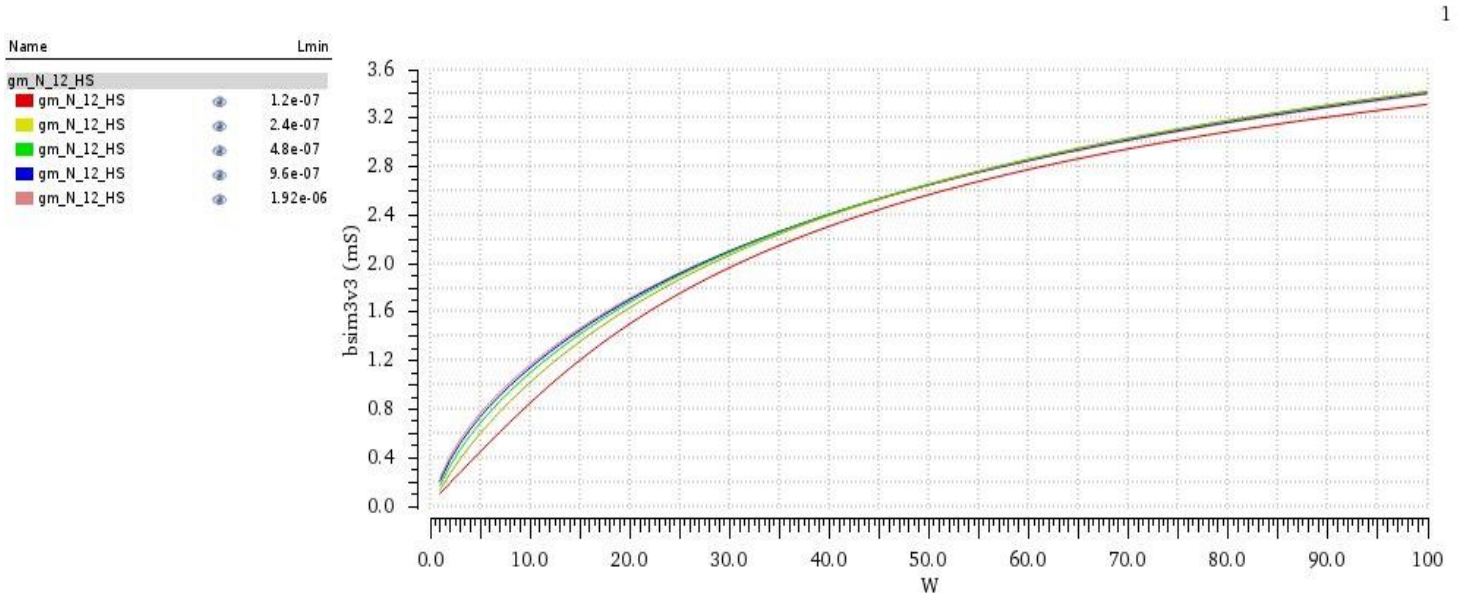


Figure 9: gm versus W/L using N_12_HS_L130E

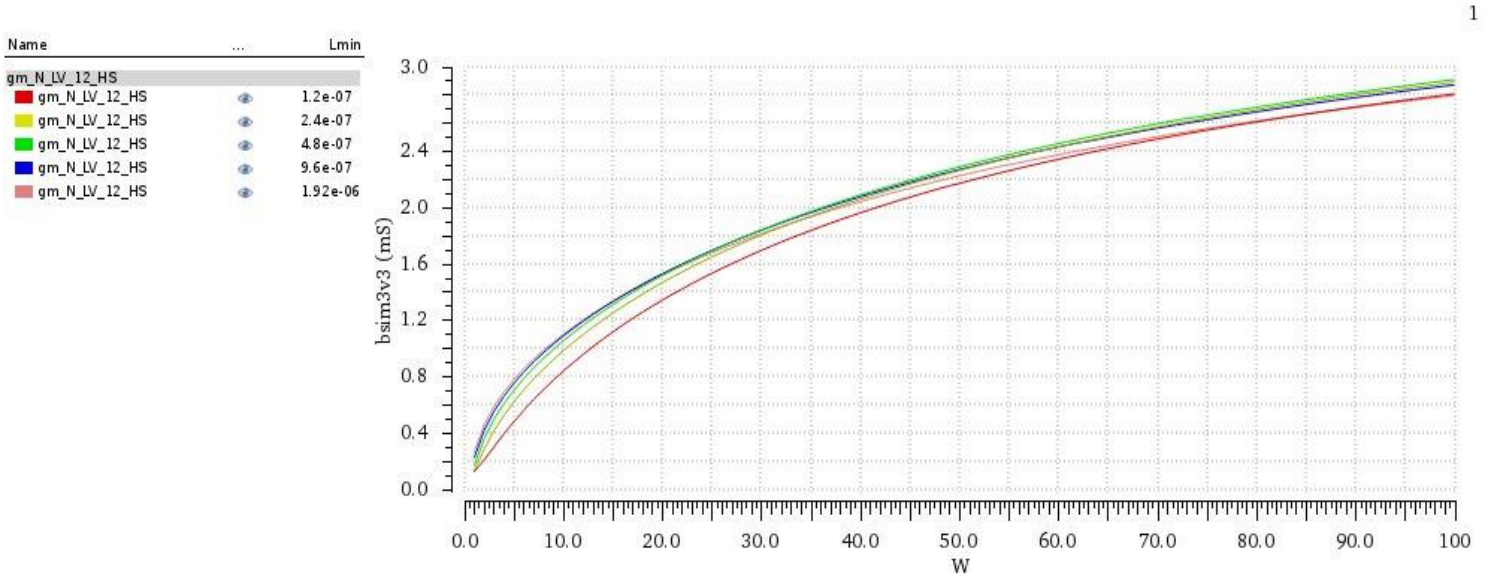


Figure 10: gm versus W/L using N_LV_12_HS_L130E

ro versus W/L

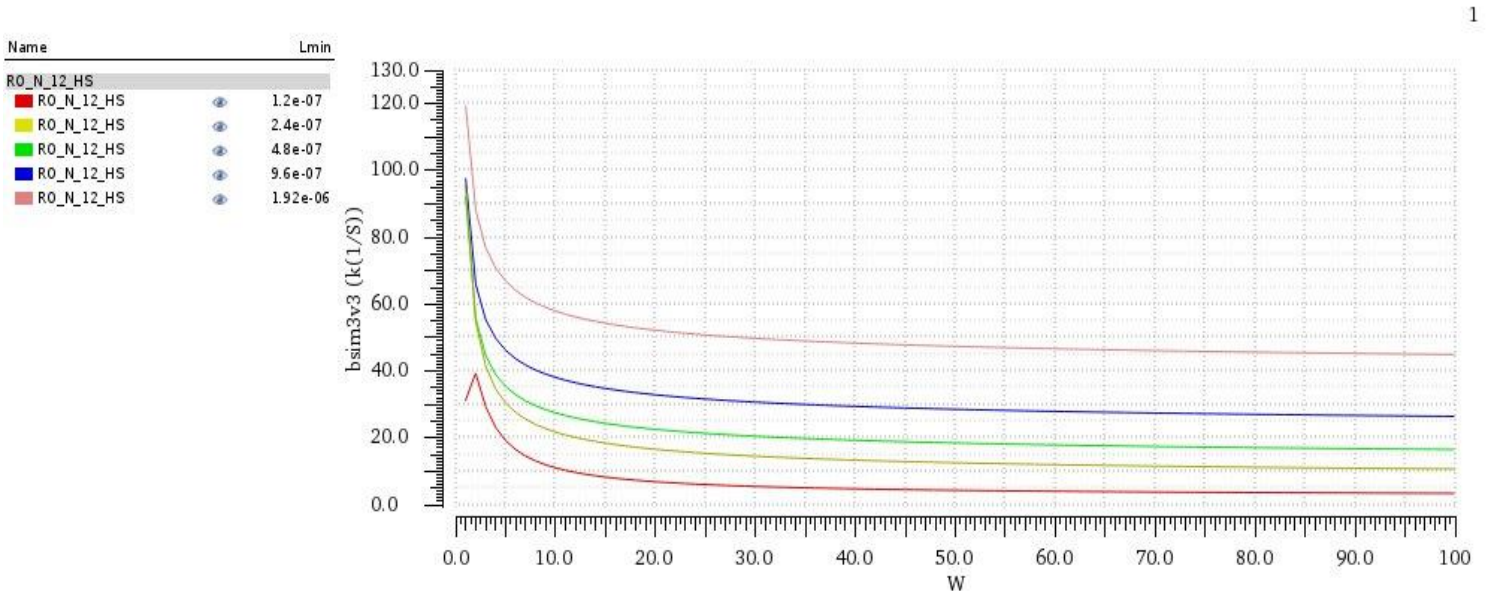


Figure 11: ro versus W/L using N_12_HS_L130E

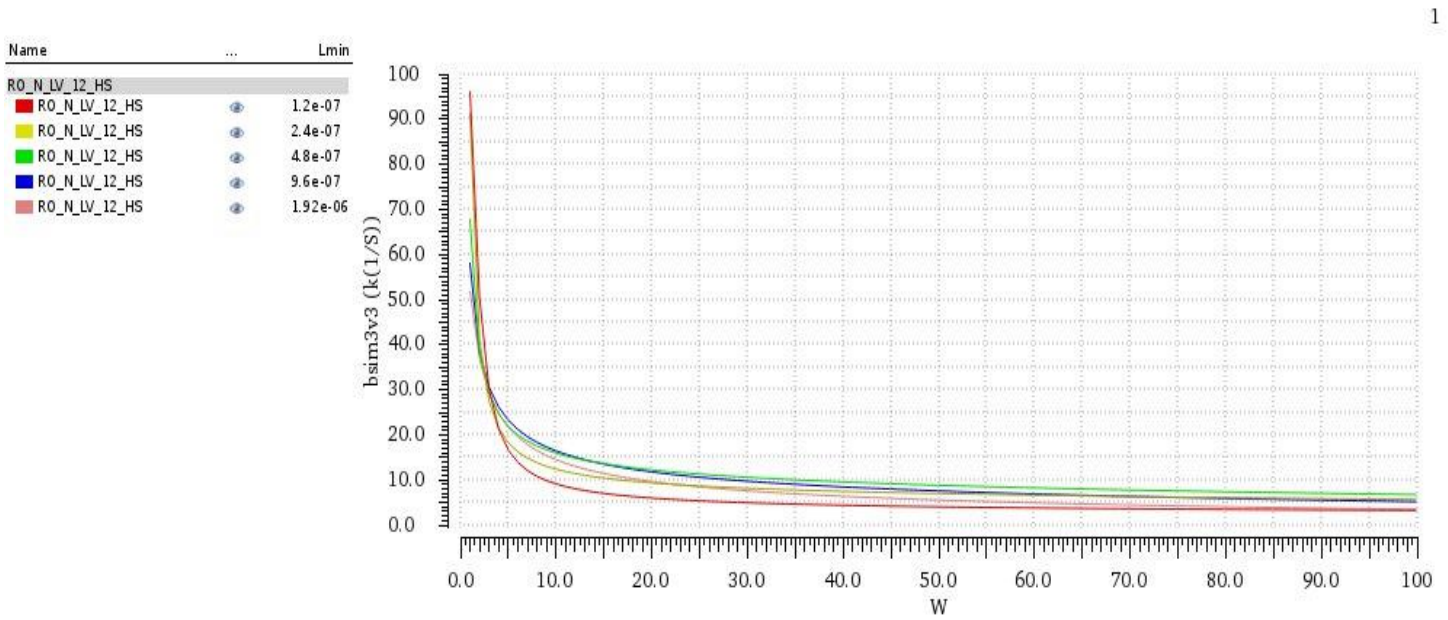


Figure 12: ro versus W/L using N_LV_12_HS_L130E

4. **Mention the long channel equation for each of the above simulated parameters. Is the trend of the simulations similar to the equations?**

1. The relation between VTH and W/L at saturation region:

$$Vth = VGS - \sqrt{\frac{2I}{\frac{W}{L}C_{ox}\mu}}$$

At Triode region:

$$Vth = VGS - \frac{I}{\frac{W}{L}C_{ox}\mu VDS} - \frac{VDS}{2}$$

2. The relation Vov (VGS-VTH) and W/L & VDSAT and W/L at saturation region:

$$Vov = \sqrt{\frac{2I}{\frac{W}{L}C_{ox}\mu}}$$

At Triode region:

$$Vov = \frac{I}{\frac{W}{L}C_{ox}\mu VDS} + \frac{VDS}{2}$$

3. The relation gm.ro and W/L:

$$ro = \frac{2}{\lambda\frac{W}{L}C_{ox}\mu(VGS - Vth)^2(1 + \lambda VDS)}$$

$$gm = \frac{W}{L}(VGS - Vth)$$

5. **Mention one advantage and one disadvantage for N_LV_12_HS_L130E compared to N_12_HS_L130E. What do you recommend to be used in a high-gain amplifier?**

An advantage for N_LV_12_HS_L130E:

The device typically has a lower threshold voltage compared to the standard high-speed NMOS. This advantage, especially for low-voltage applications, may lead to better performance in terms of switching speed and low-voltage applications.

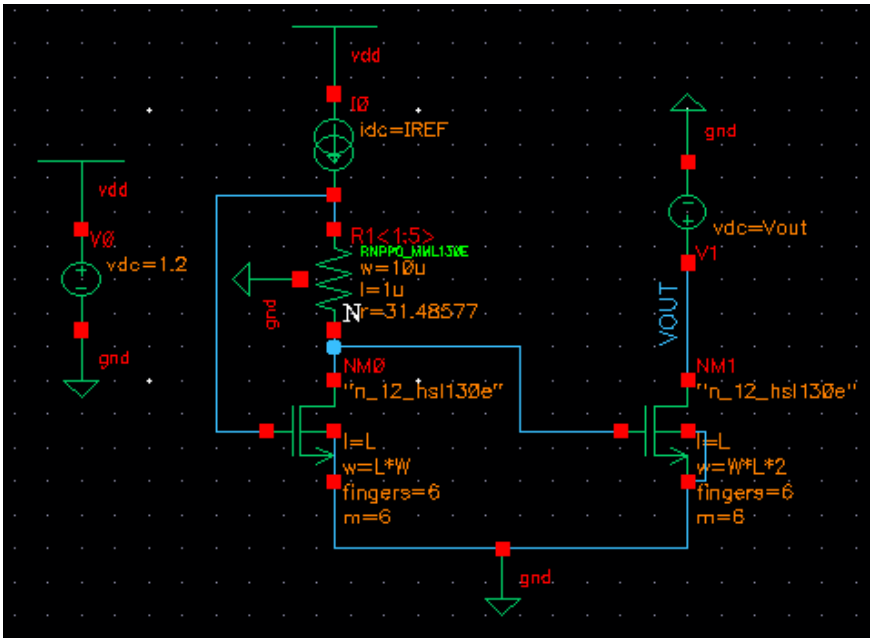
A disadvantage for N_LV_12_HS_L130E:

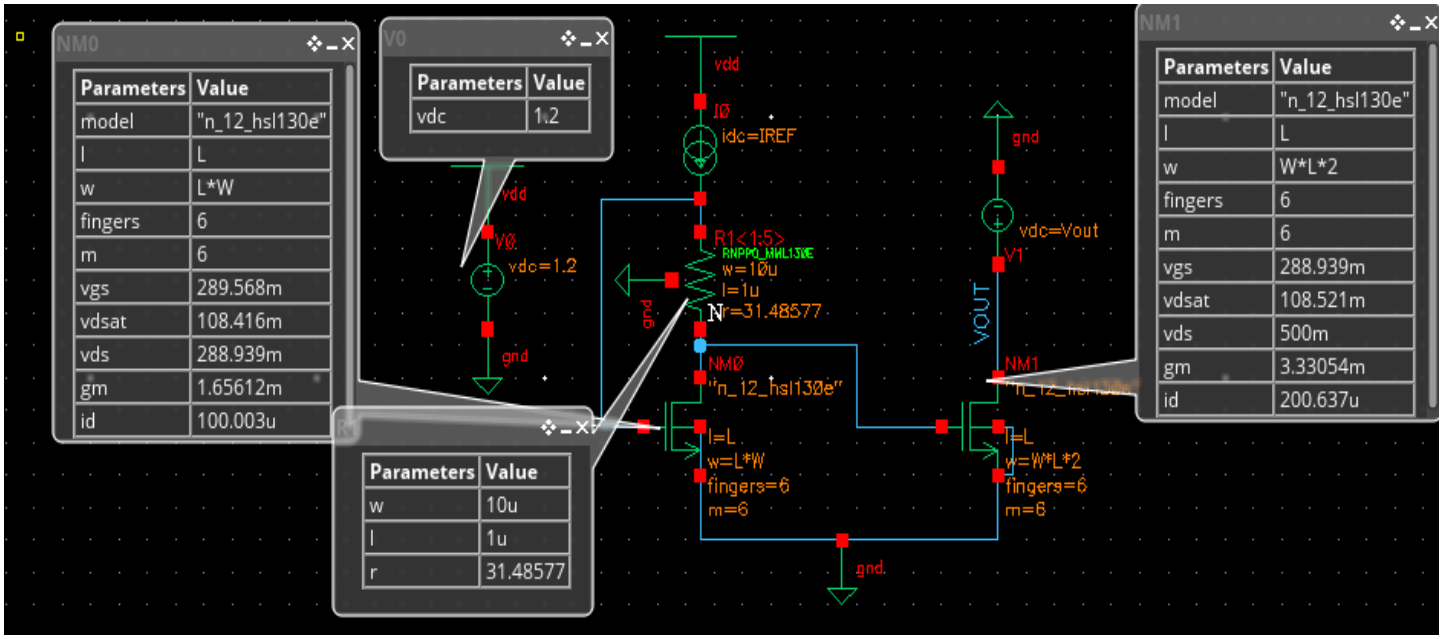
Increased Sensitivity to Process Variations: This device is more sensitive to process variations compared to its high-Vth counterparts, this sensitivity can result in greater variability in transistor performance across manufacturing lots, potentially leading to yield issues and reliability concerns.

Task #2

- First Circuit

1. Schematic diagram with dimensions and component values annotated.

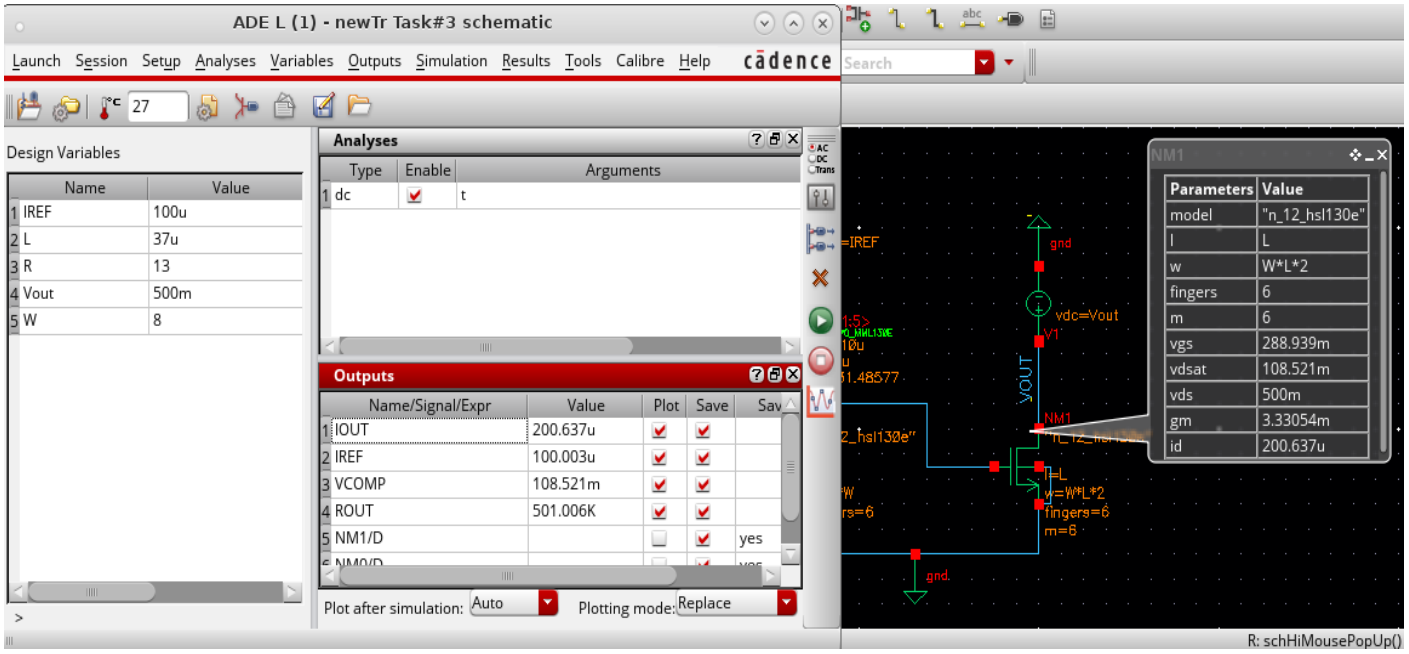




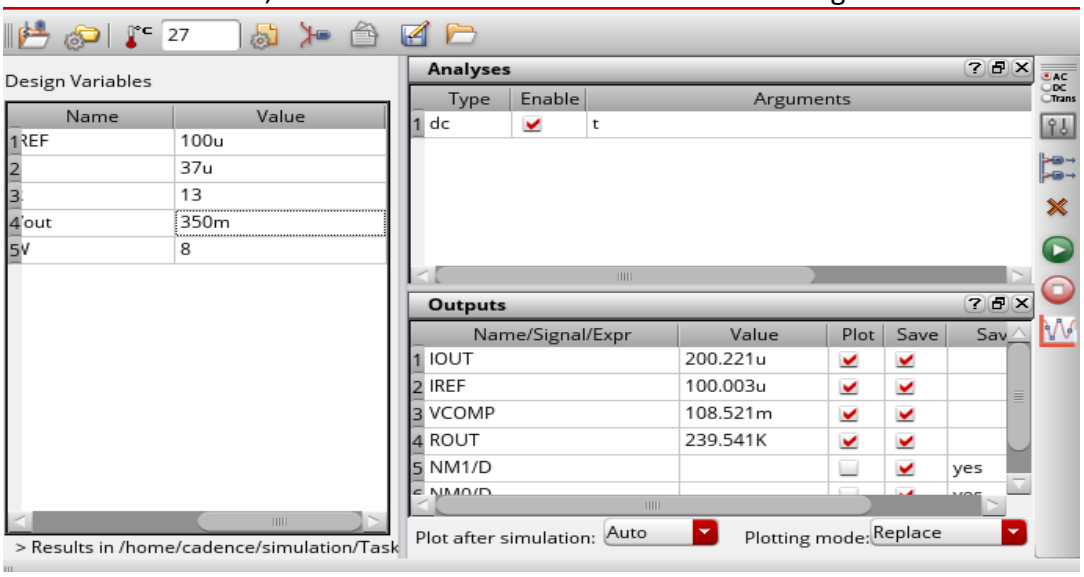
After sweeping the constant ratio W/L with ROUT and Vcomp of the design to choose the most efficiency values for this parameter to meet the required specifications.

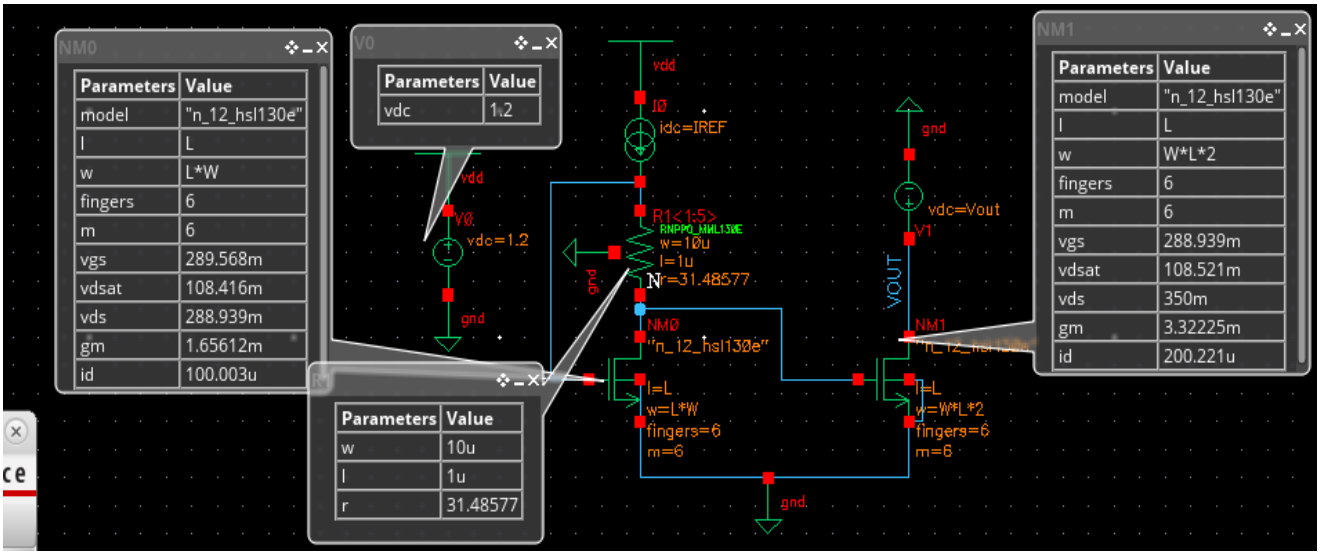
Thus, we choose W= 8, so L=37u as the best values for efficient mirroring.

So, we set this chosen parameter in AD EL testbench and get the required values, as shown in fig, we meet our specifications correctly



For $Vout = 350mV$, the results of the simulation as shown in fig.

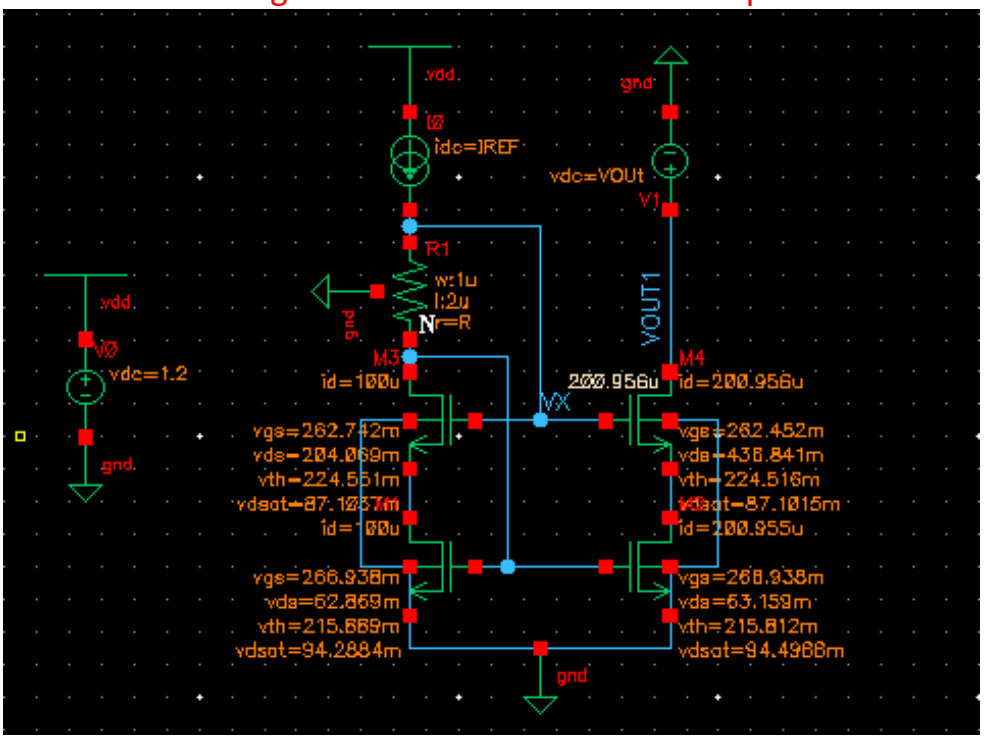


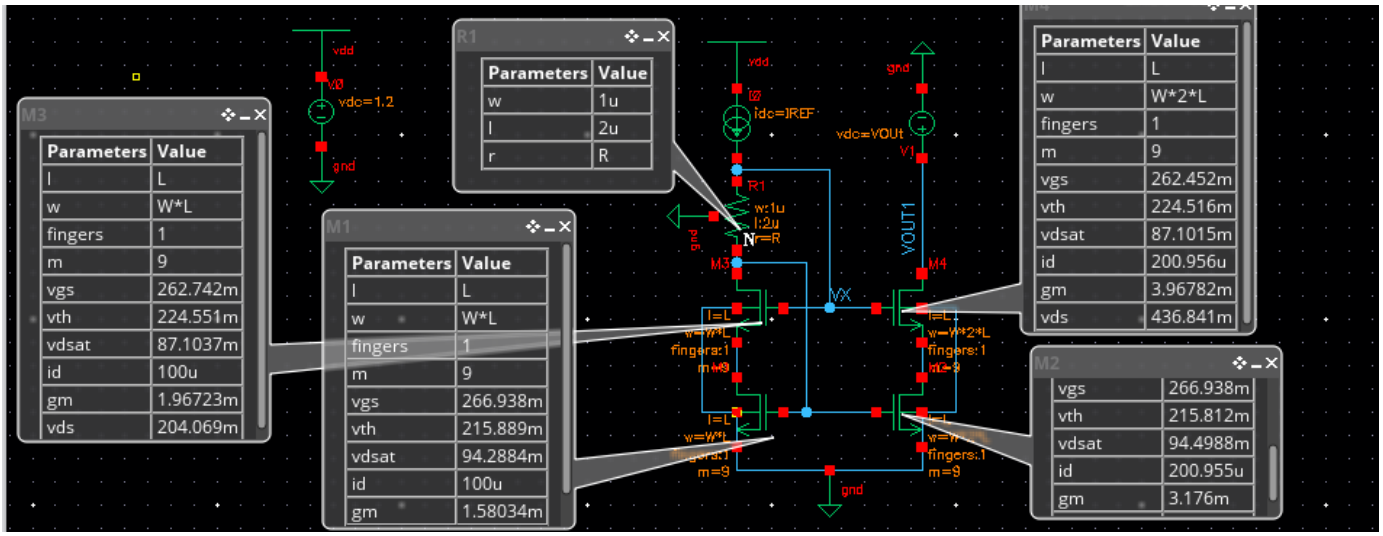


As shown in fig, we can see that both transistors are in sat, we see that rout drops but the current mirror is still accurate.

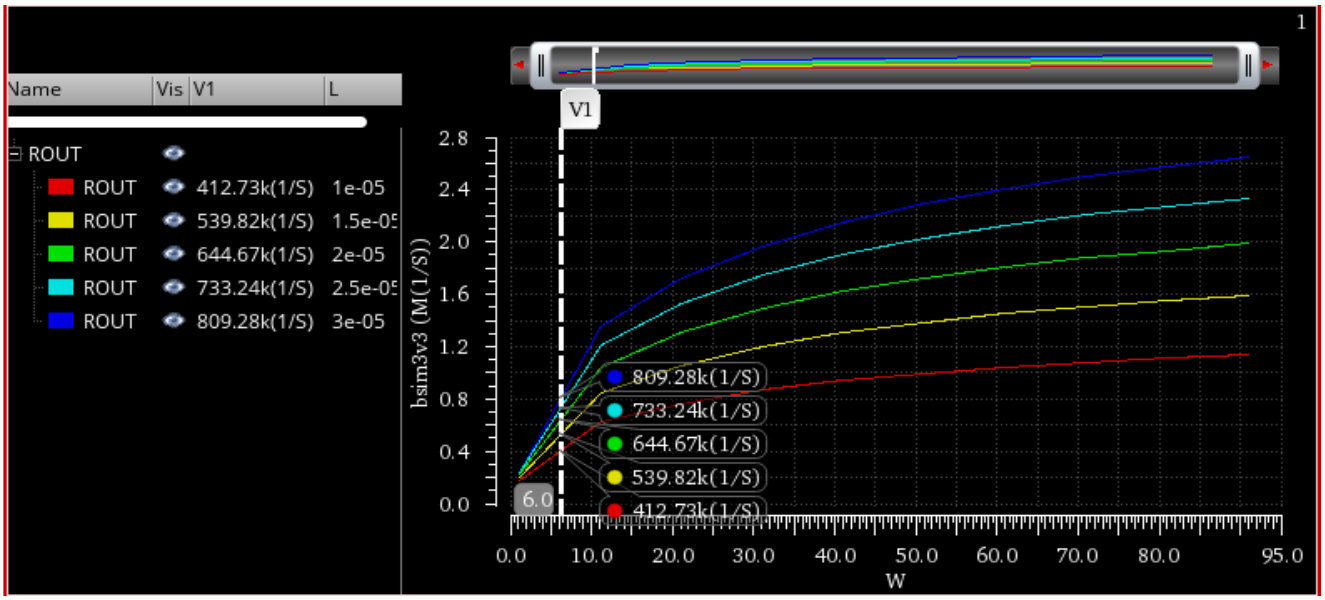
- Second Circuit

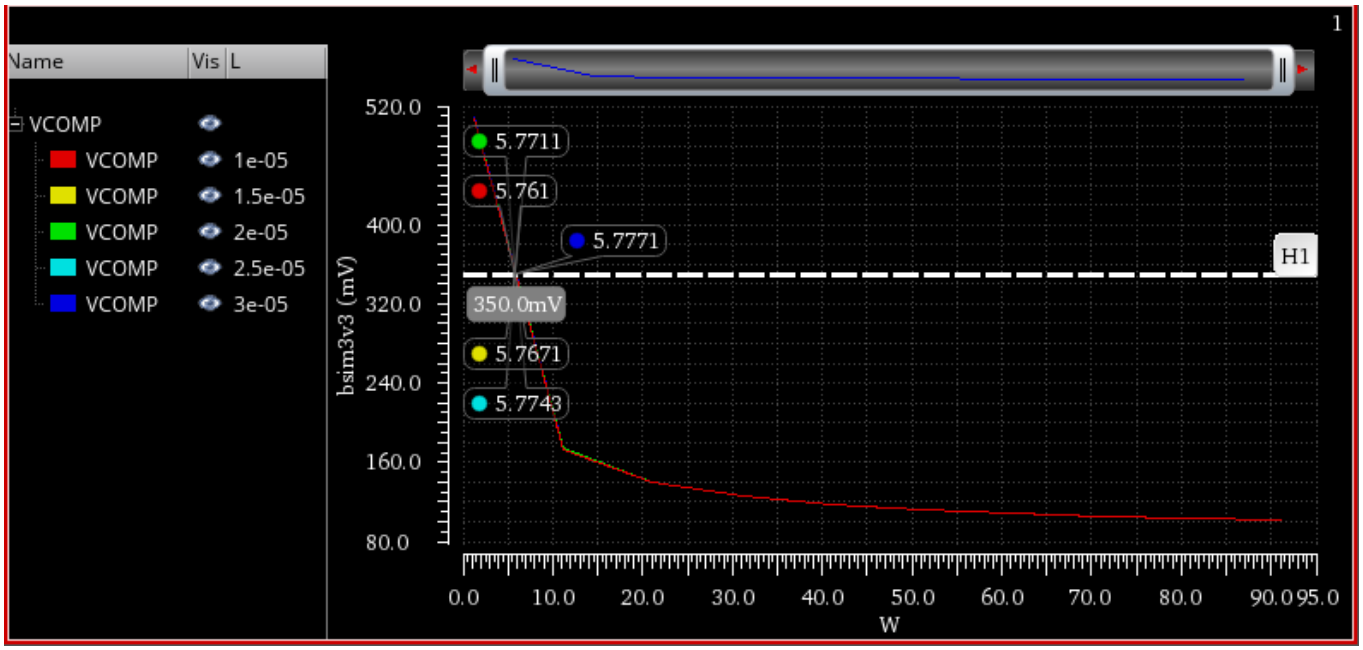
1. Schematic diagram with dimensions and component values annotated.





After sweeping the constant ratio W/L with ROUT and Vcomp of the design to choose the most efficiency values for this parameter to meet the required specifications as shown in the figures.

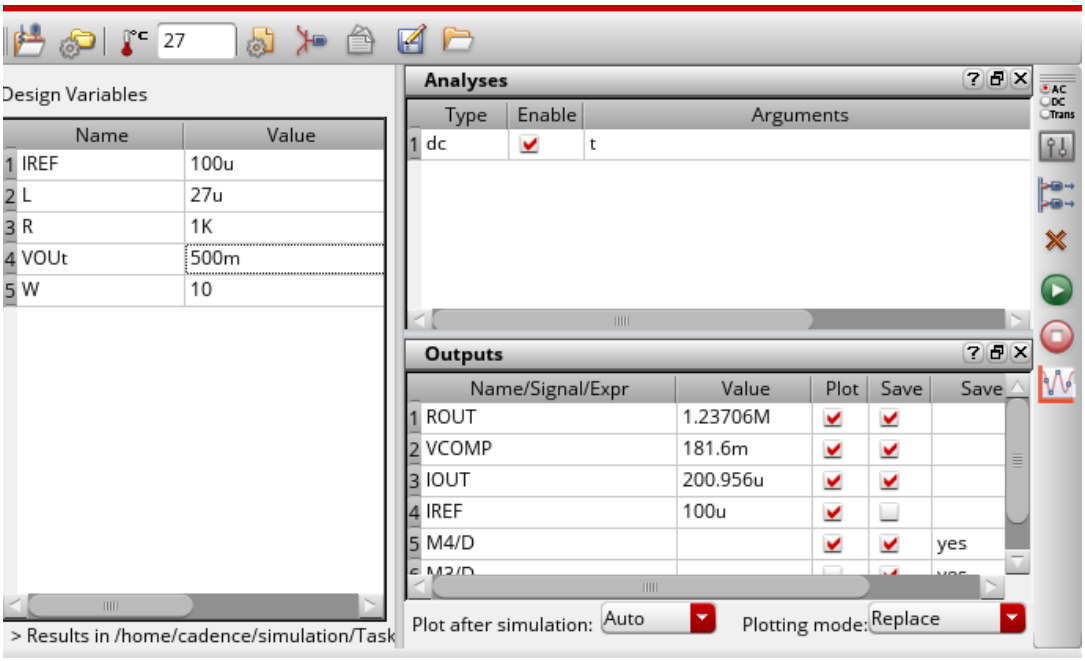




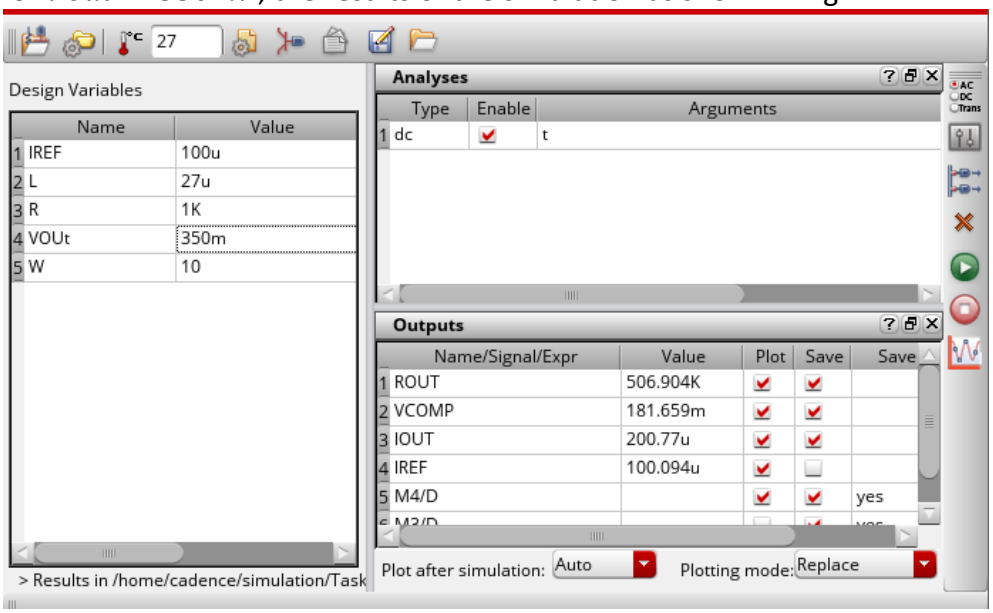
Thus, we choose W= 10, so L=27u as the best values for efficient mirroring.

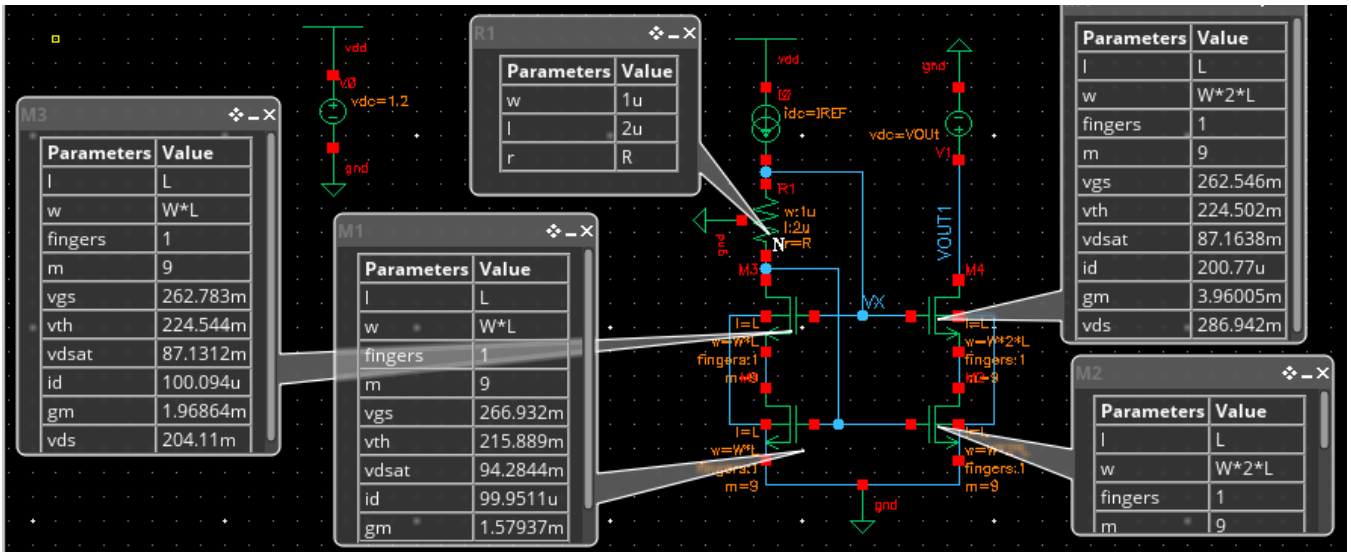
So, we set this chosen parameter in AD EL testbench and get the required values, as shown in fig, we meet our specifications correctly

CDF Parameter	Value
l (M)	L M
w (M)	W*2*L M
Number of Fingers	1
Source Drain Metal Width (M)	280.0n M
Width Per Finger	iPar("w")/iPar("fingers
Multiplier	9
Calc Diff Params	☑



For $Vout = 350mV$, the results of the simulation as shown in fig.



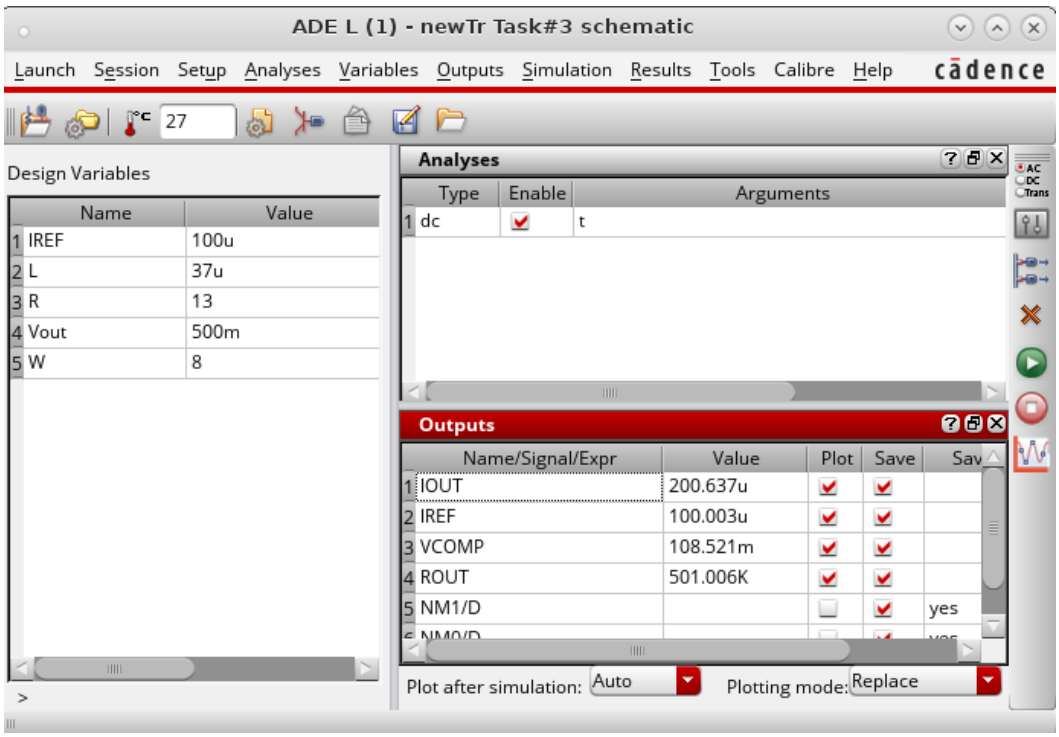


As shown in fig, we can see that all transistors are in sat.

Simulation results to verify I out and Rout specifications for both circuits.

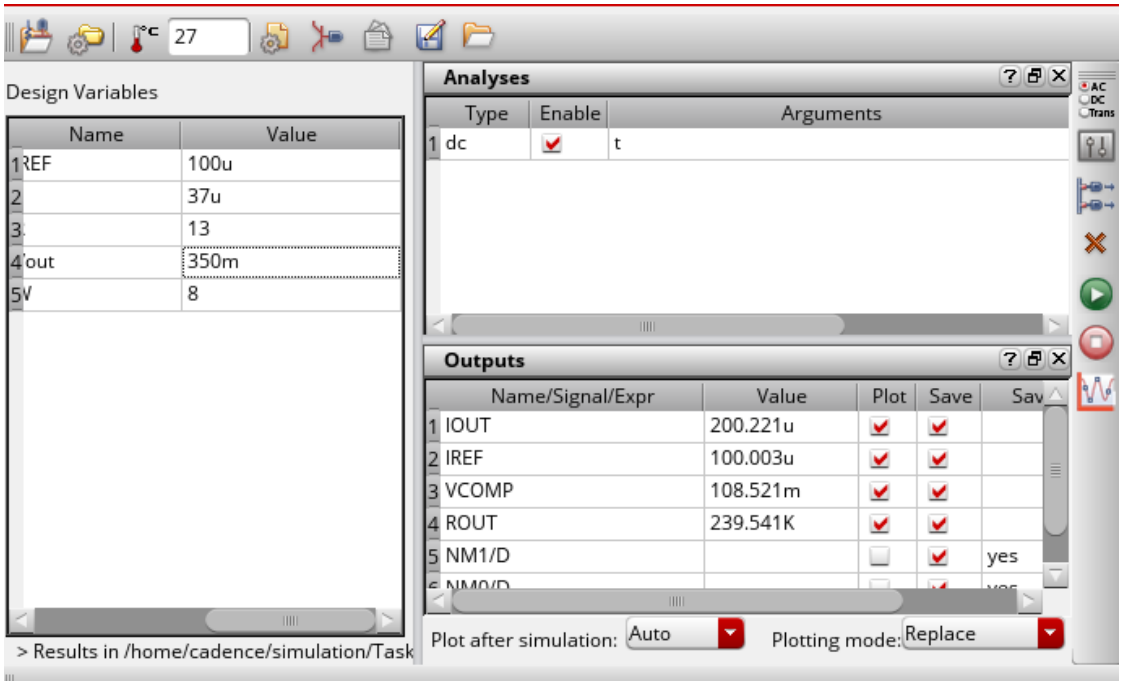
- First Circuit

- For Vout=500mV



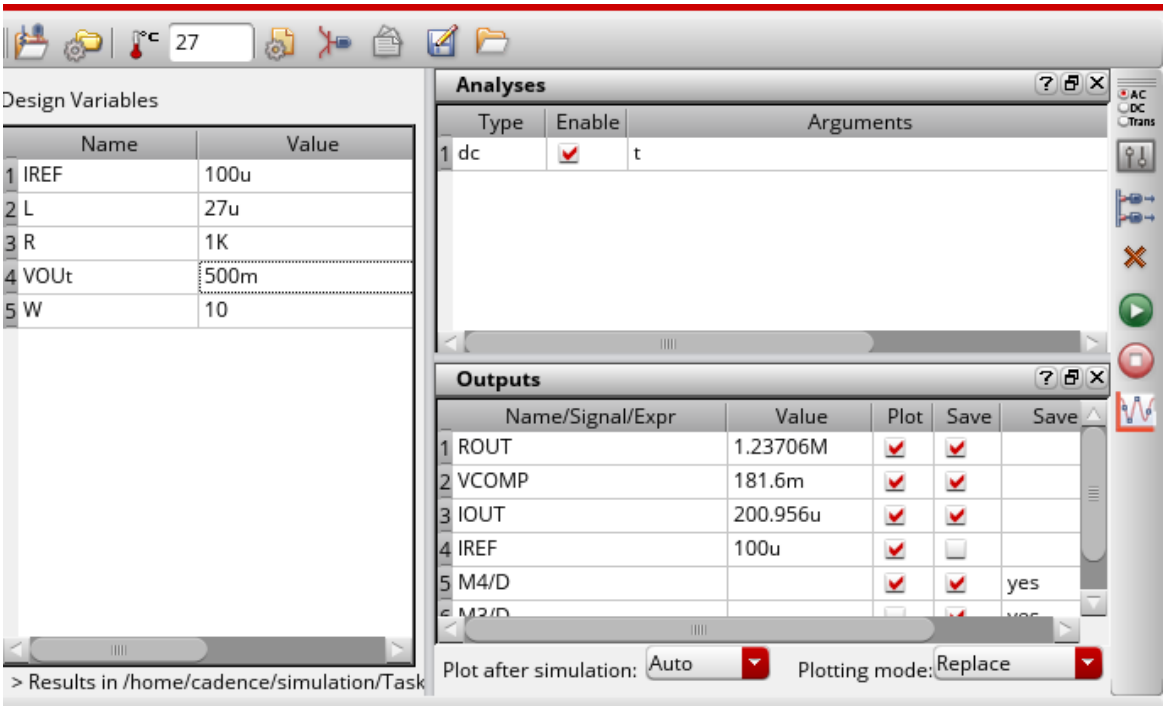
As shown in fig, we can see that rout exceeds 500k and $2IREF - IOUT \,/\, @IREF$ is less than 1.

- For $Vout = 350mV$

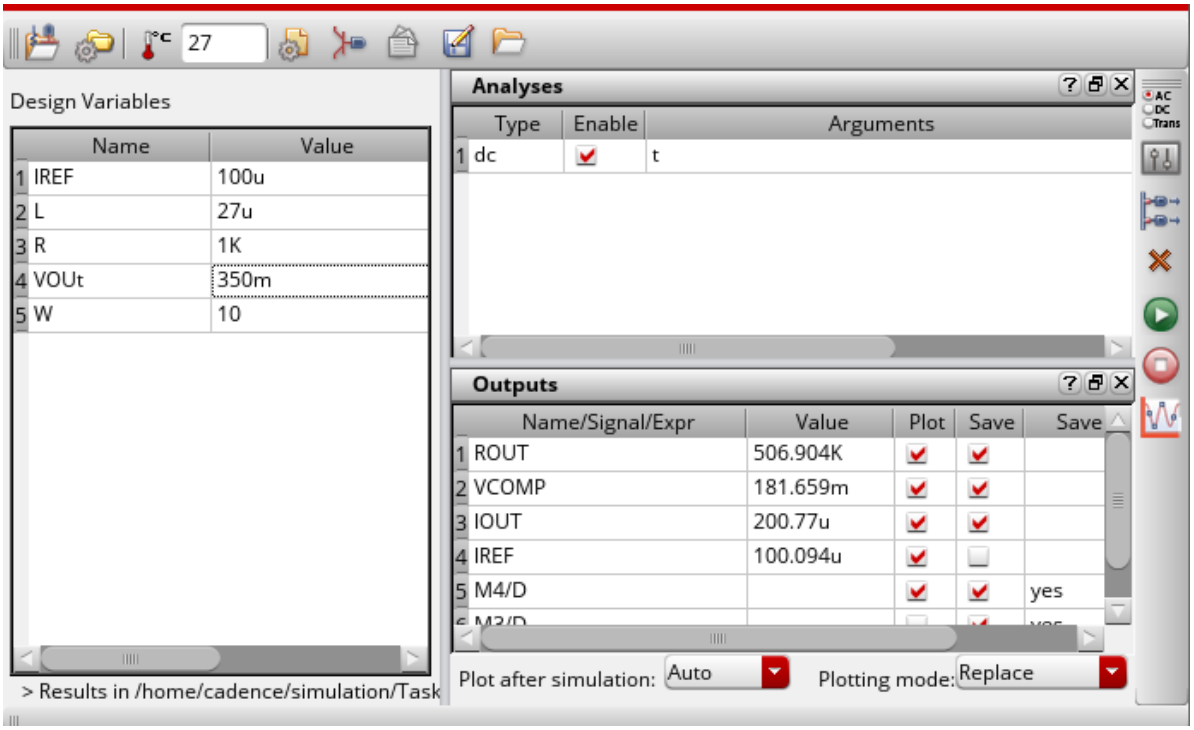


- Second Circuit

- For $Vout = 500mV$



- For $Vout = 350mV$



As shown in fig, we can see that rout exceeds 500k and 2IREF – IOUT / @IREF is less than 1.

As shown in fig, we see that rout drops but still they meet the required specifications.

An estimate of this mirror's area for both circuits.

- First Circuit

Total Area for the first MOSFET (reference MOSFET) = $W * L * M(Multipliers) = 1200\ u\text{^}2$.

Total Area for the first MOSFET (output MOSFET) = $2 * W * L * M(Multipliers) = 4200\ u\text{^}2$.

Total Area for the resistance = $W * L = 10\ u\text{^}2$.

- Second Circuit

Total Area for the first MOSFET (reference MOSFET) = $W * L * M(Multipliers) = 2430\ u\text{^}2$.

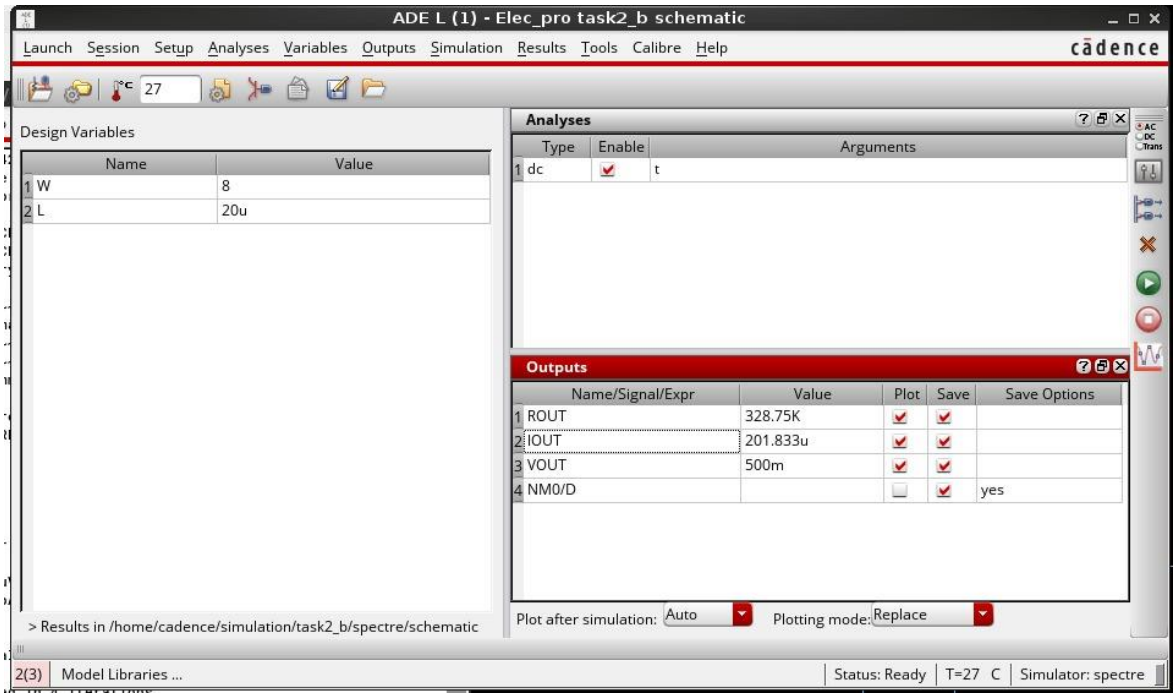
Total Area for the first MOSFET (output MOSFET) = $2 * W * L * M(Multipliers) = 4860\ u\text{^}2$.

Total Area for the resistance = $W * L = 6.58\ u\text{^}2$.

If your manager told you the area you ended up with is too large and you need to sacrifice one of the specs to have reasonable area, suggest a modification and comment on what you'll gain and lose from it.

- First Circuit

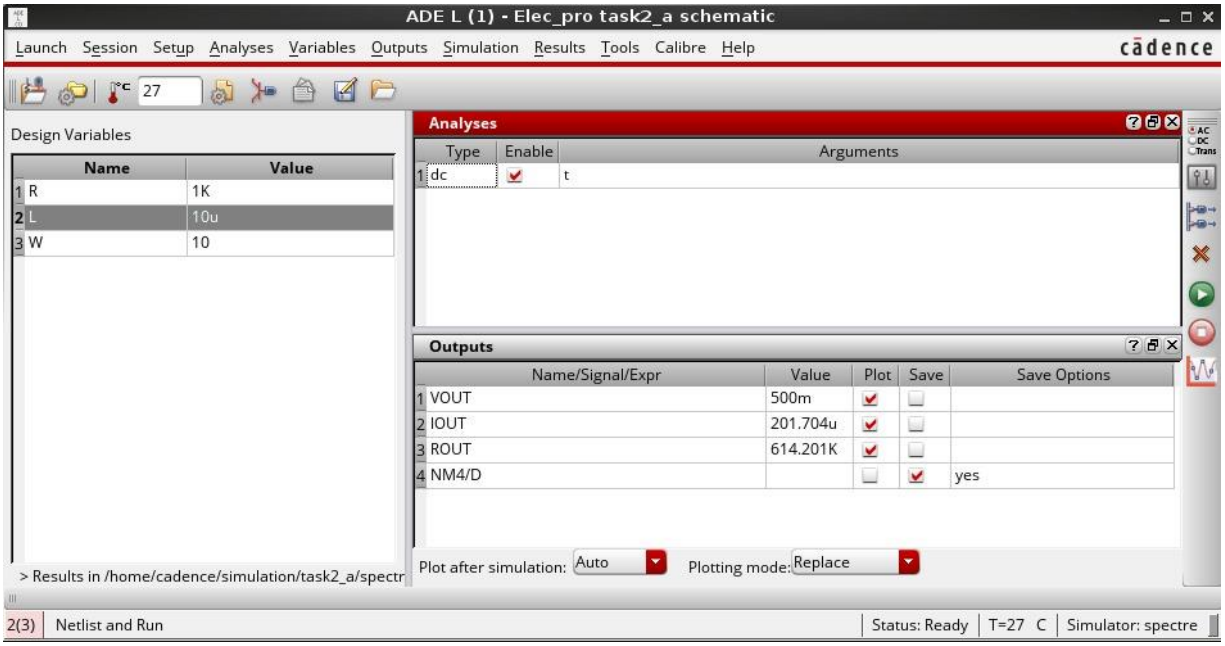
- Reducing the area for the first MOSFET (reference MOSFET) from $1200\ u^2\ to\ 648.6\ u^2$, the first MOSFET (output MOSFET) from $4200\ u^2\ to\ 2270.27\ u^2$



Rout finished! But Iout still meet the required specifications.

- Second Circuit

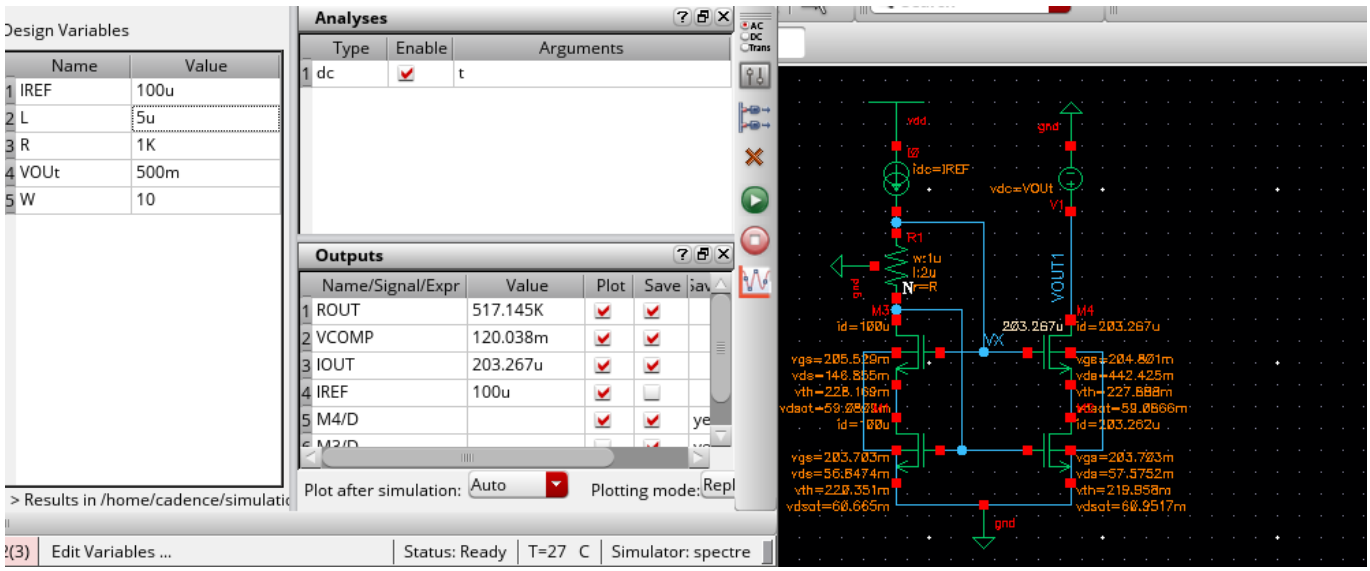
Considering L=10u reducing the area for the first MOSFET (reference MOSFET) from $2430\ u\text{^}2\ to\ 900\ u\text{^}2$, the first MOSFET (output MOSFET) from $4860\ u\text{^}2\ to\ 1800\ u\text{^}2$



So, still meet the required specifications!

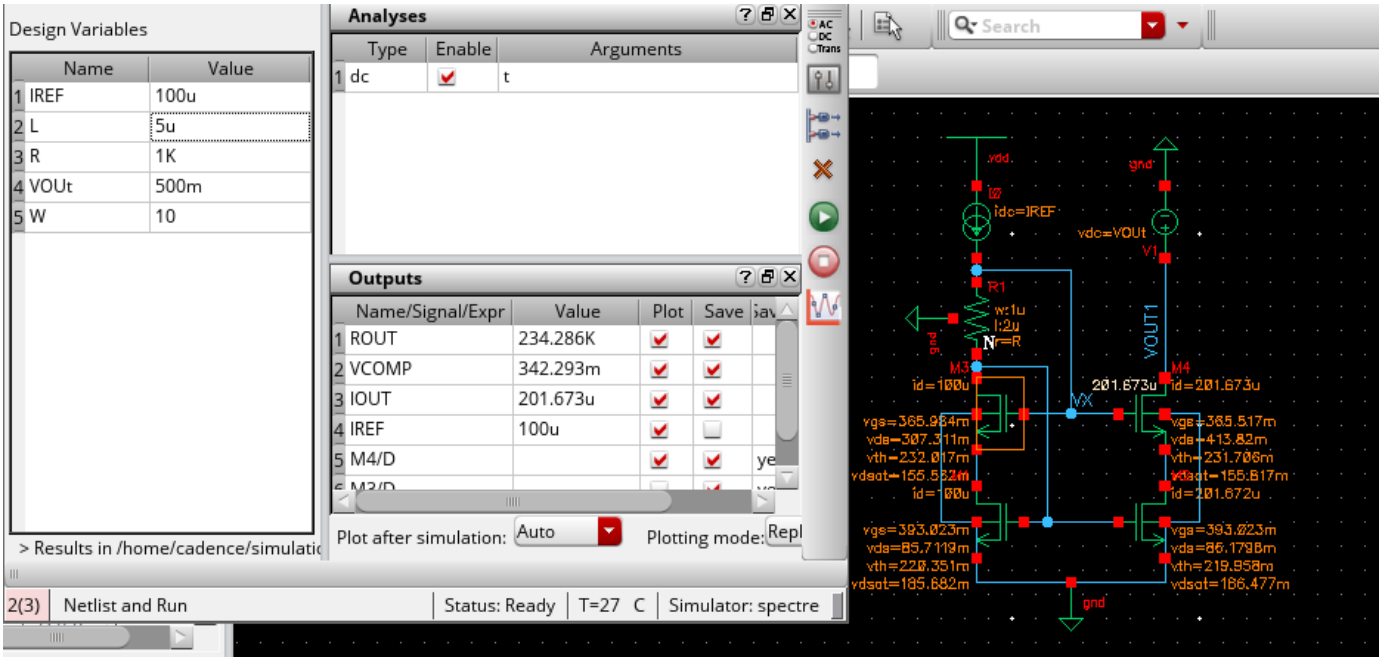
Considering L=5u reducing the area for the first MOSFET (reference MOSFET) from $2430\ u\text{^}2\ to\ 450\ u\text{^}2$, the first MOSFET (output MOSFET) from $4860\ u\text{^}2\ to\ 900\ u\text{^}2$

Considering this reasonable area so as shown in fig, we notice Iout decrease and Rout still meet the required specifications but we'll make a small modification on the multipliers in the second circuit so to set it to 2 as show in fig



CDF Parameter	Value	Display
l (M)	L M	off
w (M)	W*2*L M	off
Number of Fingers	1	off
Source Drain Metal Width (M)	280.0n M	off
Width Per Finger	iPar("w")/iPar("fingers	off
Multiplier	2	off

Thus, for the two circuits sacrificing the rout, this modification will lower the gain of the circuit and will decrease the linearity of the current mirror (ideally wish to have infinite Rout) but still we meet the required speciation of current mirroring efferently, but we will decrease the area drastically which in return lowers the costs of manufacturing.



Compare both designs in a table by adding the analyzed results with the simulated results for both designs.

Let's first set up the equations that will be used for the analysis:

Since we choose low L and designed the circuit to have VDS for both MOFSETS equal, thus we'll obtain the output current as:

$$Iout = Iref * 2 \frac{Vov_4^2}{Vov_3^2} \text{ (assuming they have same KN)}$$

$$Vov = VGS - Vth$$

$$gm = \frac{2IDS}{Vov}$$

$$Rout\ for\ cascode = ro_1 + ro_4 + ro_1\, ro_4\, gm_4 \approx ro_1\, ro_4\, gm_4$$

- First Circuit

Analysis (350mV):

Since we choose low L and designed the circuit to have VDS for both MOFSETS equal

We can Obtain the output current as follows:

$$Iout = Iref * 2 \frac{Vov_2^2}{Vov_{ref}^2} \text{ (assuming they have same KN)}$$

And knowing that: $Vov = VGS - Vth$

Getting VGS_2 = 288.939 and Vth_2 = 215.915 from DC run

And VGS_{ref} = 289.568 and Vth_{ref} = 216.306 from DC run

Substituting in the Iout equation we get:

$$\boldsymbol{Iout = 198.7\ uA}$$

$gm = \frac{2IDS}{Vov}$

Substituting we get:

$$\boldsymbol{gm_2 = 5.44}$$

$$\boldsymbol{gm_{ref} = 2.73}$$

$$\boldsymbol{Rout = ro\ (directly\ from\ run) = 239.541\ KOhm}$$

VARIABLE	ANALYZED	SIMULATED
IOUT	**198.7mA**	200.221 **mA**
gm_{ref}	2.73	1.66
gm_2	**5.44**	3.322
Rout	$239.541\ KOhm$	

Analysis (500mV):

Getting VGS_2 = 288.939 and Vth_2 = 215.915 from DC run

And VGS_{ref} = 289.568 and Vth_{ref} = 216.306 from DC run

Substituting in the $Iout$ equation we get:

$$Iout = 198.7\ uA$$

We notice that's no change from 350mV, so we get:

$gm_2 = 5.44$

$gm_{ref} = 2.73$

Rout = RO (directly from run) = $239.541\ KOhm$

VARIABLE	ANALYZED	SIMULATED
IOUT	**198.7mA**	200.637**mA**
gm_{ref}	2.73	1.66
gm_2	**5.44**	3.33
Rout	$239.541\ KOhm$	

- Second Circuit

Analysis (350mV):

Getting $VGS_2 =$ 268.938 and Vth_2 = 215.812 from DC run

And VGS_{ref} = 266.938 and Vth_{ref} = 215.669 from DC run

And VGS_4 = 262.452 and Vth_4 = 224.516 from DC run

Therefore, substituting in the $Iout$ equation we get:

$$\boldsymbol{Iout = 214.7\ uA}$$

$$gm = \frac{2IDS}{Vov}$$

Substituting we get:

$$gm_4 = 11.3$$

Getting $ro4 = 148.967k$ and $ro2 = 605.733$ from DC run.

$Rout = ro_2 + ro_4 + ro_2\ ro_4\ gm_4$ = approximately $ro_2\ ro_4\ gm_4$

Substituting in the equation above

We get $rout = 991K$

VARIABLE	ANALYZED	SIMULATED
$\boldsymbol{IOUT}$	214.7	200.956
$\boldsymbol{Rout}$	$991K$	506.9K

Analysis (500mV):

Getting VGS_2 = 268.932 and Vth_2 = 215.812 from DC run

And VGS_{ref} = 266.932 and Vth_{ref} = 215.669 from DC run

And VGS_4 = 262.546 and Vth_4 = 224.502 from DC run

Substituting in the $Iout$ equation we get:

$$\boldsymbol{Iout = 214.75\ uA}$$

$$gm = \frac{2IDS}{Vov}$$

Substituting we get:

$gm_4 = 11.3$

Getting $ro4 = 362.692k$ and $ro2 = 607.17$ from DC run.

$Rout = ro_2 + ro_4 + ro_2\ ro_4\ gm_4$ = approximately $ro_2\ ro_4\ gm_4$

Substituting in the equation above

We get rout = 2M

VARIABLE	ANALYZED	SIMULATED
IOUT	$214.75mA$	200.77mA
$\boldsymbol{Rout}$	$2M$	1.23M

Comparison

Variable	Analyzed				Simulated			
	350v 1st circuit	**350v 2nd circuit**	**500v 1st circuit**	**500v 2nd circuit**	**350v 1st circuit**	**350v 2nd circuit**	**500v 1st circuit**	**500v 2nd circuit**
IOUT	**198.7mA**	214.7	**198.7mA**	$214.75mA$	200.221 **mA**	200.956	200.637 **mA**	200.77mA
ROUT	$\mathbf{239.541}$	$991K$	$\mathbf{239.541}$	$2M$	$\mathbf{239.541\ K\Omega}$	506.9K	501K	1.23M

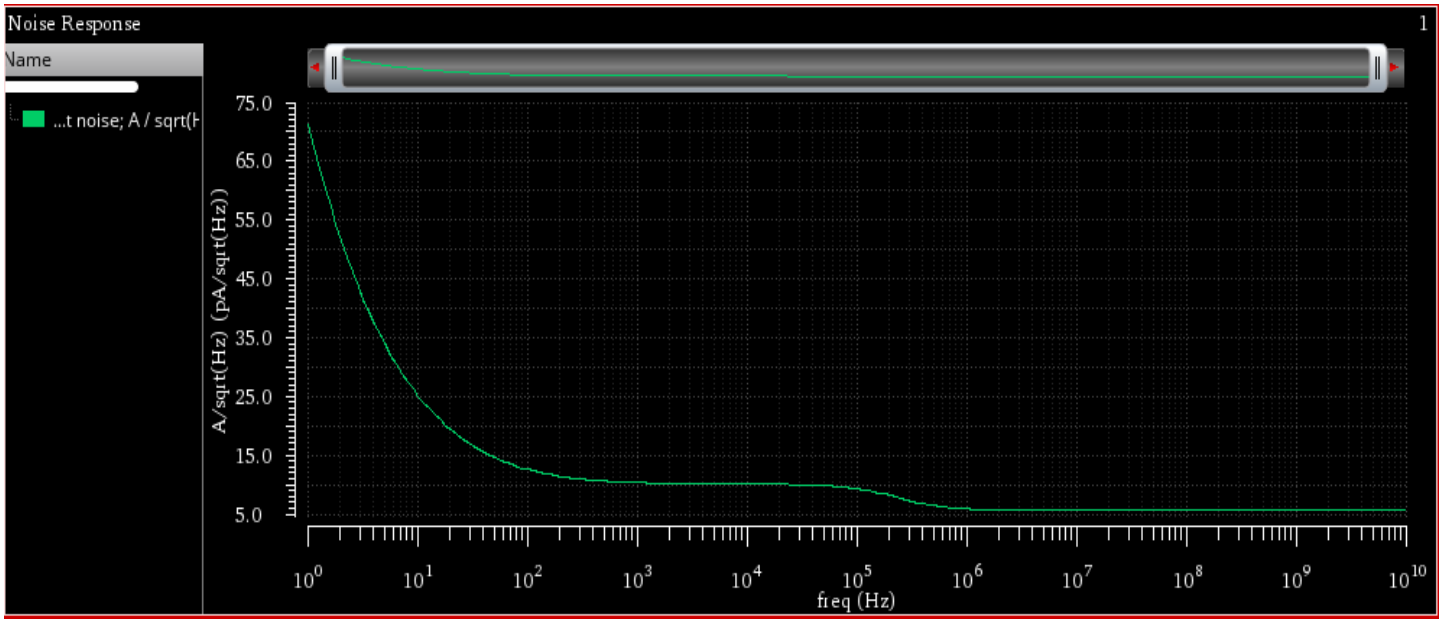
At both output voltages 500m and 350m we notice a slight difference in IOUT and a huge difference in Rout, this is because the long channel equations we use are a bit approximated and do not match the ones the simulator uses which are more accurate.

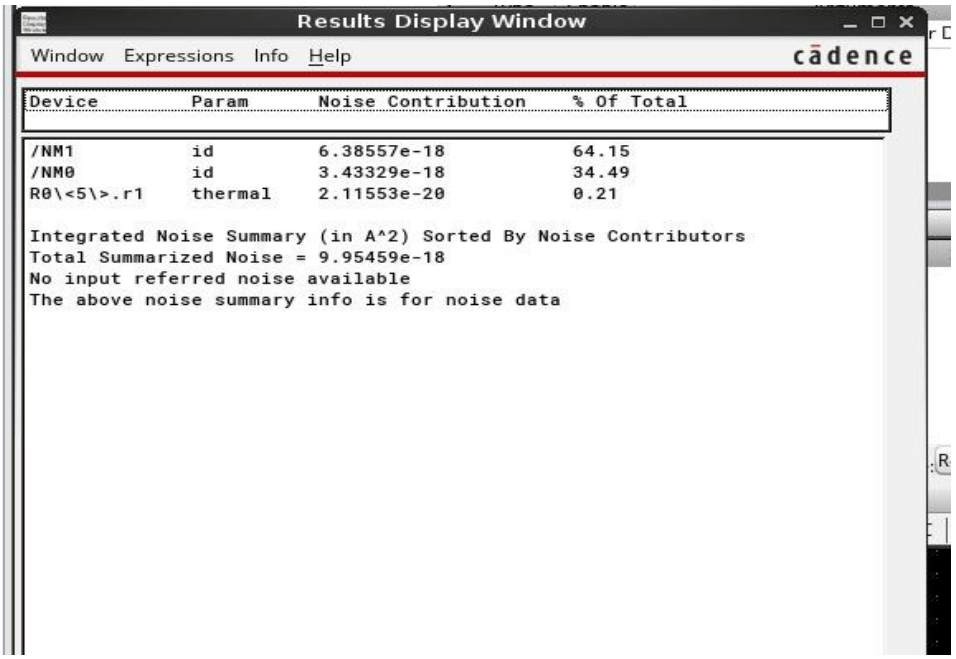
Discuss the circuits at which each circuit is more suitable to be used.

Because the first circuit has a very low Vcomp and a high output swing, it is the greatest choice when creating low power circuits. However, because of its reduced noise level, the second circuit is more suited for circuits that must handle noise.

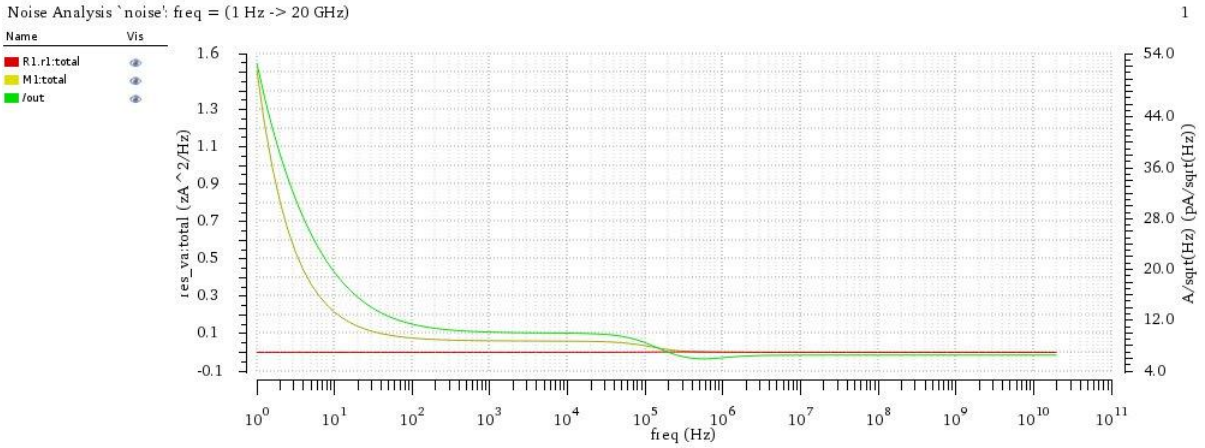
Draw and estimate the noise of both circuits and define which devices are more dominant in the total noise.

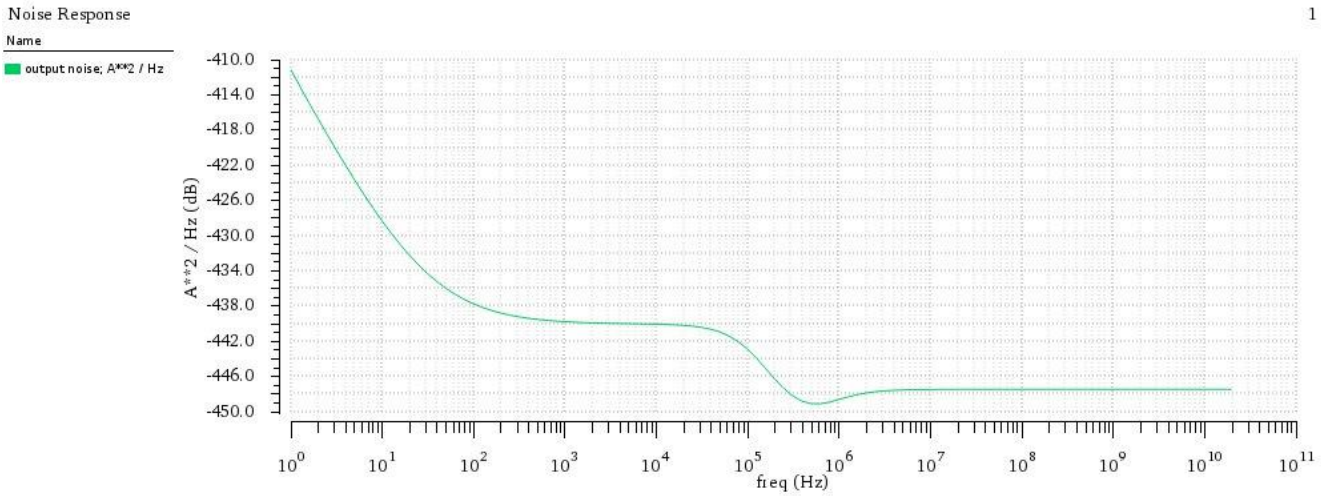
- ## First Circuit

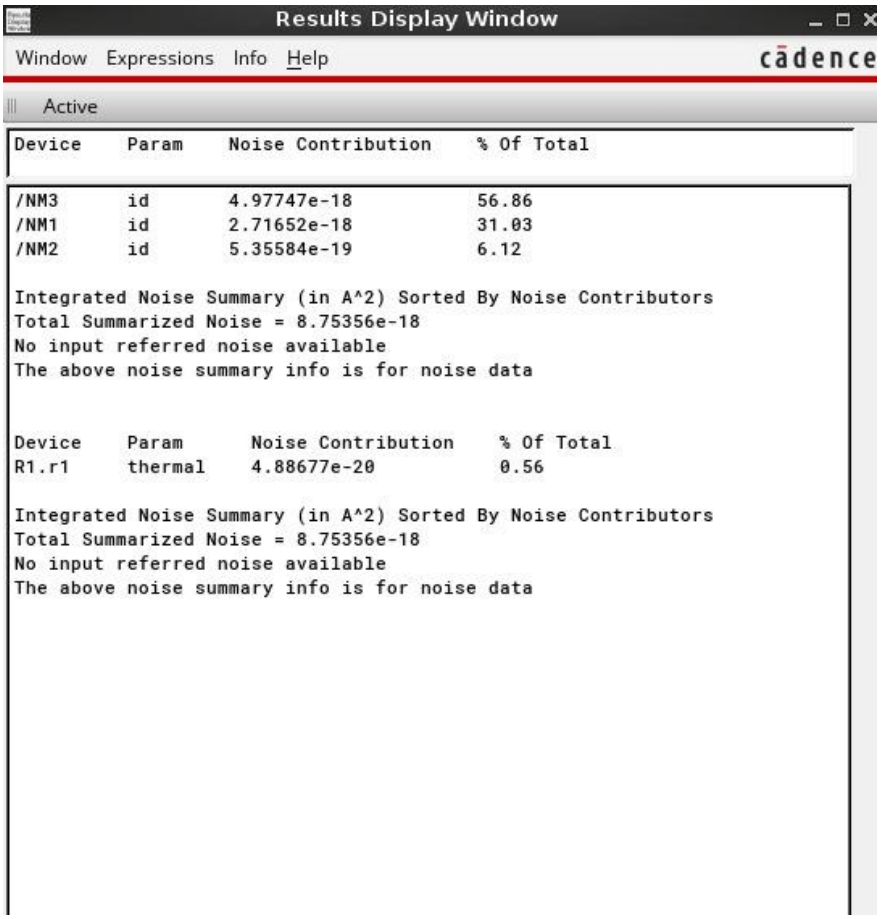




- Second Circuit





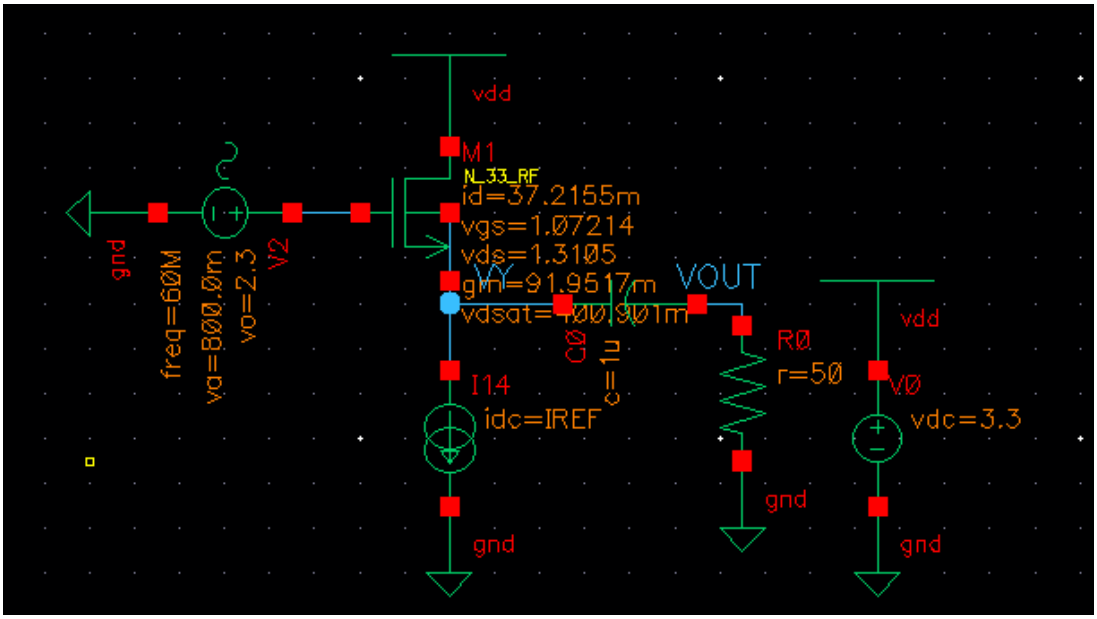

Results Display Window
Window Expressions Info Help
cadence
Active
Device Param Noise Contribution % Of Total
/NM3 id 4.97747e-18 56.86
/NM1 id 2.71652e-18 31.03
/NM2 id 5.35584e-19 6.12
Integrated Noise Summary (in A^2) Sorted By Noise Contributors
Total Summarized Noise = 8.75356e-18
No input referred noise available
The above noise summary info is for noise data
Device Param Noise Contribution % Of Total
R1.r1 thermal 4.88677e-20 0.56
Integrated Noise Summary (in A^2) Sorted By Noise Contributors
Total Summarized Noise = 8.75356e-18
No input referred noise available
The above noise summary info is for noise data

Task #3

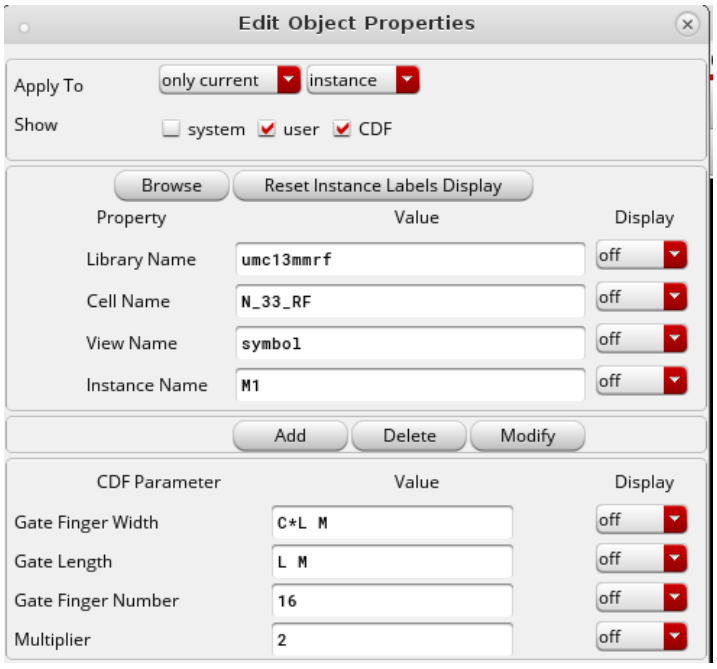
Use the NMOS core high voltage RF transistor (N_33_RF), an ideal current source, and an ideal DC blocking cap of 1µF to design a class A Power Amplifier operating at VDD = 3.3V with the following specifications:

- $Vin, DC = 2.3V$
- $Vin, AC = A\,sin(2\pi ft)\,, f = 60MHz, A = 0.8V$
- $RL = 50\Omega$? $|Vout, peak| > 600mV$
- $Output\ signal\ linearity\ is\ characterized\ as\ |Vout, max||Vout, min|\ Vout, max < 2.5\%$

First, set the schematic of the design before we go to the testbench:

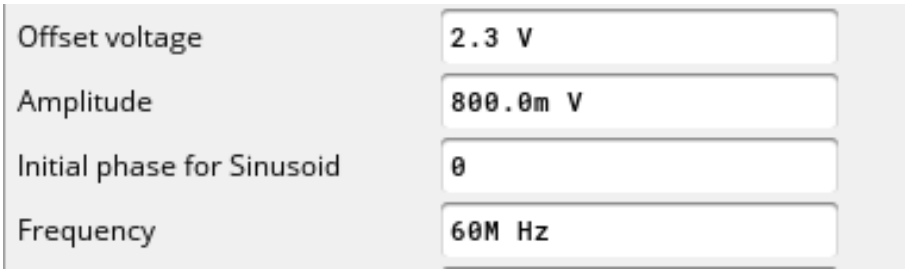


Second, we the transistor's parameters with multipliers equal to 2 to come up in the context of improving performance and to lower conduction losses for better efficiency. We'll set ratio W/L as a constant C to sweep this constant to find out what's the best value make the design work properly.

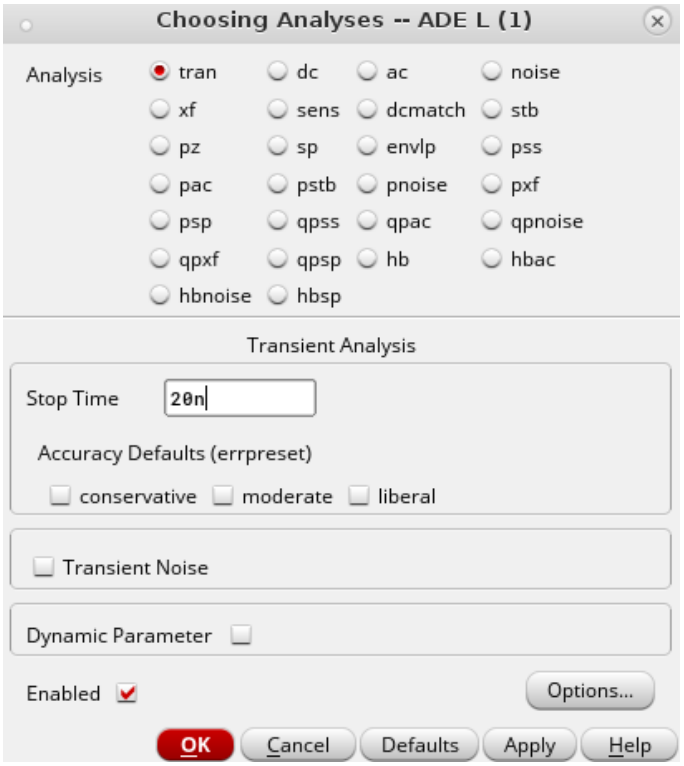


Also, we configure the $Vsin$ source to achieve the required specifications:

- $Vin, DC = 2.3V$
- $Vin, AC = A\ sin(2\pi ft)\ , f = 60MHz, A = 0.8V$

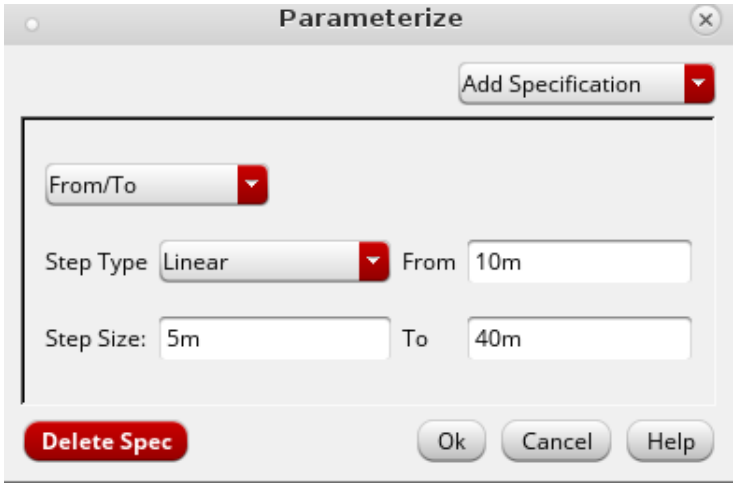


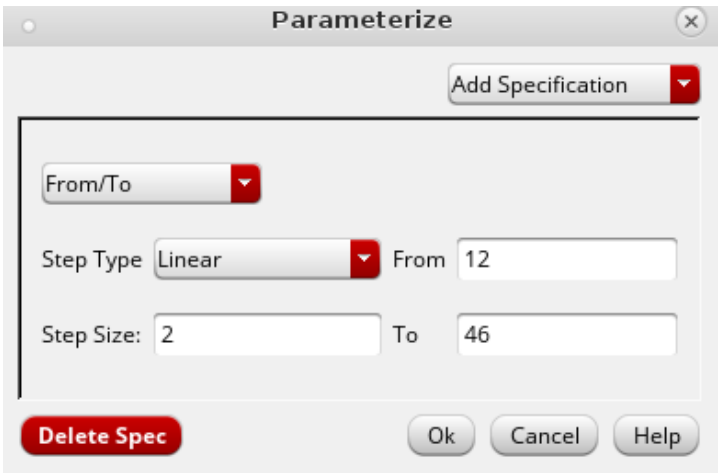
Running ADE XL testbench and choosing transient analysis using 20n as stop time just one period.



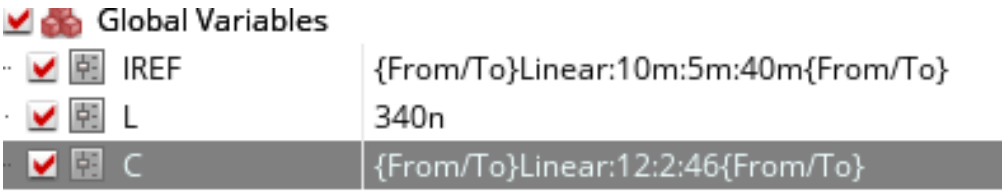
After that we'll sweep the constant C and the ideal current source's value to choose the best to meet the required specifications so:

- Sweep C from 12 to 46 with step size 2.
- Sweep IREF from 10m to 40m with step size 5m.



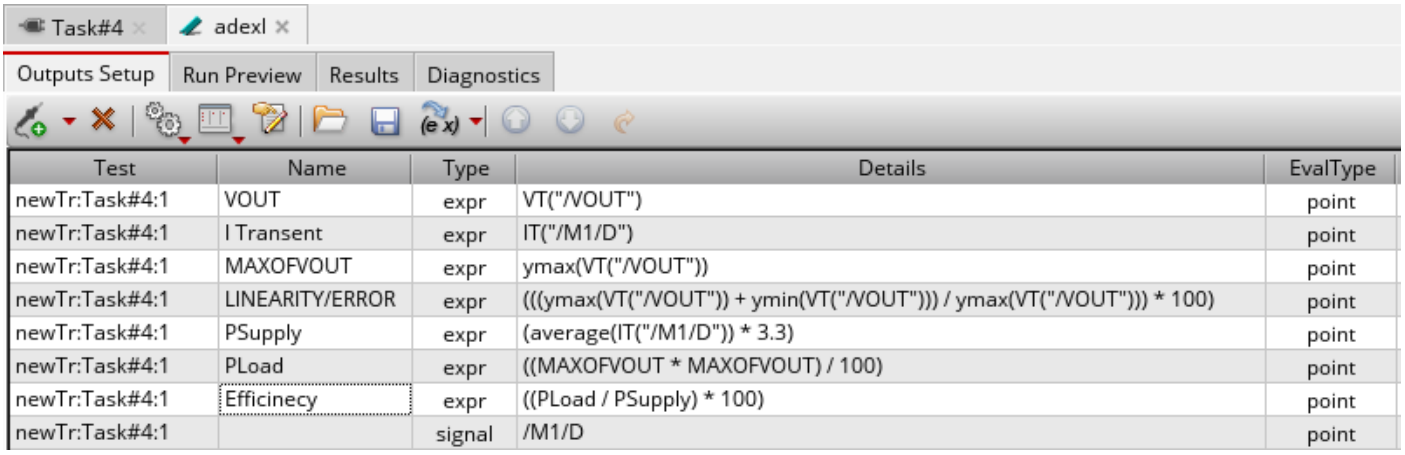


Also, choose the minimum length for the transistor thus the total global variables as shown in fig.



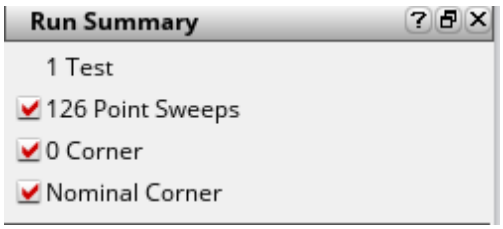
We'll write the total equations as shown in fig demonstrating that:

- VOUT is the transient value of the voltage output node.
- I Transent is the transient value of the current device.
- ERROR is the ability of the amplifier to faithfully reproduce the input signal at the output without introducing significant distortion.
- MAXOFVOUT is the max output voltage or the peak voltage of VOUT.
- PSupply is the total power dissipated in the device.
- PLoad is the output required power in the device as a power amplifer.
- Efficiency is the division of the output required power in the device over the total power dissipated.



Test	Name	Type	Details	EvalType
newTr:Task#4:1	VOUT	expr	VT("/VOUT")	point
newTr:Task#4:1	I Transent	expr	IT("/M1/D")	point
newTr:Task#4:1	MAXOFVOUT	expr	ymax(VT("/VOUT"))	point
newTr:Task#4:1	LINEARITY/ERROR	expr	(((ymax(VT("/VOUT")) + ymin(VT("/VOUT"))) / ymax(VT("/VOUT"))) * 100)	point
newTr:Task#4:1	PSupply	expr	(average(IT("/M1/D")) * 3.3)	point
newTr:Task#4:1	PLoad	expr	((MAXOFVOUT * MAXOFVOUT) / 100)	point
newTr:Task#4:1	Efficinecy	expr	((PLoad / PSupply) * 100)	point
newTr:Task#4:1		signal	/M1/D	point

Thus, we'll sweep over 126 points.

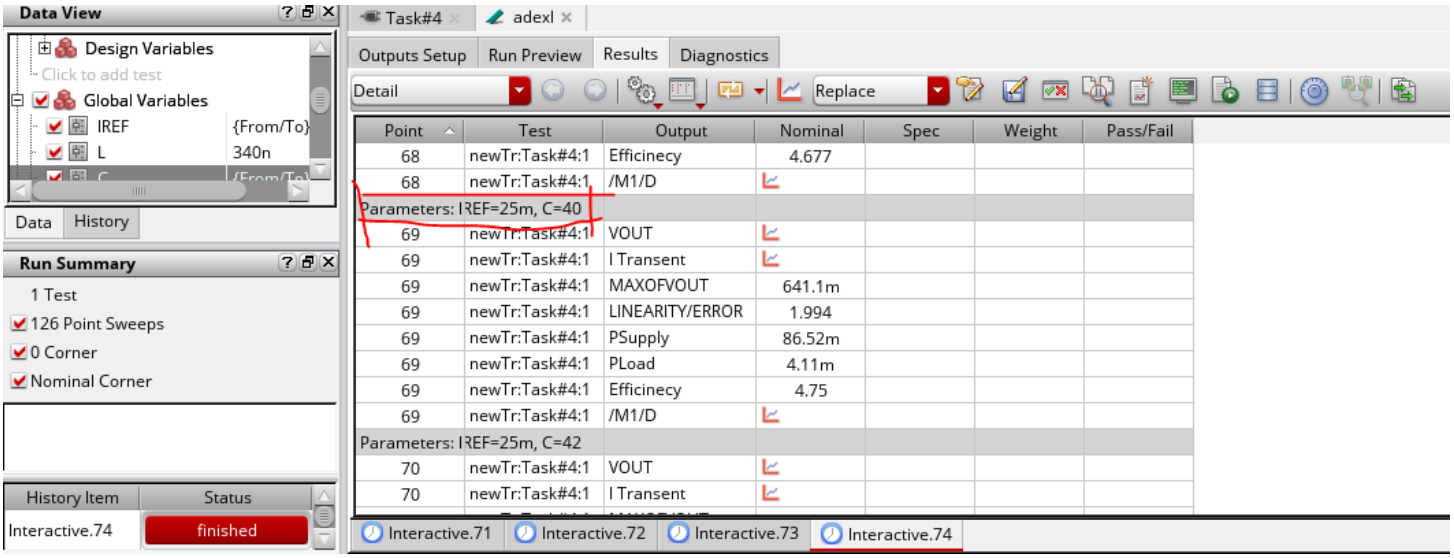


After the sweeping ‘step, we notice the most faithfully required values for C & IREF to achieve the required specifications:

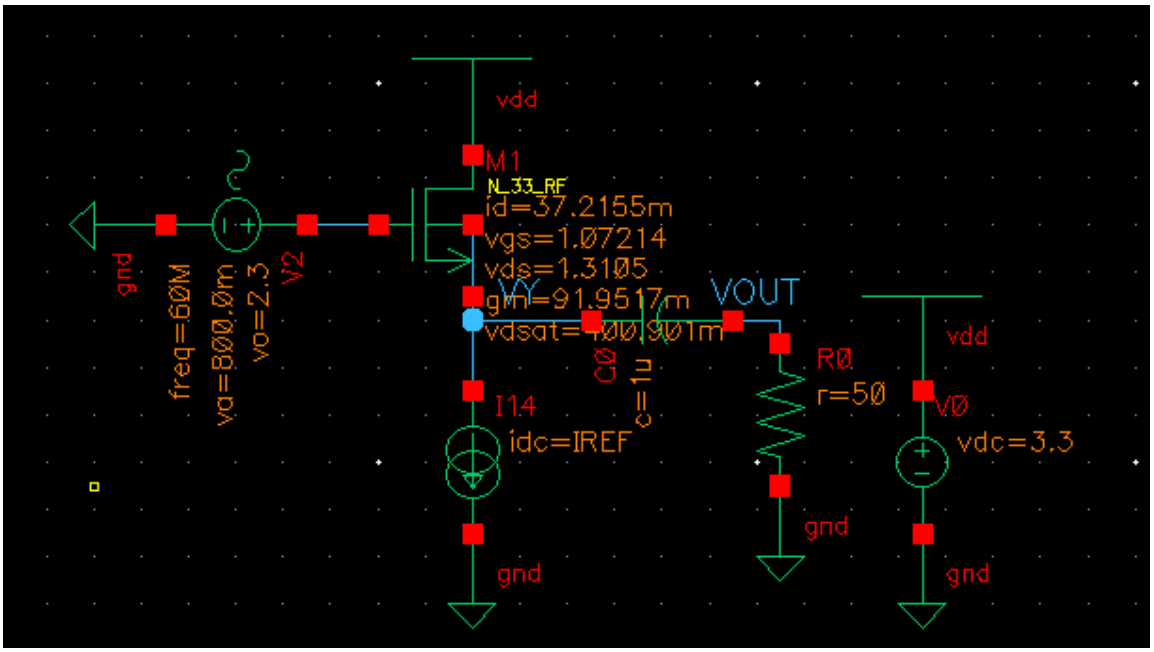
- $IREF = 25m$
- $C = 40$

We got all achieve the required specifications with:

1. $|Vout, peak| > 600mV$
2. $|Vout, max| - |Vout, min|\ Vout, max < 2.5\%$

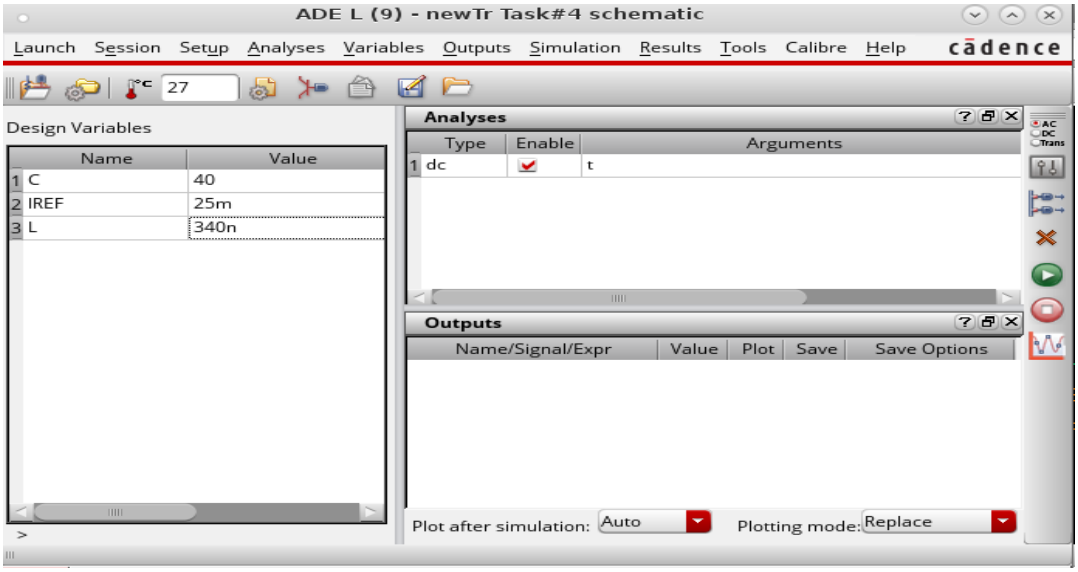


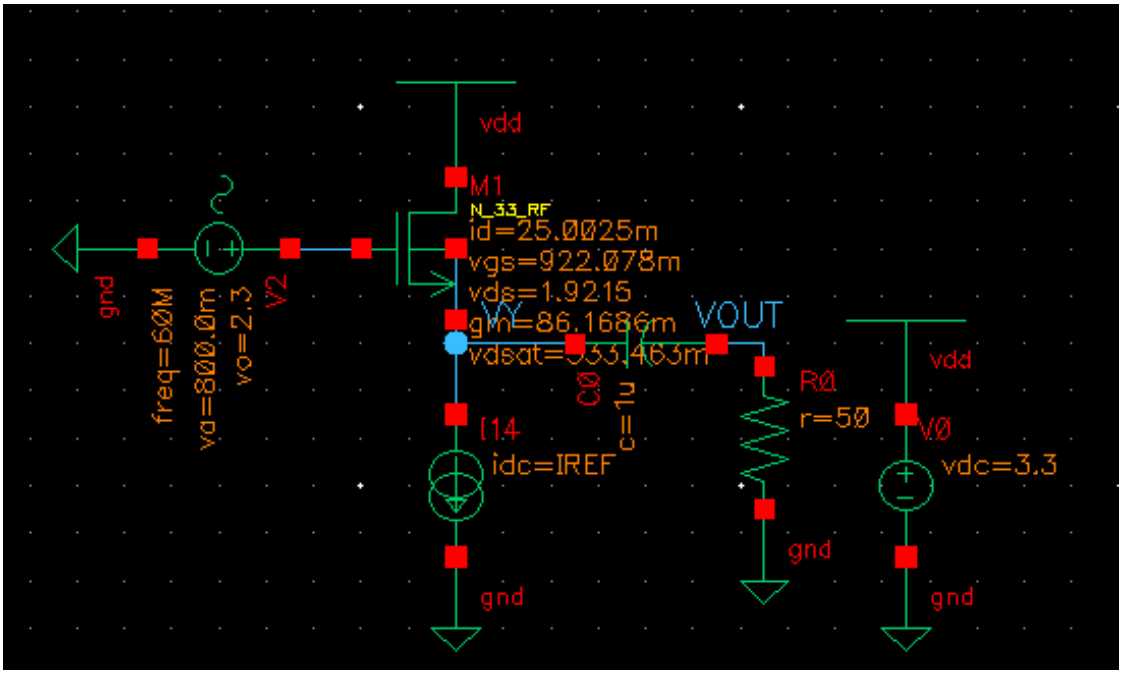
1. Schematic diagram with dimensions and component values annotated.

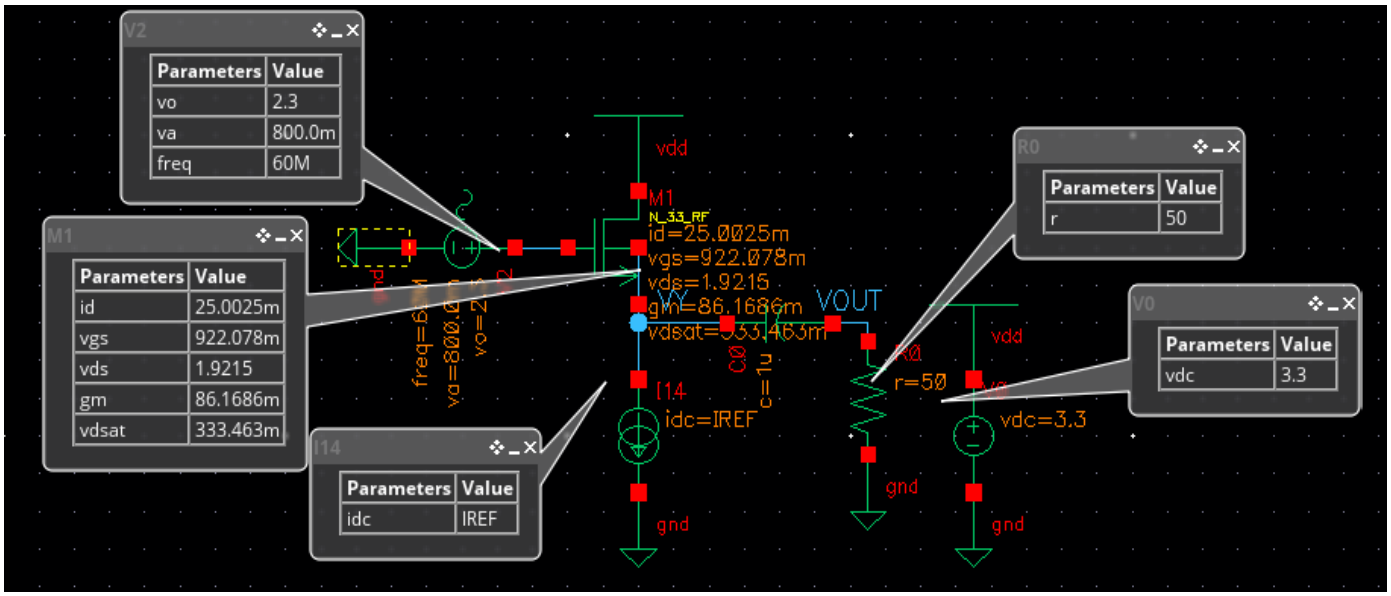


2. Schematic diagram with DC operating point annotated.

To get the DC operating point, we'll run ADE L testbench and set the design variables we got from ADE XL from the sweeping we made.







3. Transient simulation results to verify the required specifications:

Now we able to plot the required transient graphs thus:

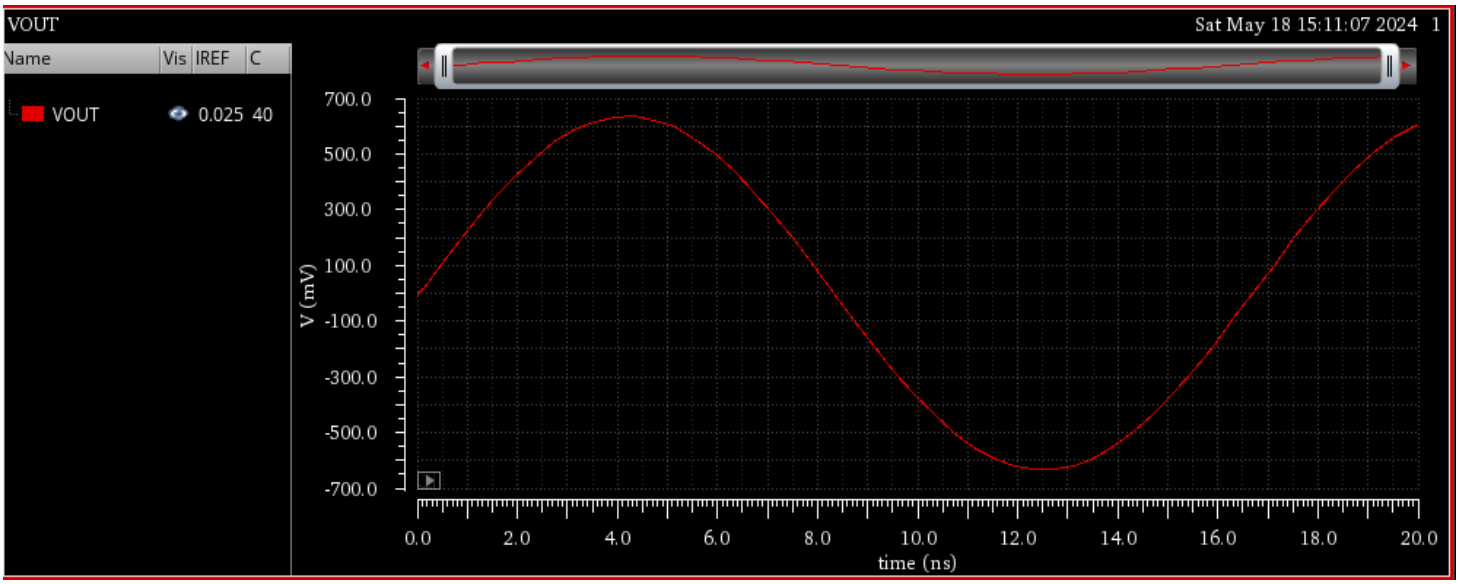


Figure 13: A complete period of Vout vs time.

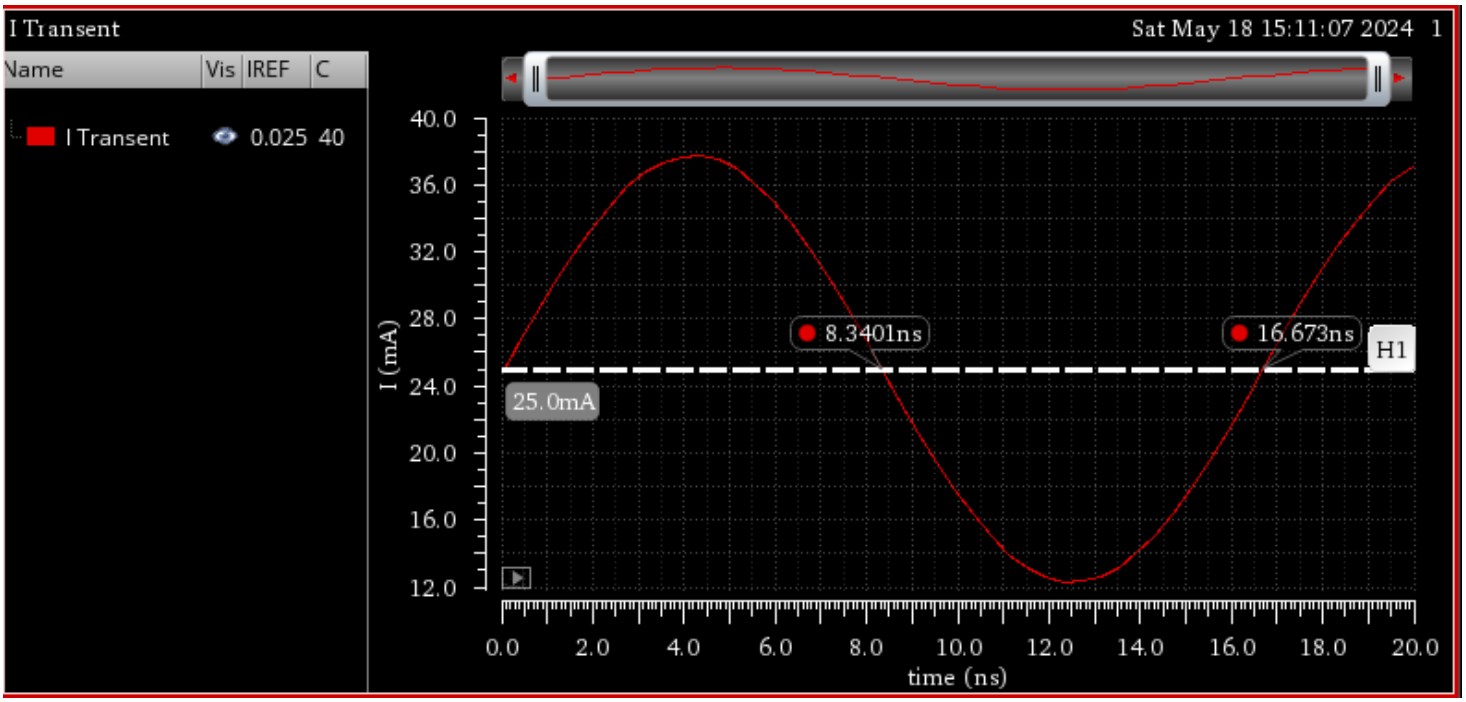
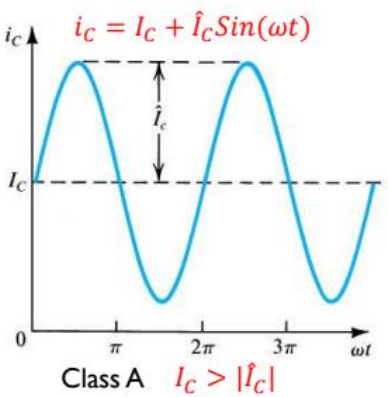


Figure 14: A complete period of I vs time.

As shown in fig 14, we verified that the device doesn't turn off and meet the specifications of class A power Amplifier.



4. Calculation of the efficiency using simulations and compare it with the theoretical equation.

Parameters: IREF=25m, C=40						
69	newTr:Task#4:1	VOUT				
69	newTr:Task#4:1	I Transent				
69	newTr:Task#4:1	MAXOFVOUT	641.1m			
69	newTr:Task#4:1	LINEARITY/ERROR	1.994			
69	newTr:Task#4:1	PSupply	86.52m			
69	newTr:Task#4:1	PLoad	4.11m			
69	newTr:Task#4:1	Efficinecy	4.75			
69	newTr:Task#4:1	/M1/D				

Simulated	Theoretical
$\eta = 4.75\%$	$\eta = \frac{P_{load}}{P_{source}} * 100$ $P_{Load} = \frac{(MAXOFVOUT)^2}{2^* R_L}$ $P_{source} = V_{CC} I_{Dc}$ $\therefore \quad \eta = \frac{(MAXVOUT)^2}{2^* R_L * V_{CC} * I_{DC}} * 100$ MAXVOUT=641.1m, RL=50 Ω, $I_{DC} = 25m$ VCC=3.3V $\therefore \quad \eta = 4.982\%$

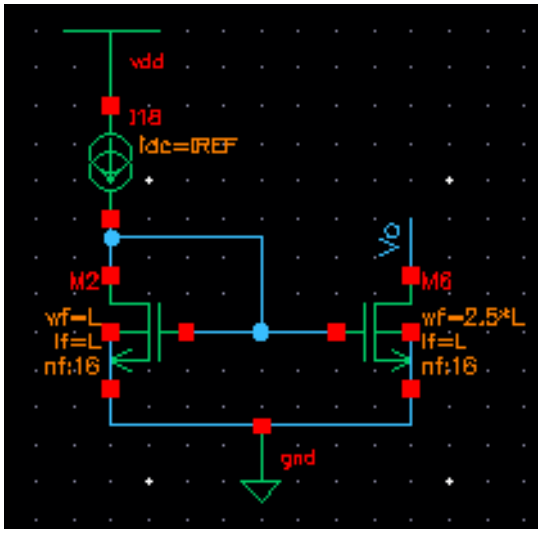
By observation we notice that there is a little difference between the two values and that may be because we deal with minimum length with 340n so consider short channel device thus the simulation work on a complex current equation so not the exact current in both or it can be not the exact value of MAXOFVOUT as we consider an approximated value.

$$I_d = \mu C_{ox} \frac{W_{eff}}{L_{eff}} \left[(V_{GS} - V_{th0}) - (1 + \frac{F_s \gamma}{4\sqrt{2\phi_s - V_{BS}}} + F_n) \frac{V_{DS}}{2} \right] V_{DS} \quad , \qquad \mu = \frac{\mu_{eff}}{1 + \frac{\mu_{eff} * V_{DS}}{v_{max} * L}}$$

5. **Replace the ideal current source with a current mirror with $IREF = 10mA$ using N_33_RF device, design the mirror using a suitable topology of your choice, and plot $Vout$ and $Imain$ device. Did the linearity degrade? Why/why not?**

Yes, it degraded due to the Rout of the mirroring design (compared to the ideal current source) and the usage of multiple components may lead to some non-idealities.

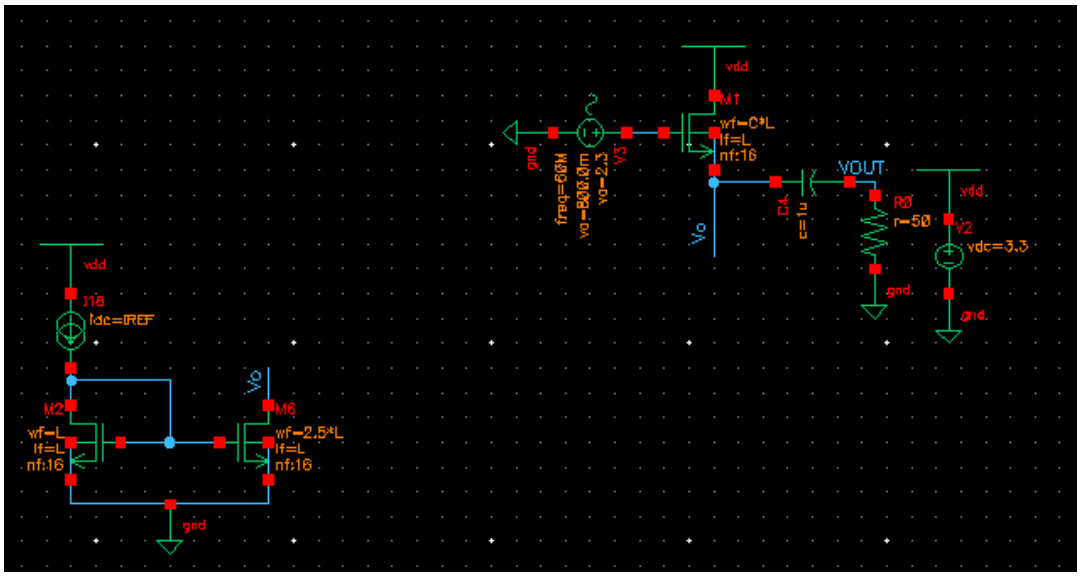
We used MOSFET current mirror as a suitable topology for our design so as we mentioned before we set the values of constant C and IREF based on the sweeping' steps so we design the area of the MOSFET become:



- Length=L (340n as usual)
- Width=2.5(as the used ideal current source of 10mA so we need current mirroring of 25mA based on the value chosen before but we able readjust it by increasing the number of multipliers& fingers and so on so that's as first as observation and then modified it) *L.
- We set the number of multiplier equal to 30 as primarily related to improving performance and the total output current capability of the current mirror circuit increases (it's not final value but we'll monitor and readjust it to suit our specifications).

CDF Parameter	Value	Display
Gate Finger Width	2.5*L M	off
Gate Length	L M	off
Gate Finger Number	16	off
Multiplier	30	off

Thus, the final design:



So, the result of the simulation using 30 multipliers, we notice here the error increase little and exit out of the required range but $Vout$ peak is still in safe, so what if we continue to increase the number of multipliers!

Design Variables

	Name	Value
1	C	40
2	IREF	10m
3	L	340n

> Results in /home/cadence/simulation/test/

Analyses

	Type	Enable	Arguments
1	tran	☑	0 20n

Outputs

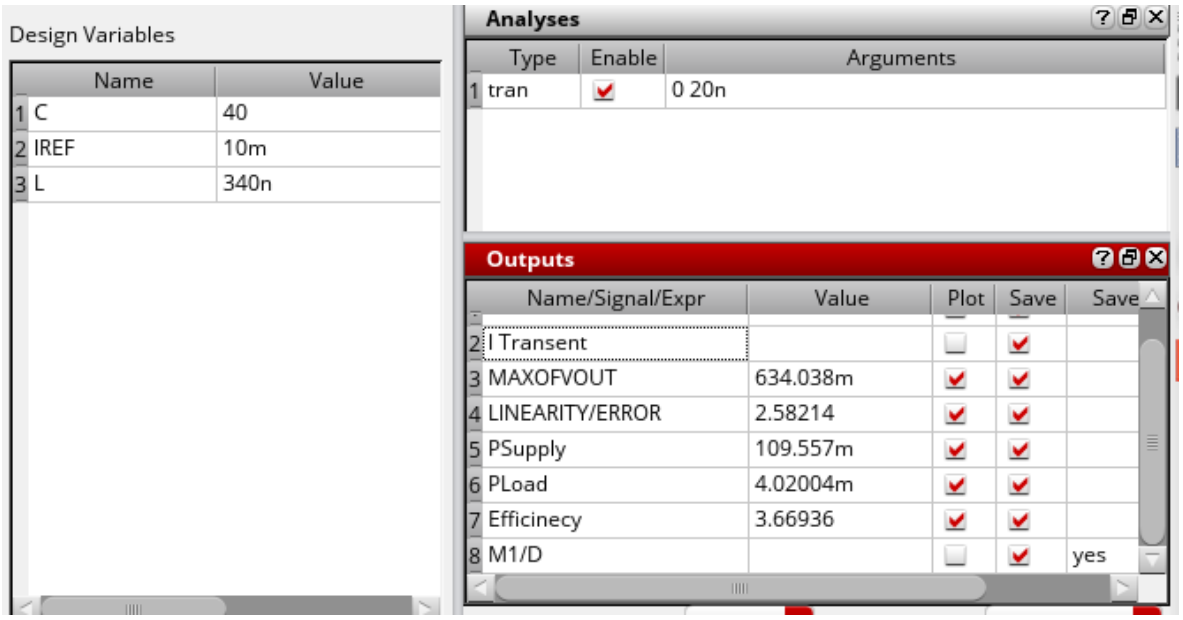
	Name/Signal/Expr	Value	Plot	Save	Save
2	I Transent		☐	☑	
3	MAXOFVOUT	634.632m	☑	☑	
4	LINEARITY/ERROR	2.65229	☑	☑	
5	PSupply	106.614m	☑	☑	
6	PLoad	4.02758m	☑	☑	
7	Efficinecy	3.77773	☑	☑	
8	M1/D		☐	☑	yes

Plot after simulation: Auto Plotting mode: Replace

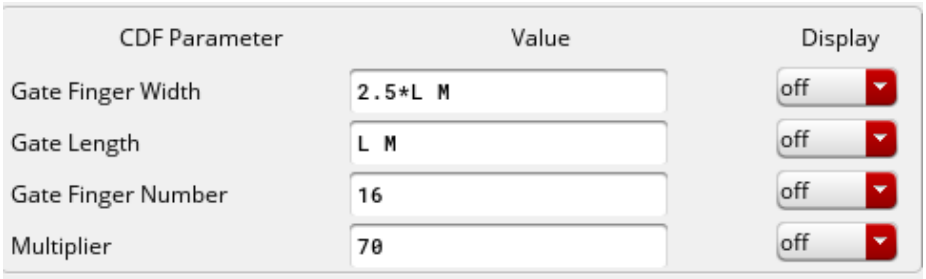
We'll increase the number of multipliers to 35 and check for the required values 'specifications

CDF Parameter	Value	Display
Gate Finger Width	2.5*L M	off
Gate Length	L M	off
Gate Finger Number	16	off
Multiplier	35	off

from fig, we notice the error decreased nearly 0.1 and Vout nearly 0.594, thus we can increase the number of multipliers again to make the error less than 2.5



As shown in below fig, we increased the number of multipliers to 70(double of its previous value) and check for specifications:



As shown in fig, after run here's we meet the required specifications:

1. $|Vout, peak| > 600mV$
2. $|Vout, max| - |Vout, min|\ Vout, max < 2.5\%$

but we sacrifice with some Important parameters:

- Power supply is the power dissipated in the design so by observation in the process of increasing the number of multipliers, we notice it increase by 18.386m Watt and can affect in thermal problems in the total device.
- We can neglect the decrease in the power load as it's very small change.
- We notice that the efficiency of the device decreased by 0.6045, it's may be bad for the quality

of the total device.

Design Variables

	Name	Value
1	C	40
2	IREF	10m
3	L	340n

> Results in /home/cadence/simulation/test/

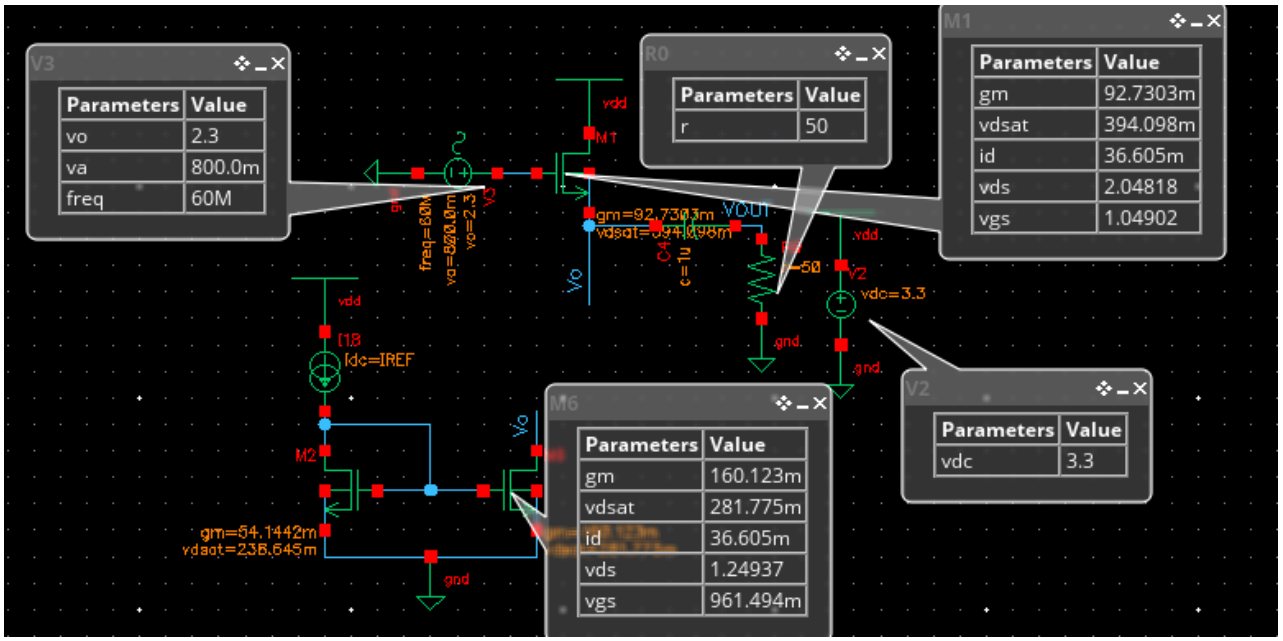
Analyses

	Type	Enable	Arguments
1	tran	☑	0 20n

Outputs

	Name/Signal/Expr	Value	Plot	Save	Save
2	I Transent		☐	☑	
3	MAXOFVOUT	629.788m	☑	☑	
4	LINEARITY/ERROR	2.35323	☑	☑	
5	PSupply	125.011m	☑	☑	
6	PLoad	3.96633m	☑	☑	
7	Efficinecy	3.1728	☑	☑	
8	M1/D		☐	☑	yes

Plot after simulation: Auto Plotting mode: Replace



So, to answer to this question, we'll compare the two designs shown in fig and fig:

Device with the ideal current source *Device with a suitable topology for*

		current mirroring
Vout Peak	641.1mV	629.788mV
Linearity/Error	1.994	2.35523
Power supply	125.011mW	86.52mW
Efficiency	4.75	3.17