Final Project of RTLtoGDSII Physical Design Diploma

MIPS_16 Physical Design

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$1GHz + 0.8\ utilization$ with Total Area $0.03713\ \mathrm{mm}^2$

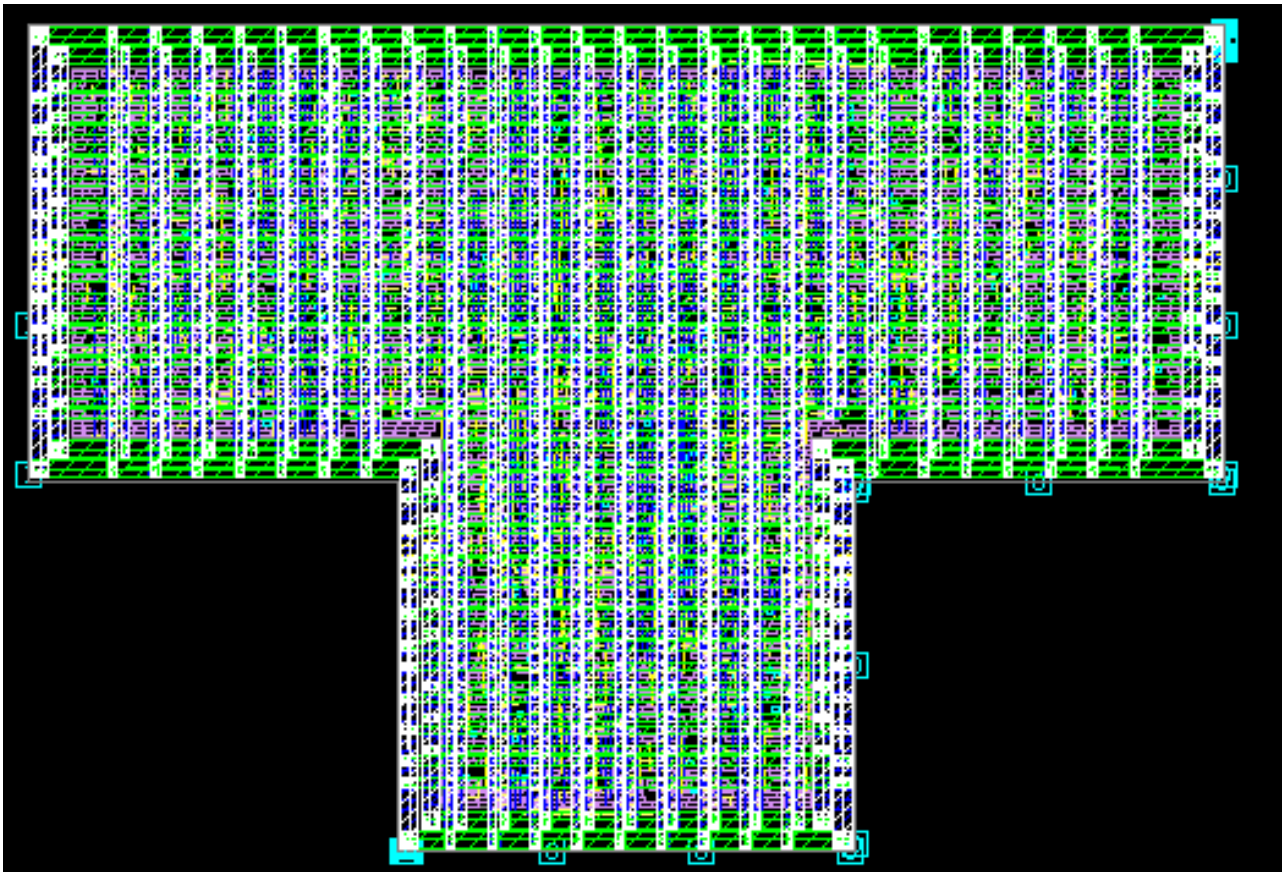


Table of Contents

Project Specs 3
SDC Constraints 4
Synthesis Results 5
  First Trial 5
  Second Trial 6
  Third Trial 7
Formal verification Post Synthesis 8
PnR Hard Constraints 9
PnR Flow 11
  Floorplanning 11
  Powerplanning 11
  Placement 12
  CTS 14
  Routing & Chip finishing 15
Formal verification Post PnR 22

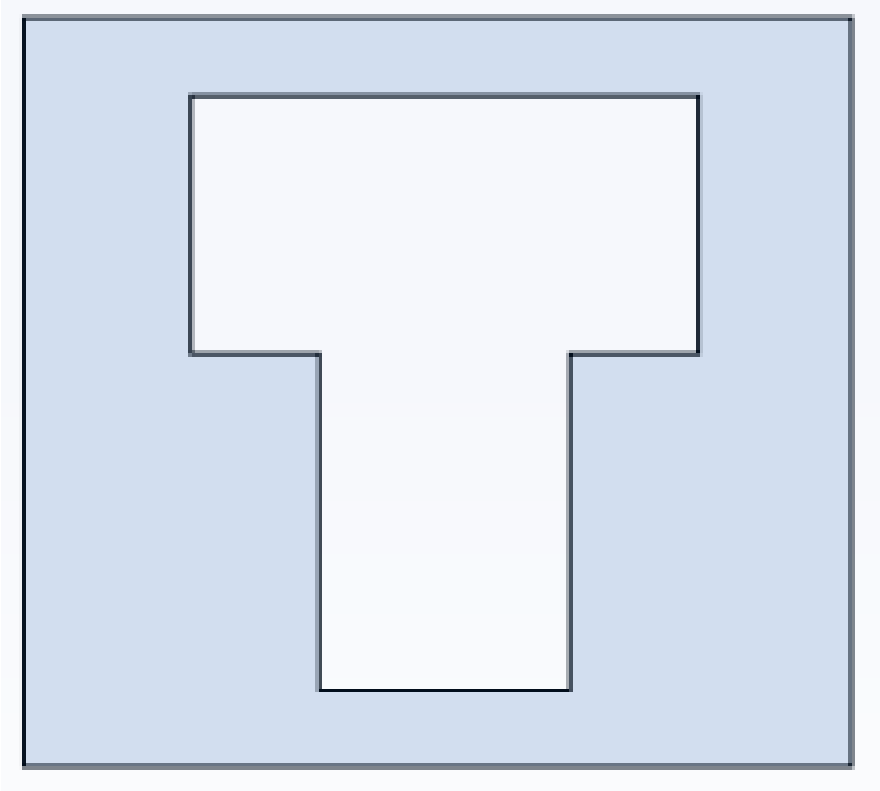
Project Specs

RTL: MIPS-16.

- Pins to be on metal4 and metal5.
    - Inputs on top side and left side.
    - Outputs on right and bottom side.
- Floorplan to be T-shaped.
- IR not to exceed 2%.
- Formality is passing (RTL vs pre-layout netlist and RTL vs post-layout netlist).

Challenge is to have the fastest frequency and the smallest area.

Starting point should be clock period of 4ns and same area as if it is utilization 0.25 (note Input delay and output delay are factors (30%) from Clock Period, Clock uncertainties depend on the tech node should not be touched 0.35 ps)



SDC Constraints

First, we create a clock object named clk on the port clk with clock period = **4 ns** (i.e. 250 MHz), rising edge at 0 ns, falling edge at 2 ns (50% duty) and finally attach this clock to the physical port named clk, knowing that we will change this period later.

Second, we define **max input/output delay** for primary inputs(except the clk port)/outputs as factors (30%) from Clock Period.

Third, we set clock uncertainty (jitter/skew margin) to **0.35 ns** on the clock(s) returned by [get_clocks] as a factor of the clock period(nearly 12%).

Fourth, we declare a **false path** for **hold analysis** for paths *originating* from all inputs (except clk) and for any paths ending at primary outputs.

Finally, we define group_path commands for reporting and for applying group-specific constraints.

```
create_clock -name clk -period 4 -waveform {0 2} [get_ports clk]

set_input_delay -max 1.2 -clock [get_clocks clk] [remove_from_collection [all_inputs] [get_ports clk]]

set_output_delay -max 1.2 -clock [get_clocks clk] [all_outputs]

set_clock_uncertainty 0.35 [get_clocks]

set_false_path -hold -from [remove_from_collection [all_inputs] [get_ports clk]]

set_false_path -hold -to [all_outputs]

group_path -name INREG -from [all_inputs]

group_path -name REGOUT -to [all_outputs]

group_path -name INOUT -from [all_inputs] -to [all_outputs]

group_path -name REG2REG -from [all_registers] -to [all_registers]
```

Synthesis Results

First Trial

At Clock period 4ns, we got max worst slack is 2.08 which is very large and can be optimized and decrease the clock period.

```
Startpoint: reset (input port clocked by clk)
Endpoint: reg_file/reg_array_reg[0][0]
          (rising edge-triggered flip-flop clocked by clk)
Path Group: INREG
Path Type: max

-------------------------------------------------------------------------

data required time                                3.62
data arrival time                                -1.54

-------------------------------------------------------------------------

slack (MET)                                       2.08
```

Other results, knowing that the hold violations will be solved lately in CTS stage or in primetime:

```
Timing Path Group 'INREG'
-----------------------------------
Levels of Logic:                7.00
Critical Path Length:           0.34
Critical Path Slack:            2.08
Critical Path Clk Period:       4.00
Total Negative Slack:           0.00
No. of Violating Paths:         0.00
Worst Hold Violation:           0.00
Total Hold Violation:           0.00
No. of Hold Violations:         0.00
-----------------------------------
```

```
Timing Path Group 'REGOUT'
-----------------------------------
Levels of Logic:                0.00
Critical Path Length:           0.10
Critical Path Slack:            2.35
Critical Path Clk Period:       4.00
Total Negative Slack:           0.00
No. of Violating Paths:         0.00
Worst Hold Violation:           0.00
Total Hold Violation:           0.00
No. of Hold Violations:         0.00
-----------------------------------
```

```
Timing Path Group 'REG2REG'
-----------------------------------
Levels of Logic:               15.00
Critical Path Length:           0.79
Critical Path Slack:            2.82
Critical Path Clk Period:       4.00
Total Negative Slack:           0.00
No. of Violating Paths:         0.00
Worst Hold Violation:          -0.23
Total Hold Violation:        -920.61
No. of Hold Violations:      4240.00
-----------------------------------
```

```
Area
-----------------------------------
Combinational Area:    17508.918128
Noncombinational Area: 19288.191353
Buf/Inv Area:           3037.454006
Net Area:                  0.000000
-----------------------------------
Cell Area:             36797.109481
Design Area:           36797.109481
```

Second Trial

In this trial we will decrease the period to half its value from first trial so it will become 2ns and change the other parameters.

```
create_clock -name clk -period 2 -waveform {0 1} [get_ports clk]

set_input_delay -max 0.6 -clock [get_clocks clk] [remove_from_collection [all_inputs] [get_ports clk]]

set_output_delay -max 0.6 -clock [get_clocks clk] [all_outputs]

set_clock_uncertainty 0.175 [get_clocks]
```

At Clock period 2ns, we got max worst slack is 0.85 which is still large and can be optimized, decreasing the clock period.

Startpoint: reset (input port clocked by clk)	
Endpoint: reg_file/reg_array_reg[0][0]	
(rising edge-triggered flip-flop clocked by clk)	
Path Group: INREG	
Path Type: max	
data required time	1.79
data arrival time	-0.94
slack (MET)	0.85

Other results, knowing that the hold violations will be solved lately in CTS stage or in primetime:

Timing Path Group 'REGOUT'	
Levels of Logic:	0.00
Critical Path Length:	0.10
Critical Path Slack:	1.12
Critical Path Clk Period:	2.00
Total Negative Slack:	0.00
No. of Violating Paths:	0.00
Worst Hold Violation:	0.00
Total Hold Violation:	0.00
No. of Hold Violations:	0.00

Timing Path Group 'INREG'	
Levels of Logic:	7.00
Critical Path Length:	0.34
Critical Path Slack:	0.85
Critical Path Clk Period:	2.00
Total Negative Slack:	0.00
No. of Violating Paths:	0.00
Worst Hold Violation:	0.00
Total Hold Violation:	0.00
No. of Hold Violations:	0.00

Timing Path Group 'REG2REG'	
Levels of Logic:	15.00
Critical Path Length:	0.79
Critical Path Slack:	1.00
Critical Path Clk Period:	2.00
Total Negative Slack:	0.00
No. of Violating Paths:	0.00
Worst Hold Violation:	-0.05
Total Hold Violation:	-178.95
No. of Hold Violations:	4227.00

Area	
Combinational Area:	17508.918128
Noncombinational Area:	19288.191353
Buf/Inv Area:	3037.454006
Net Area:	0.000000
Cell Area:	36797.109481
Design Area:	36797.109481

Third Trial

In this trial we will decrease the period to half its value from first trial so it will become 1ns and keep the other parameters as we consider the worst cases occur.

```
create_clock -name clk -period 1 -waveform {0 0.5} [get_ports clk]

set_input_delay -max 0.6 -clock [get_clocks clk] [remove_from_collection [all_inputs] [get_ports clk]]

set_output_delay -max 0.6 -clock [get_clocks clk] [all_outputs]

set_clock_uncertainty 0.175 [get_clocks]
```

At Clock period 1ns, we got max worst slack is -0.01 which the max optimization we got in the synthesis stage so will continue with this value in the pnr.

Startpoint: reset (input port clocked by clk)	
Endpoint: reg_file/reg_array_reg[0][0]	
(rising edge-triggered flip-flop clocked by clk)	
Path Group: INREG	
Path Type: max	
data required time	0.79
data arrival time	-0.80
slack (MET)	-0.01

Other results, knowing that the hold violations will be solved lately in CTS stage or in primetime:

```
Timing Path Group 'REGOUT'
-----------------------------------
Levels of Logic:                0.00
Critical Path Length:           0.11
Critical Path Slack:            0.12
Critical Path Clk Period:       1.00
Total Negative Slack:           0.00
No. of Violating Paths:         0.00
Worst Hold Violation:           0.00
Total Hold Violation:           0.00
No. of Hold Violations:         0.00
-----------------------------------

Timing Path Group 'REG2REG'
-----------------------------------
Levels of Logic:               15.00
Critical Path Length:           0.71
Critical Path Slack:            0.08
Critical Path Clk Period:       1.00
Total Negative Slack:           0.00
No. of Violating Paths:         0.00
Worst Hold Violation:          -0.04
Total Hold Violation:        -178.95
No. of Hold Violations:      4235.00
-----------------------------------
```

```
Timing Path Group 'INREG'
-----------------------------------
Levels of Logic:                5.00
Critical Path Length:           0.20
Critical Path Slack:           -0.01
Critical Path Clk Period:       1.00
Total Negative Slack:          -0.11
No. of Violating Paths:        16.00
Worst Hold Violation:           0.00
Total Hold Violation:           0.00
No. of Hold Violations:         0.00
-----------------------------------
Area
-----------------------------------
Combinational Area:    17281.488136
Noncombinational Area: 19288.191353
Buf/Inv Area:           2824.388013
Net Area:                  0.000000
-----------------------------------
Cell Area:             36569.679489
Design Area:           36569.679489
```

Formal verification Post Synthesis

```
*****************************************************
Report          : failing_points

Reference       : Ref:/WORK/mips_16
Implementation  : Imp:/WORK/mips_16
Version         : G-2012.06-SP2
Date            : Fri Sep  5 14:17:40 2014
*****************************************************

No failing compare points.

1
```

```
********************************* Verification Results *************************
********
Verification SUCCEEDED
   ATTENTION: synopsys_auto_setup mode was enabled.
              See Synopsys Auto Setup Summary for details.
---------------------------------------------------------
 Reference design: Ref:/WORK/mips_16
 Implementation design: Imp:/WORK/mips_16
 47 Passing compare points
-------------------------------------------------------------------------------
--------
Matched Compare Points     BBPin    Loop   BBNet     Cut    Port     DFF     LAT
   TOTAL
-------------------------------------------------------------------------------
--------
Passing (equivalent)           0       0       0       0      32      15       0
      47
Failing (not equivalent)       0       0       0       0       0       0       0
       0
Not Compared
  Constant reg                                                   129       0
     129
```

PnR Hard Constraints

- Pins to be on metal4 and metal5.
    - Inputs on top side and left side.
    - Outputs on right and bottom side.
- Floorplan to be T-shaped.

We make trails on core_utilization but we reach to 0.8 which is suitable for congestion and get clean physical DRCS at the same time get the minimum area possible.

```
set_pin_physical_constraints -pin_name "clk" -exclude_sides {4,3,5,6}

set_pin_physical_constraints -pin_name "reset" -exclude_sides {4,3,5,6}

for {set i 0} {$i <= 15} {incr i} {

   set_pin_physical_constraints -pin_name "pc_out[$i]" -exclude_sides {1,2,7,8}

   set_pin_physical_constraints -pin_name "alu_result[$i]" -exclude_sides {1,2,7,8}

}

initialize_rectilinear_block -shape T -control_type ratio -core_side_dim {1.0 1.0 1.0 1.0 1.0 1.0} -
orientation N -core_utilization 0.8 -row_core_ratio 1.00 -start_first_row -flip_first_row -
left_io2core 12.4 -right_io2core 12.4 -top_io2core 12.4 -bottom_io2core 12.4 -keep_io_place
```

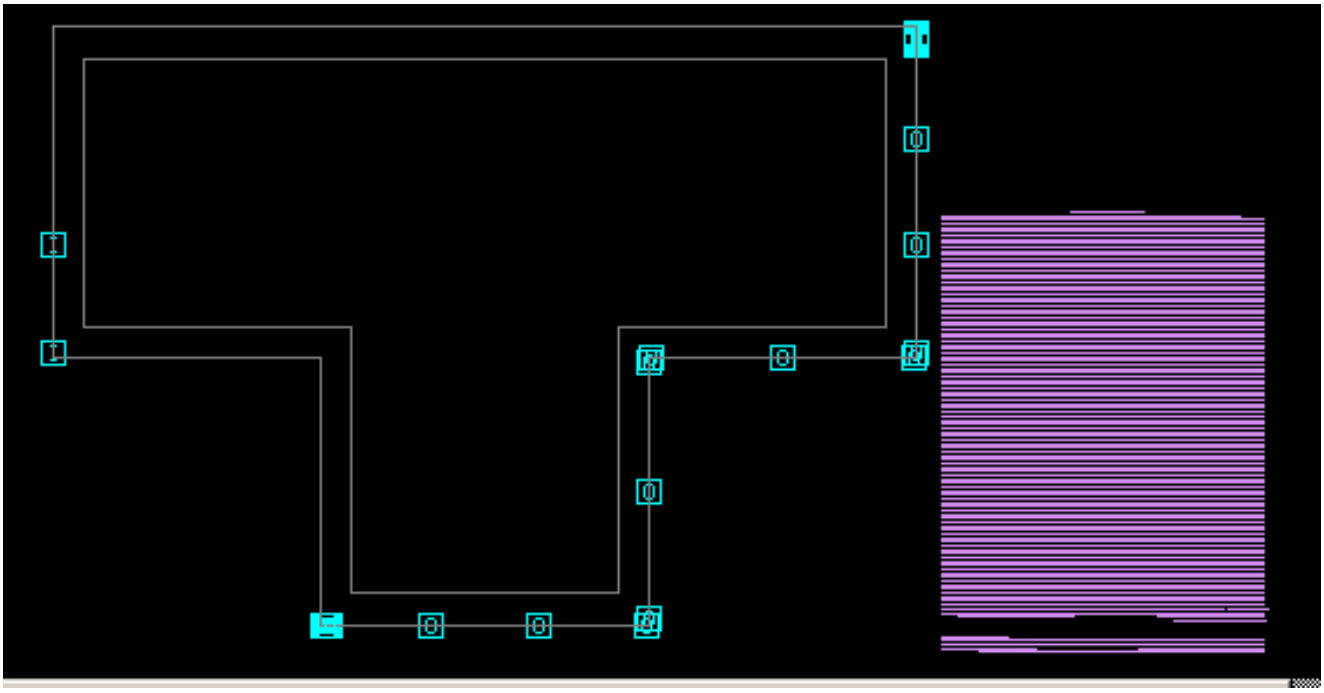
We make the last three layers 10,9,8 for power mesh only with these constraints so 7,6,5,4,3,2 for routing.

```
## Define Power Ring

set_fp_rail_constraints -set_ring -nets {VDD VSS} -horizontal_ring_layer { metal9 } \

-vertical_ring_layer { metal8 metal10 } -ring_spacing 0.8 -ring_width 5 -ring_offset 0.8 \

-extend_strap core_ring

## Define Power Mesh

set_fp_rail_constraints -add_layer -layer metal10 -direction vertical -max_strap 128 -
min_strap 25 -min_width 2.5 -spacing minimum

set_fp_rail_constraints -add_layer -layer metal9 -direction horizontal -max_strap 128 -
min_strap 25 -min_width 2.5 -spacing minimum

set_fp_rail_constraints -add_layer -layer metal8 -direction vertical -max_strap 128 -
min_strap 25 -min_width 2.5 -spacing minimum
```

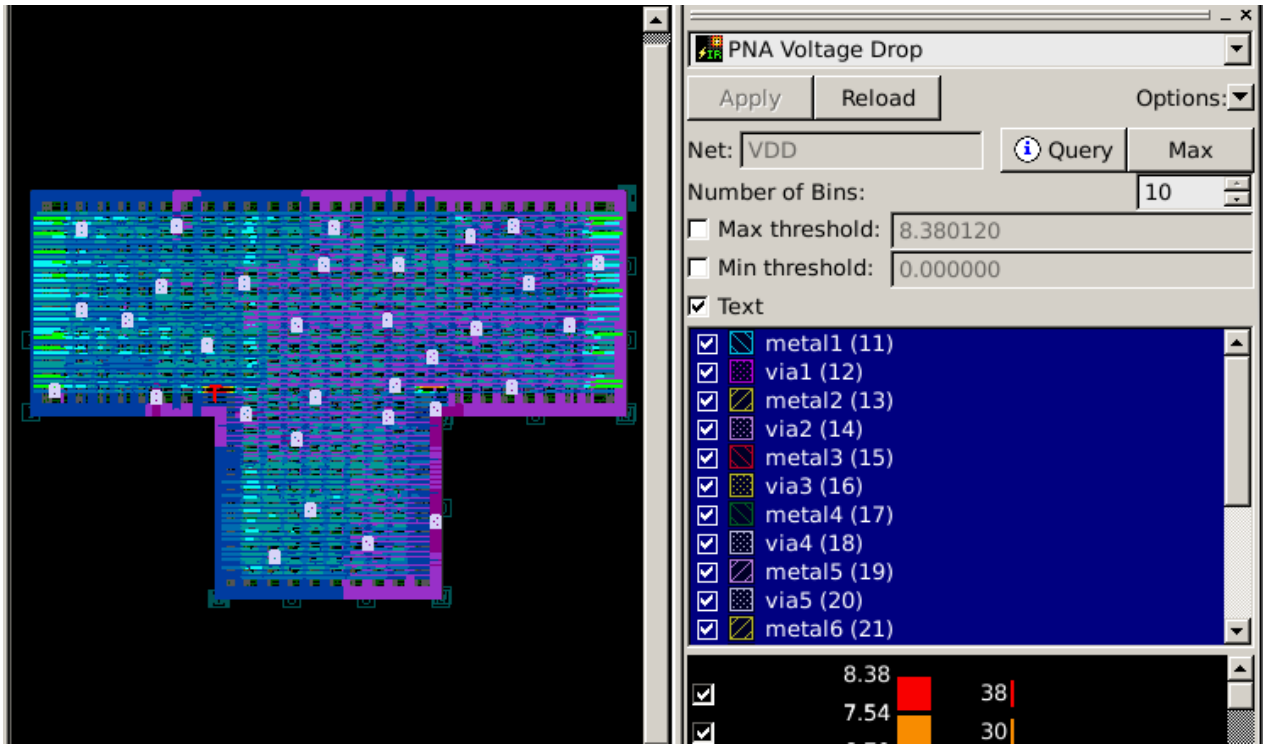
```
### Set Clock Physical Constraints

## Clock Non-Default Ruls (NDR) - Set it to be double width and double spacing

define_routing_rule my_route_rule  \

  -widths   {metal5 0.14 metal6 0.28 metal7 0.28} \

  -spacings {metal5 0.14 metal6 0.28 metal7 0.28}
```

PnR Flow

Floorplanning



Powerplanning



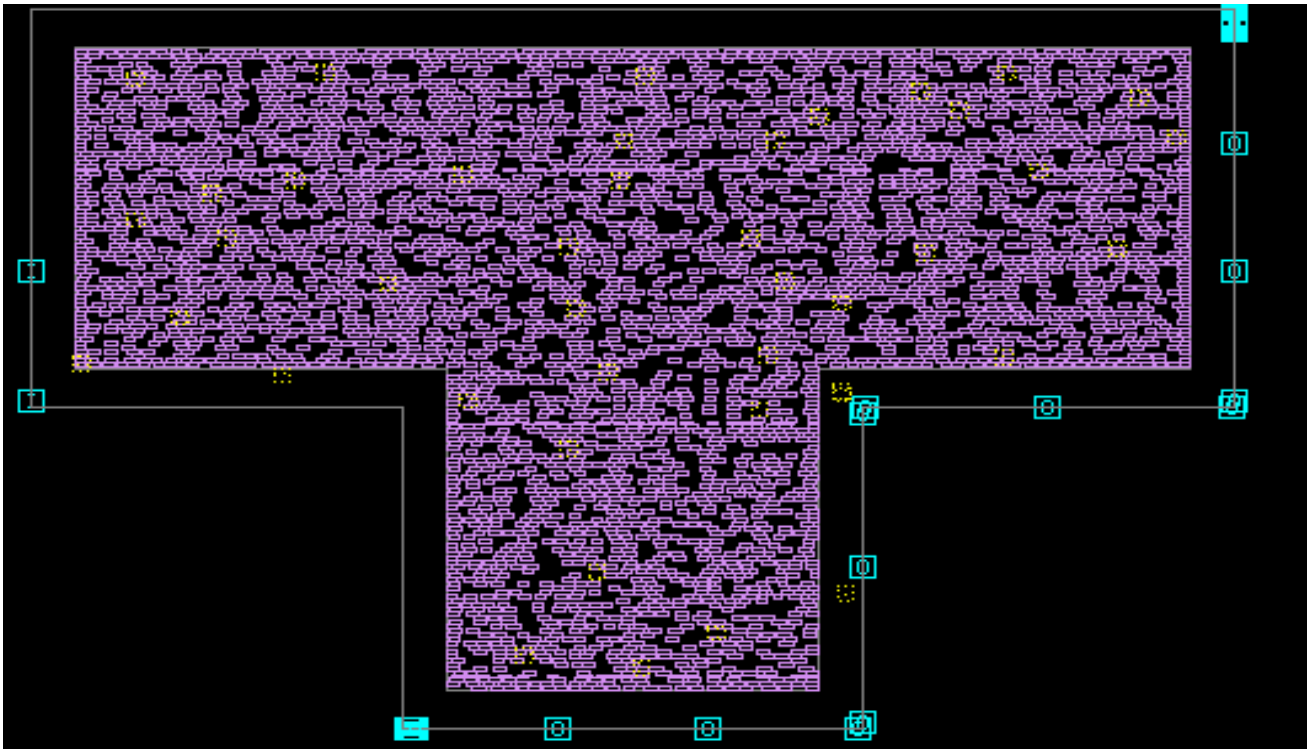
Placement

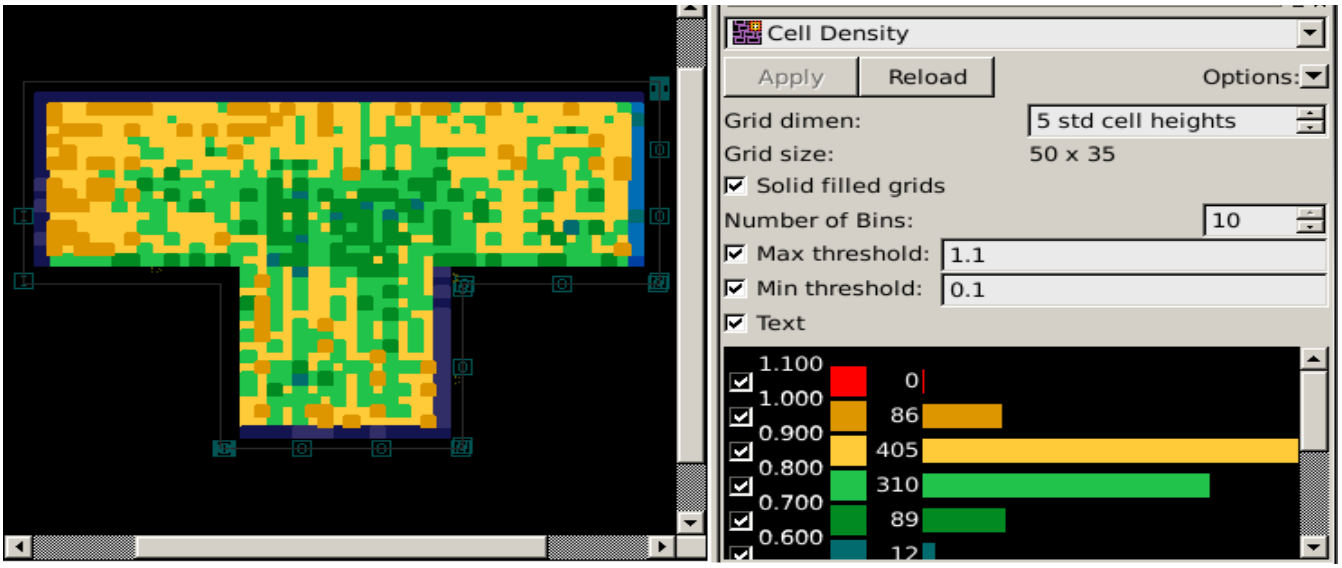
We create routing blockage in different places in the metal 2 as it has a lot of short DRCs so it will help.

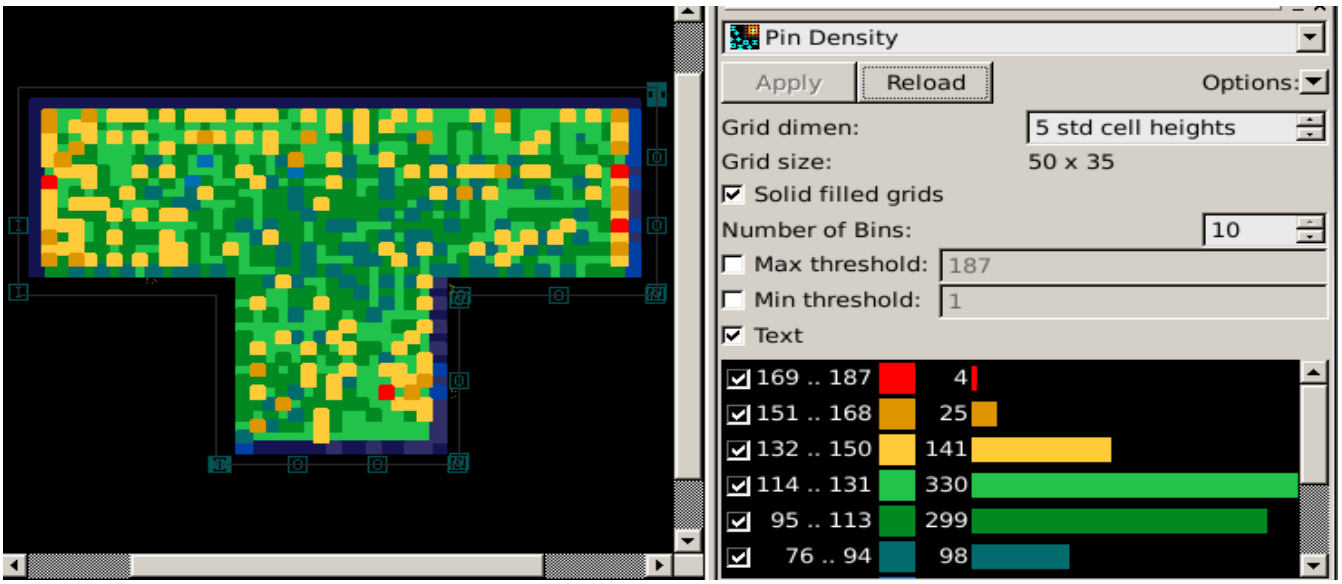
```
create_routing_blockage -layers metal2Blockage -bbox {{184.0750 169.3400} {185.300 171.5800}}
create_routing_blockage -layers metal2Blockage -bbox {{179.410 143.1200} {197.27 172.38}}
create_routing_blockage -layers metal2Blockage -bbox {{188.72 120.7250} {193.85 125.5600}}
create_routing_blockage -layers metal2Blockage -bbox {{142.55 34.7150} {146.73 39.3250}}
create_routing_blockage -layers metal2Blockage -bbox {{177.96 84.43} {203.92 110.44}}
create_routing_blockage -layers metal2Blockage -bbox {{141.6 32.92} {145.4585 39.5600}}
create_routing_blockage -layers metal2Blockage -bbox {{178.27 86.3200} {199.4265 111.1}}
create_routing_blockage -layers metal2Blockage -bbox {{308.61 173.12} {318.75 180.4}}
```

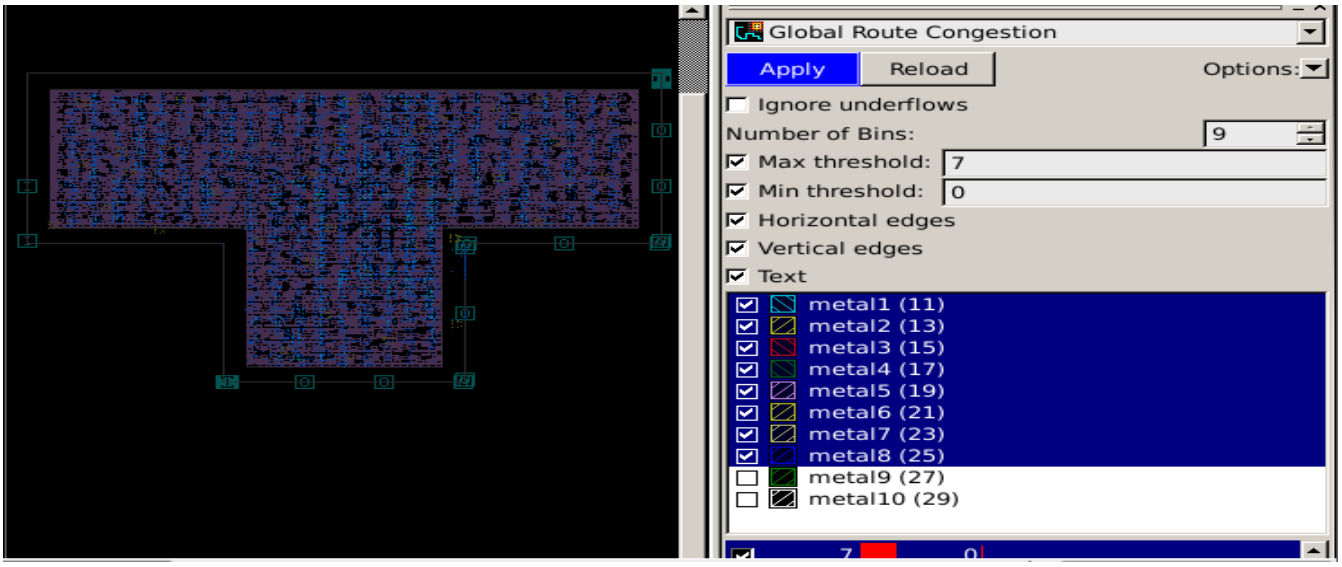
make place_opt its target option is congestion with its high effort

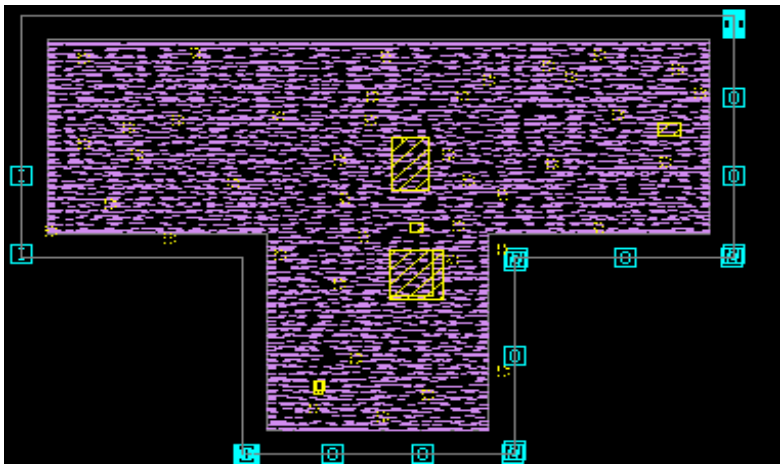
```
place_opt -effort high -congestion

## OPTIMIZATION

psynopt -congestion
```



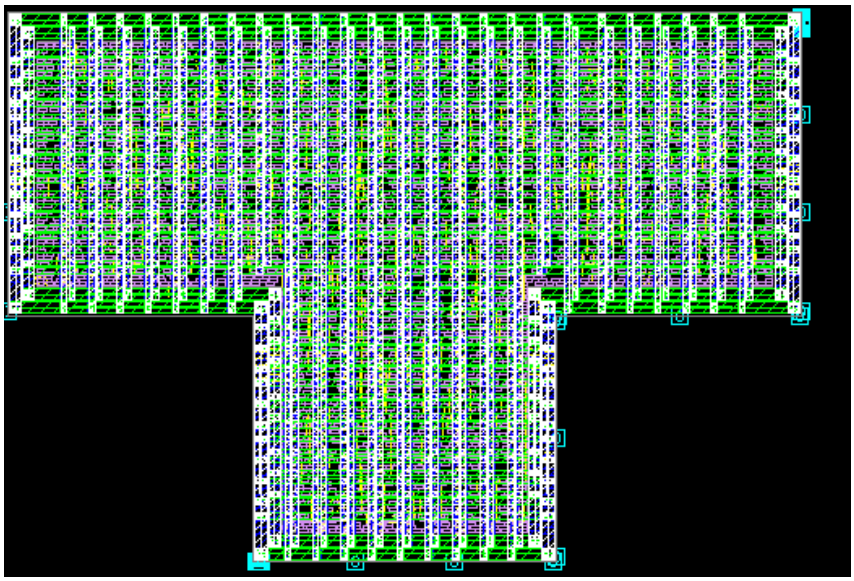

Cell Density
Apply
Reload
Options:
Grid dimen:
5 std cell heights
Grid size:
50 x 35
Solid filled grids
Number of Bins:
10
Max threshold:
1.1
Min threshold:
0.1
Text
1.100
1.000
0.900
0.800
0.700
0.600
0
86
405
310
89
12


Pin Density
Apply
Reload
Options:
Grid dimen:
5 std cell heights
Grid size:
50 x 35
Solid filled grids
Number of Bins:
10
Max threshold:
187
Min threshold:
1
Text
169 .. 187
151 .. 168
132 .. 150
114 .. 131
95 .. 113
76 .. 94
4
25
141
330
299
98


Global Route Congestion
Apply
Reload
Options:
Ignore underflows
Number of Bins:
9
Max threshold:
7
Min threshold:
0
Horizontal edges
Vertical edges
Text
metal1 (11)
metal2 (13)
metal3 (15)
metal4 (17)
metal5 (19)
metal6 (21)
metal7 (23)
metal8 (25)
metal9 (27)
metal10 (29)



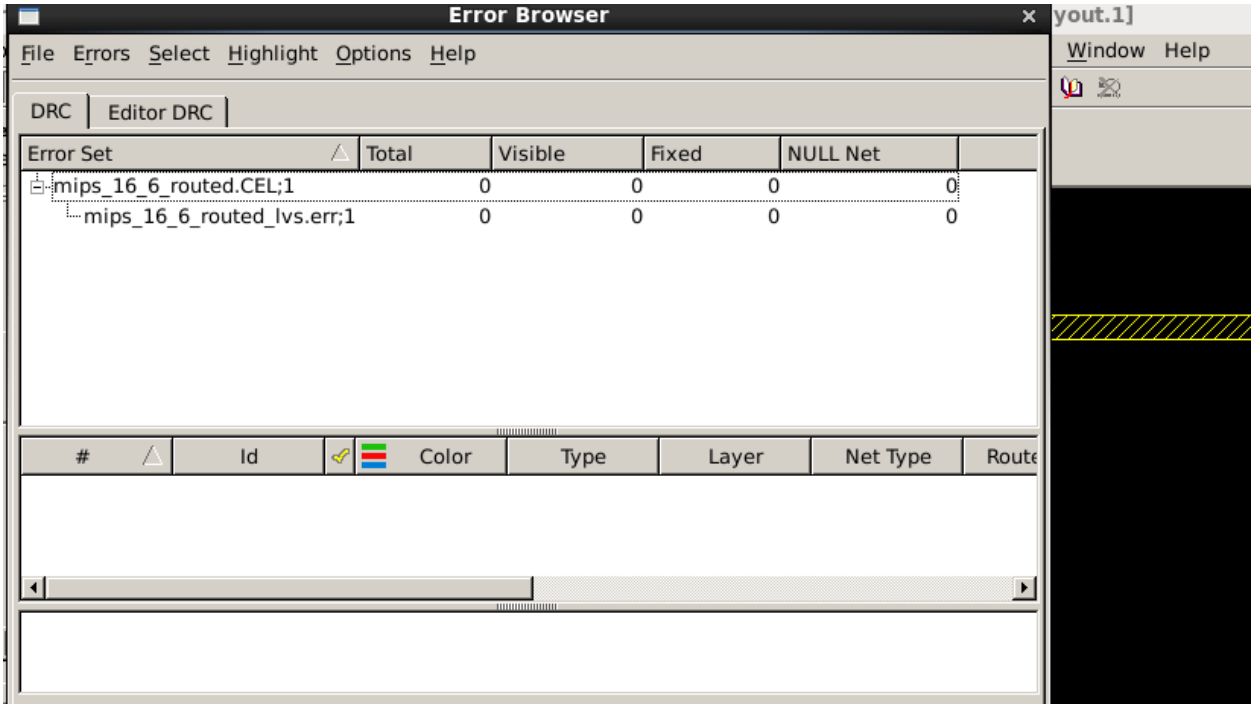
CTS




Clock Trees
Apply
Reload
Options:
clk: AllLevel 6447
clk: Level 0 2
clk: Level 1 27
clk: Level 2 138
clk: Level 3 657
clk: Level 4 2393
clk: Level 5 3230

Routing & Chip finishing

There was about 32 shorted DRCs, after solve them manaully:



The utilization after routing:

```
  Report : Chip Summary
  Design : mips_16
  Version: G-2012.06-ICC-SP2
  Date   : Thu Sep  4 00:33:07 2014
****************************************
Std cell utilization: 82.05%  (139252/(256272-86548))
(Non-fixed + Fixed)
Std cell utilization: 82.94%  (136827/(256272-91309))
(Non-fixed only)
Chip area:            256272   sites, bbox (12.40 12.40 332.74 226.20) um
Std cell area:        139252   sites, (non-fixed:136827 fixed:2425)
                      18996    cells, (non-fixed:18261  fixed:735)
Macro cell area:      0        sites
                      0        cells
Placement blockages:  86548    sites, (excluding fixed std cells)
                      91309    sites, (include fixed std cells & chimney area
                      0        sites, (complete p/g net blockages)
Routing blockages:    0        sites, (partial p/g net blockages)
                      0        sites, (routing blockages and signal pre-route
Lib cell count:       40
Avg. std cell width:  1.45 um
Site array:           unit     (width: 0.19 um, height: 1.40 um, rows: 152)
Physical DB scale:    10000 db_unit = 1 um
```

We will check timing by primetime with an accurate RC extraction from starrc so:

Max check:

```
****************************************
Report : global_timing
Design : mips_16
Version: G-2012.06-SP2
Date   : Thu Sep  4 01:10:54 2014
****************************************

No setup violations found.


Hold violations
-------------------------------------------------------------
         Total  reg->reg   in->reg  reg->out   in->out
-------------------------------------------------------------
WNS     -0.056    -0.056     0.000     0.000     0.000
TNS     -0.605    -0.605     0.000     0.000     0.000
NUM         16        16         0         0         0
```

So, run eco commands to solve them and generate the ECO_changes to source it in the routing stage.

```
#fixing

fix_eco_timing -type hold -methods {size_cell insert_buffer}

set eco_hold_buf_list [list BUF_X2 BUF_X1]

fix_eco_timing -type hold -buffer_list $eco_hold_buf_list
```

After fix them the primetime results:

```
Report : global_timing
Design : mips_16
Version: G-2012.06-SP2
Date   : Thu Sep  4 01:17:35 2014
****************************************

No setup violations found.


No hold violations found.
```

Min check:

```
Report : global_timing
Design : mips_16
Version: G-2012.06-SP2
Date   : Thu Sep  4 01:23:38 2014
****************************************

No setup violations found.


Hold violations
-------------------------------------------------------------
         Total  reg->reg   in->reg  reg->out   in->out
-------------------------------------------------------------
WNS     -0.096    -0.096     0.000     0.000     0.000
TNS     -1.309    -1.309     0.000     0.000     0.000
NUM         16        16         0         0         0
```

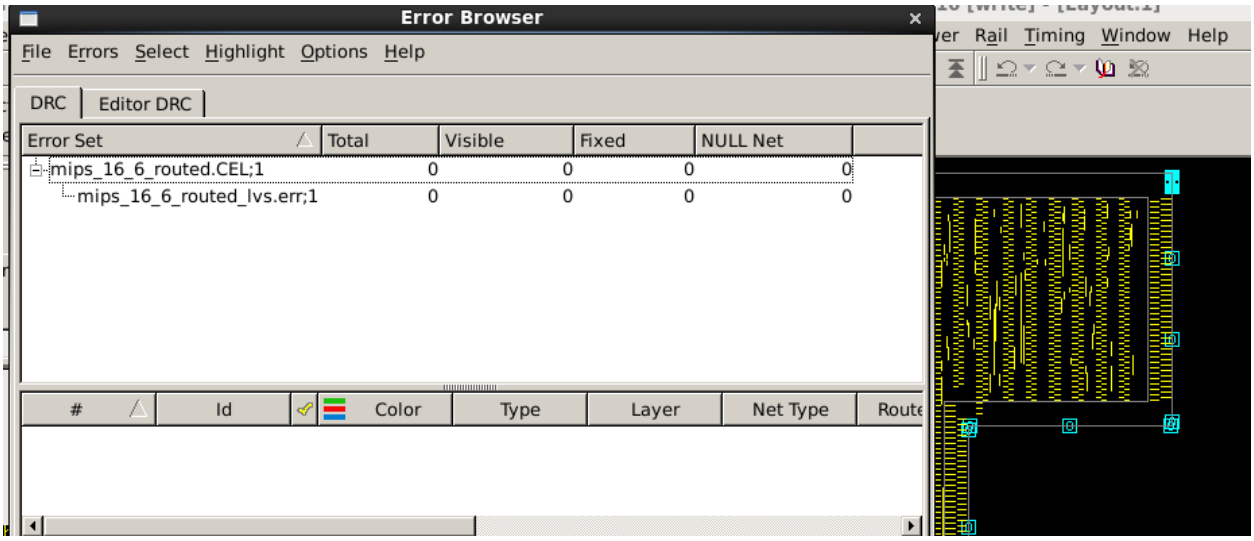
So, run eco commands to solve them and generate the ECO_changes to source it in the routing stage.

```
#fixing

fix_eco_timing -type hold -methods {size_cell insert_buffer}

set eco_hold_buf_list [list BUF_X2 BUF_X1]

fix_eco_timing -type hold -buffer_list $eco_hold_buf_list
```

After fix them the primetime results:

```
Report : global_timing
Design : mips_16
Version: G-2012.06-SP2
Date   : Thu Sep  4 01:24:04 2014
****************************************

No setup violations found.


No hold violations found.
```

After source the ECO commands of max and min in the routing stage we got nearly 6 shorted DRCs and we solved them:



Then we will check timing again in the primetime:

Max:

```
Report : global_timing
Design : mips_16
Version: G-2012.06-SP2
Date   : Thu Sep  4 15:15:00 2014
****************************************

No setup violations found.


No hold violations found.

1
```

Min:

```
Report : global_timing
Design : mips_16
Version: G-2012.06-SP2
Date   : Thu Sep  4 15:16:12 2014
****************************************

No setup violations found.


Hold violations
-------------------------------------------------------------
         Total  reg->reg   in->reg  reg->out   in->out
-------------------------------------------------------------
WNS     -0.019    -0.019     0.000     0.000     0.000
TNS     -0.072    -0.072     0.000     0.000     0.000
NUM          8         8         0         0         0
-------------------------------------------------------------
```

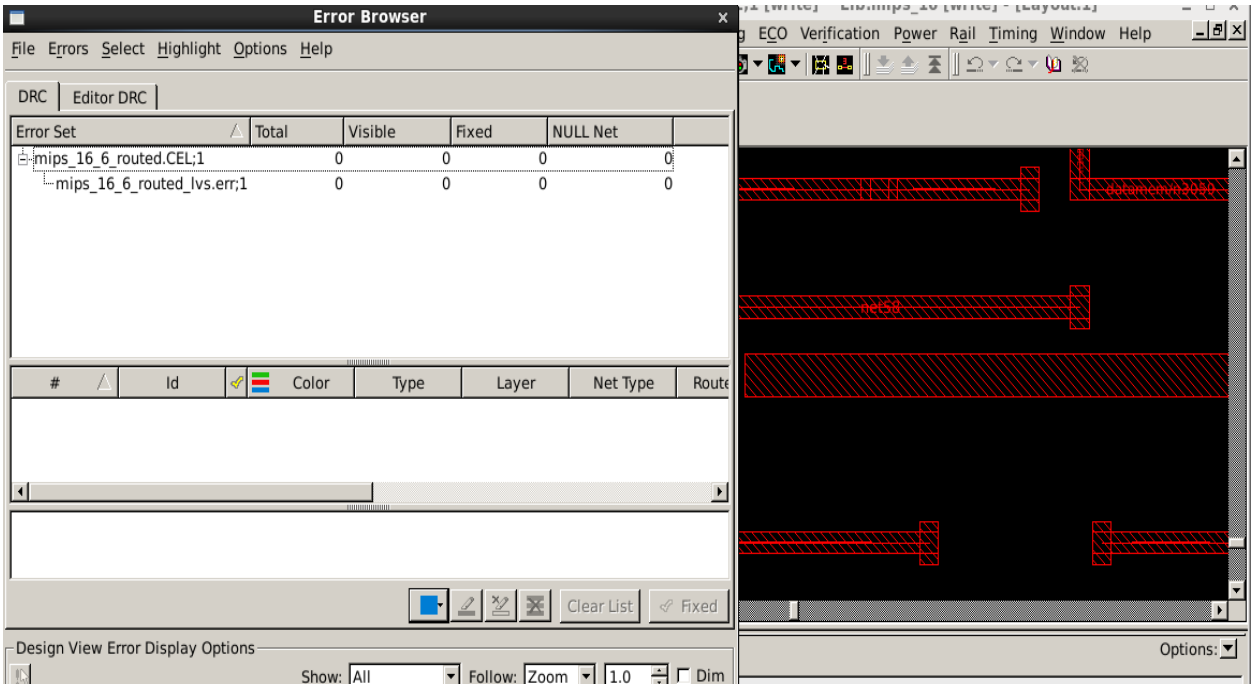
So, run eco commands to solve them and generate the ECO_changes to source it in the routing stage.

```
#fixing

fix_eco_timing -type hold -methods {size_cell insert_buffer}

set eco_hold_buf_list [list BUF_X2 BUF_X1]

fix_eco_timing -type hold -buffer_list $eco_hold_buf_list
```

After fix them the primetime results:

```
Report : global_timing
Design : mips_16
Version: G-2012.06-SP2
Date   : Thu Sep  4 01:24:04 2014
****************************************

No setup violations found.


No hold violations found.
```

After source the ECO commands of max and min in the routing stage we got nearly 2 shorted DRCs and we solved them:



Then we will check timing again in the primetime:

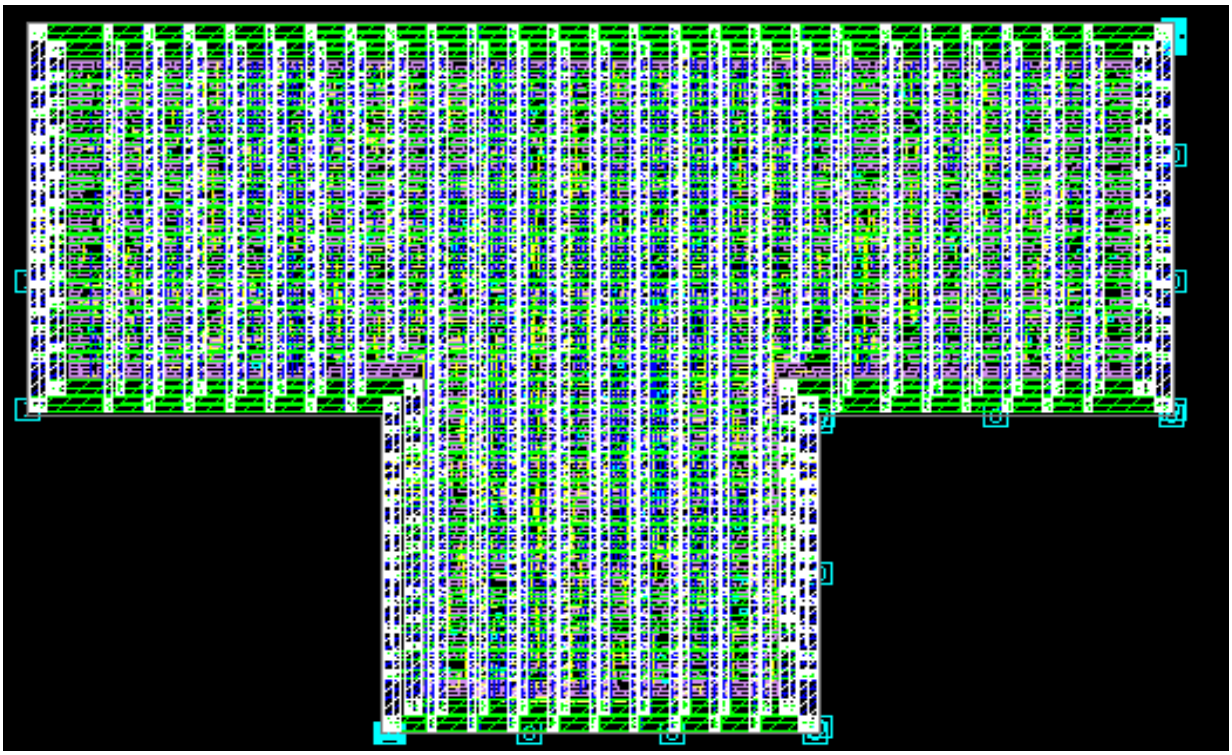
Max:

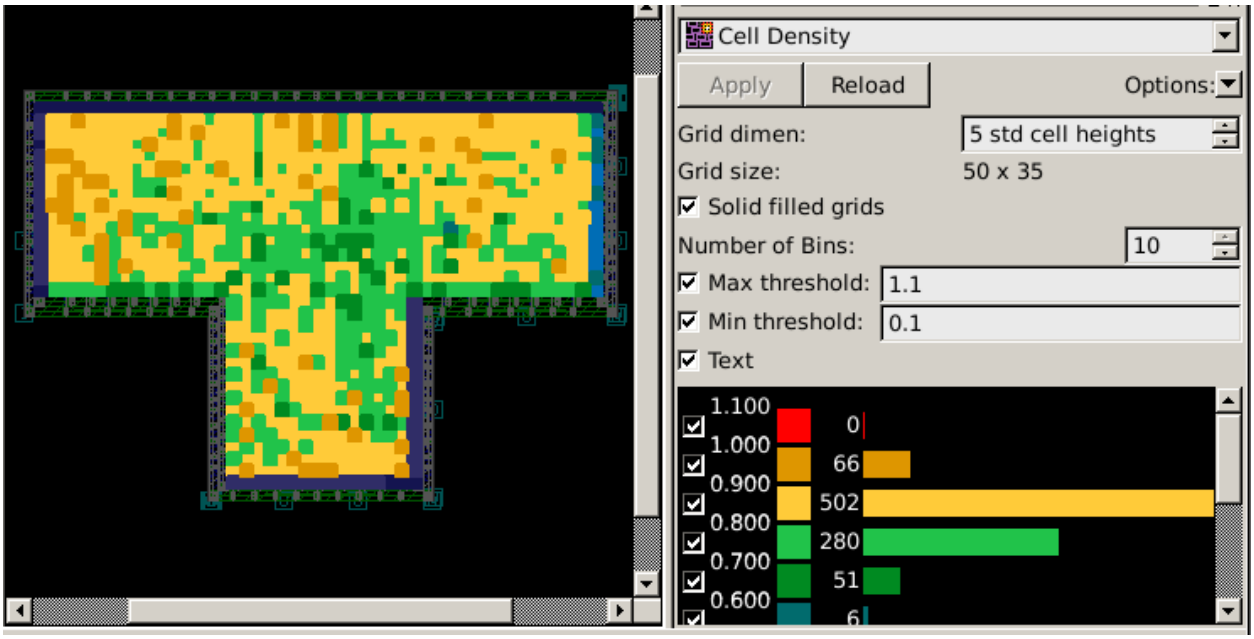
```
Report : global_timing
Design : mips_16
Version: G-2012.06-SP2
Date   : Thu Sep  4 15:15:00 2014
****************************************

No setup violations found.


No hold violations found.

1
```

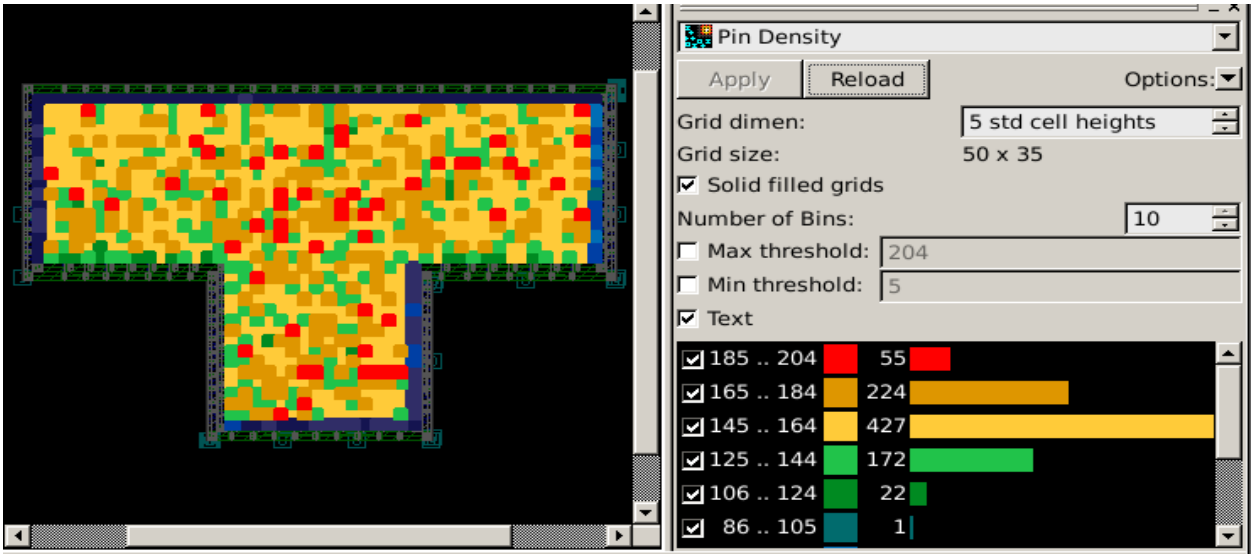
Min:

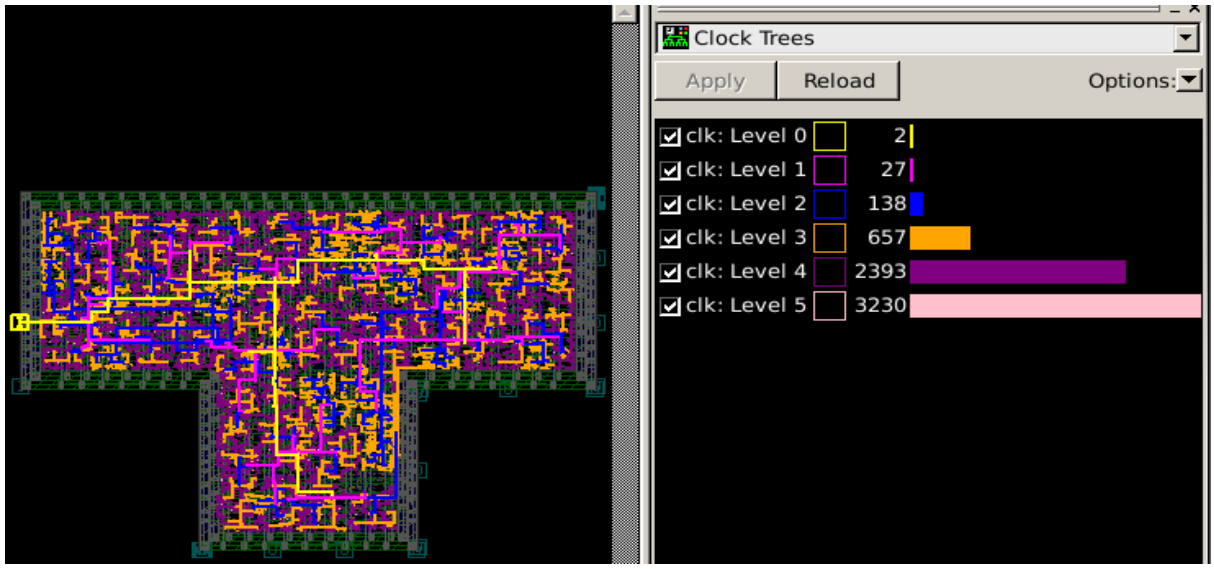
```
Report : global_timing
Design : mips_16
Version: G-2012.06-SP2
Date   : Thu Sep  4 16:07:41 2014
****************************************

No setup violations found.


No hold violations found.
```

So, we are clean timing with an accurate RC extraction. The final layout after adding filler cells and fill metal in the chip finishing stage so total area becomes 37131.471 um^2:




Cell Density
Apply
Reload
Options:
Grid dimen:
5 std cell heights
Grid size:
50 x 35
Solid filled grids
Number of Bins:
10
Max threshold:
1.1
Min threshold:
0.1
Text
1.100
1.000
0.900
0.800
0.700
0.600
0
66
502
280
51
6


Pin Density
Apply
Reload
Options:
Grid dimen:
5 std cell heights
Grid size:
50 x 35
Solid filled grids
Number of Bins:
10
Max threshold:
204
Min threshold:
5
Text
185 .. 204
165 .. 184
145 .. 164
125 .. 144
106 .. 124
86 .. 105
55
224
427
172
22
1


Clock Trees
Apply
Reload
Options:
clk: Level 0
clk: Level 1
clk: Level 2
clk: Level 3
clk: Level 4
clk: Level 5
2
27
138
657
2393
3230

Formal verification Post PnR

```
********************************** Verification Results **************************
********
Verification SUCCEEDED
   ATTENTION: synopsys_auto_setup mode was enabled.
              See Synopsys Auto Setup Summary for details.
---------------------------------------------------------
 Reference design: Ref:/WORK/mips_16
 Implementation design: Imp:/WORK/mips_16
 47 Passing compare points
---------------------------------------------------------------------------------
--------
Matched Compare Points     BBPin    Loop   BBNet     Cut    Port     DFF     LAT
   TOTAL
---------------------------------------------------------------------------------
--------
Passing (equivalent)           0       0       0       0      32      15       0
      47
Failing (not equivalent)       0       0       0       0       0       0       0
       0
Not Compared
  Constant reg                                                    129       0
     129
  Unread                       0       0       0       0       0    4096       0
    4096
*********************************************************************************
********
```

```
Report          : failing_points

Reference       : Ref:/WORK/mips_16
Implementation  : Imp:/WORK/mips_16
Version         : G-2012.06-SP2
Date            : Fri Sep  5 15:37:29 2014
*************************************************

No failing compare points.
```