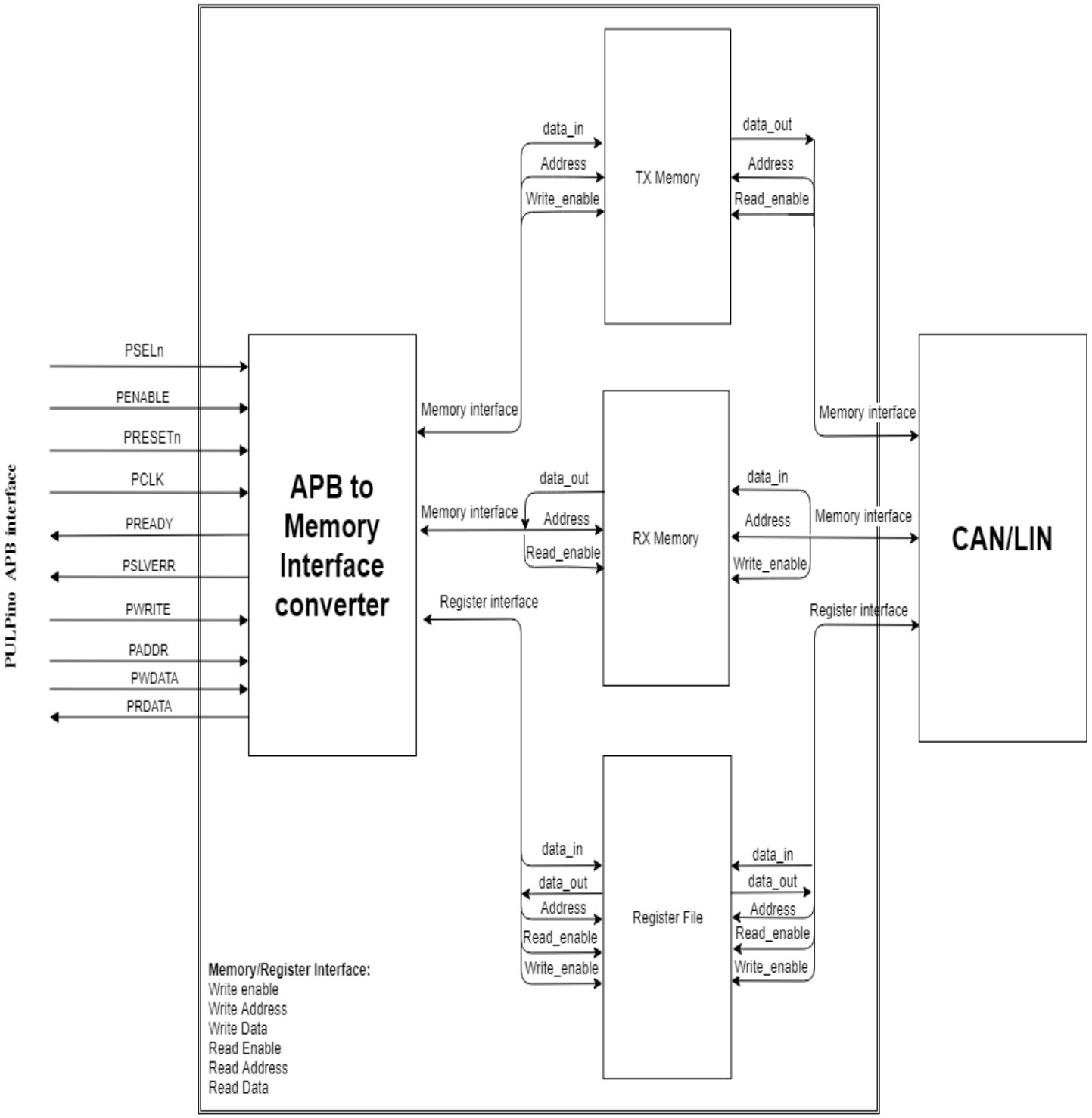
APB INTERCONNECT

V2.0

1.APB interconnect Block Diagram:



APB Interconnect

2. Signal Description:

2.1.APB Brigde Signals:

Signal	Description
PCLK	The rising edge of PCLK times all transfers on the APB.
PRESETn	The APB reset signal is active LOW and normally connected to the system bus reset signal.
PADDR	This is the APB address bus – up to 32 bits wide.
PSELx	It indicates that the slave device is selected and that a data transfer is required.
PENABLE	This signal indicates the second and subsequent cycles of an APB transfer.
PWRITE	This signal indicates an APB write access when HIGH and an APB read access when LOW.
PWDATA	This bus is driven by the peripheral bus bridge unit during write cycles when PWRITE is HIGH. Up to 32 bits wide
PREADY	The slave uses this signal to extend an APB transfer
PRDATA	The selected slave drives this bus during read cycles when PWRITE is LOW. up to 32-bits wide
PSLVERR	This signal indicates a transfer failure.

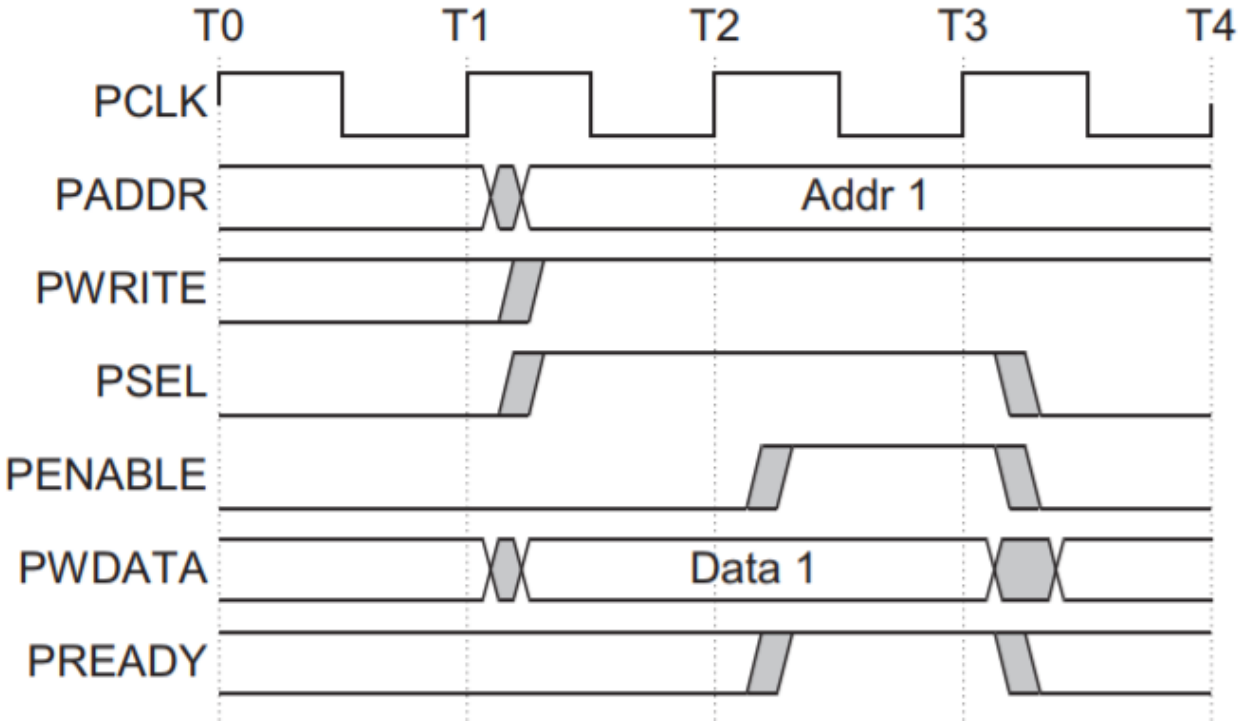
3. APB Transfers:

a) Write Transfer :

1- with no wait states:

The write transfer starts with the address, write data, write signal and select signal all changing after the rising edge of the clock. The first clock cycle of the transfer is called the **Setup phase**. After the following clock edge the enable signal is asserted, **PENABLE**, and this indicates that the **Access phase** is taking place. The address, data and control signals all remain valid throughout the Access phase. The transfer completes at the end of this cycle.

The enable signal, **PENABLE**, is deasserted at the end of the transfer. The select signal, **PSELx**, also goes LOW unless the transfer is to be followed immediately by another transfer to the same peripheral.

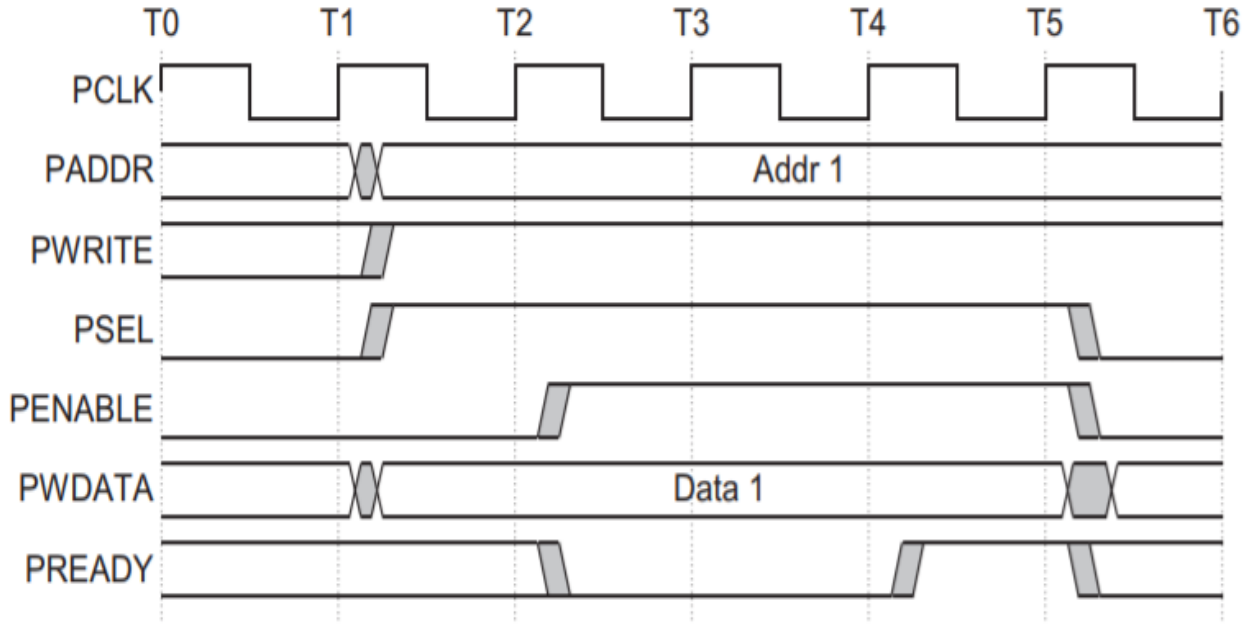


2- with wait states:

During an Access phase, when PENABLE is HIGH, the transfer can be extended by driving PREADY LOW. The following signals remain unchanged for the additional cycles:

- address, **PADDR**
- write signal, **PWRITE**
- select signal, **PSEL**
- enable signal, **PENABLE**
- write data, **PWDATA**

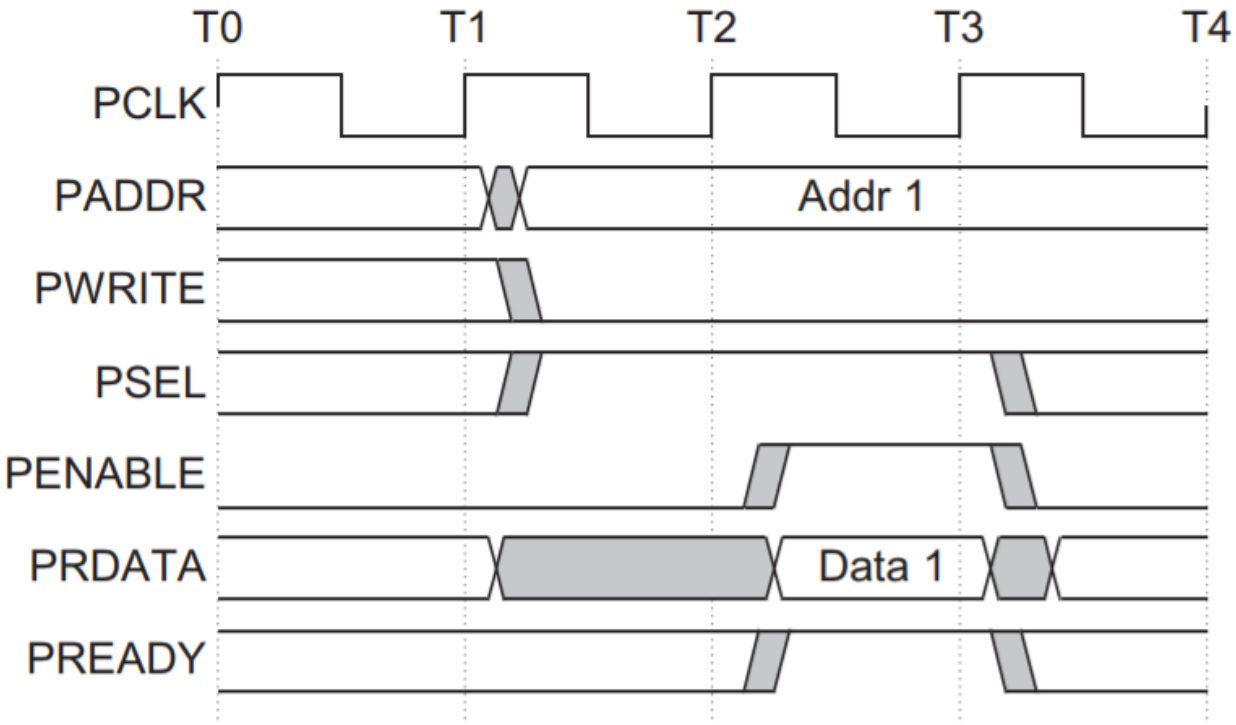
PREADY can take any value when PENABLE is LOW. This ensures that peripherals that have a fixed two cycle access can tie PREADY HIGH.



b) Read Transfer :

1- with no wait states:

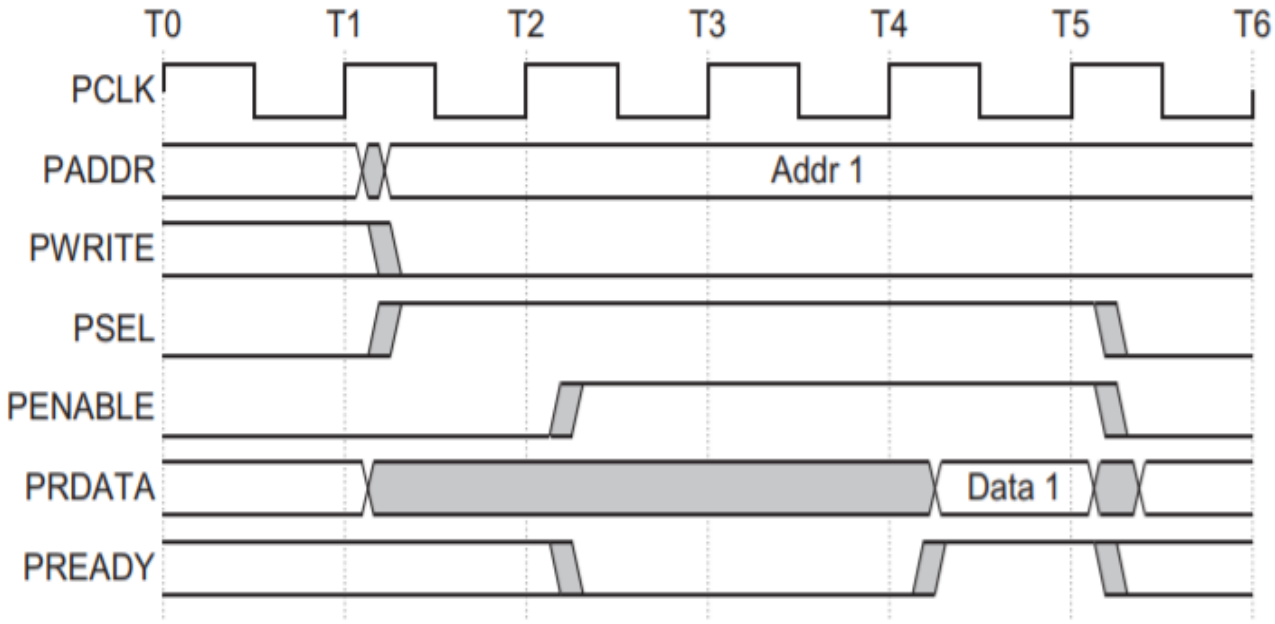
Same as the write transfer described before. The slave must provide the data before the end of the read transfer.



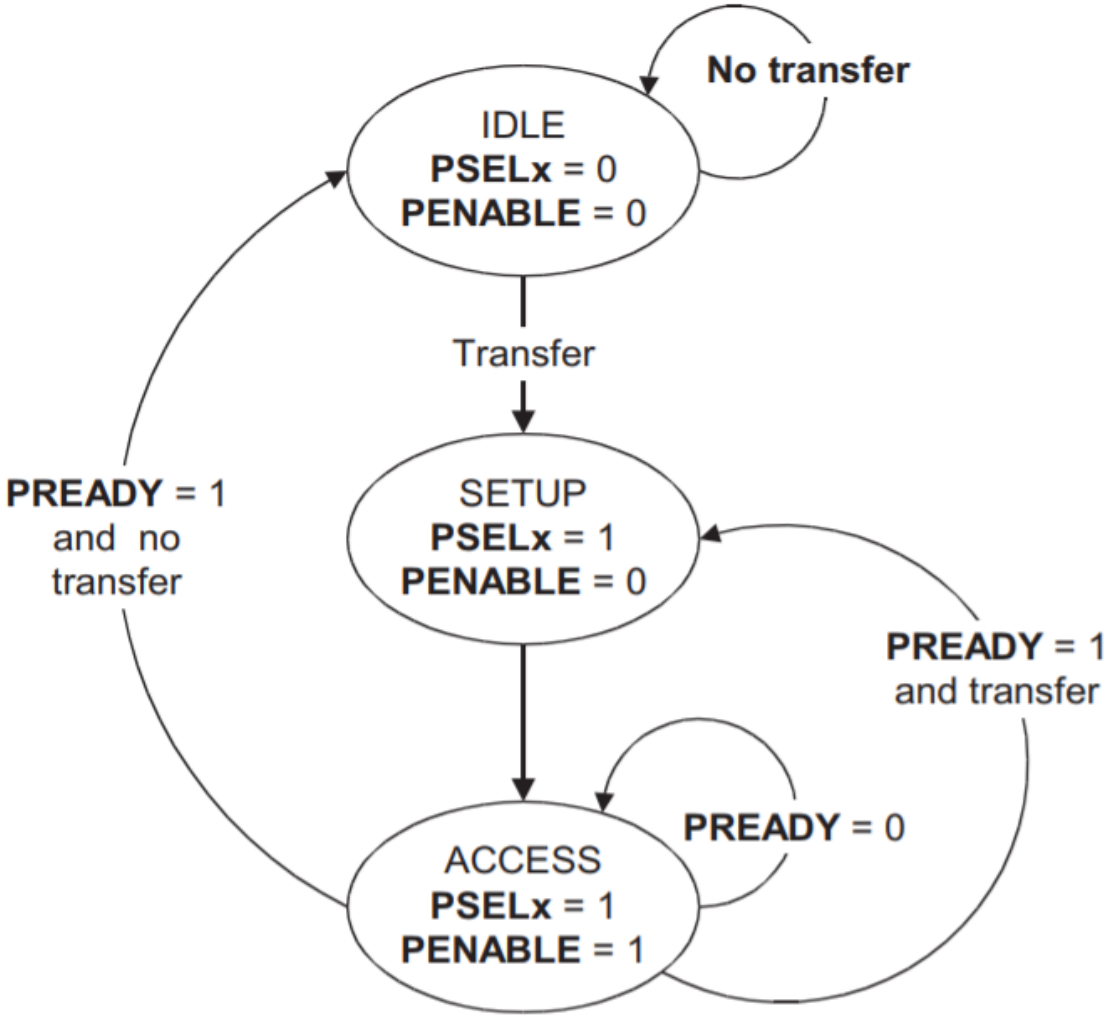
2- with wait states:

The transfer is extended if PREADY is driven LOW during an Access phase. The protocol ensures that the following remain unchanged for the additional cycles:

- address, **PADDR**
- write signal, **PWRITE**
- select signal, **PSEL**
- enable signal, **PENABLE**



4. APB Bridge Operating States:



The state machine operates through the following states:

IDLE This is the default state of the APB.

SETUP When a transfer is required the bus moves into the **SETUP** state, where the appropriate select signal, **PSELx**, is asserted. The bus only remains in the SETUP state for one clock cycle and always moves to the **ACCESS** state on the next rising edge of the clock.

ACCESS The enable signal, **PENABLE**, is asserted in the **ACCESS** state. The address, write, select, and write data signals must remain stable during the transition from the **SETUP** to **ACCESS** state.

Exit from the **ACCESS** state is controlled by the **PREADY** signal from the slave:

- If **PREADY** is held LOW by the slave then the peripheral bus remains in the **ACCESS** state.

- If **PREADY** is driven HIGH by the slave then the **ACCESS** state is exited and the bus returns to the **IDLE** state if no more transfers are required. Alternatively, the bus moves directly to the **SETUP** state if another transfer follows.