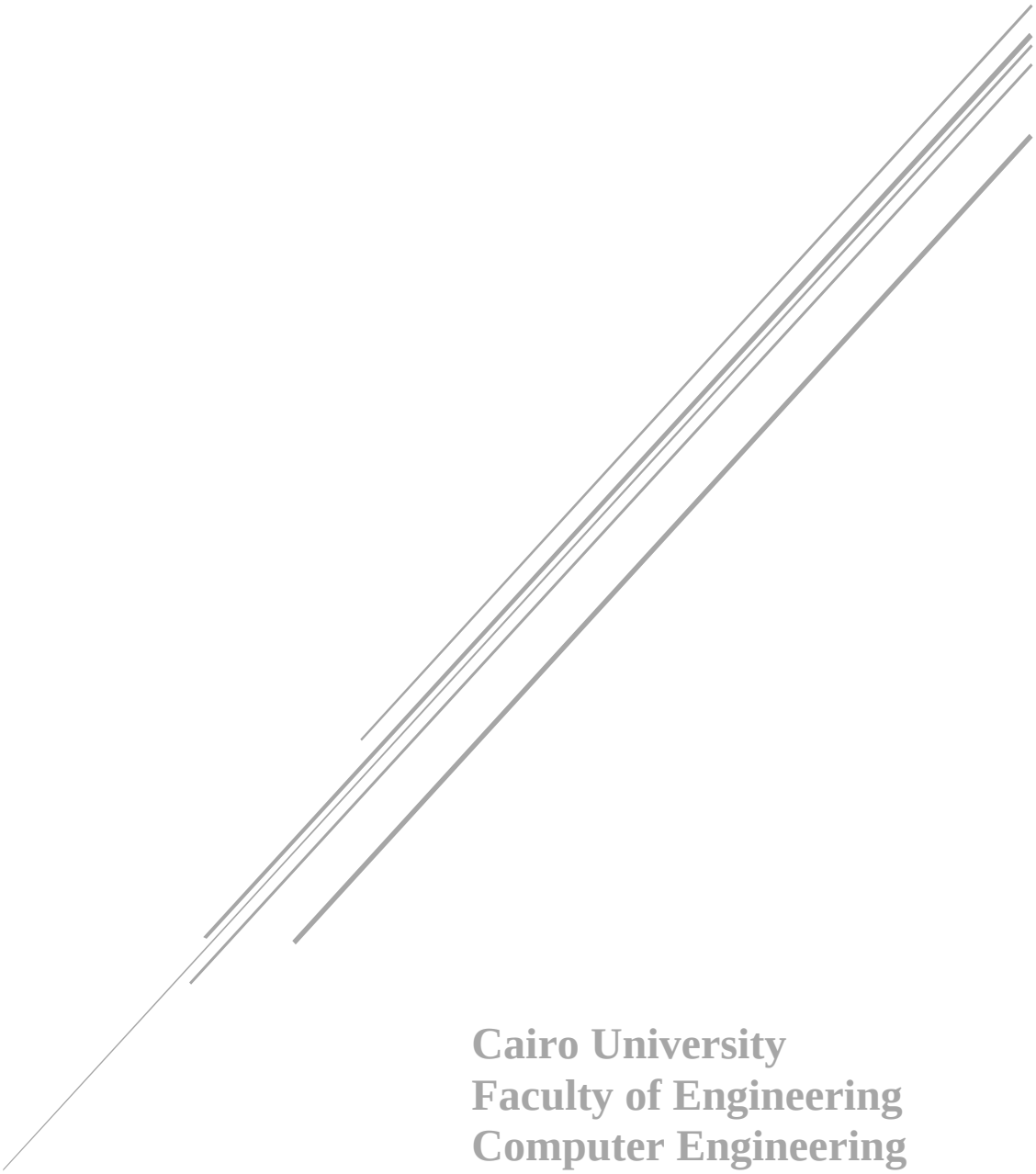
DIVISION MODULE

Phase #2



Cairo University
Faculty of Engineering
Computer Engineering
Spring 2020

	Using Carry look ahead adder	Using carry select adder
Placeable Area	1897	2142
Movable Cell Area	1097	1196
Utilization (%)	57	55
Total Power(uw)	2497.855225	3379.492676
Data arrival time	1434.1	1359.9
Slack	35.5	102.1

To run the simulation:
Python3 division 0000000000000111 0000000000000010
Dividend divisor
The output will be overFlow, result, divide by zero, ready

To the Verilog files:
We have to types from the division
1- division with carry select adder.
We need to include:
1- carry_select_adder_2bit
2- carry_select_adder_16bit
3- Division_CSA
4- full_adder
5- mux2x1
6- ripple_adder_2bit
7- Division_CSA_TestBench
And then we can run the test bench file from the do-file called testbench_dofile.
2- division with carry look a head adder.
We need to include:
1- carry_lookahead_adder_4bit
2- carry_lookahead_adder_16bit
3- Division_CLHA
4- Division_LHA_tb
And then we can run the test bench file from the do-file called testbench_dofile.