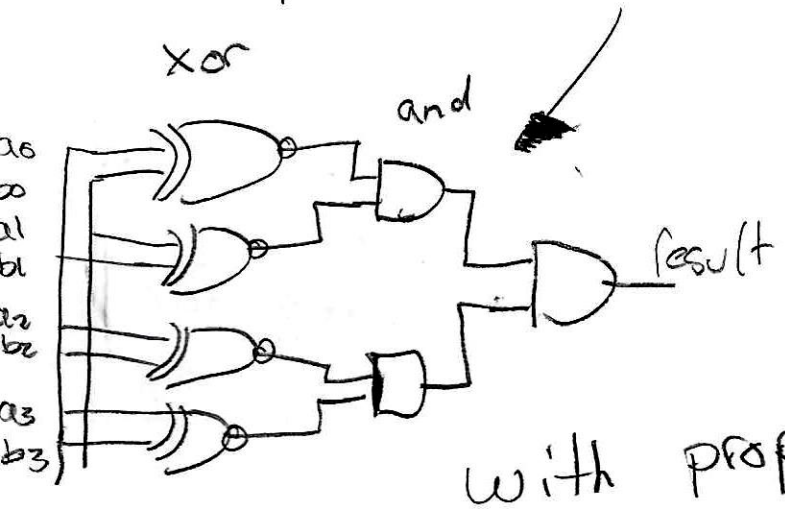
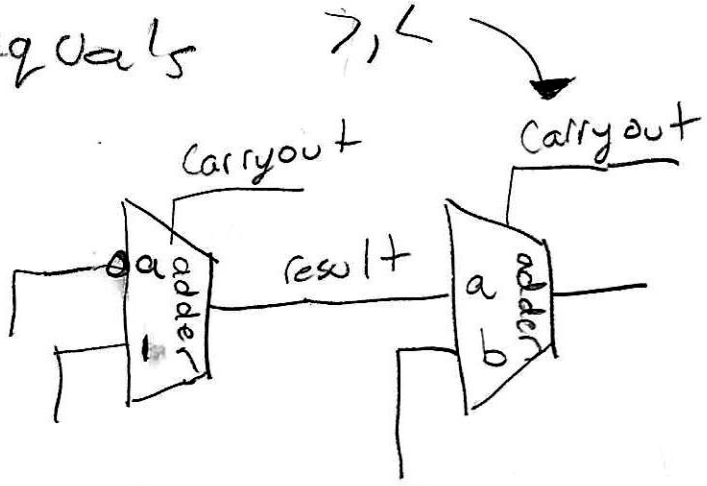
for equals all we have to do is compare bne a,b, false for a>b all we have to do is invert a add 1 then add (-a)+b if there is carry out than a>b for a<b we can use the same hardware carry out can be used as the result in a>b if a is greater than b carry out will be 1 if it isn't 0 for <=, >= all we need to do is or gate == and either < or >, thus we need 2 digital circuits that can compute theese results and by changing the targets of a and b we can get all if statements

Example circuit For equals





with proper routing of =, >, < and a, and b all would take 1 instruction

Case 1 : if (a != b)

```
bne  a, b, true      # branch true
b    false           # branch false
```

Case 2: if (a != b)

```
bne  a, b, false     # branch false
b    true            # branch true
```

Case 3: if (a < b)

```
not  b               # invert b
add  c, b, 1         # add 1 to b
add  c, a, c         # add a and c
sll  a, 31           # Shift left 31
sll  c, 31             get last bit
sll  b, 31
and  a, a, b
and  a, a, c
bne  a, zero, true
b    false
```

> Swap true and false for a ≥ b.
> Combine cases for >= <=

Ideal Pipeline

Sw R16, 12 (r6)	IF	ID	EX	MEM	WB				
lw R16, 8(r6)		IF	ID	EX	MEM	WB			
beq r5, r4, Label			IF	ID	EX	MEM	WB		
add r5, r1, r4				IF	ID	EX	MEM	WB	
Slt					IF	ID	EX	MEM	WB

add and Slt try to access memory at same time as ID from earlier comands

Sw R16, 12 r(6)	IF	ID	EX	MEM	WB					
lw R16, 8(r6)		IF	ID	EX	MeM	WB				
beq r5, r4, Label			IF	ID	EX	MEM				
add r5, r1, r4				X	X	IF	ID	EX	MEM	WB
Slt r5, r15, r4							IF	ID	EX	MEM

∴ a total of 11 clock cycles is needed and nops cant solve the hazard because it is a hardware Problem and the problem must be addressed within the hardware

no branches, no hazards, no delays

Sw R16, 12(R6)	IF	ID	EX	MEM	WB				
lw R16, 8(R6)		IF	ID	EX	MEM	WB			
Beq R5, R4, Label			IF	ID	EX	MEM	WB		
Add R5, R1, R4				IF	ID	EX	MEM	WB	
Slt R5, R15, R4					IF	ID	EX	MEM	WB

9 cycles

overlap EX/MEM

Sw R16, 12(R6)	IF	ID	EX/MEM	WB				
lw R16, 8(R6)		IF	ID	EX/MEM	WB			
Beq R5, R4, Label			IF	ID	EX/MEM	WB		
Add R5, R1, R4				IF	ID	EX/MEM	WB	
Slt R5, R15, R4					IF	ID	EX/MEM	WB

8 cycles

∴ The speedup is 9/8

Pipeline with Stall-on-branches determined In ID stage

Sw R16, 12(R6)	IF	ID	EXE	MEM	WB						
Lw		IF	ID	X	EXE	MEM	WB				
BEQ			IF	ID	X	EXE	MEM	WB			
Add				IF	ID	X	EXE	MEM	WB		
SLT					IF	ID	X	EXE	MEM	WB	

# of clock cycles is 10

∴ the Speedup is $\frac{11}{10} = 1.1$

IF	ID	EX	MEM	WB
200ps	120ps	150ps	190 ps	100 ps

The latency of MEM is 190 and EX is 150
The latency of MEM is big

190 + 20 ps = 210 4 stage 8 X 210 = 1680ps

200 ps 5 stage 9 X 200 = 1800ps

Speed up = $\frac{1800}{1680} = 1.07$

latency of ID = 120 + 1/2 X 120 = 180

latency of EX = 150 - 10
= 140

IF	ID	EX	MEM	WB
200	180	140	190	100

Speed up = $\frac{11 \times 200}{10 \times 200} = 1.1$

No change

IF	ID	EX	MEM	WB
200ps	120ps	130ps	190ps	100ps

Moving BEQ computation to the MEM Stage adds One Clock Cycle

cycles = 4+5 + 1X2
= 11

11 X 200 = 2200
Execution time

number cycles with Branch In MEM
= 4+5+ 1X3 = 12

200 X 12 = 2400
Execution time

∴ Speed Up is $\frac{2200}{2400} = 0.92$