ECE3623 Embedded System Design Laboratory

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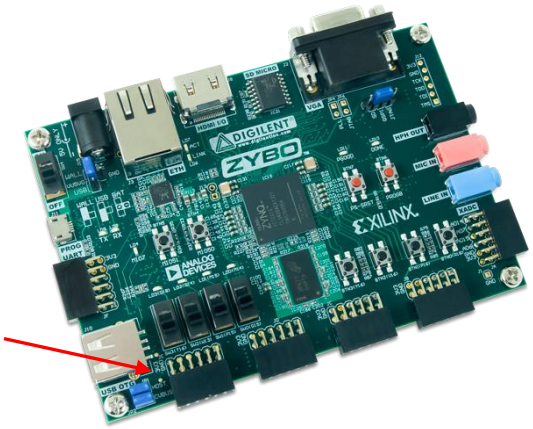
PmodAD1 and PmodDA2 Peripherals

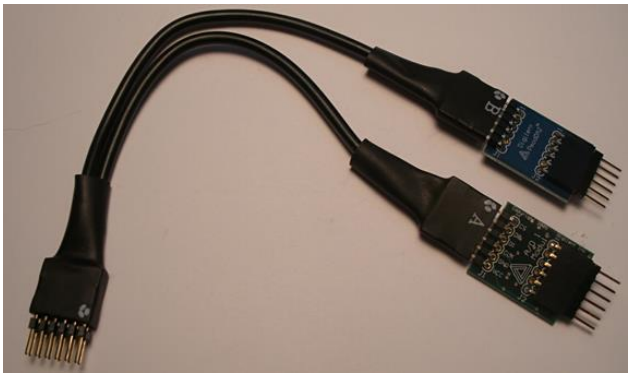
Although the Zynq SoC of the Digilent Zybo Board features an integral analog-to-digital converter (XADC) its use is simple and there is no digital-to-analog converter (DAC). The Digilent PmodAD1 and PmodDA2 provide this external functionality and both 6-pin peripheral devices can be installed on the 12-pin Pmod jack on the lower left side of the Zybo Board.

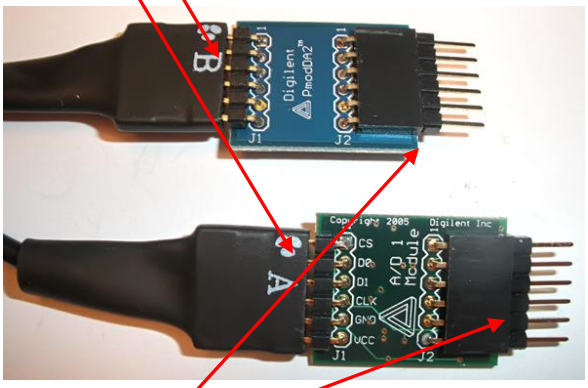


The leftmost, front Pmod jack (JE) is available from the programmable logic (PL) of the Zynq SoC device and is shown as a *front view*. Note the location of pin 1 on the top right. Pin 7 is immediately below pin 1 on the bottom right. To facilitate the connection a 12 pin to two 6 pin cable is provided as shown in the Figure.

The PmodAD1 ADC is connected to the cable 6 pin connector A with the index mark positioned on pin 1 of J1 the SPI interface, as shown in the Pictures. The PmodDA2 is connected to the cable 6 pin connector B with the index mark position on pin 1 of J1 the SPI interface as shown in the Pictures**.**

J1: index marks





J2: 6 pin headers input or output connectors

Make sure that the SPI interface (fixed connector) of the PmodAD1 ADC and PmodDA2 DAC is connected to the A and B 6 pin connector as shown.

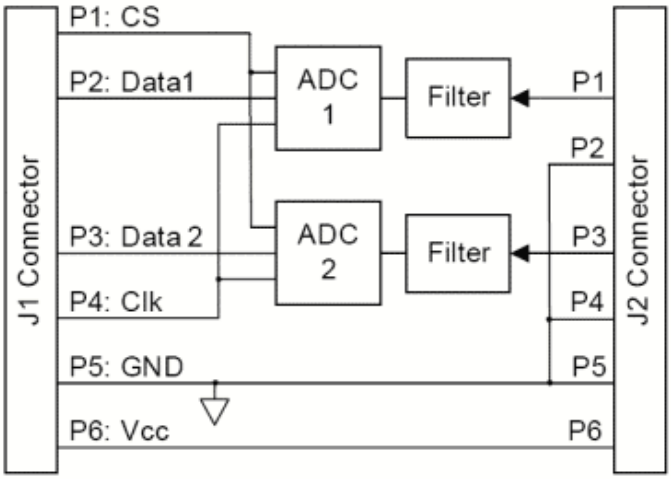
Zybo Board Pmod Jack

The 12 pin connector of the cable is provided with a 12 pin header which is inserted into the 12-pin Pmod jack on the lower left side of the Zybo Board (JE). The index mark shown in the picture **must be on the lower right side and not visible from the top surface** of the Zybo Board.

This insures that V_{CC} for the PmodAD1 and PmodDA2 are connected properly at pins 6 and 12 of the 12 pin Pmod connector of the Zybo Board. **Improper connection can damage the Zybo Board and the Pmod peripherals** and is your responsibility.

PmodAD1 ADC

The PmodAD1 ADC signal input is on connector J2 which is provided with a 6 pin header for ease in connection as shown in the Pictures. Pin1 (top right in the Picture) is ADC channel 0 and pin 3 is ADC channel 1. Pins 2, 4 and 5 are signal ground. Do not use pin 6 which is $V_{CC.}$ The schematic for PmodAD1 is shown below.



PmodAD1 ADC

The SPI interface for the PmodAD1 has CS (ADCSS) on J1 pin 1, Clk (ADCSCLK) on J1 pin 4, ADC channel 0 serial data input (ADC0SD) on J1 pin 2 and ADC channel 1 serial data input (ADC1SD) on J1 pin 3. J1 pin 5 is ground and J1 pin 6 is $V_{CC.}$

The digital output D for an analog input voltage V_{IN} is given by the equation below. With V_{REF} = 0 V, V_{FS} = 3.3 V, G = 1 and n = 12 the PmodAD1 output data D ranges from 0 to 4095_{10} for an analog signal input V_{IN} of approximately 0 to 3.30 V

$$D[n-1:0] = G\,\frac{V_{IN} - V_{REF}}{V_{FS}}\,2^{n-1}$$

The maximum SPI clock (SCLK) frequency for the PmodAD1 is approximately 20 MHz, although both channels can acquire data simultaneously.

PmodDA2 DAC

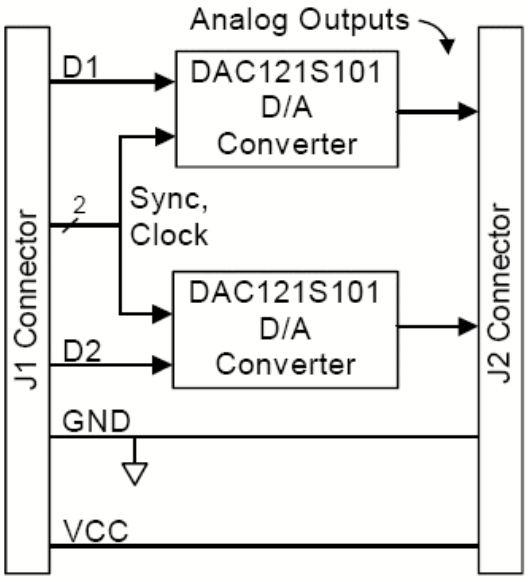
The SPI interface for the PmodDA2 has SYNC (DACSS) on J1 pin 1, SCLK (DACSCLK) on J1 pin 4, DAC channel 0 serial data input (DAC0SD) on J1 pin 2 and DAC channel 1 serial data input (DAC1SD) on J1 pin 3. J1 pin 5 is ground and J1 pin 6 is $V_{CC.}$.

The PmodDA2 DAC signal output is on connector J2 which is provided with a 6 pin header for ease in connection. Pin1 (top right in the Picture) is DAC channel 0 and pin 3 is DAC channel 1. Pins 2 and 4 are not connected (N/C), pin 5 is signal ground. Do not use pin 6 which is $V_{CC.}$ The schematic for PmodDA2 is shown above.

The analog output voltage of the PmodDA2 DAC is determined by Equation 3.3 in the text. With V_{REF} = 3.3 V, n = 12 and the data D ranging from 0 to 4095_{10} the analog signal output V_{OUT} is approximately 0 to 3.299 V

$$V_{OUT} = \frac{D[n\text{-}1:0] \times V_{REF}}{2^{n}} \quad V$$

The maximum SPI clock (SCLK) frequency for the PmodDA2 is approximately 30 MHz, although both channels can output data simultaneously.



PmodDA2 DA2

Table 1: Interface Connector Signal Descriptions

Digital Interface – J1	
1	SYNC (common)
2	DINA (converter IC1)
3	DINB (converter IC2)
4	SCLK (common)
5	GND
6	VCC
Analog Interface – J2	
1	VOUTA (converter IC1)
2	N/C
3	VOUTB (converter IC2)
4	N/C
5	GND
6	VCC