نماذج الاختبارات الشهرية

تجميع :

نور الجفري & فاطمة عاشور

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كلية الحاسبات و تقنية المعلومات
College of Computers & Information Technology

Specialization. CS

Second Semester Examination

Hadhramout University

Faculty of Computing

Subject. C-O

الاسم "CS"

Class. Level 2

Q1- A- Fill the blanks with correct words:

a. **Each gate is defined in three ways:** grphic symbols, Algebric nation, **and** truth table

b. **Timing signals indicate the** validiond **of** data **and** Access **information.**

c. clocks **: Used to synchronize operations.**

d. **The hierarchical nature of complex systems is essential to their** structure **and their** function **------**

B- When the process was halting?

if the machine turneed off or program occur error on it

the program halts

Q2- Define each of the following Terms:

A- Analysis ibs an ecnomical way to describ thier function and opration ↙ Perform digital

A- Gate: electronic cuircut that enable of input signal to go in and Boolean opration to get output signals

2- Describe general purpose of hard ware?

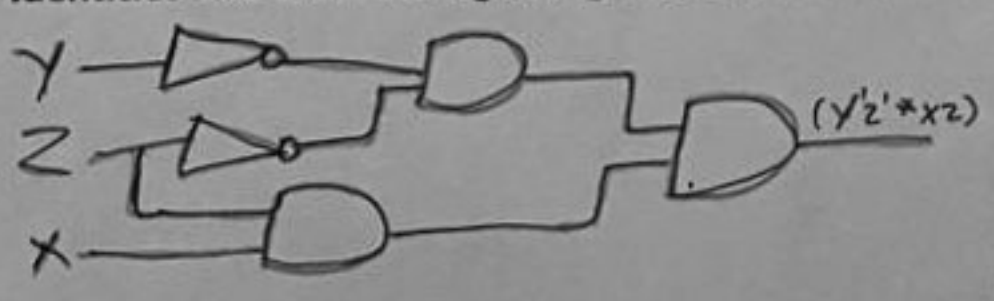
it is the control signals and data, and each of control signal is essentiall for each code data and instruction the general-purpose intrprets dat and generated control signal

Q3- What is types of exchanges that are needed by indicating the major forms of input and output for CPU module?

I/O to Prosser: prosser that read data from an I/O device via I/O model

Proseeer to I/O: send data to I/o device

Q4- identities and draw the logic diagram for the simplified expression. (y'z' * xz)?



Y	z	x	y'	z'	y'z'	xz	y'z'+xz
0	0	0	1	1	1	0	1
0	0	1	1	1	1	0	1
0	1	0	1	0	0	0	0
0	1	1	1	0	0	1	1
1	0	0	0	1	0	0	0
1	0	1	0	1	0	0	0
1	1	0	0	0	0	0	0
1	1	1	0	0	0	1	1

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Second Semester Examination

Hadhramout University

Faculty of Computing

Subject. C-O

Specialization. IT

Class. Level 2

الاسم

Q1- A- Fill the blanks with correct words:

a. **Each gate is defined in three ways:** logic circut, logic catation, **and** truth table.

b. **Timing signals indicate the** validity **of** data **and** performance **information.**

c. Clock: **Used to synchronize operations.**

d. **The hierarchical nature of complex systems is essential to their** function **and their** structure

storage

B- When the process was halting?

1) The device turned off

2) There is some errors occurs during the processing

3) The it recive the instruction that turn off the computer.

Q2- 1- Define each of the following Terms:

A- System interconnection provide pathyay between system modules to transfer data between them.

B- Registers

it's a flip-flop that using to store instructions and perform the operation

it has two types 1) parallel register 2) shift register.

C- Gate:

It's a cuircut that transfer the electrical signals in zero-one form.

(binary digit

2- Computer component top level veiw.?

خلف الورقة

Q3- Given the function: F(x,y,z)= xy'z + x'y'z + xyz, simplify the expression using Boolean algebra and

identities and draw the logic diagram for the simplified expression?

خلف الورقة

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نماذج الامتحانات النهائية

تجميع :

نور الجفري & فاطمة عاشور

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HADHRAMOUT UNIVERSITY
COLLEGE OF COMPUTERS & INFORMATION TECHNOLOGY
TEST (B)

Academic year: 2020-2021
Lecturer: Dr. Saeed Mohammed Baneamoon
Level : Second

Subject: Computer Organization & Architecture
Department: IT (A موازي)
Time allowed : 60 Minutes

Name: .....

A موازي

Total marks: 11 / 20

Answer all questions

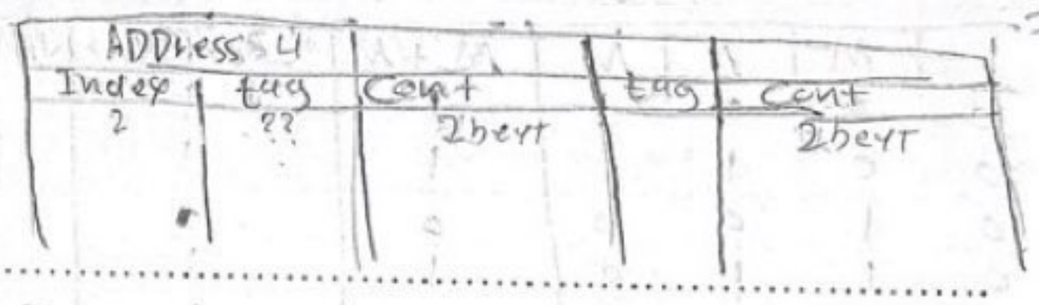
Q1) Compare between RAM and EEPROM? (4 marks) 3

	RAM: Volaite	Read-Write Mucanrsim	Size	speed	Example.
RAM	Volait	Electcally	Smaller	Fase	Cashe memo
EEPRom	Nonvolait	Electrecally	Larger	Lower	~~main memory~~ Hard disk

EEPRom = ~~Cash~~ next leve

Q2) Assume: (6 marks) 3

- A processor has a set- associative mapped cache.
- Each content with 4 bytes long.
- Index is 16 bits long.
- Address is 4 bytes long.
- Number of contents in cache is 20.



(a) What is the size of Tag?

Address = Index + tag
4 = 2 + tag
tag = 4 - 2
Tag = 2 bytes

(b) What is the size of cache for contents?

Content in cach / Each content
Size of cach = 4
20 / 4 = 5 bytes
Data size = Size / Data

Q3) Correct interconnection buses between CPU and I/O modules as shown in Figure 1. (4 marks) 0.5

Figure 1

Good Luck

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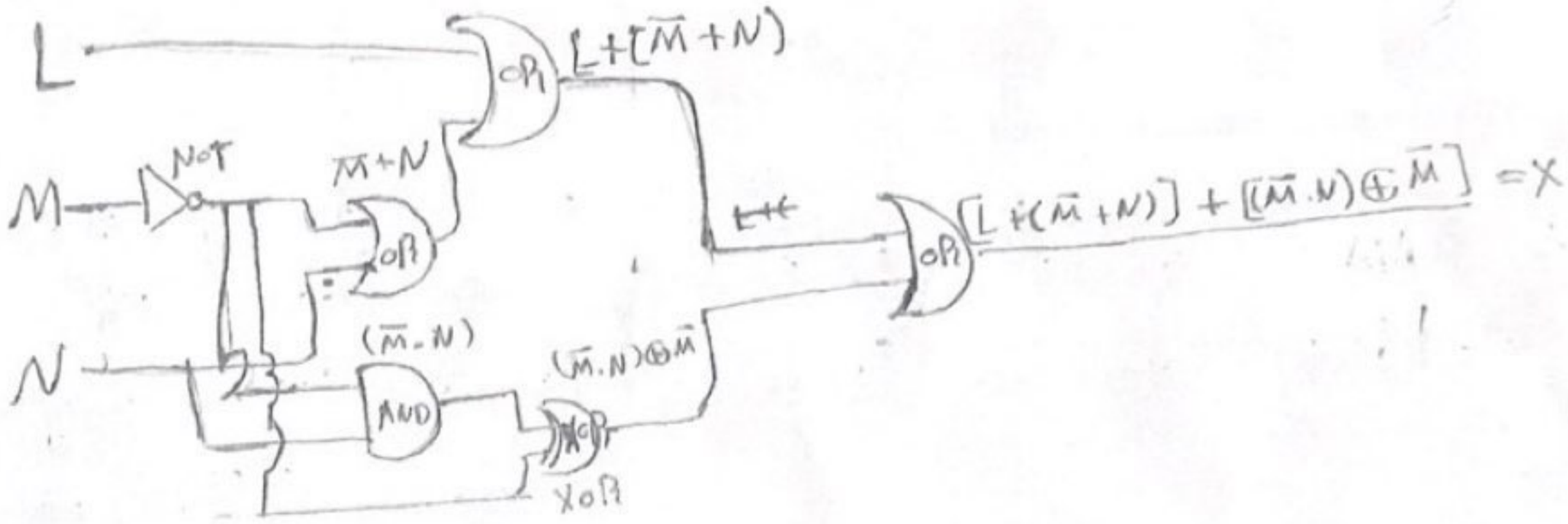
Q4) Consider the following expression:

$$[L + (\overline{M} + N)] + [(\overline{M}.N) \oplus \overline{M}]$$

(a) **Draw the logic circuit** represented by the given expression, then name each gate used? **(3 marks)**



(b) Construct the truth table of the logic circuit in [Q4-(a)]? **(3 marks)**

L	M	N	$\overline{M}$	$\overline{M}+N$	$L+\overline{M}+N$	$\overline{M}.N$	$(\overline{M}.N)\oplus\overline{M}$
0	0	0	1	1	1	0	1
0	0	1	1	1	1	1	0
0	1	0	0	0	0	0	0
0	1	1	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	1	1	1	1	0
1	1	0	0	0	1	0	0
1	1	1	0	1	1	0	0

Good Luck

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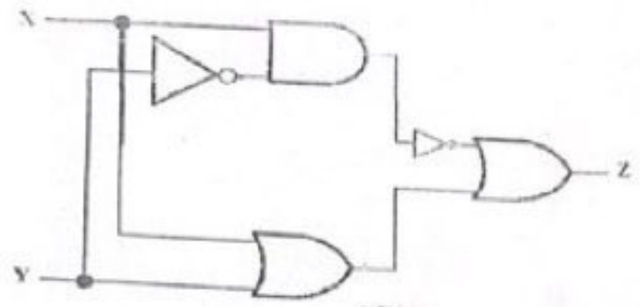
3) Draw the functional view of the computer? and show their possible operations that can be performed by computer? Apply one of these operations by using real component of computer?

Question 3: (15 + + 5 + 5= **25 marks**)

1) Consider the following logic circuit:



1) Derived an expression for the output of the logic circuit?

2) Write a truth table of the logic circuit?

3) Name each gate of the logic circuit

2) List أذكر two factors for increasing Microprocessor speed?

3) Plot أرسم a structure view of the computer?

Question 4: (8 + 8 + 9 = **25 marks**)

1) Show the main structural components of a control unit?

2) Draw the memory hierarchy and show their parameters?

3) What is the best method of writing in cache memory? Why?

Good Luck

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Final Exam of First Semester of Academic Year 2018/2019

Answer all questions:

Question 1: (10 + 15 = 25 marks)

1) Use the appropriate lines that shown below for connecting the following modules together

2) Compare ... between the following:

i. Hardwired program **and** Software program.
ii. PROM and EPROM.
iii. Associative mapping and Direct Mapping *(in Cache Memory)*

Question 2: (5+ 15 + 5 = 25 marks)

1) List steps of fetch cycle?

2) The hypothetical machine has three instructions.

0000: Load AC from Memory
0001: Store AC to Memory
0010: Load Memory to I/O buffer

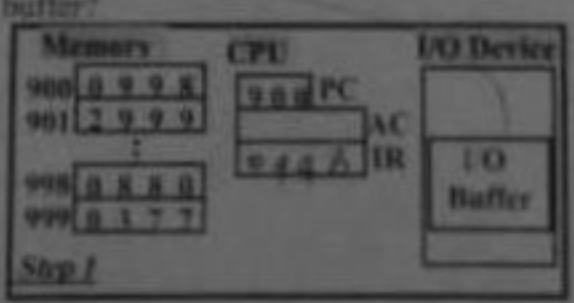
and the instruction format as follows:

Instruction Format

a) Show the program execution (using the format of Figure 4) to transfer the value **0377** at **999** address into I/O buffer?

b) Determine step and type of execution for each execute cycle?

c) How many instruction cycles are performed to transfer the value **0377** at **999** address into I/O buffer?



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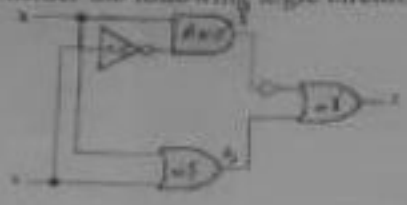
3) Draw the functional view of the computer? and show their possible operations that can be performed by computer? Apply one of these operations by using real components of computer?

Question 3 (15 + 5 + 5= **25 marks**)

1) Consider the following logic circuit:



1) Derived an expression for the output of the logic circuit?

2) Write a truth table of the logic circuit?

3) Name each gate of the logic circuit

2) List two factors for increasing Microprocessor speed?

2)Explain read operation of cache?

3) Plot a structure view of the computer?

Question 4: (8 + 8 + 9 = **25 marks**)

1) Show the main structural components of a control unit?

1)what is Bus structure explain it in detail?

2)Draw the memory hierarchy and show their parameters?

3)What is the best method of writing in cache memory? Why?

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HADHRAMOUT UNIVERSITY
COLLEGE OF COMPUTERS & INFORMATION TECHNOLOGY
FINAL EXAMINATION
Second Attempt

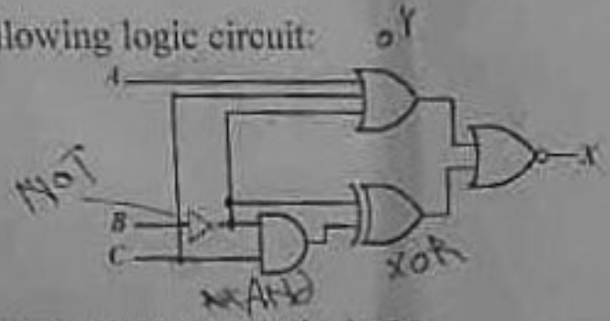
Academic year: 2018 – 2019
Day and Date: / July - 2019
Examiner: Dr. Saeed Bamaarnoon
Time allowed: 2 Hours & 30 Minutes

Exam Semester: First
Level: Second
Department: CS & IT
Subject: Computer Organization & Architecture

Answer all of the following questions:

Question 1: (5 x 3 = 15 marks)

Consider the following logic circuit:



1) Name all gates are used in the given logic circuit?

2) Write the logic expression of the given logic circuit?

3) Construct the truth table of the given logic circuit?

Question 2: (5 + 6 + 4 = 15 marks)

1) List key concepts suggested by Von-Neumann in designing of computer architecture?

2) Illustrate by drawing the following:

1. Computer component top-level view (structure).
2. Data Storage function.

3) How are data organized in direct mapping of cache memory?

See page (2) →

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Question 3: (5 + 10 = **15 marks**)

1) Use Hamming error-correcting codes on 4-bit data in (1000) and data out with error (1100)?

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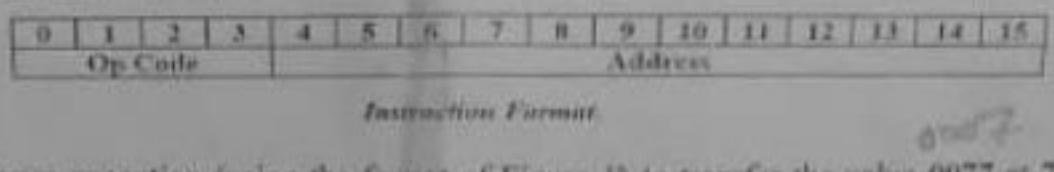
2) The hypothetical machine has three instructions:

0000: Load AC from Memory

0001: Store AC to Memory

0010: Load Memory to I/O buffer

and the instruction format as follows:



Instruction Format

1. Show the program execution (using the format of Figure 1) to transfer the value **0077** at **734** address into I/O buffer?
2. Determine step and type of execution for each execute cycle?
3. How many instruction cycles are performed to transfer the value **0077** at **734** address into I/O buffer?

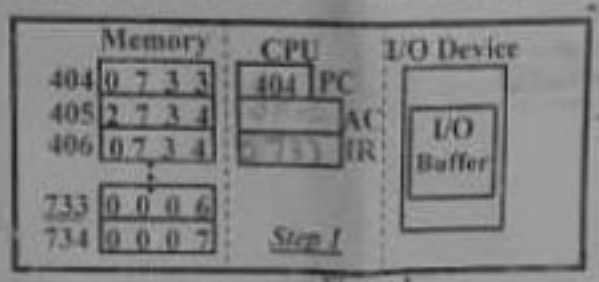
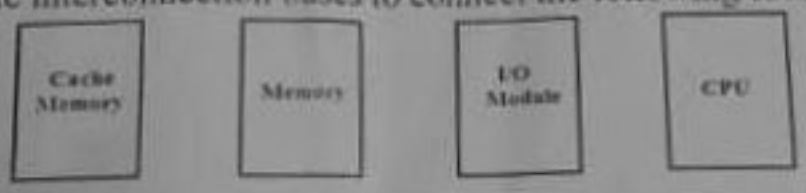


Figure 1

Question 4: (6 + 9 + 9 = **25 marks**)

1) Use the appropriate interconnection buses to connect the following four modules:



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2) Compare between the following:

1. Hard disk & Floppy disk
2. SRAM & DRAM
3. Hardwired program & Software program

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3) Determine the reason of the following:

1. Interface (Controller).
2. One address to pointed each Page.
3. Direct Memory Access (DMA)

Good Luck

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COLLEGE OF COMPUTER & INFORMATION TECH...

FINAL EXAMINATION

Academic year: 2018 - 2019
Day and Date: Thursday / 3rd January - 2019
Examiner: Dr. Saeed Mohammed Rawashdeh
Time allowed: 1 Hours & 30 Minutes

Exam Semester: Second
Level: Second (Grade Six + Seven)
Department: CS & IT
Subject: Computer Organization & Architecture

Answer all of the following questions:

Question 1: (15 marks)

Consider the following expression:

$$(A + \overline{B} + C) + [\,(\overline{B}C) \oplus \overline{B}\,]$$

1) Draw the logic circuit represented by the given expression?

2) Name all gates are used in the logic circuit of the given expression?

3) Construct the truth table of the logic circuit in (1)?

Question 2: (9 + 6 + 9 = 25 marks)

1)Determine the reason of the following:

1. Interrupt driven technique.
2. One address to pointed each Page.
3. Microprogram in control unit.

2) Sketch all input and output lines for the I/O module, then connect it to the CPU unit?

3)Compare between the following:

1. CD & DVD
2. EEPROM & FLASH
3. Real memory & Virtual memory

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Question 3: (5 x 3 = 15 marks)

1) Explain the real memory management?

2) Consider a microprocessor with 4-bit address bus and 8-bit data bus:

1. Compute a maximum memory size supported by the processor?
2. Calculate a number cycles are required to transfer 3 bytes data into memory? Why?

3) Assume:

- A processor has a set-associative mapped cache.
- Data word are 16 bits long.
- Total number of word can be stored in cache is 8 words.
- Tag is 8 bits long.
- Address is 2 bytes.

What is the size of Index and the size of this cache?

Question 4: (5 + 6 + 4 = 15 marks)

1) How can reduce the frequency of main memory access by CPU?

2) Illustrate by drawing the following:

1. SIMD (Parallel Processing).
2. Memory hierarchy with its factors.

3) How are data organized in set-associative mapping of cache memory?

Good Luck

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