Lecture 5

- Interconnection Structures
- Bus Interconnection
- Bus Structure

Interconnection Structures:

A computer consists of a set of components or modules of three basic types (processor, memory, I/O) that communicate with each other. In effect, a computer is a network of basic modules. Thus, there must be paths for connecting the modules.

- The collection of paths connecting the various modules is called the *interconnection structure*.
- The design of this structure will depend on the exchanges that must be made among modules.
- Figure 3.15 suggests the types of exchanges that are needed by indicating the major forms of input and output for each module type:

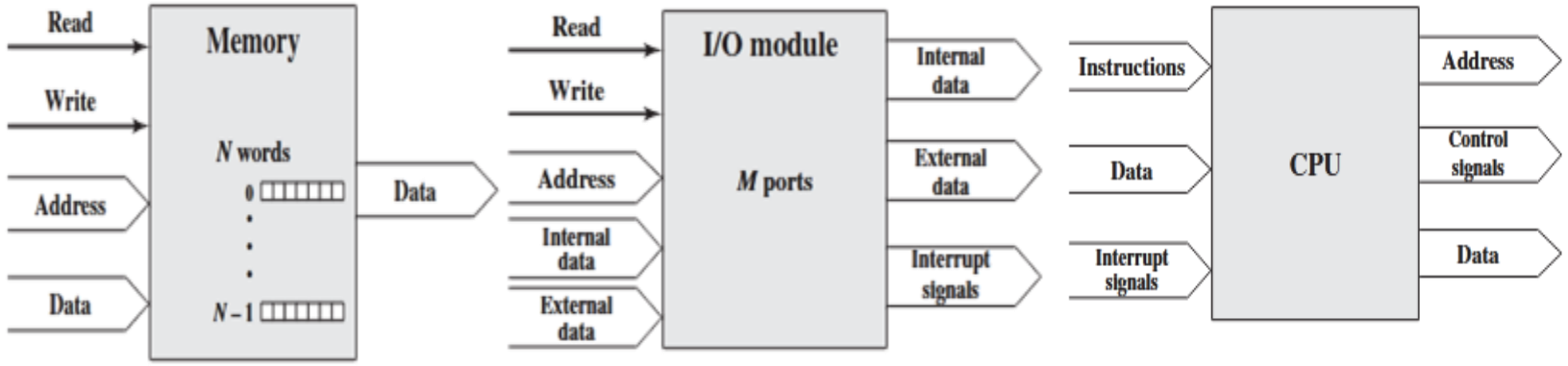


Figure 3.15 Computer Modules

The interconnection structure must support the following types of transfers:

- **Memory to processor:** The processor reads an instruction or a unit of data from memory.
- **Processor to memory:** The processor writes a unit of data to memory.
- **I/O to processor:** The processor reads data from an I/O device via an I/O module.
- **Processor to I/O:** The processor sends data to the I/O device.
- **I/O to or from memory:** For these two cases, an I/O module is allowed to exchange data directly with memory, without going through the processor, using Direct Memory Access(DMA).

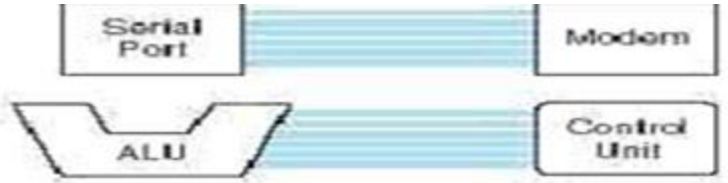
Bus Interconnection :

– A bus is a **communication pathway** connecting two or more devices. A key characteristic of a bus is that it is **a shared transmission medium.**

– A bus that connects **major computer components (CPU, memory, I/O)** is called **a system bus.**

– A bus can **be point-to-point,** connecting two specific components (as seen in Figure 3a)

a:



or it can be a common pathway that connects a number of devices, requiring these devices to share the bus (referred to as a multipoint bus and shown in Figure 3b).

B:

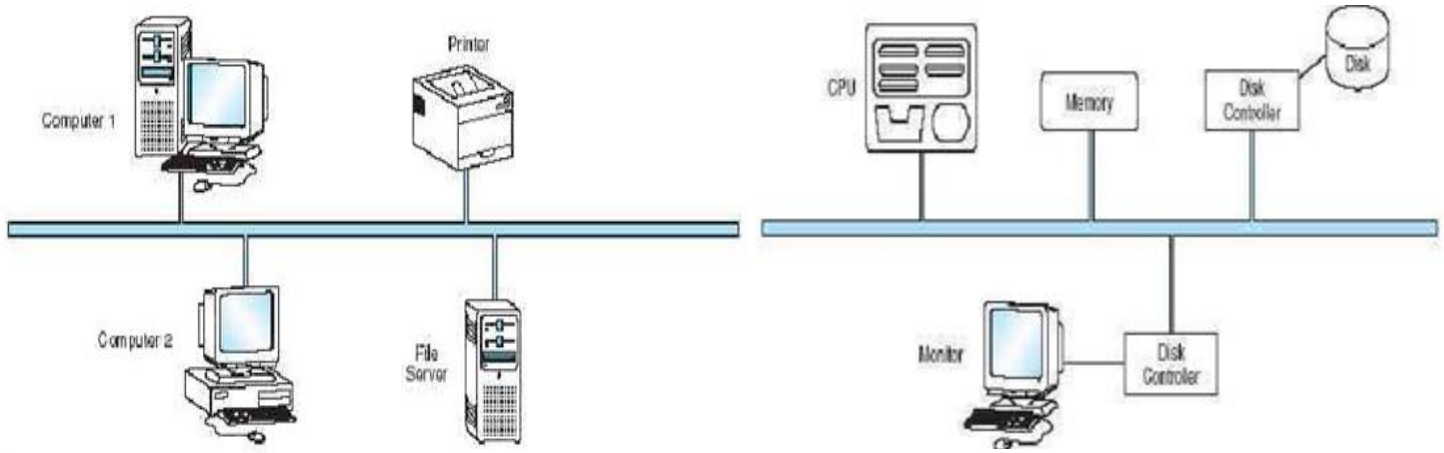


Figure 15: (a) Point-to-Point Buses. (b) A Multipoint Bus.

Computer systems contain a number of different buses that provide pathways between components at various levels of the computer system hierarchy.

The most common computer interconnection structures are based on the use of one or more system buses

- Bus Structure:

There are many different bus designs, on any bus the lines can be classified into three functional groups (Figure 16): data, address, and control lines. In addition, there may be power distribution lines that supply power to the attached modules.

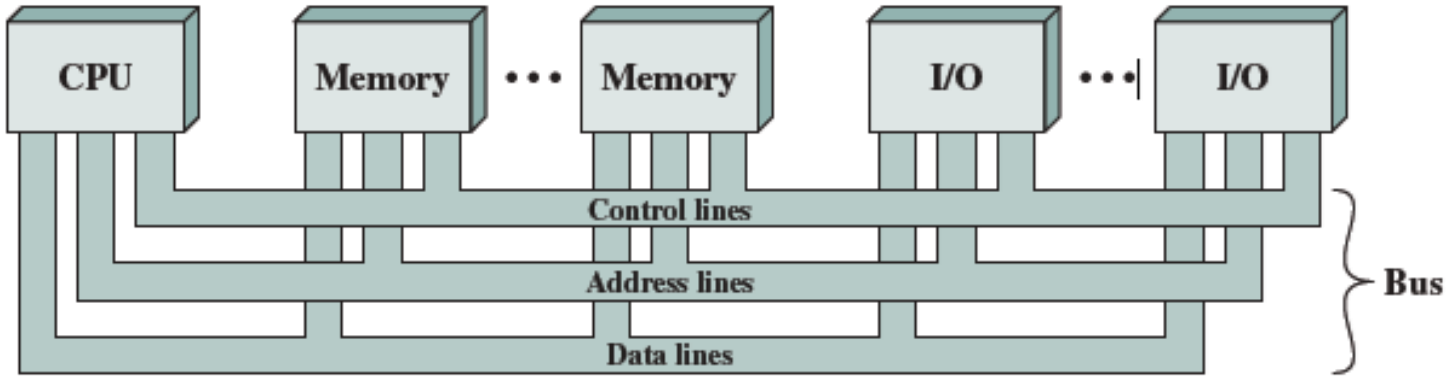


Figure 3.16 Bus Interconnection Scheme

The data lines provide a path for moving data between system modules. These lines, collectively, are called the data bus; the bus typically consists of 8, 16, or 32 separate lines, the number of lines being referred to as the width of the data bus. Since each line can carry only, 1 bit at a time, the number of lines determines how many bits can be transferred at a time.

- The address lines are used to designate the **source or destination of the data on the data bus.** For example, if the CPU wishes to read a word (8, 16, 32 bits" of data from memory, it puts the address of the desired word on the address clearly, the width of the address bus determines the maximum possible memory capacity of the system. Furthermore, the address lines are generally also use to address I/O ports.

- The control lines are used to **control the access to and the use of the data and address lines.** Since the data and address lines are shared by all components, there must be a means of controlling their use. Control signals transmit both command and timing information between system modules. Timing signals indicate the validity of data and address information. Common, signals specify operations to be performed typical control lines include.

- **Memory Write**: Causes data on the bus to be written into the addressed location.
- **Memory Read**: Causes data from the addressed location to be placed on the bus.
- **I/O Write**: Causes data on the bus to be output to the addressed I/O port.
- **I/O Read**: Causes data from the addressed I/O port to be placed on the bus.
- **Transfer ACK**: Indicates that data have been accepted from or placed on the bus.
- **Bus Request**: Indicates that a module needs to gain control of the bus.
- **Bus Grant**: Indicates that a requesting module has been granted control of the bus.
- **Interrupt Request**: Indicates that an interrupt is pending.
- **Interrupt ACK**: Acknowledges that the pending interrupt has been recognized.
- **Clock**: Used to synchronize operations.
- **Reset**: Initializes all modules.

- The operation of the bus is as follows. **If one module wishes to send data to another, it must do two things**: (1) obtain the use of the bus, and (2) transfer data via the bus.
- It must then wait for that second module to send the data.

Lecture 6

Memory Hierarchy