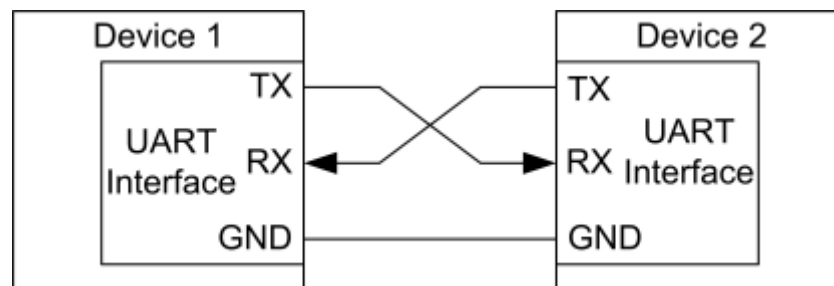


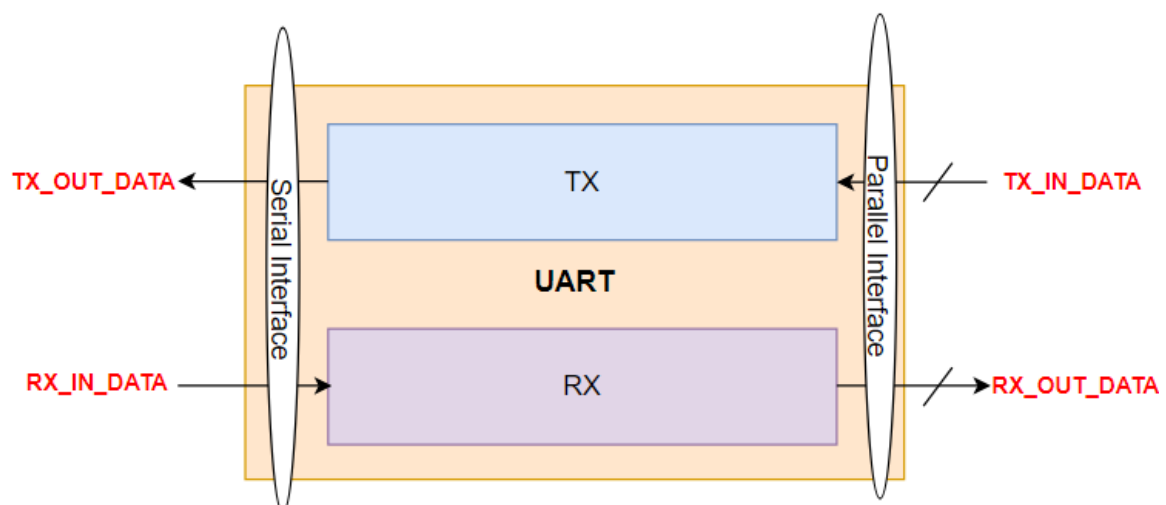
# UART Transmitter

## Introduction: -

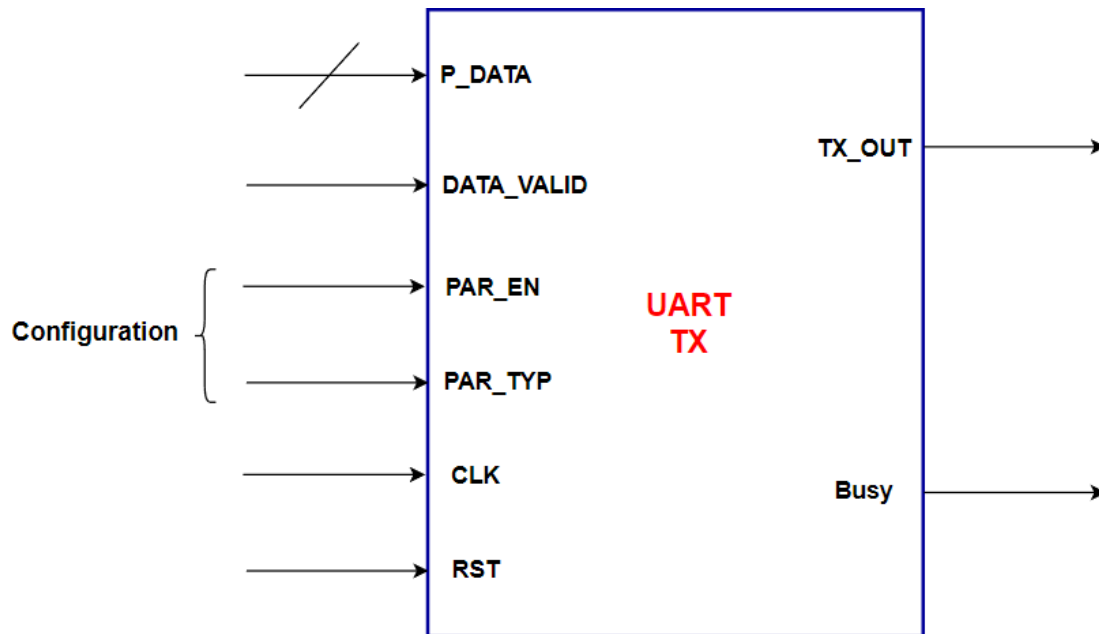
- There are many serial communication protocols as I2C, UART and SPI.
- A **U**niversal **A**synchronous **R**eceiver/**T**ransmitter (UART) is a block of circuitry responsible for implementing serial communication.
- UART is Full Duplex protocol (data transmission in both directions simultaneously)



- **Transmitting UART** converts parallel data from the master device (eg. CPU) into serial form and transmits in serial to the receiving UART.
- **Receiving UART** will then convert the serial data back into parallel data for the receiving device.



## Block Interface: -



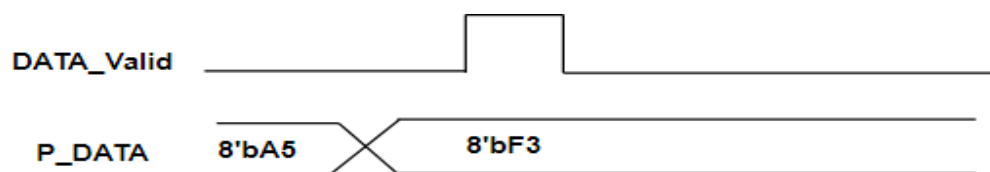
Port	Width	Description
CLK	1	UART TX Clock Signal
RST	1	Synchronized reset signal
PAR_TYP	1	Parity Type
PAR_EN	1	Parity_Enable
P_DATA	Parameterized (Default = 8)	Input data byte
DATA_VALID	1	Input data valid signal
TX_OUT	1	Serial Data OUT
Busy	1	High signal during transmission, otherwise low

## Specifications: -

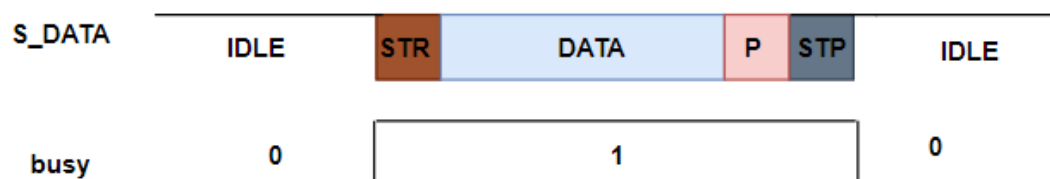
- UART TX receive the new data on **P\_DATA** Bus only when **Data\_Valid** Signal is **high**.
- Registers are cleared using asynchronous active low reset
- **Data\_Valid** is high for only 1 clock cycle
- **Busy** signal is **high** as long as UART\_TX is transmitting the frame, otherwise **low**.
- UART\_TX couldn't accept any data on **P\_DATA** during UART\_TX processing, however **Data\_Valid** get high.
- **S\_DATA** is high in the **IDLE** case (No transmission).
- **PAR\_EN** (Configuration)
  - 0: To disable frame parity bit
  - 1: To enable frame parity bit
- **PAR\_TYP** (Configuration)
  - 0: Even parity bit
  - 1: Odd parity bit

## Waveforms: -

### Expected Input: -



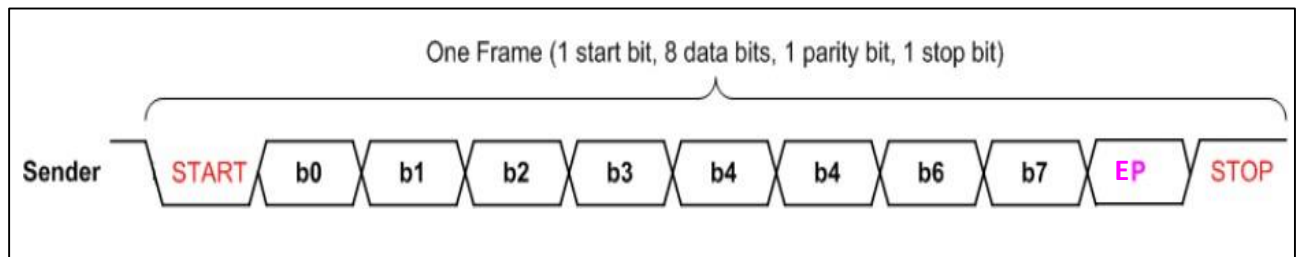
### Expected Output: -



## All Expected Output Frames: -

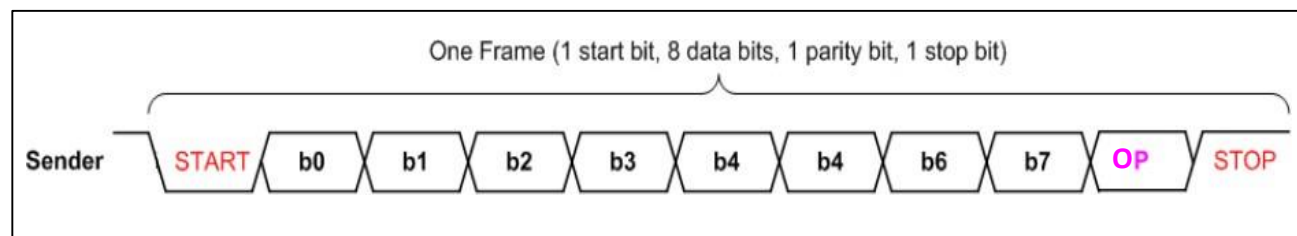
### 1. Data Frame (in case of Parity is enabled & Parity Type is even)

- One start bit (1'b0)
- Data (LSB first or MSB, 8 bits)
- Even Parity bit
- One stop bit



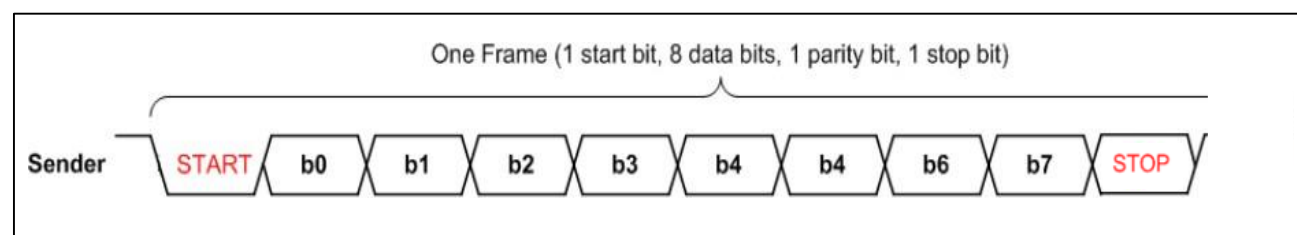
### 2. Data Frame (in case of Parity is enabled & Parity Type is odd)

- One start bit (1'b0)
- Data (LSB first or MSB, 8 bits)
- Odd Parity bit
- One stop bit

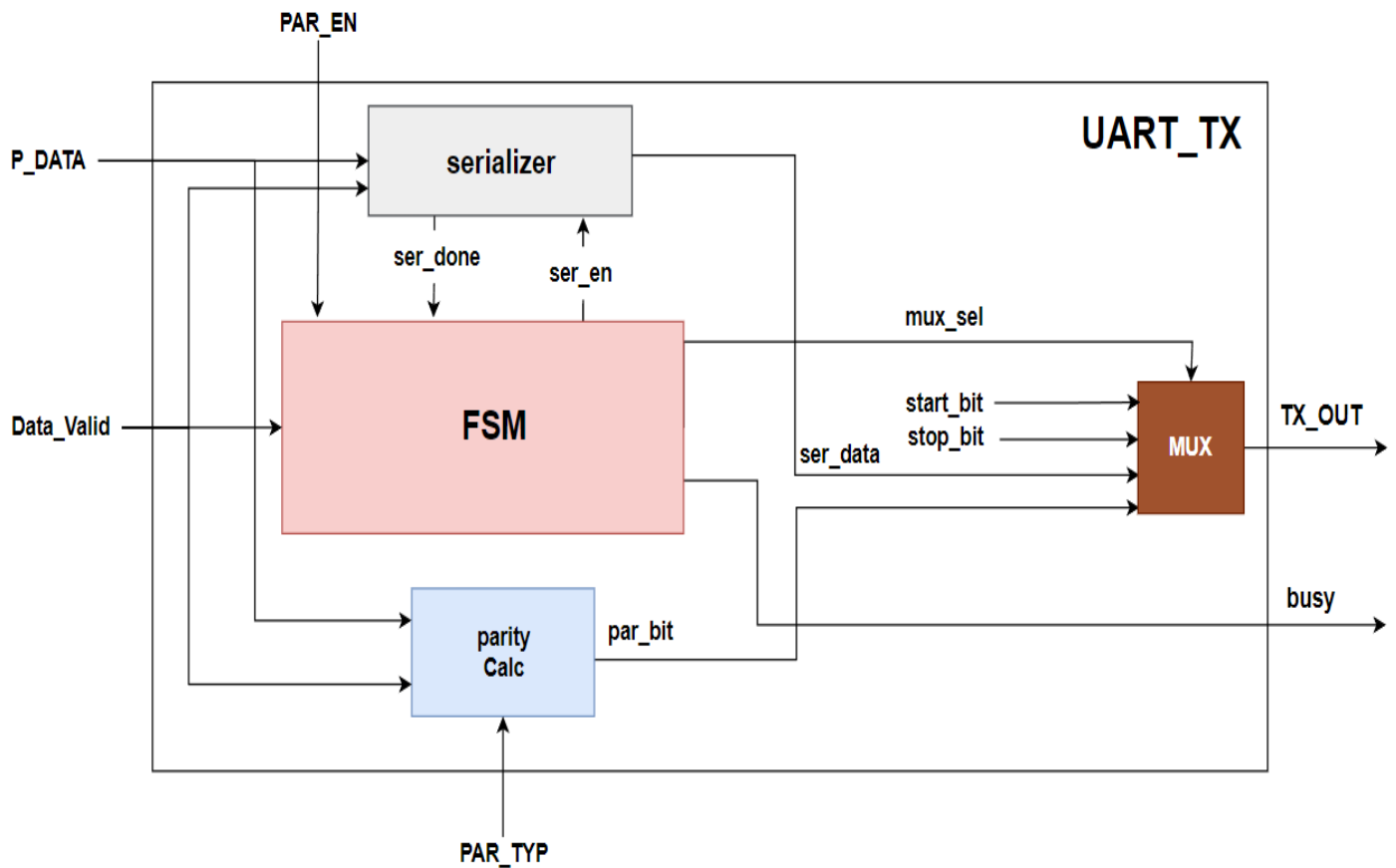


### 3. Data Frame (in case of Parity is not Enabled)

- One start bit (1'b0)
- Data (LSB first or MSB, 8 bits)
- One stop bit



## Recommended Block Diagram: -



## Requirements: -

- 1- Implement the above Specifications for UART TX using Verilog language.
- 2- Write a testbench to validate your design using 115.2 KHz clock frequency.