COMP 273
Introduction to Computer Systems

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Project & Midterm

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Project

Development Order

- Oct 28 – Pick your team members & name
- Nov 4 – Select the circuits you will reuse from your assignments and divide the work up between team members, construct the high level architecture (make a non-parallel and parallel plan with merge)
- Nov 18 – Working (non-parallel) pipeline
- Dec 3 – Working parallel pipeline
- (bonus only if there is extra time)

Suggestions

- Divide the CPU into modules and make each one work on its own as a black box.
- Merge working black boxes one at a time.
- Have an overall architectural plan for the CPU early, then
  - Built it in increments
  - Test each increment
- Only think about the bonus if you've got extra time.

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Midterm Exam

Midterm Structure

- Midterm Oct 25 (Thursday, in class)
  - 4 questions (1 easy, 2 medium, 1 harder)
  - Topics:
    - Operation of motherboard
    - Number systems and data representation
    - Digital circuit logic problems
    - The operation of a basic CPU
    - Pipeline and Classical CPU knowledge
  - Possibly 1 definition question and 3 problems, expect a circuit design question.

Midterm Content

- Content:
  - Number representations and conversions
  - Memory representations
  - Hardware parts / definitions
  - Circuit problems
  - Basic circuits: PAL, Flip-flops, MUX, etc.
    - Be sure to know how to use and build
  - Different CPUs and how they function
    - Classical & Pipeline
  - All class slides and readings not related to MIPS programming
    - This is a hardware & circuit exam

Circuit Question

- Candy dispenser machine. Input device signals when a coin is inserted (assume only 25 cent coins accepted). Gum costs $0.75 and user presses 1A (two buttons), chocolate costs $1.00 with 1B, candy is $0.50 with 2A. Assume each dispenser item has a motor that requires a single signal to drop the candy.

Bus Controller

- A bus is shared between many system-board slots that may be wanting to access the bus at the same time. Discuss the following bus controller architectures:
  - Slot asks permission (by byte, by job)
    - First come first serve
    - Priority based
  - Collision detection
  - What does this say about performance?

Peripheral Questions

- Communicate with a modem card: status register (dial tone, signal, busy, received, send, dial), data register, phone-number (destination) register.
  - Describe how we might control this from assembler if we wanted to send a string?
    - Masking bits
    - Dialling

Stall Question

- Assume a 4-stage pipeline where each stage takes 1 ns to complete. The stages are: fetch instruction, get register data, ALU, save register data. Assuming dump is the only solution the CPU uses, what is the execution loss given the following:
  - A save reg followed by a load reg instr.?
    - What circuitry would detect this?
  - A branch?

DMA Question

- A hard disk with DMA has a controller with five registers: source address on disk, destination address in RAM, number of bytes to transfer, a byte data register, and a command register. Assume it uses its own private DMA bus. The data register uses the system bus.
  - Describe how to program DMA in assembler
  - Compare speed with a standard byte by byte read, fgetc() vs. DMA read, fread().
    - Read in 10 consecutive bytes from disk. Assume seek 100 ns, byte read 1 ns, load & save 10 ns (/2 using private bus).