COMP 273

Introduction to Computer Systems

Part 2

Prof. Joseph Vybihal

Announcements

-

Last class

- Introduction to
  - Machine language
  - The system board / mother board
  - Encoding instructions in binary
  - The AND, OR and NOT gates

Any questions?

COMP 273
Introduction to Computer Systems

Lecture Outline

- Introduction to the Classical CPU
- Introduction to the hardware level
- Evolution of the CPU
    - Problematic issues and possible solutions

Try This Out At Home

- Using the CPU schematic from this lecture, think about how a FOR-LOOP would flow through the chip. Consider the following:
  - Registers,
  - ALU, and
  - Addressing

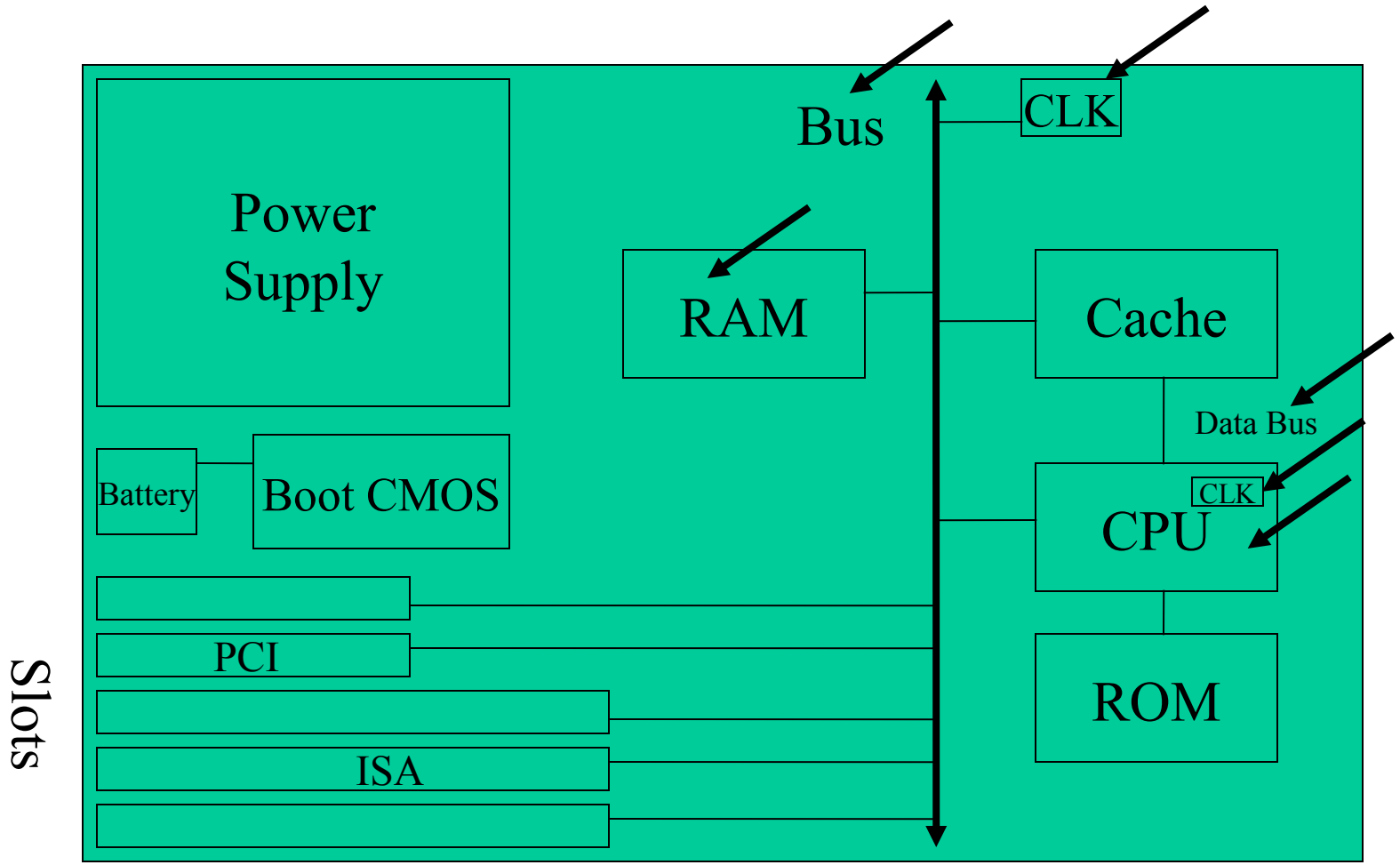
  Use this for loop:

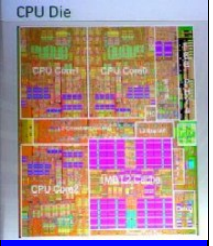
```
for (i=0; i<10; i++) print("%d",i);
```

Part 1

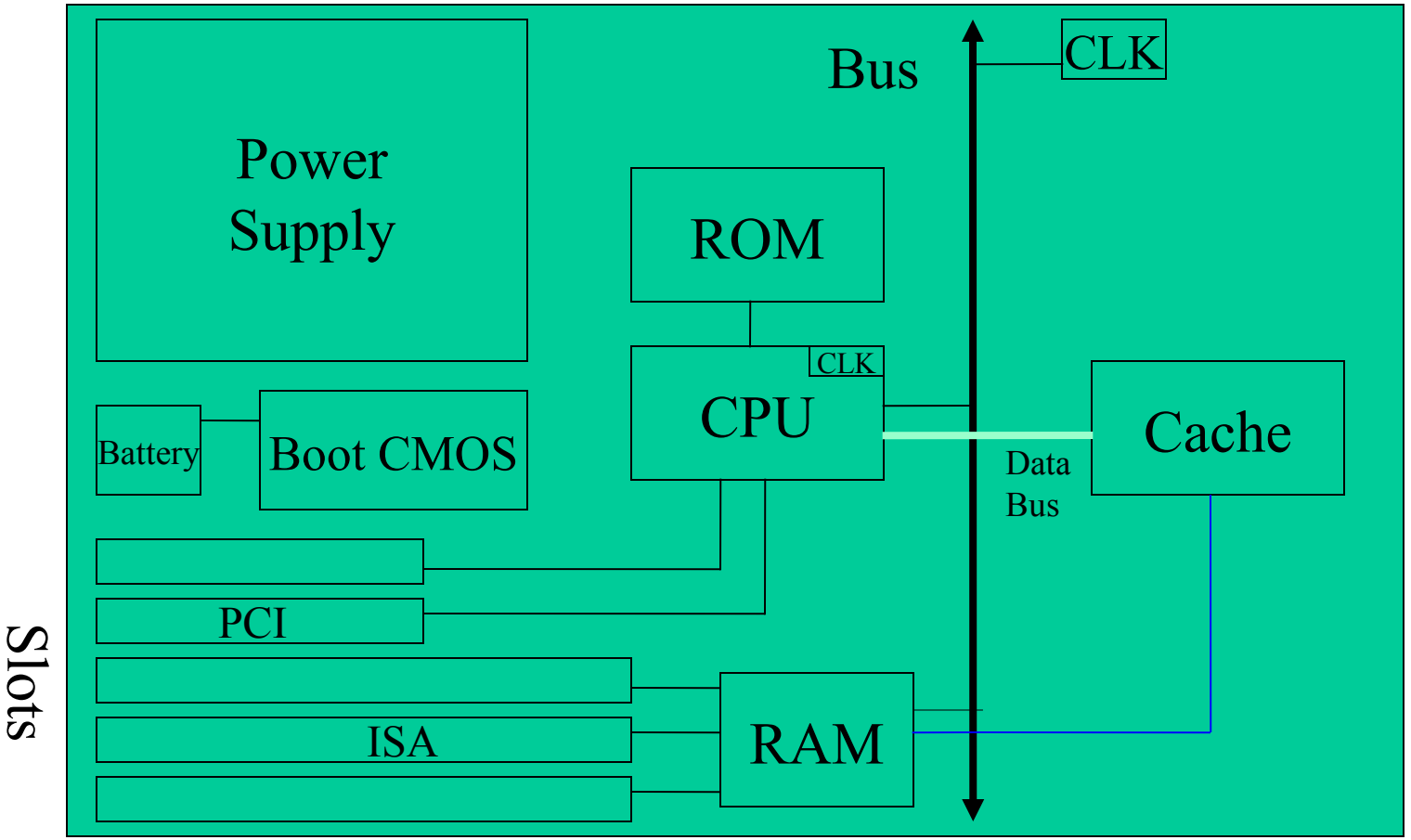
System board Specifics

System Board Schematic Traditional





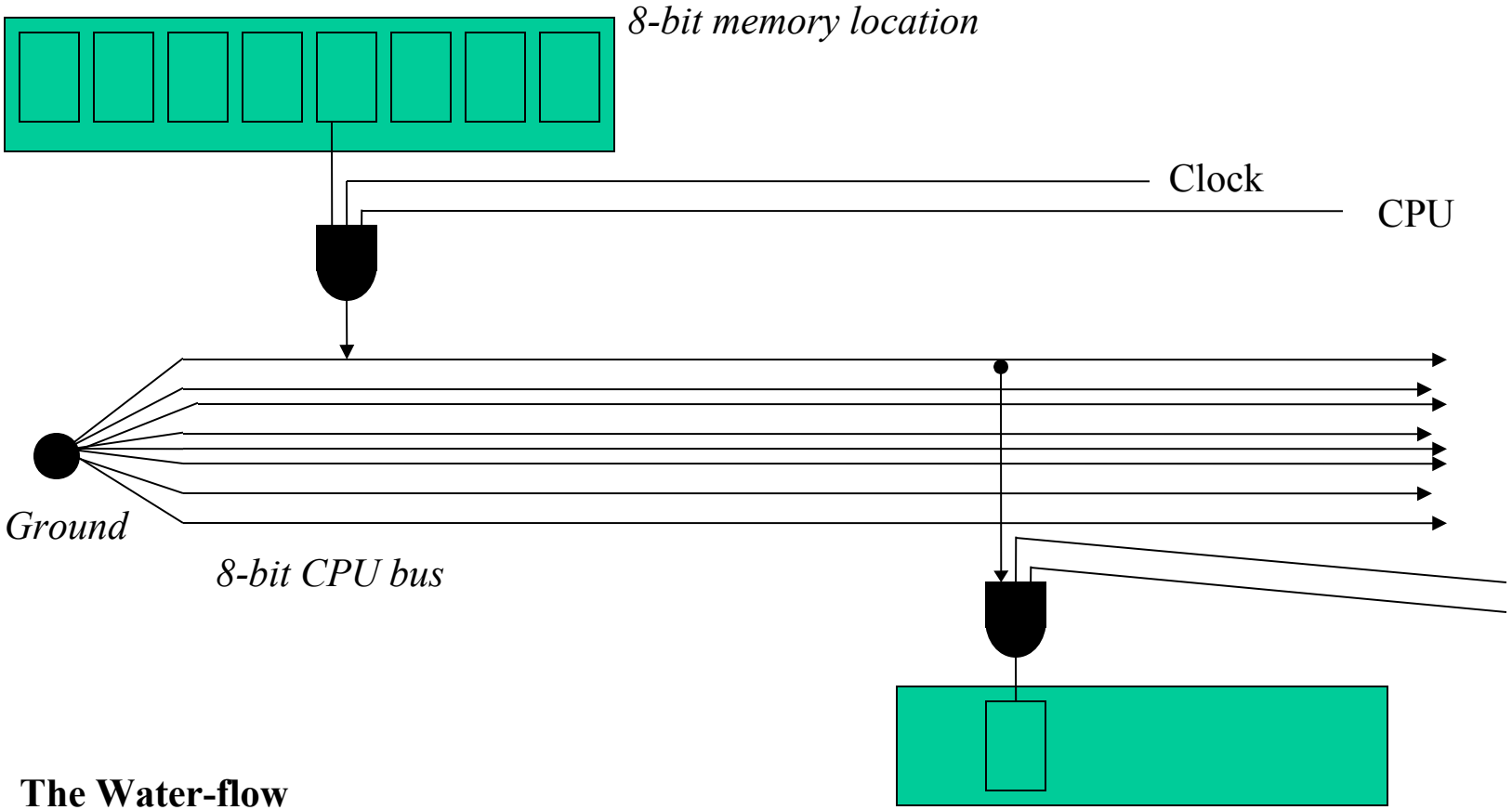
Motherboard Schematic Optimized



Communication Pathways

- Many:
  - System Buses (ISA, PCI), Data Bus, CPU Bus
- Purpose:
  - To simplify wiring by providing a common shared pathway for the electricity.
- Formation:
  - Composed of multiple wires, each wire for 1 bit.
- Functionality:
  - Each can execute independently of the other, therefore parallel
  - Individually, data must take turns to use a bus.
  - One byte passes through a bus per tick of the clock

A BUS



The Water-flow Analogy

Question

- How would a 10 byte string travel from RAM to a slot, assuming traditional motherboard?
- If I have a single byte in RAM and a single CPU instruction in RAM that both needed to exit RAM at the same time (one to go to the CPU the other to go to a slot), what would we do? (assuming traditional motherboard)
- In a traditional motherboard, what would happen if the CPU and a slot would need to save a single byte into RAM at the same time?

Timing

- Bus Clock (System Board Clock)
  - Byte (word) movement timing
  - Primary responsibility is gated access to the bus
  - Secondary effect: regulates data movement on motherboard
- CPU Clock
  - Byte (word) movement within the CPU chip
  - Instruction execution within the CPU chip
  - Influence does not reach outside of CPU chip

2GHz advertisement is the CPU clock…

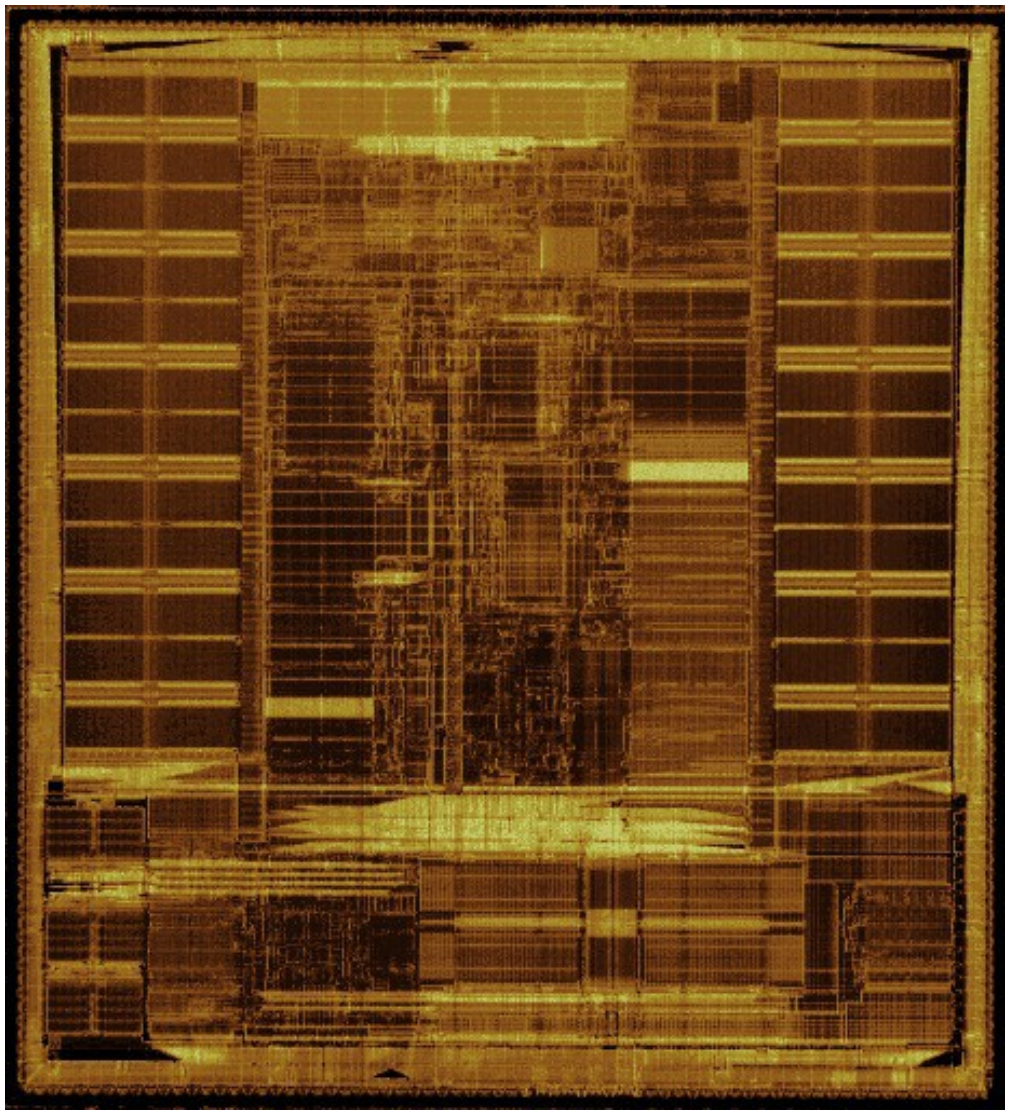
Question

- In a traditional motherboard, what effect does the two different clocks have on the execution of 10 sequential instructions without cache?
- In the optimized motherboard, answer the above question, without cache?
- In the optimized motherboard...
  - assume instructions want to copy a series of characters from one array into another array. How would this happen?
  - ...copy the contents of an array to a slot?

Part 2

CPU Specifics

The CPU



Basic Contents:

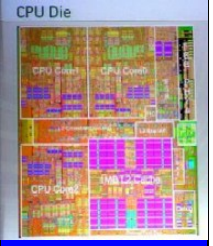
ALU
(Arithmetic Logic Unit)
(+ - > < ==, etc.)

Registers
(Fast Live Memory Locations)

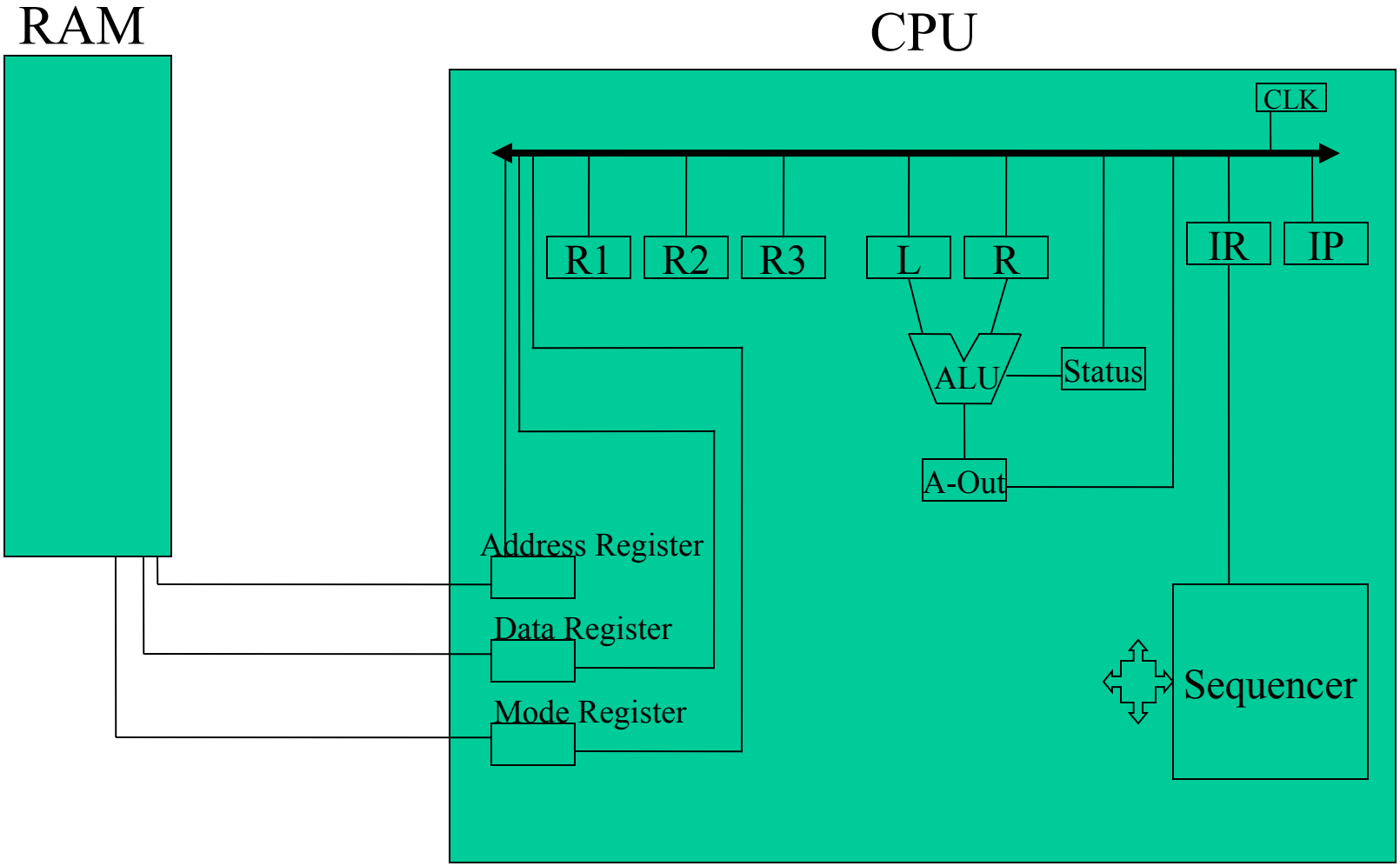
IP
(Instruction Pointer)
(a.k.a IC, Instr. Counter)
(points to the next instruction)

IR
(Instruction Register)
(stores the current instruction)

On-board Cache
(specially constructed for speed)



Classical CPU Schematic (no cache)



How does this work?

CPU Definitions 1/3

- Registers:
  - N general purpose registers 8, 64, or 128 bits long
  - Think of them as temp variables for the CPU

- The ALU System (Arithmetic Logic Unit)
  - Arithmetic and Logic operations
  - L, R, A-Out and Status are Specific Purpose Registers
    - L (left) and R (right) are inputs to ALU (binary op)
    - A-Out is the result of the operation
    - Status is used as input and output flag bits
      - input to tell ALU operation to perform (+ - * / or < > ! =)
      - output to report errors (overflow, divide by zero)

CPU Definitions 2/3

- IP (Instruction Pointer) or IC (Instr. Counter)
  - Next instruction address to execute
  - Loaded into/Used with the Address Register
- IR (Instruction Register)
  - Stores the current instruction being executed
  - Received from the Data Register
- The RAM Access Register System
  - Provides communication between CPU and RAM
  - Address Register: Please get/put data from/to this address
  - Data Register: Here is the data I just got/need to send
  - Mode Register: Flag register that selects between get & put

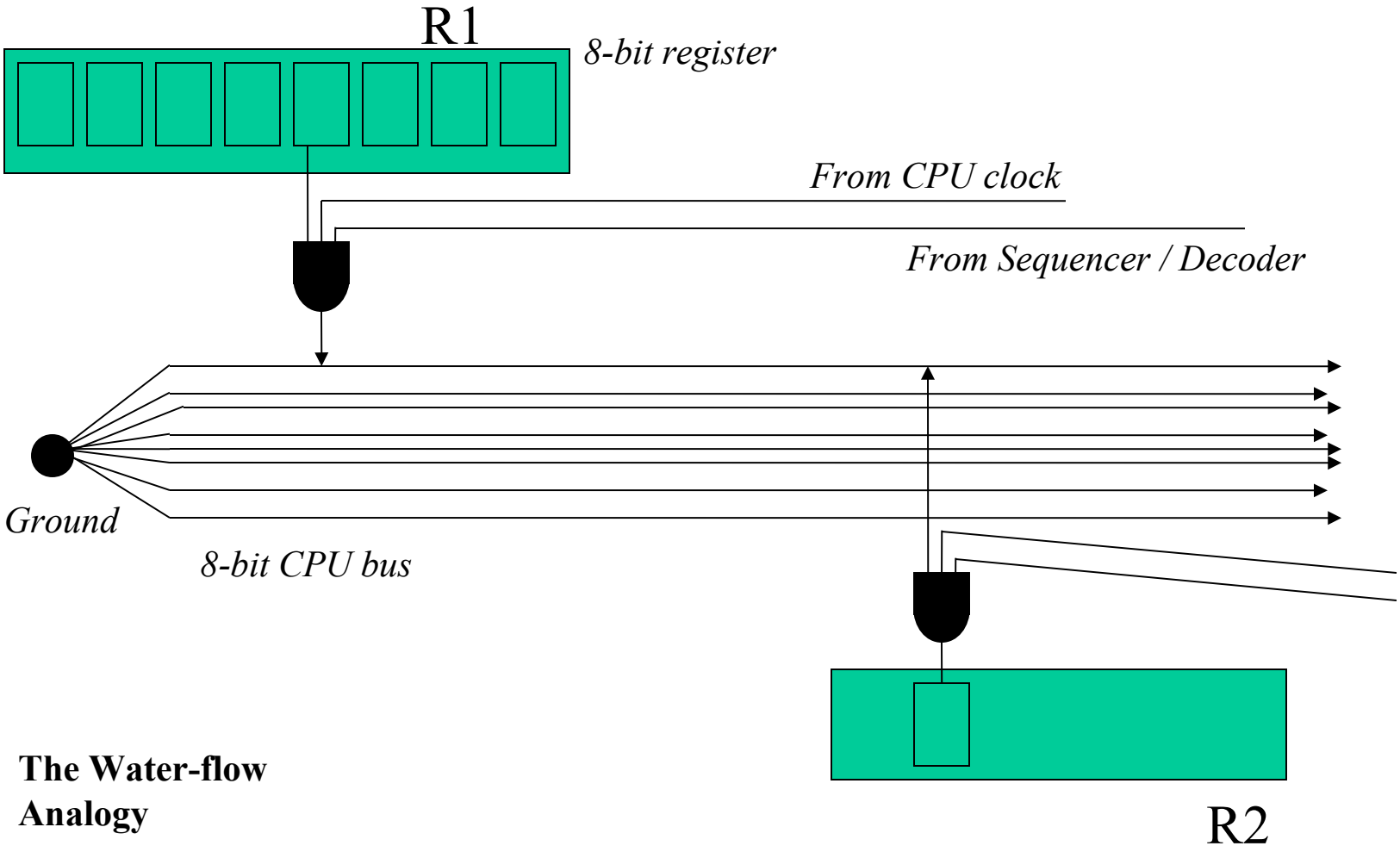
CPU Definitions 3/3

- CPU Clock
  - Each beat of the clock either:
    - Moves data across CPU bus, or
    - Moves the code from the IP to the sequencer
      - Some operations need the sequencer to function in ordered steps (each clock beat executes one step)
- Sequencer
  - A table of codes with circuits
  - Each circuit is a system of gated triggers
  - These triggers permit data to flow in a pre-determined order

CPU Data Flow & Control

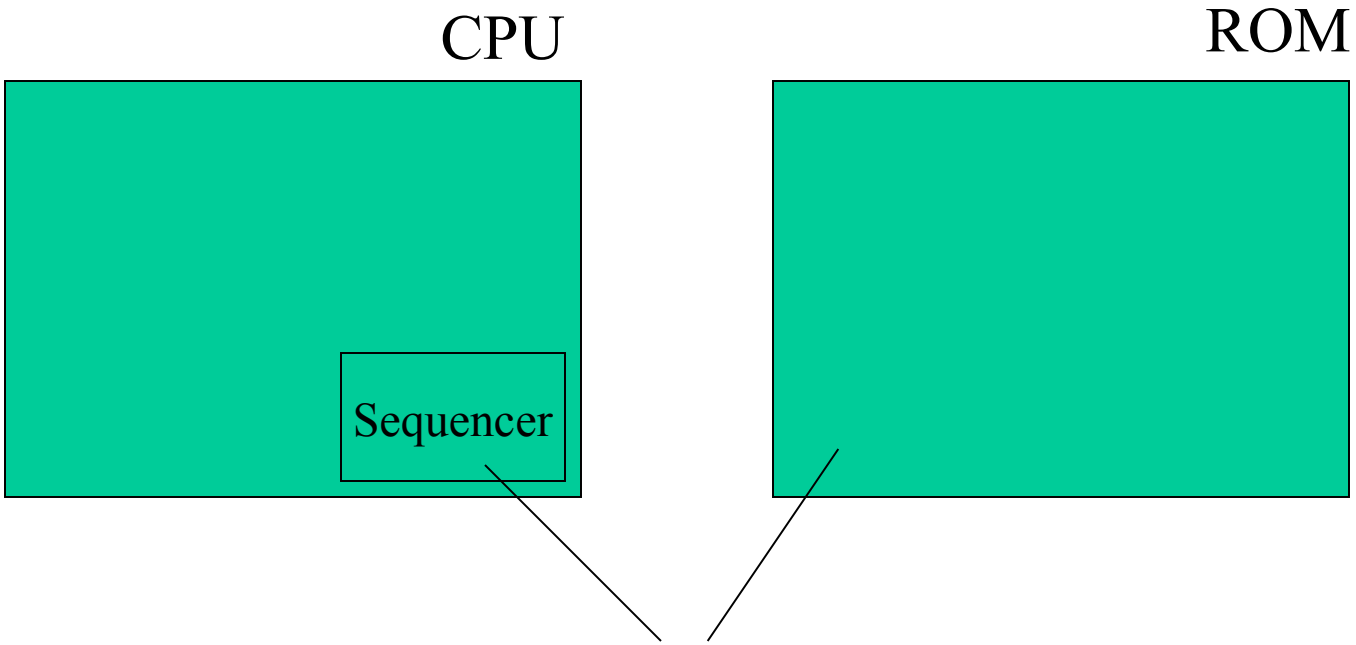
How the bus works

Motorola 6502 CPU



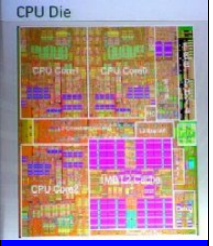
The Water-flow Analogy

Machine Language Exists in...



The Sequencer and the ROM contain circuitry that responds to machine language. These devices then cause the computer to execute the command.

Sequencer: “built-in” instructions ROM: “Extended” instructions



The Sequencer

Code look-up	Circuitry mapping
00000000 →	Each pattern triggers specific gates, and this causes specific things to happen
00000001	
00000010	
00000011	
00000100	
00000101	
00000110	
00000111	
00001000	

Assembler

Programming is about combing these codes into an order that makes the computer do interesting things

Different manufacturers:
Apply, Intel, AMD build their own circuitry and Codes, therefore Codes may be different

It's a TABLE!

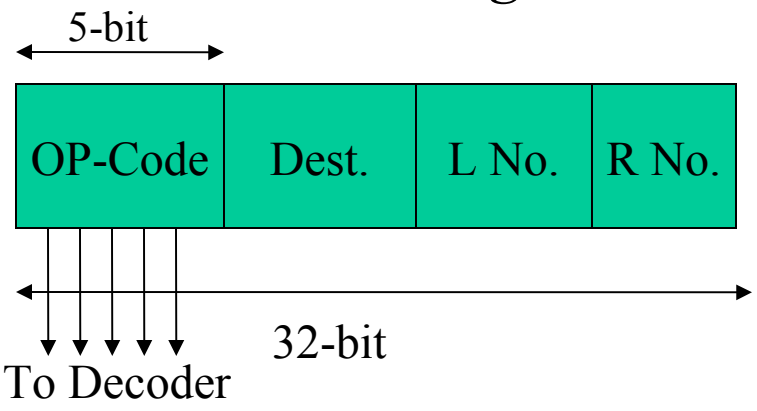
The IR & Decoder (Sequencer)

How does the computer know which gates to open and when?

Assume: R1 = R2 + R3 → ADD r1, r2, r3

Question: How does this addition function in the CPU?

The Instruction Register

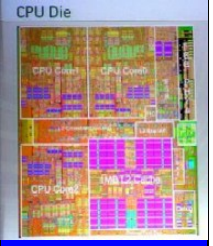


L No. → R# put into L register
R No. → R# put into R register
Dest → R# to put A-Out into
OP-Code:

- Used by decoder to trigger a circuit set to sequence and trigger the gates in a predetermined, built-in hardware order.

PART 3

The Evolution of the CPU



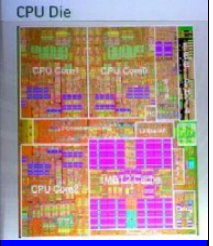
Intel CPU Family

Chip	Date	MHz	Transistors	Memory	Notes
4004	4/1971	0.108	2300	640	First microprocessor on a chip
8008	4/1972	0.108	3500	16 KB	First 8-bit microprocessor
8080	4/1974	2	6000	64 KB	First general-purpose CPU on a chip
8086	6/1978	5–10	29,000	1 MB	First 16-bit CPU on a chip
8088	6/1979	5–8	29,000	1 MB	Used in IBM PC
80286	2/1982	8–12	134,000	16 MB	Memory protection present
80386	10/1985	16–33	275,000	4 GB	First 32-bit CPU
80486	4/1989	25–100	1.2M	4 GB	Built-in 8-KB cache memory
Pentium	3/1993	60–233	3.1M	4 GB	Two pipelines; later models had MMX
Pentium Pro	3/1995	150–200	5.5M	4 GB	Two levels of cache built in
Pentium II	5/1997	233–450	7.5M	4 GB	Pentium Pro plus MMX instructions
Pentium III	2/1999	650–1400	9.5M	4 GB	SSE Instructions for 3D graphics
Pentium 4	11/2000	1300–3800	42M	4 GB	Hyperthreading; more SSE instructions

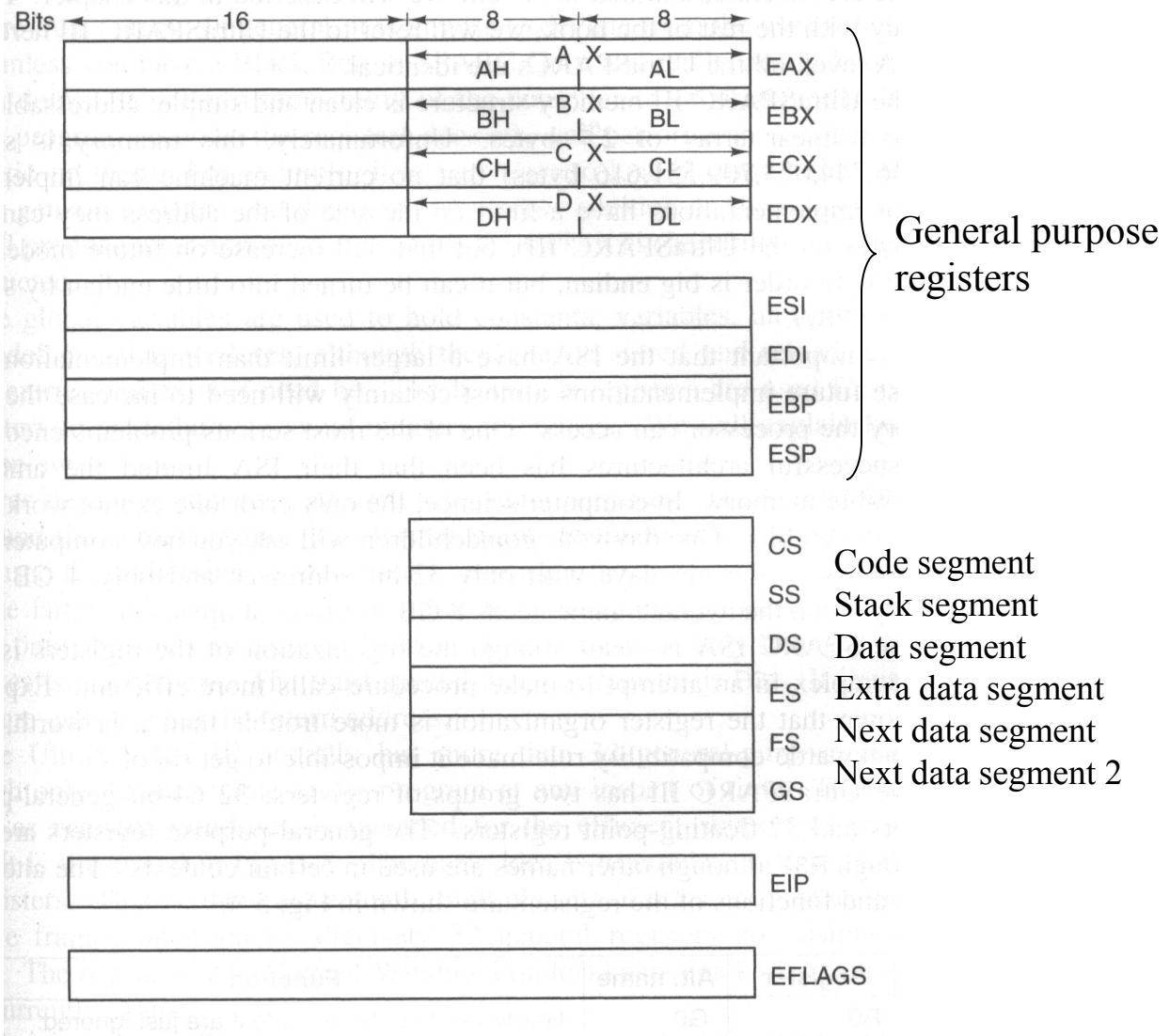
Itanium 2 7/8/02 1000
Core 2 Ex 7/27/06 3200

P4 Extreme 2004

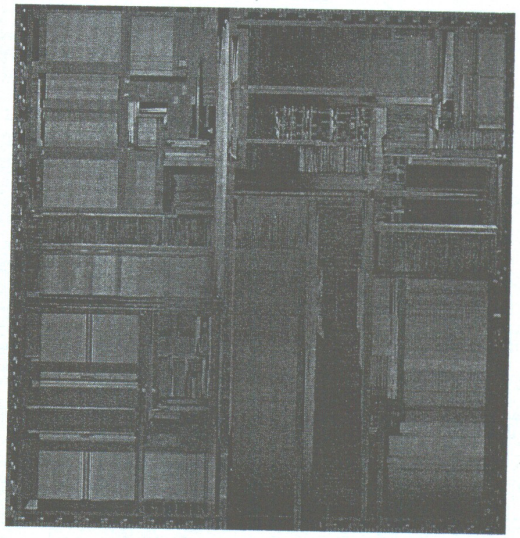
MMX – Multi media
SSE – Streaming multi data

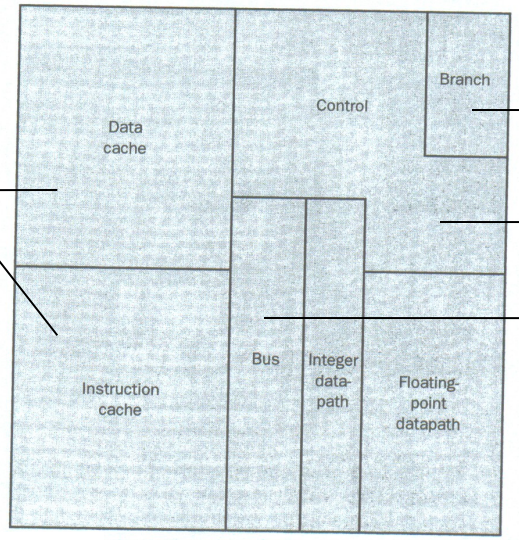


80x86 Registers



Intel Pentium





Cache:
Data
Instr.

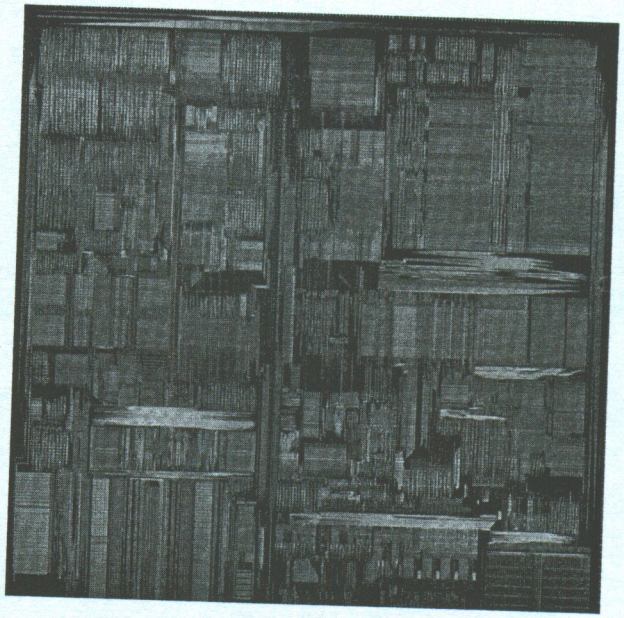
Branch

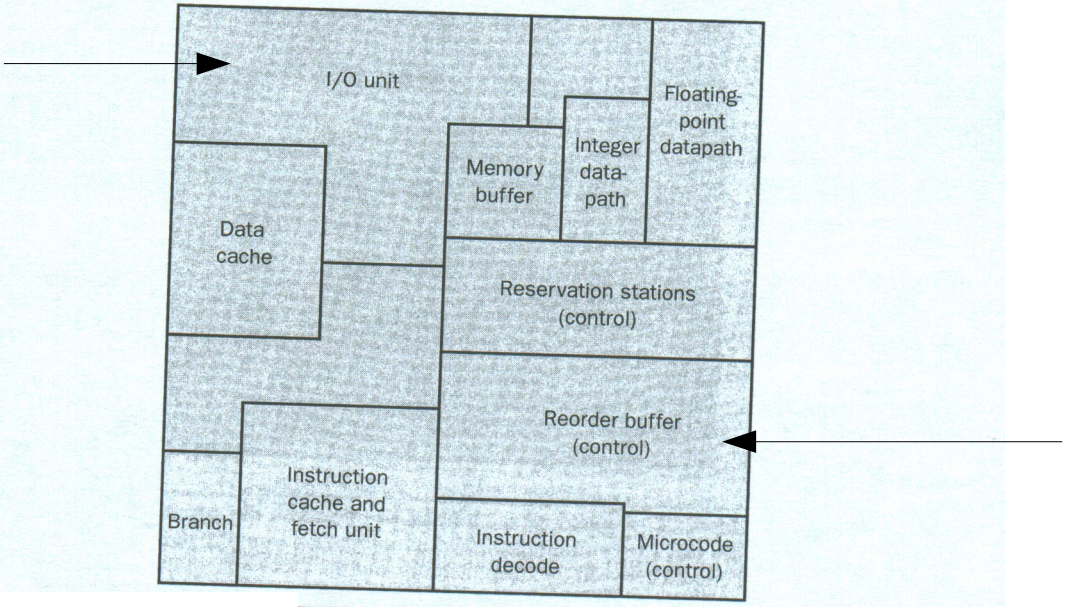
Sequencer

Buses: general, int, float


CPU Die

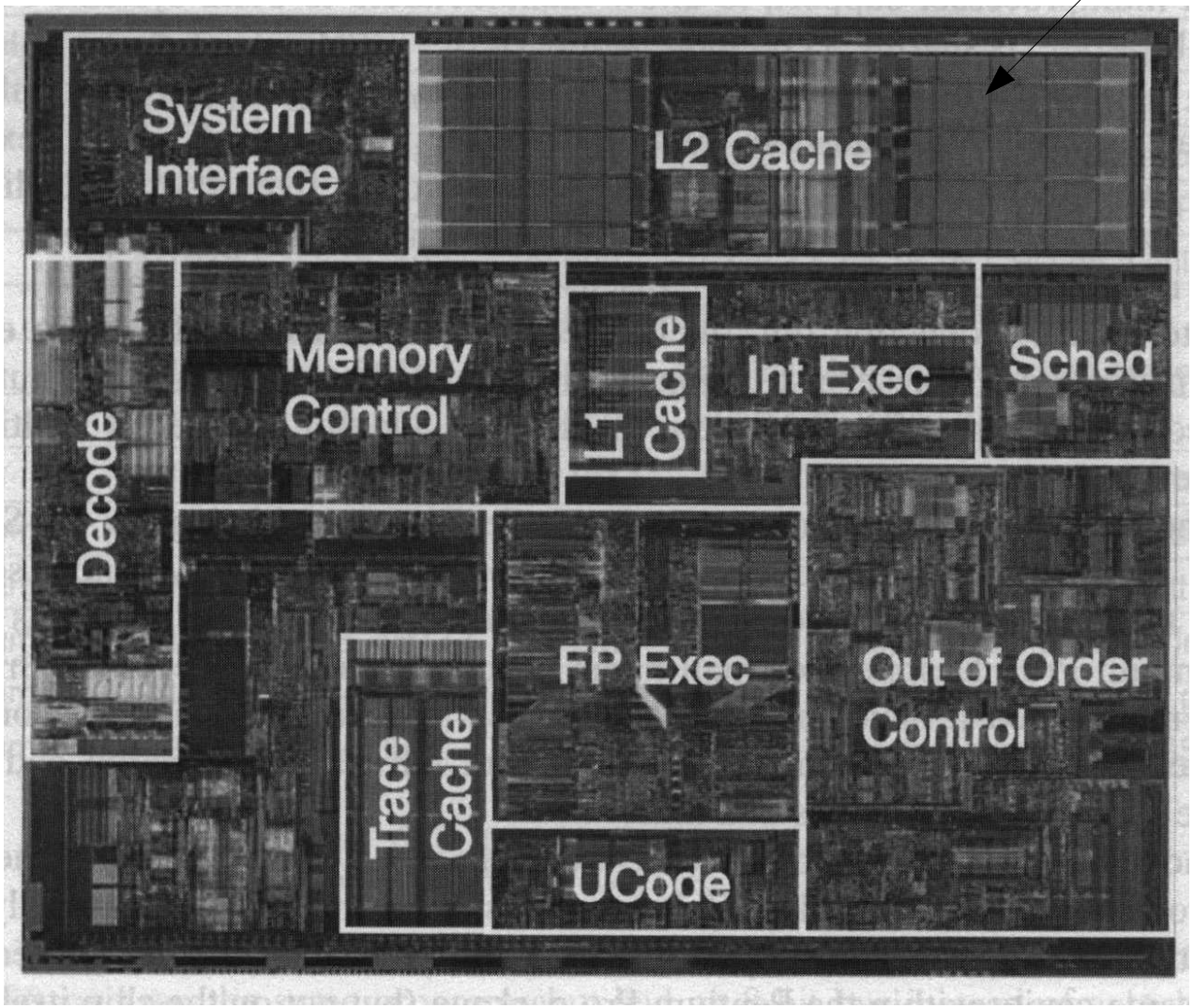
Pentium Pro



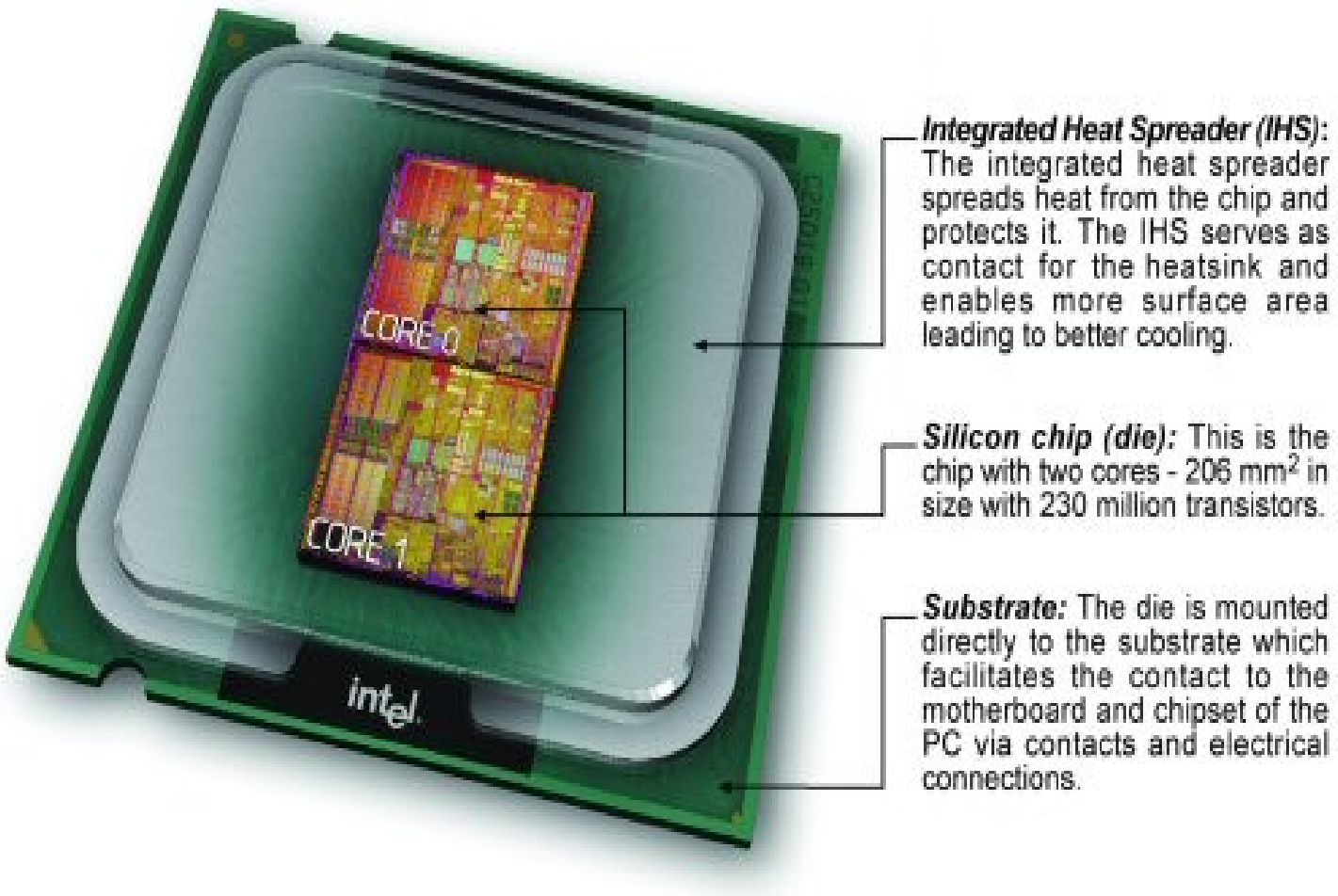

I/O unit
Floating-point datapath
Integer data-path
Memory buffer
Data cache
Reservation stations (control)
Reorder buffer (control)
Instruction cache and fetch unit
Branch
Instruction decode
Microcode (control)

Pentium 4

2004



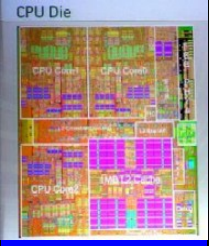
Pentium 5



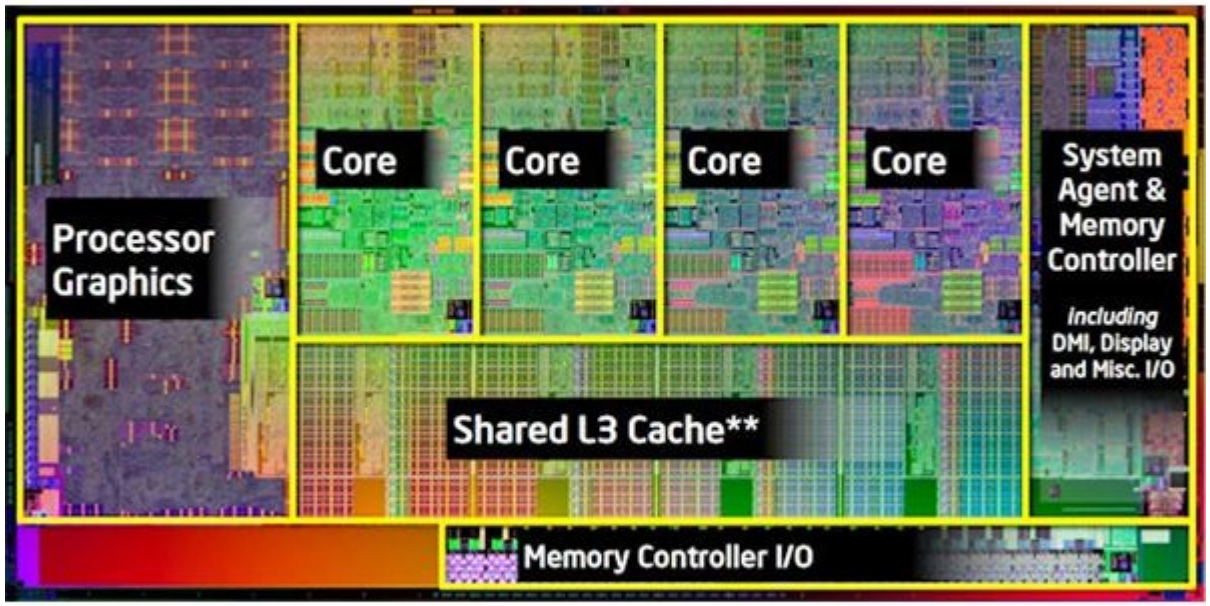
Integrated Heat Spreader (IHS): The integrated heat spreader spreads heat from the chip and protects it. The IHS serves as contact for the heatsink and enables more surface area leading to better cooling.

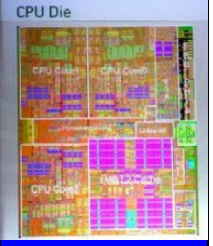
Silicon chip (die): This is the chip with two cores - 206 mm^2 in size with 230 million transistors.

Substrate: The die is mounted directly to the substrate which facilitates the contact to the motherboard and chipset of the PC via contacts and electrical connections.

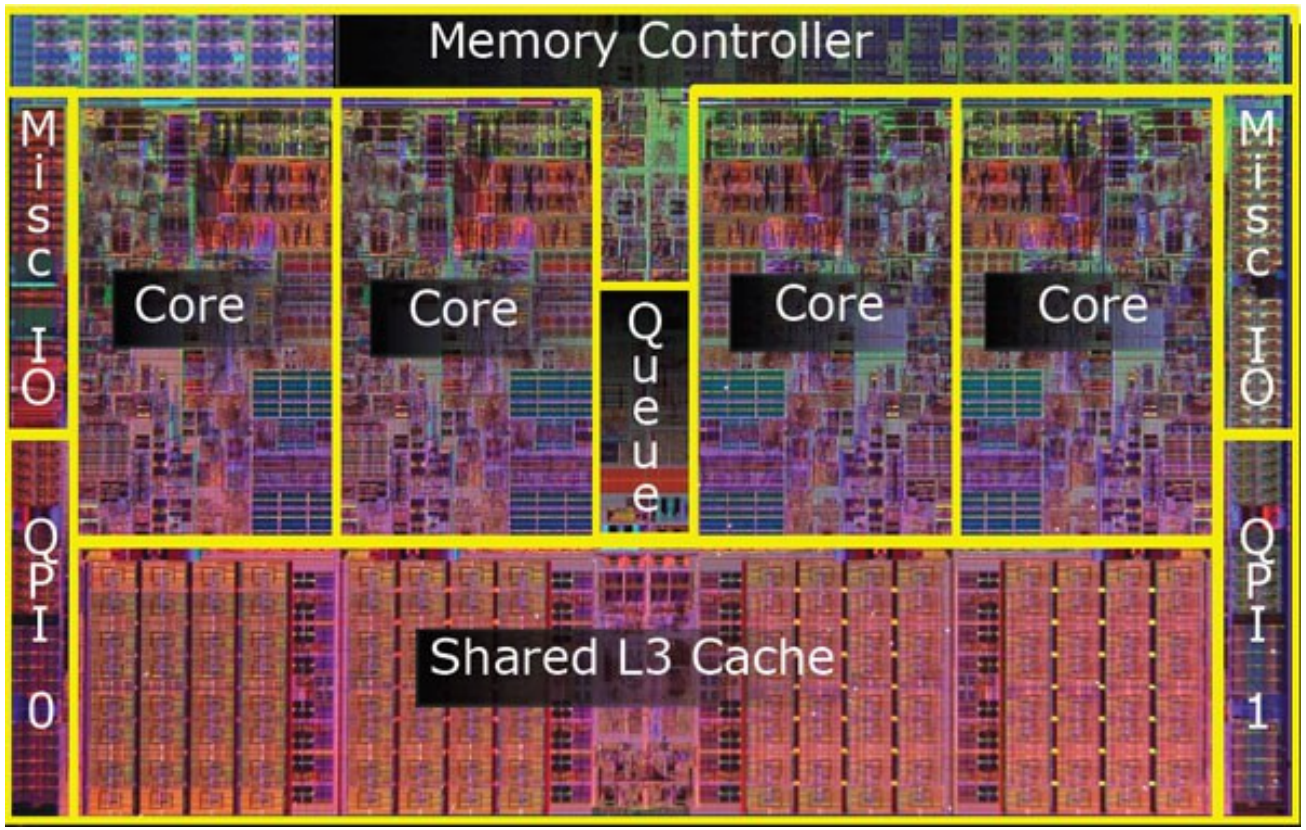

CPU Die

i5


Processor Graphics
Core
Core
Core
Core
System Agent & Memory Controller
Including DMI, Display and Misc. I/O
Shared L3 Cache**
Memory Controller I/O



i7



QPI = Quick Path Interconnect – 20 lanes, 80-bit "flit", 2 ticks per move, full duplex (replaces the FSB – Front Side Bus)

i7

Intel® 2nd Generation Core™ i7 Processor Family Comparison

Brand Name & Processor Number[1]	Base Clock Speed (GHz)	Turbo Frequency[2] (GHz)	Cores/ Threads	Cache	Memory Support	TDP	Socket (LGA)	Pricing (1k USD)
Intel® Core™ i7 NEW 3960X Unlocked	3.3	Up to 3.9	6/12	15 MB	4 channels DDR3 1600	130W	2011	$990
Intel® Core™ i7 NEW 3930K Unlocked	3.2	Up to 3.8	6/12	12 MB	4 channels DDR3 1600	130W	2011	$555
Intel® Core™ i7 Q1 20123820 Partially Unlocked	3.6	Up to 3.9	4/8	10 MB	4 channels DDR3 1600	130W	2011	TBD
Intel® Core™ i7-2700K Unlocked	3.5	Up to 3.9	4/8	8 MB	2 channels DDR3 1066/1333	95W	1155	$332
Intel® Core™ i7-2600K Unlocked	3.4	Up to 3.8	4/8	8 MB	2 channels DDR3 1066/1333	95W	1155	$317
Intel® Core™ i7-2600	3.4	Up to 3.8	4/8	8 MB	2 channels DDR3 1066/1333	95W	1155	$294

TDP = Thermal Design Power (needed to cool it down)

LGA = Land Grid Array (square socket shape, pins)

COMP 273
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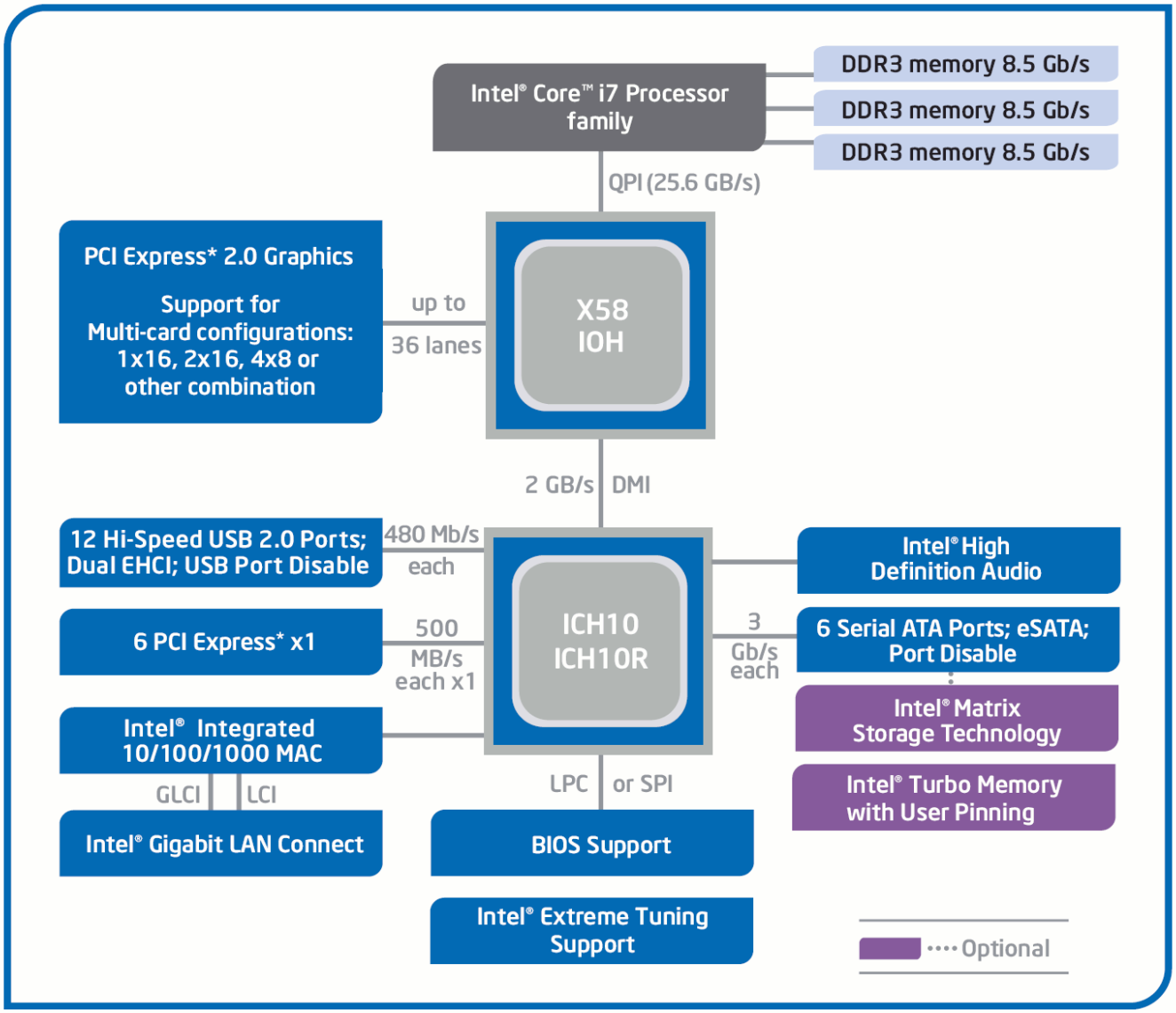
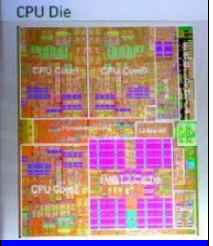
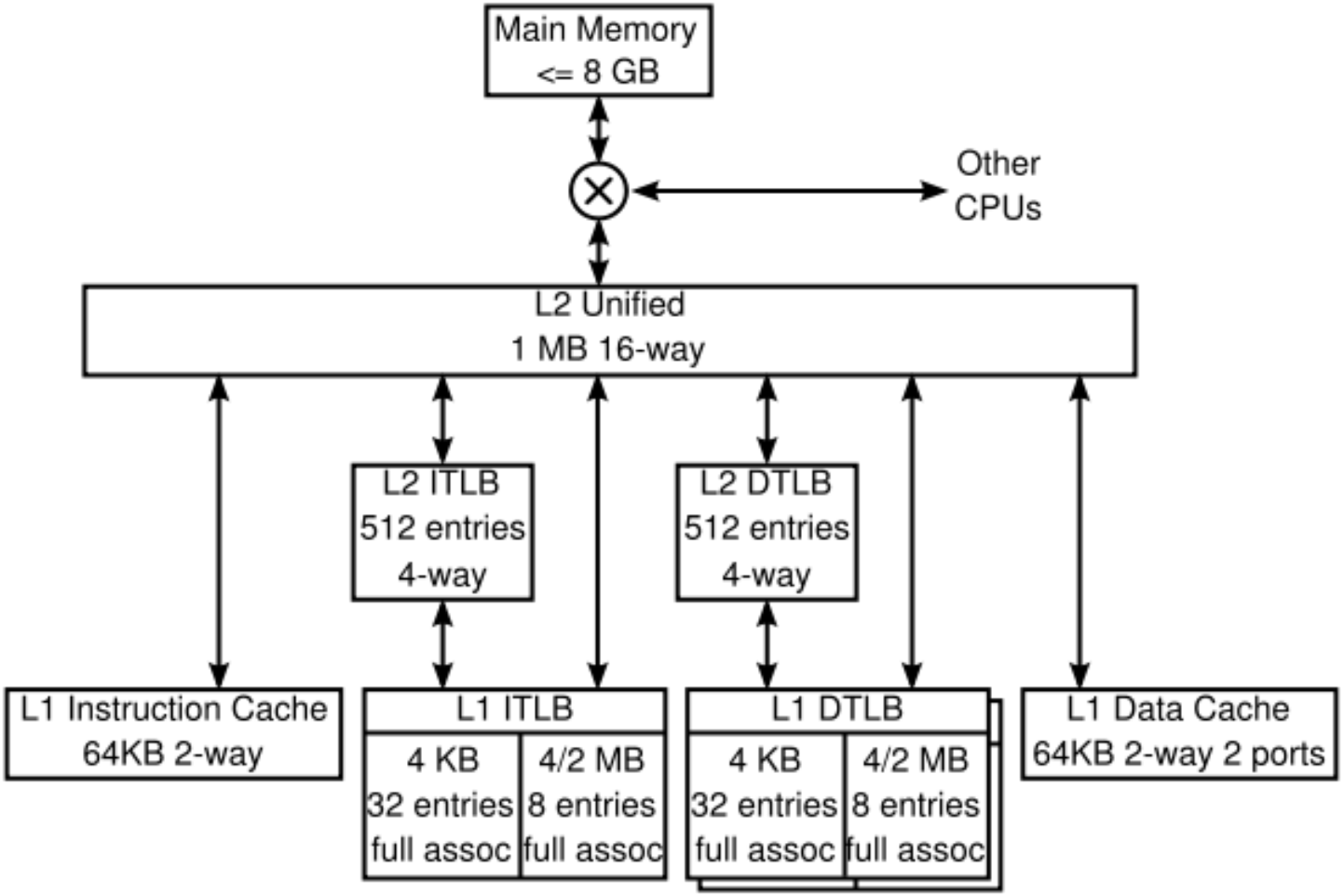
i7 Chip Set





L1 and L2 Cache

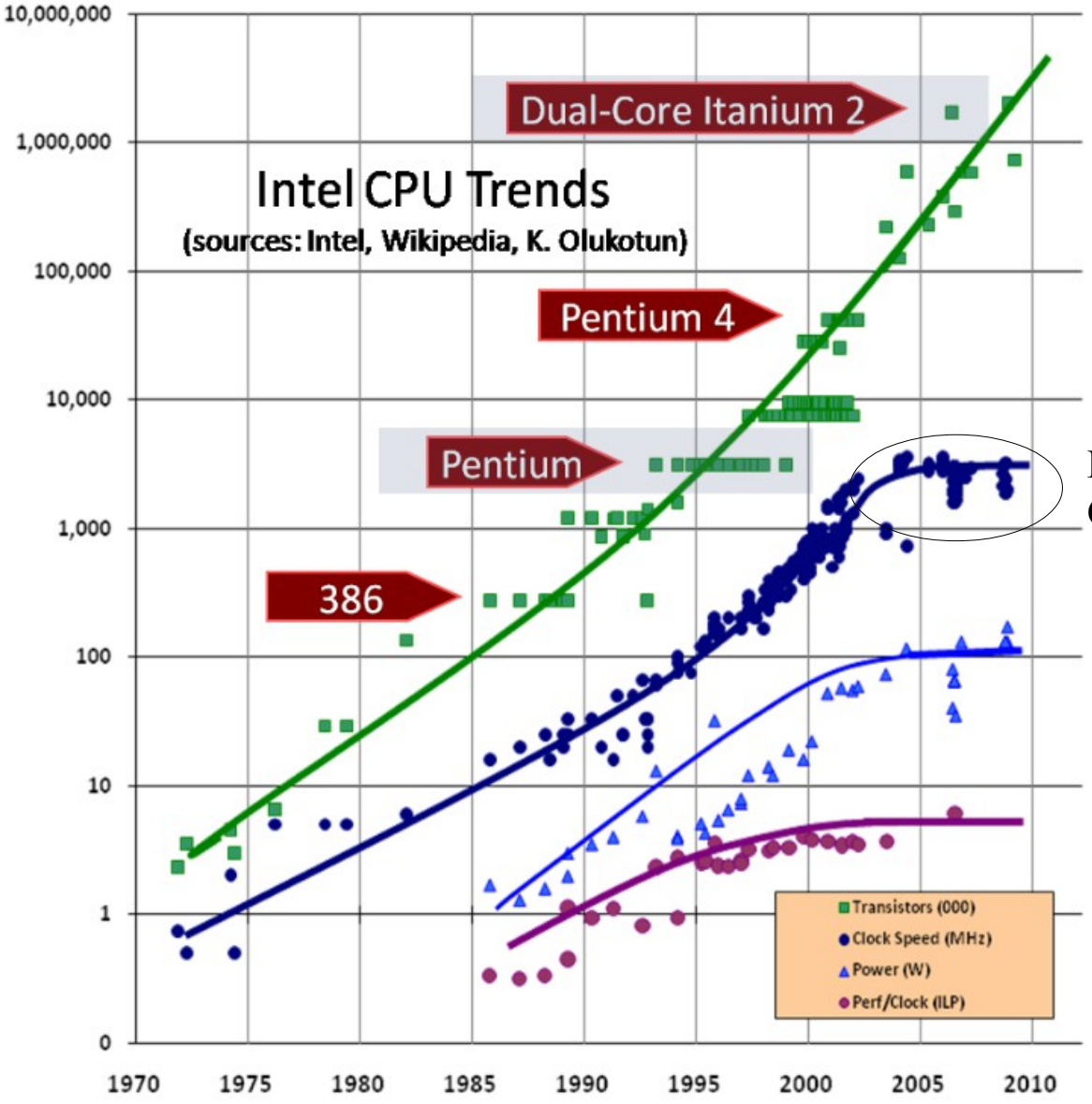


L1 – First level cache: fast and small

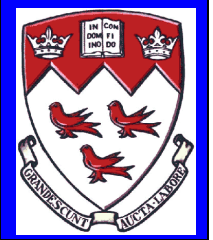
L2 – Second level cache: slower and bigger

L3 and then RAM

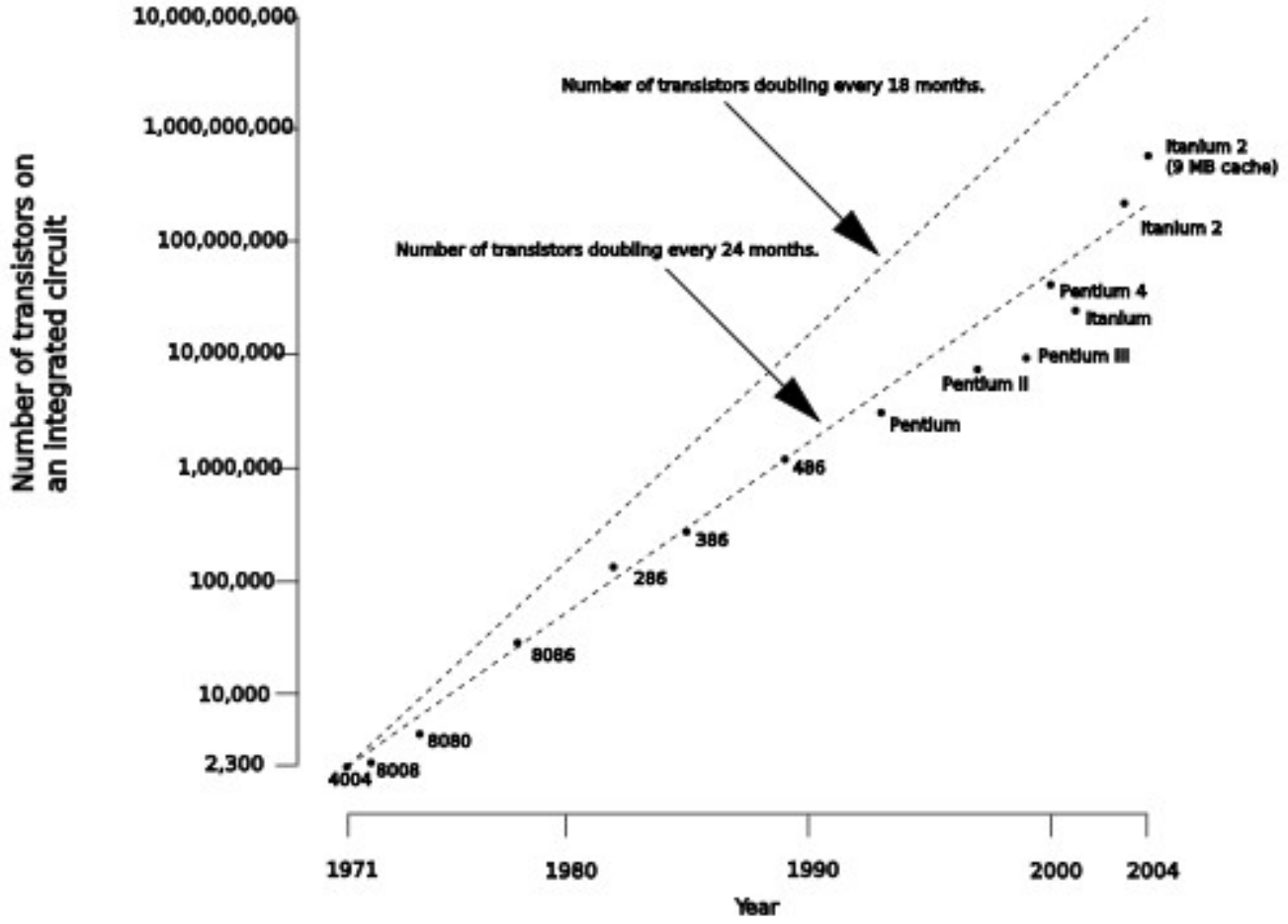
Intel Chip Performance




CPU Die



Moore's Law


Number of transistors on an integrated circuit
10,000,000,000
1,000,000,000
100,000,000
10,000,000
1,000,000
100,000
10,000
2,300
Number of transistors doubling every 18 months.
Number of transistors doubling every 24 months.
Itanium 2 (9 MB cache)
Itanium 2
Pentium 4
Itanium
Pentium III
Pentium II
Pentium
486
386
286
8086
8080
8008
4004
1971
1980
1990
2000
2004
Year

Multi-core problem

- Parallel processing requires communication
- More things in parallel the more communication is needed
- Eventually performance is lost due to the communication
- If your problem does not need communication then the cores can go full speed.

A multi-core solution

- Solution
  - Core 1 dedicated to OS
  - Core 2 dedicated to all your programs
    - Your programs run in a queue
    - At each quanta it switches programs