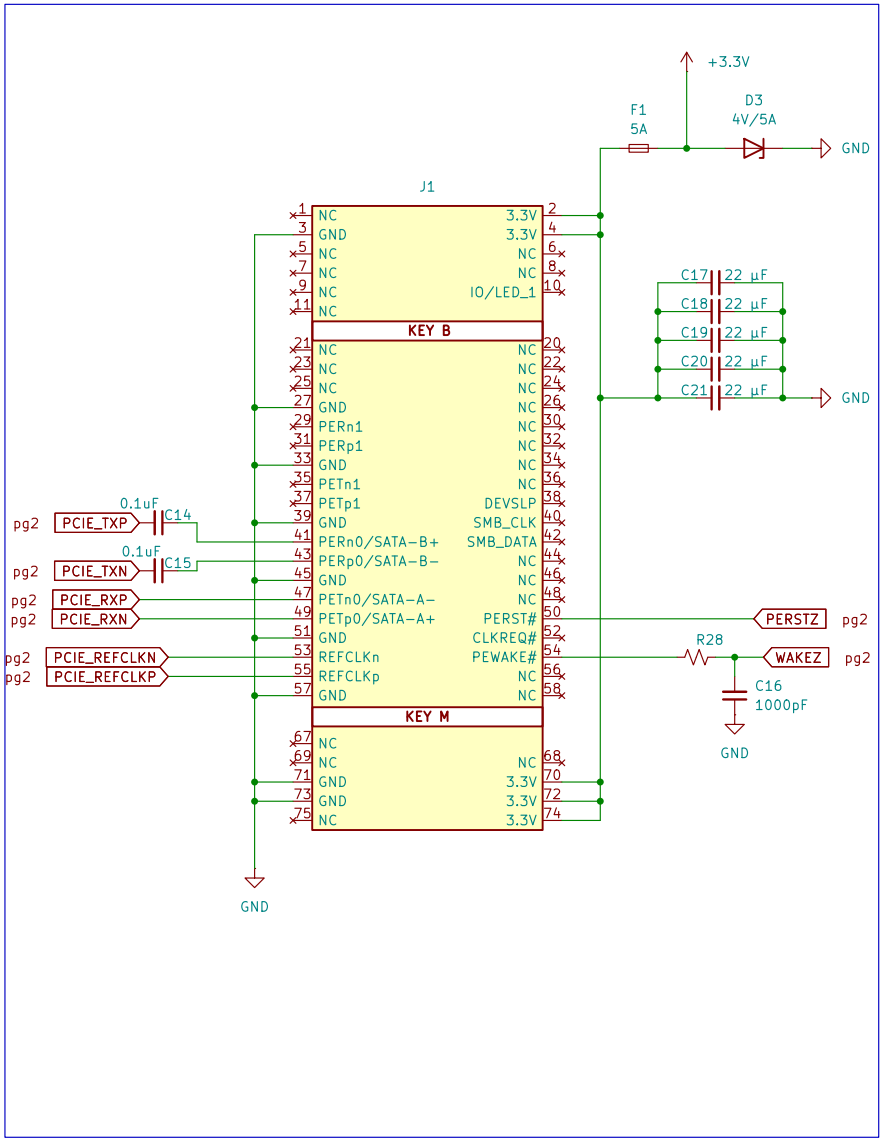
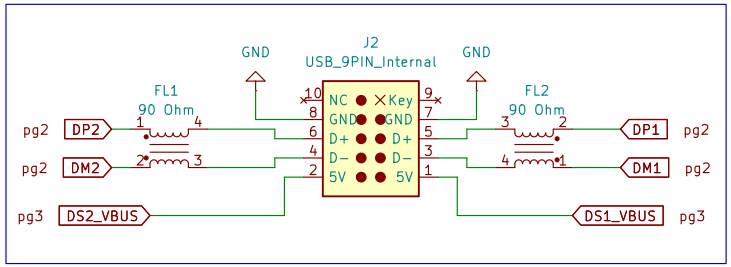
## PCIe
## M2 Key M+B




## DOWNSTREAM
## PORT1 / PORT2




### VIA AND TRACE REQUIREMENTS:

- MIN VIA PAD SIZE 20mils
- MIN spacing between trace and pad is 5mils
- MIN spacing between VIA and pad is 5mils
- MIN width of trace is 4mils

### IMPEDANCE REQUIREMENTS:

- USB_DP/M must be 90-ohm differential (+/-15%)
- PCIE_TXP/N must be 100-ohms differential (+/-10%)
- PCIE_RXP/N must be 100-ohms differential (+/-10%)
- PCIE_REFCLKP/N must be 100-ohms differential (+/-10%)

### LENGTH MATCHING REQUIREMENTS:

- USB_DP/M within 25mils
- PCIE_TXP/N within 5mils
- PCIE_RXP/N within 5mils
- PCIE_REFCLKP/N within 25mils

Initial Connectors
Based on:
https://wiki.congatec.com/wiki/M.2_Pinout_Descriptions_and_Reference_Designs_(AN43)
https://www.ti.com/lit/ug/sllu146d/sllu146d.pdf

**3mdeb Sp. z o.o  Jakub Sobota**

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***Title: PCI2USB***

| Size: A4 | Date: 2025-11-17 | **Rev: 1.0.0** |
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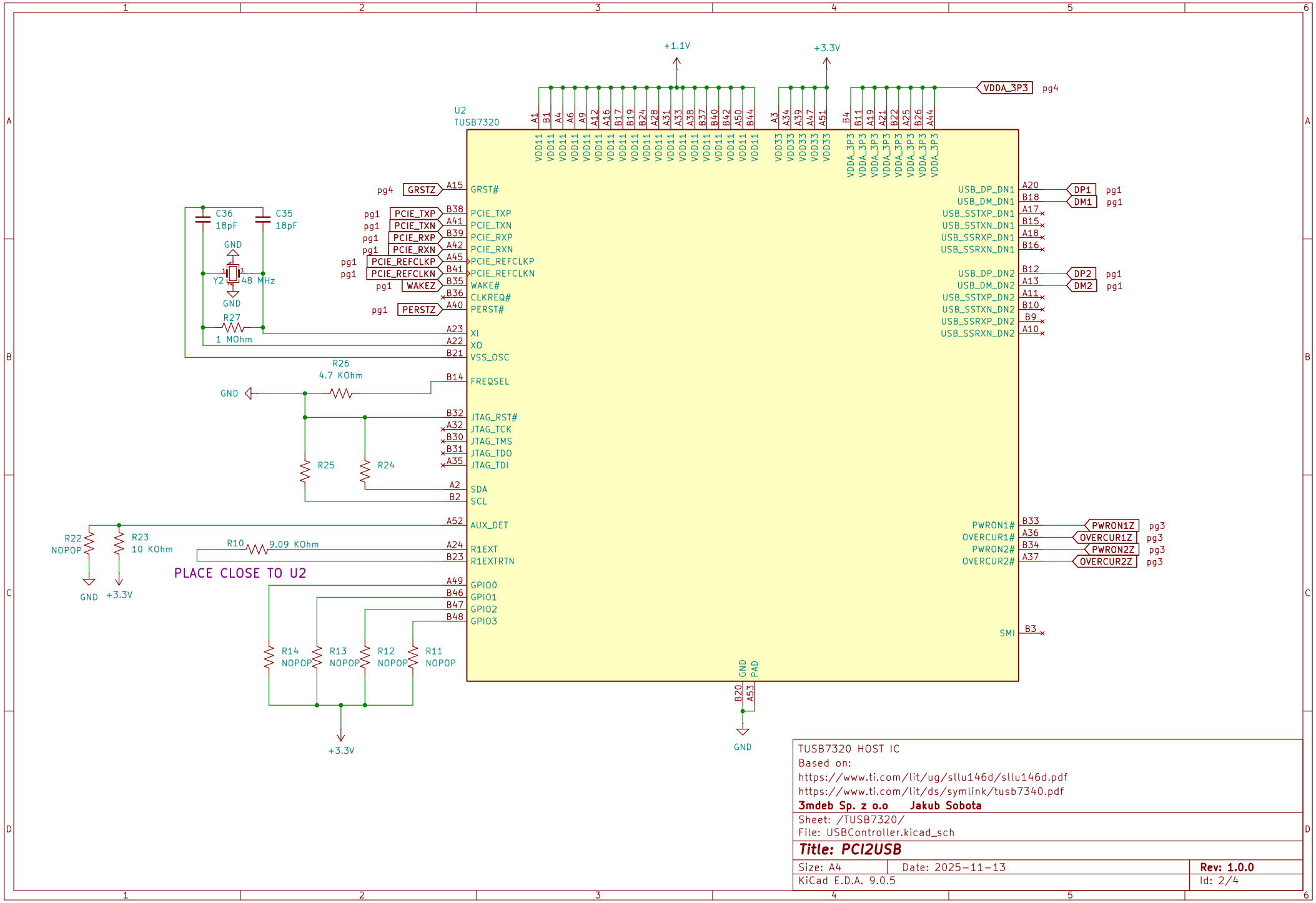
| KiCad E.D.A. 9.0.5 | | Id: 1/4 |




TUSB7320 HOST IC
Based on:
https://www.ti.com/lit/ug/sllu146d/sllu146d.pdf
https://www.ti.com/lit/ds/symlink/tusb7340.pdf
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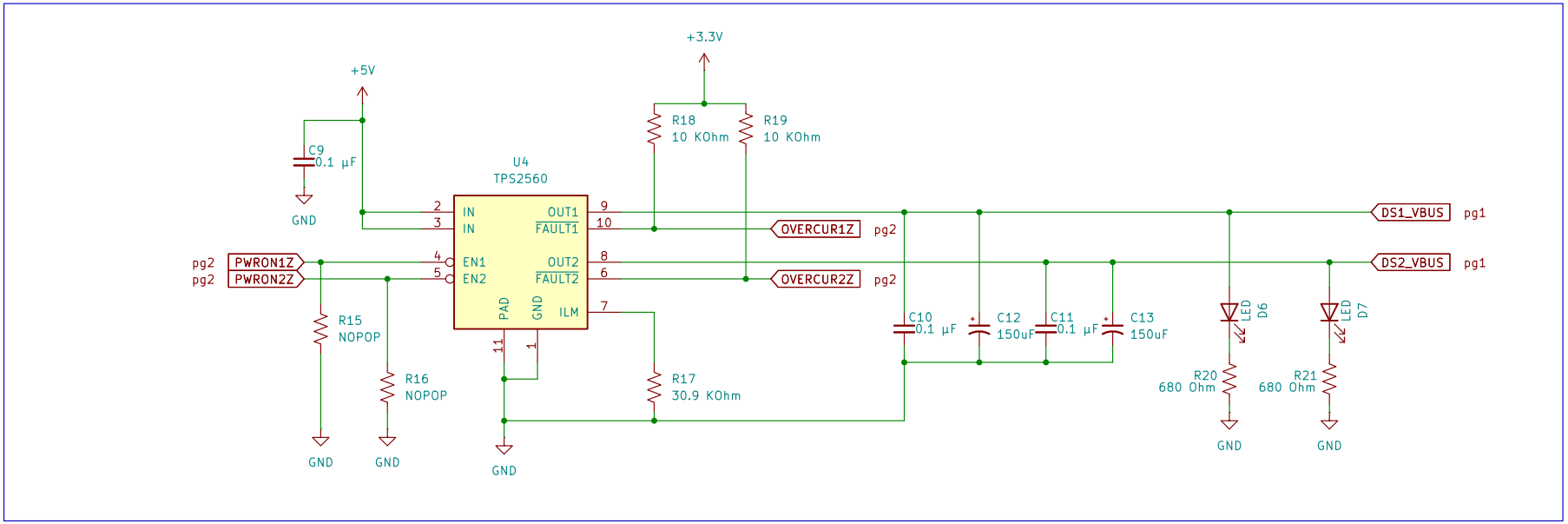
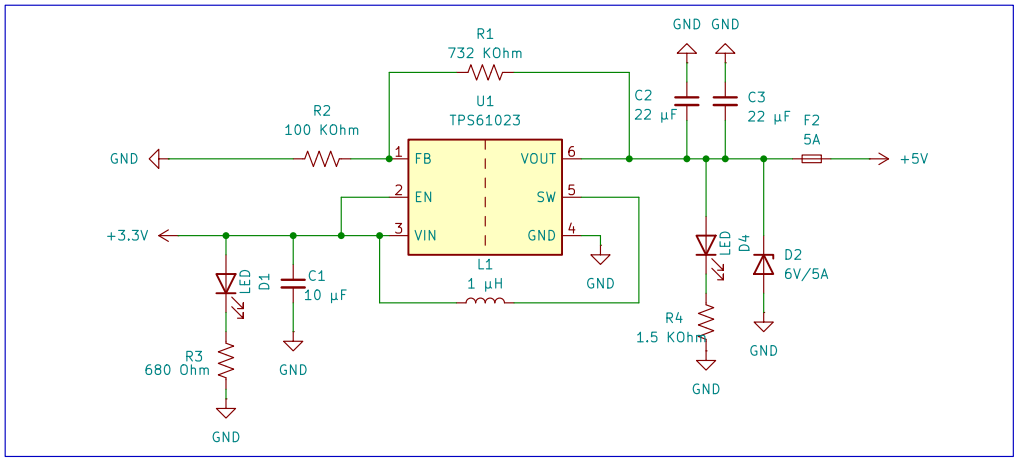
***Title: PCI2USB***

| Size: A4 | Date: 2025-11-13 | **Rev: 1.0.0** |
|---|---|---|
| KiCad E.D.A. 9.0.5 | | Id: 2/4 |

## DOWNSTREAM POWER SWITCH




## 5V REGULATOR




USB Power
Based on:
https://www.ti.com/lit/ug/sllu146d/sllu146d.pdf
https://www.ti.com/lit/ds/symlink/tps61023.pdf
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***Title: PCI2USB***

| Size: A4 | Date: 2025-10-13 | **Rev: 1.0.0** |
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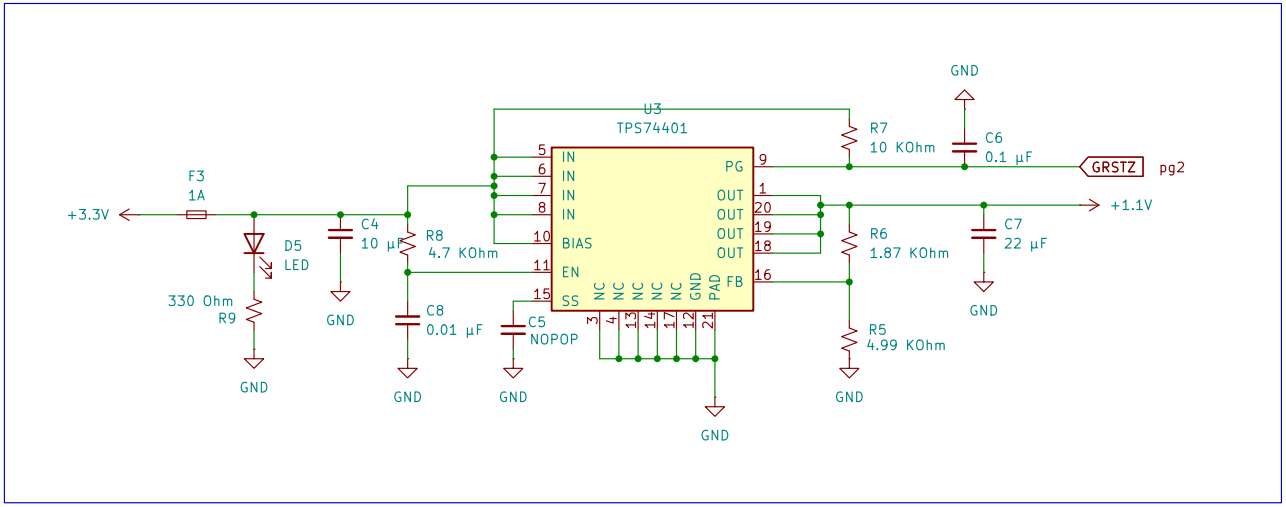
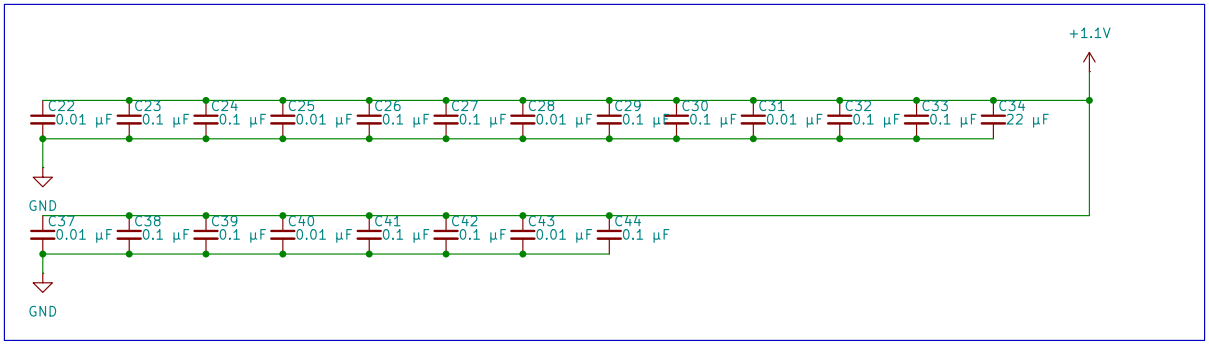
| KiCad E.D.A. 9.0.5 | | Id: 3/4 |

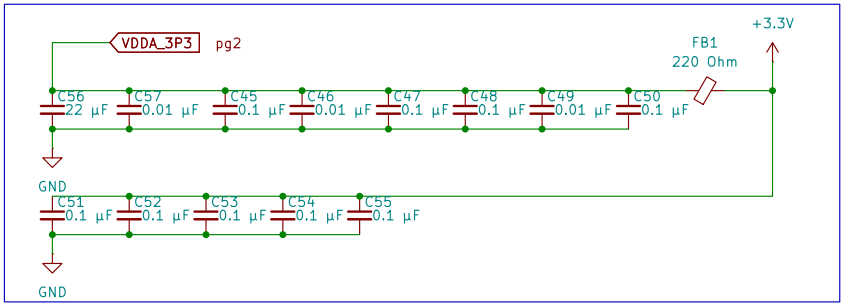
## 1.1V REGULATOR




## 1.1V LINE CAPACITORS




## 3.3V LINE CAPACITORS




1.1V Regulator
Based on:
https://www.ti.com/lit/ug/sllu146d/sllu146d.pdf
https://www.ti.com/lit/ds/symlink/tps74401.pdf
**3mdeb Sp. z o.o  Jakub Sobota**

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***Title: PCI2USB***

| Size: A4 | Date: 2025-10-29 | **Rev: 1.0.0** |
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| KiCad E.D.A. 9.0.5 | | Id: 4/4 |