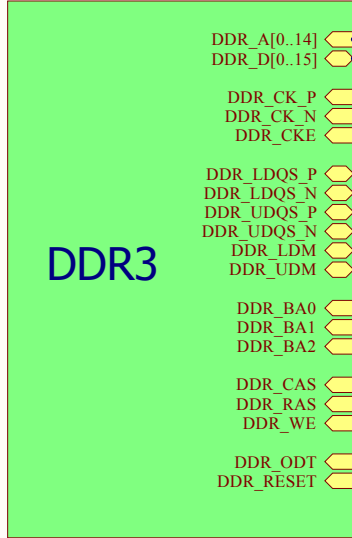
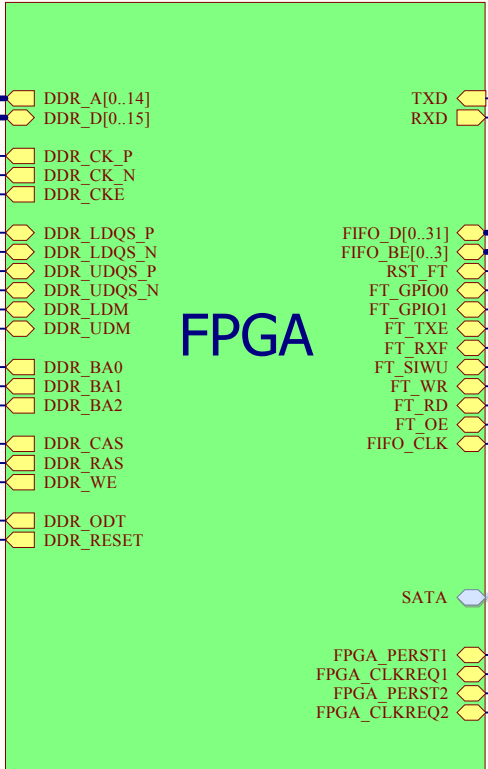


DDR3.SchDoc



FPGA.SchDoc



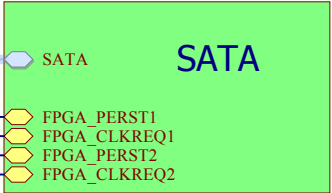
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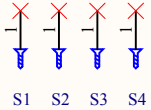
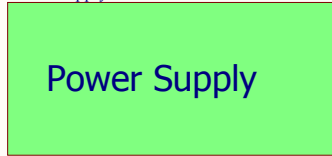
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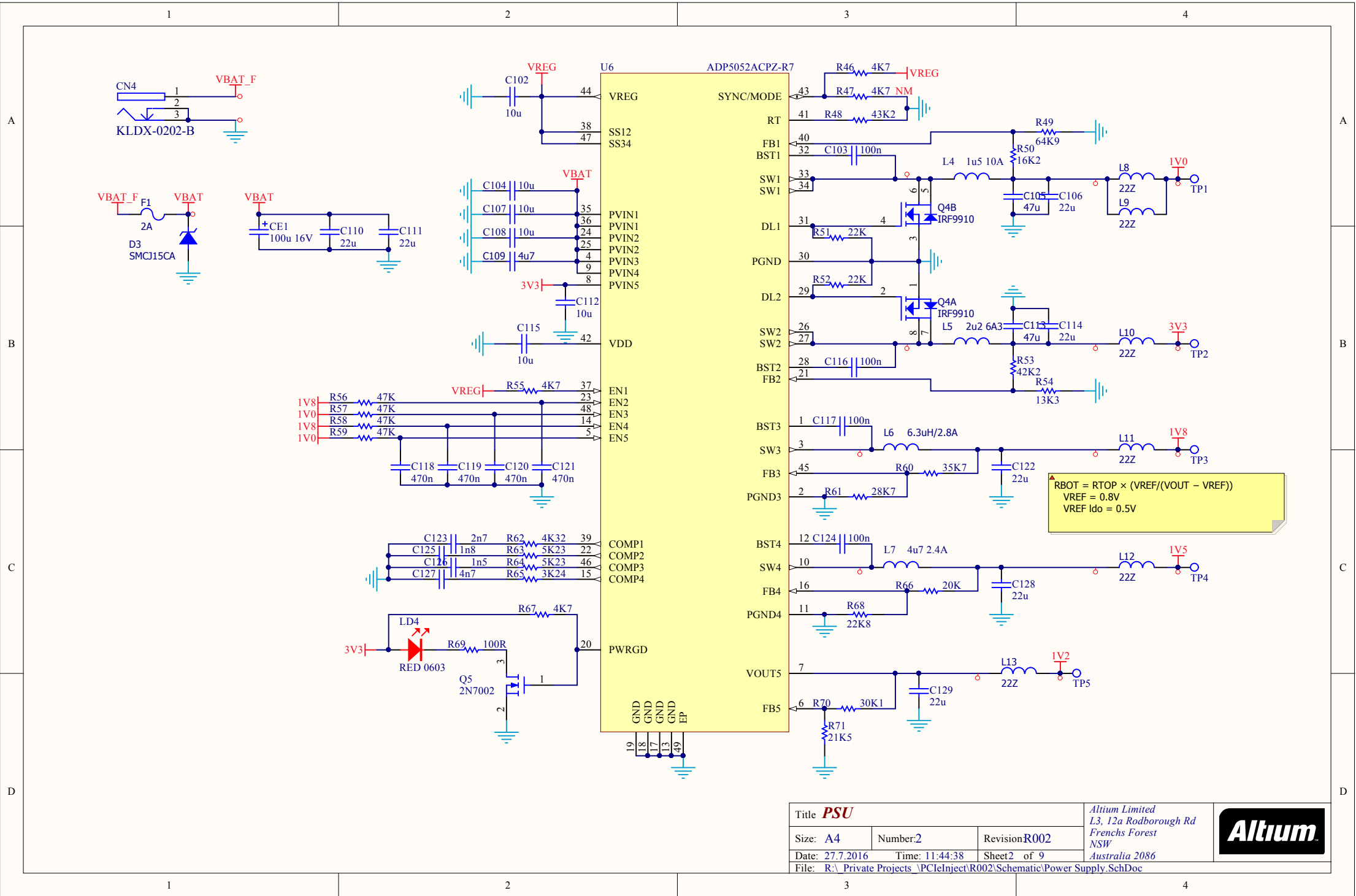
SATA.SchDoc



Power Supply.SchDoc



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Size: A4	Number:1	Revision R002		
Date: 27.7.2016	Time: 11:44:38	Sheet 1 of 9		
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Title **PSU**

Size: **A4**

Number: **2**

Revision: **R002**

Date: **27.7.2016**

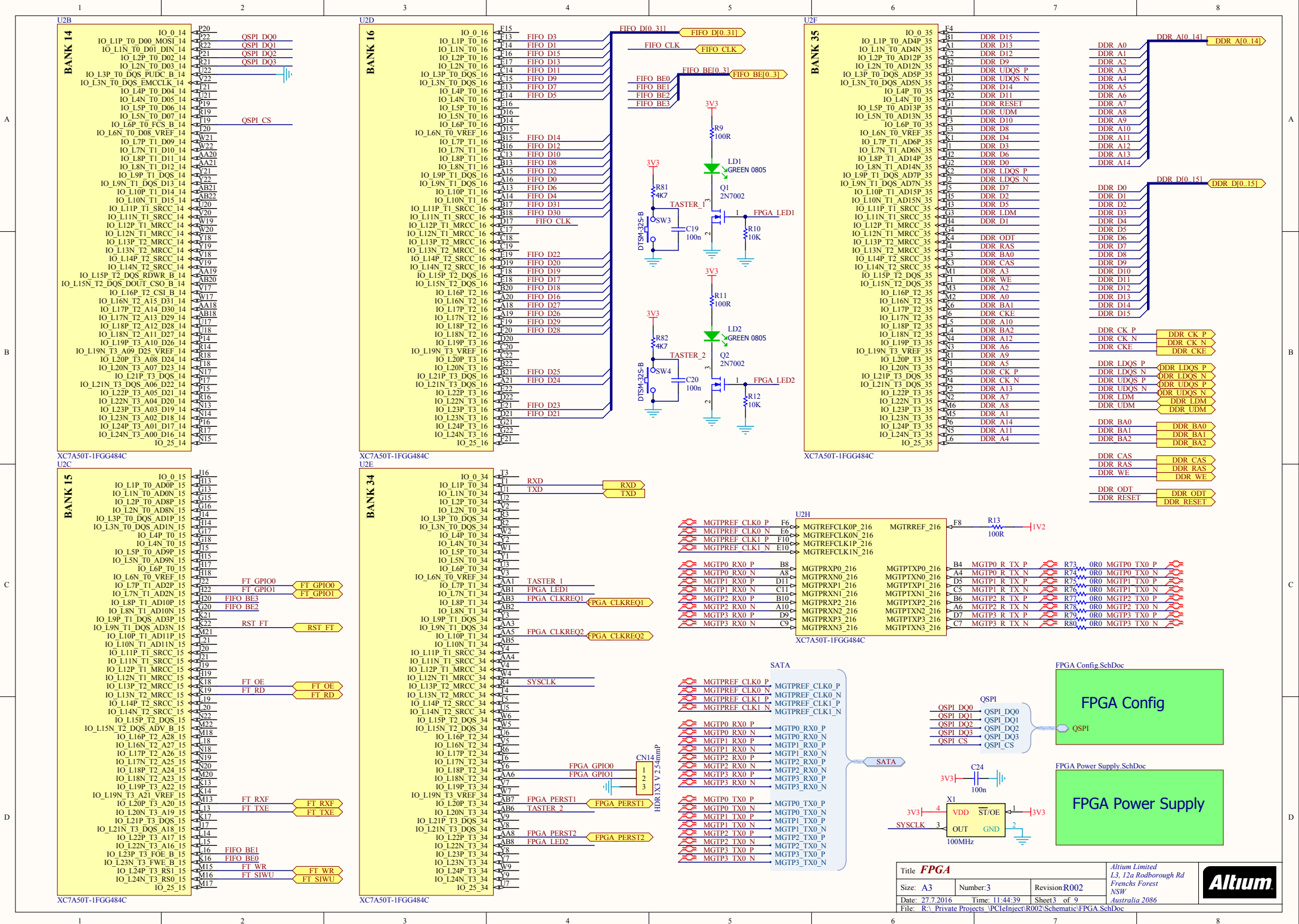
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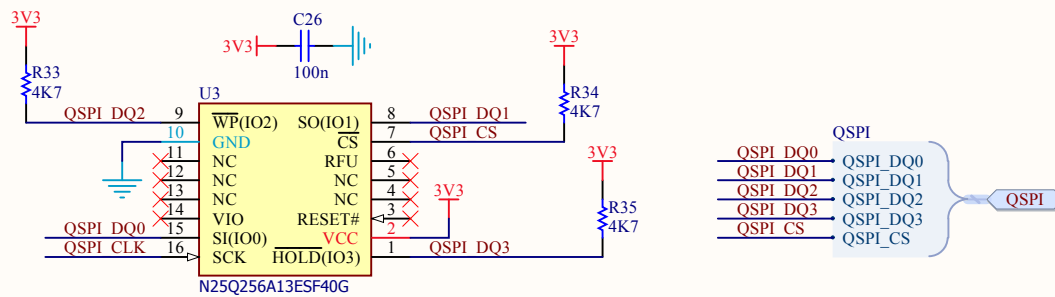
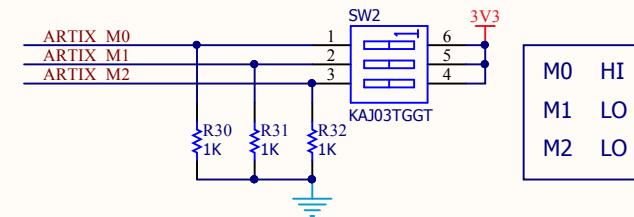
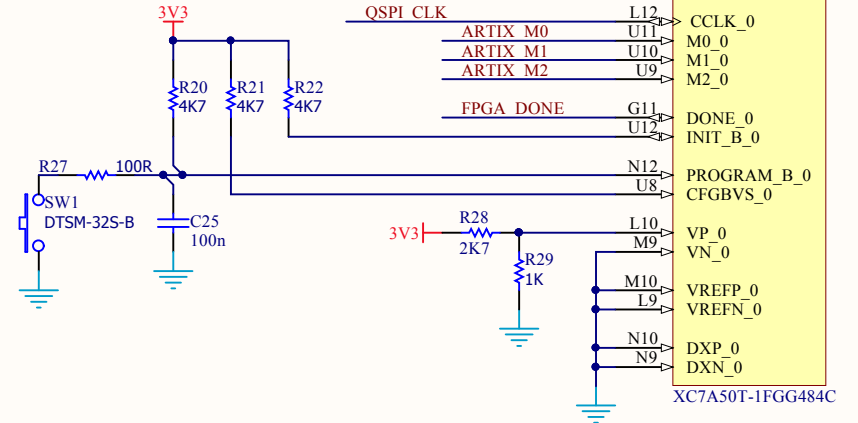
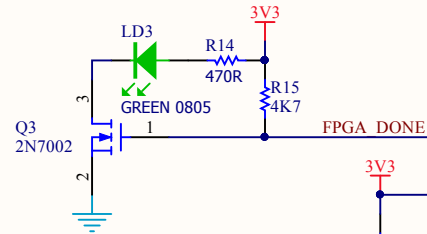
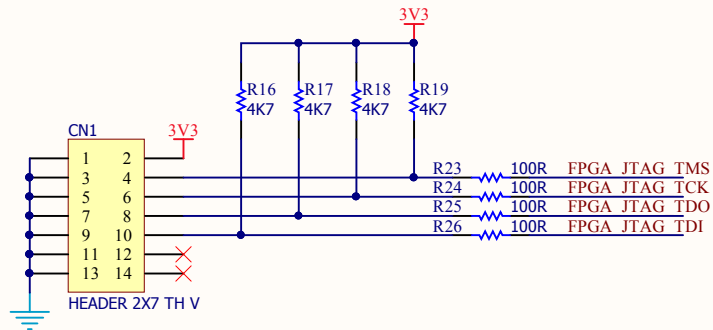
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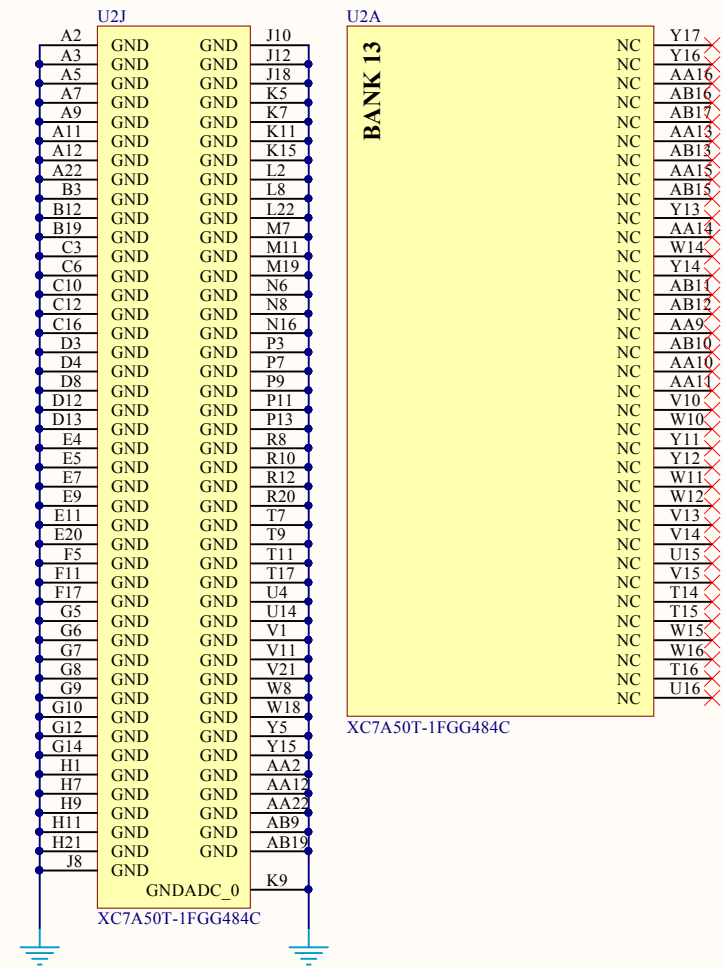
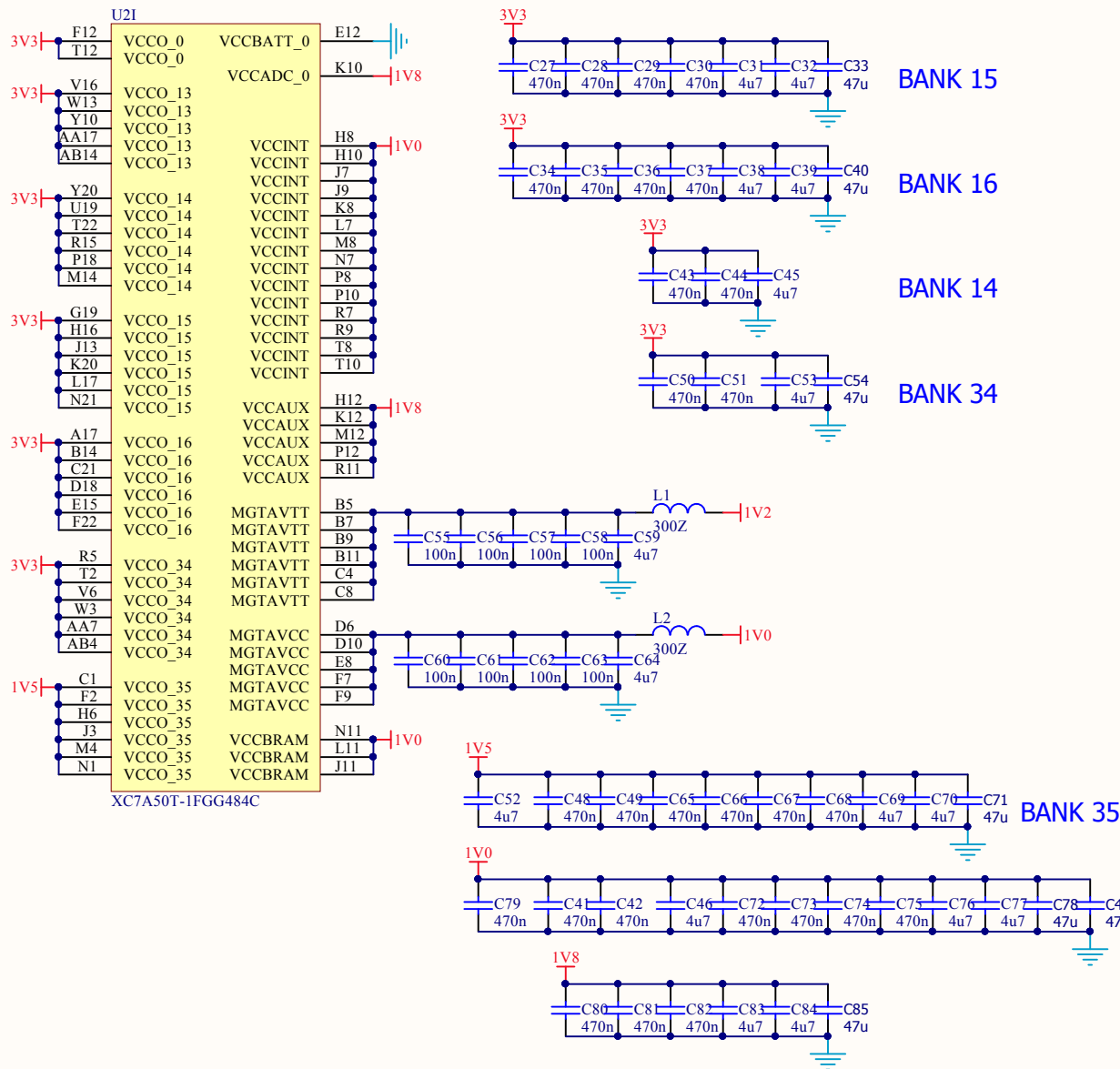
Altium Limited
L3, 12a Rodborough Rd
Frenchs Forest
NSW
Australia 2086

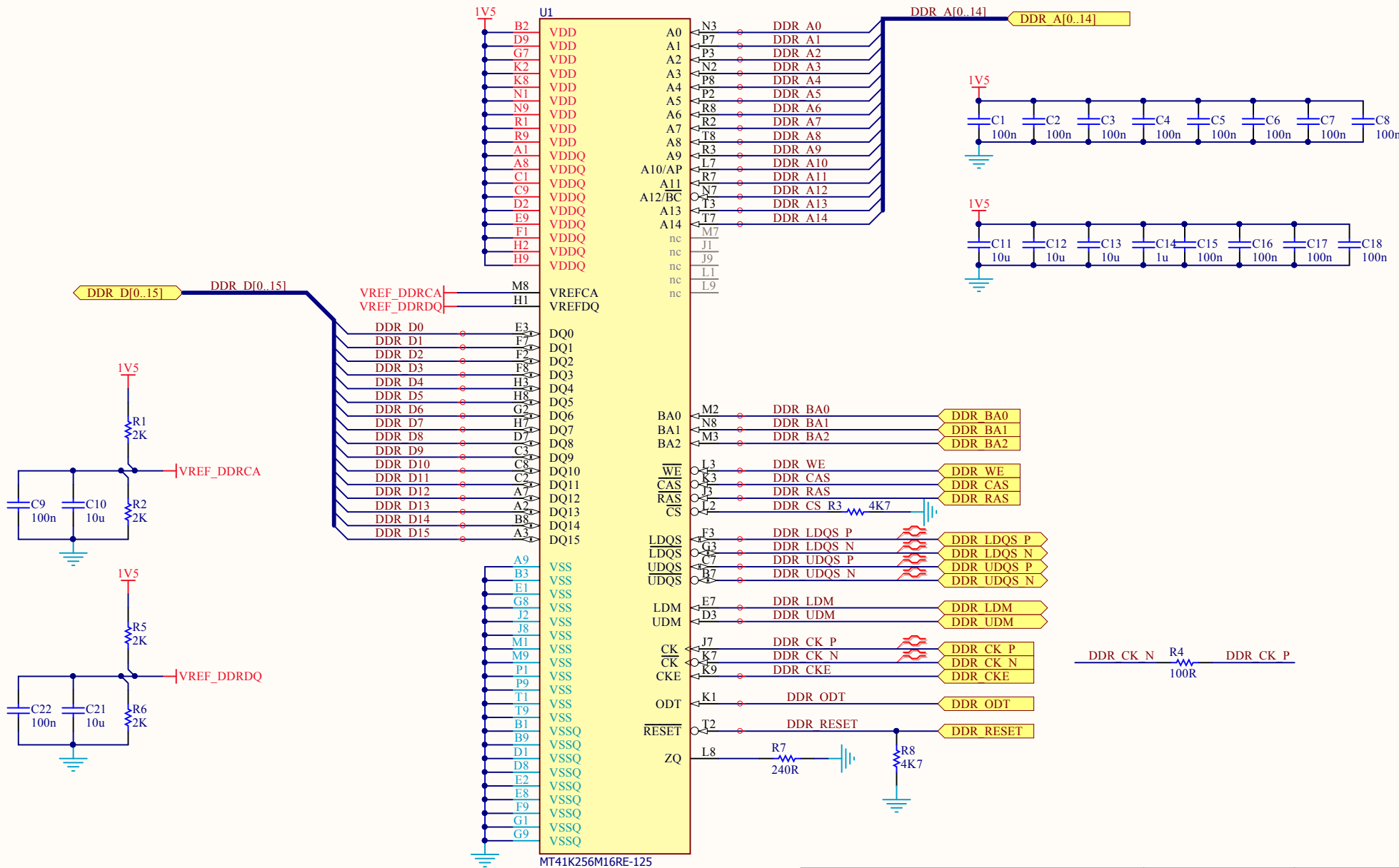
Altium






Title FPGA - Config			Altium Limited L3, 12a Rodborough Rd Frenchs Forest NSW Australia 2086	
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Title DDR3			Altium Limited L3, 12a Rodborough Rd Frenchs Forest NSW Australia 2086	
Size: A4	Number: 6	Revision R002		
Date: 27.7.2016	Time: 11:44:39	Sheet 6 of 9		
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