Better PCBs in Eagle

Skill Level: Intermediate

by Nate | November 06, 2008 | *41 comments*

Designing a Better PCB:

We are constantly pushing ourselves for better printed circuit boards (PCB). One thing we've learned is that PCB fab houses (such as Advanced Circuits, BatchPCB, PCB123, Gold Phoenix, Bare Bones PCB, anyone really) have a very hard job to do. Creating a PCB is not an easy task and there are many ways for a fab house to mess it up. Unfortunately, fab houses tend to spend less time on prototypes than on production runs. Therefore, we try to design products and PCBs for 'manufacturability'. This tutorial will show you how to minimize the number of ways the fab house can screw up a PCB.

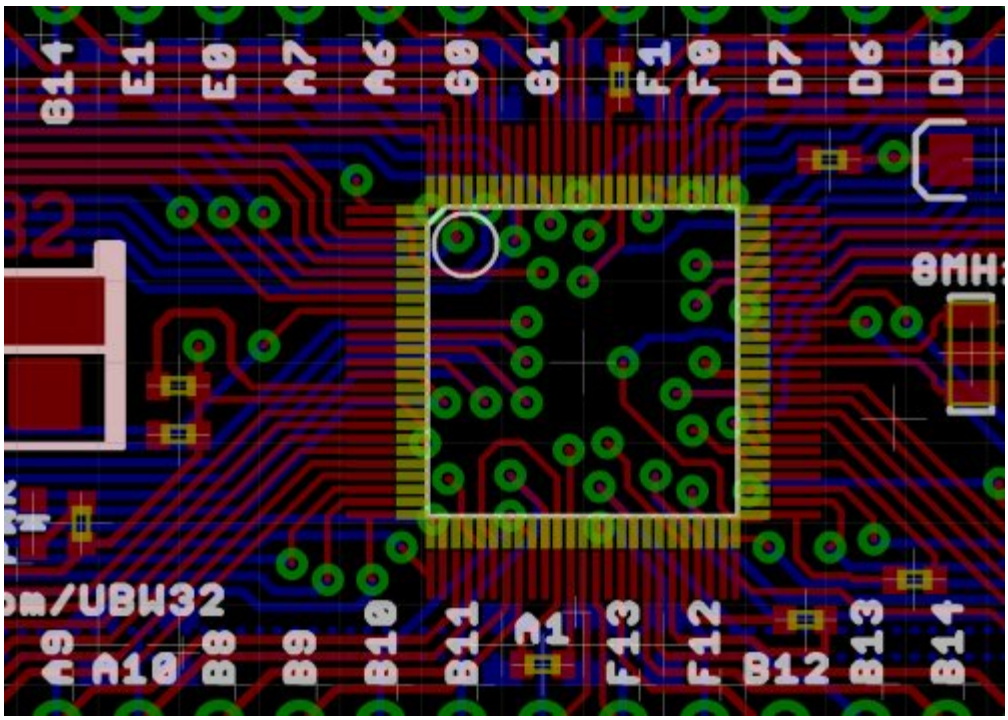
We've messed up piles of PCBs over the years. We want to share with you some of the DFM (design for manufacture) rules and tricks and tips we've learned to get a good PCB, every time. If you're creating a prototype PCB, we highly recommend you use these rules to increase the chances that your proto will work!

Important Files:

- SparkFun Eagle Rules for designing PCBs in Eagle. This is a list of rules that we have forged over the years. You are welcome to use or dismiss them. Some only apply directly to the engineers here at SparkFun, most of the rules apply to everyone.
- SparkFun DRC file for Eagle. Right click on the link, select 'Save Link As' and save this file to your Eagle/dru directory.
- SparkFun CAM file for Eagle. Right click on the link, select 'Save Link As' and save this file to your Eagle/cam directory.

Trace Width and Spacing:

Just because a fab house can handle down to 5mil traces and 6mil space doesn't mean you should design with those sizes. If your board can be routed with 10mil traces and 10mil spaces, do it! The smaller you make things, the more likely you will get a PCB with broken trace (traces less than 10mil) or two traces touching each other (less than 10mil spacing between traces).

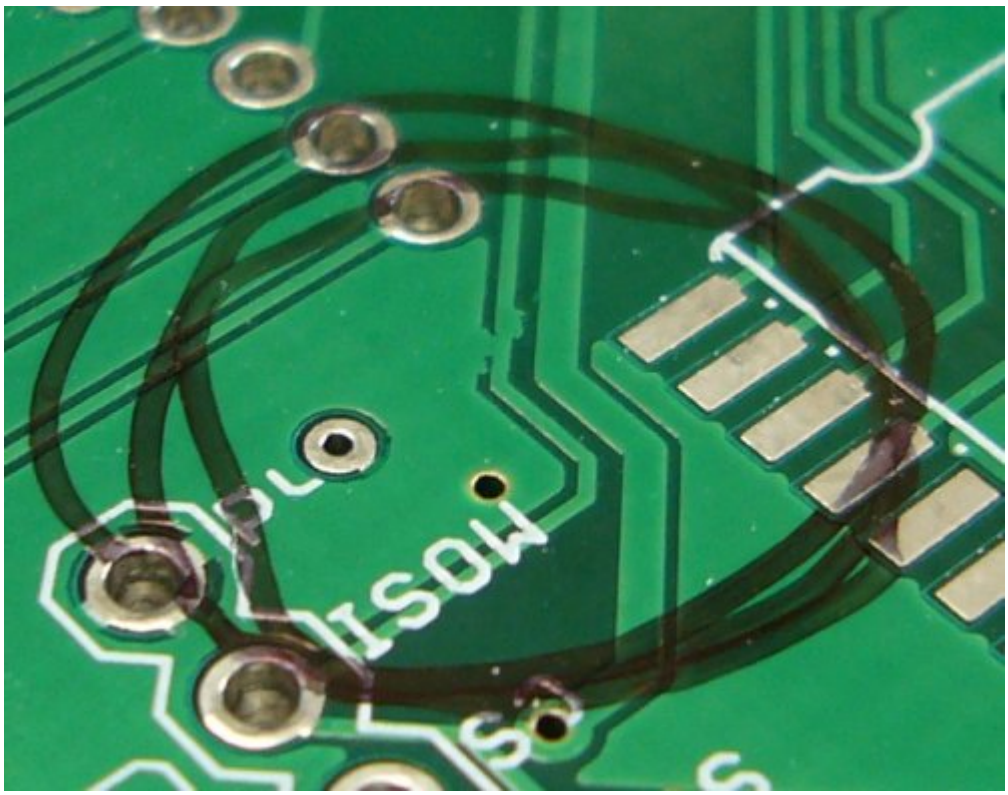


PIC32 development board

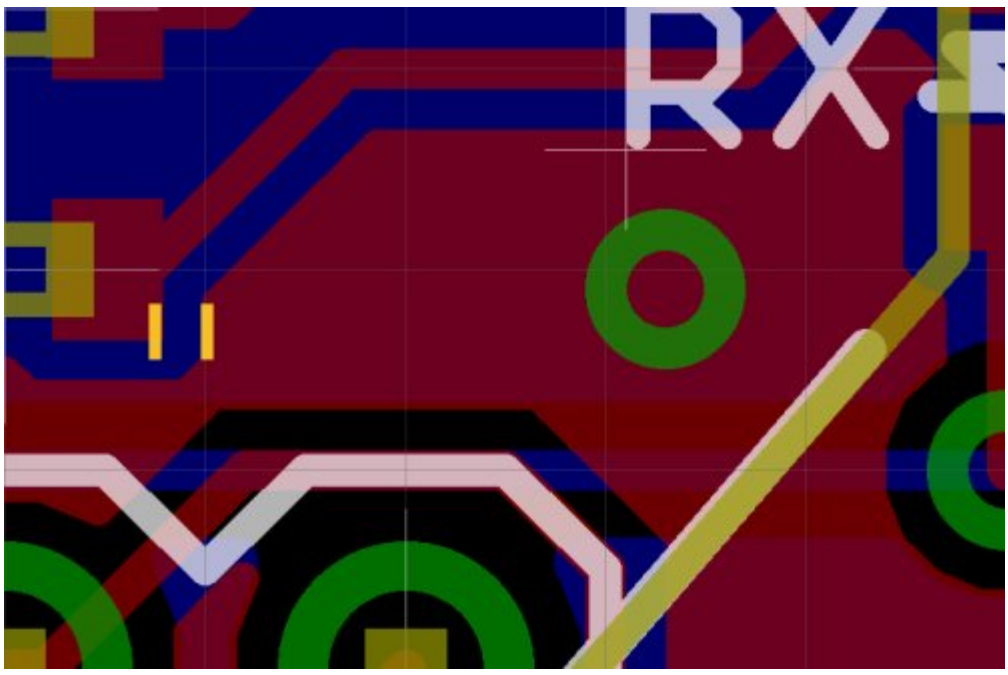
Even complex boards with tight pitch packages and a horrible rat's nest of traces can be routed with 10mil traces and 8mil spacing. Next time you route a board, try it with 10mil traces and see just how far you can go – you'll be suprised. If things get really tough, 8mil is usually ok. The goal of all these tricks and rules is the limit the spots where manufacturing failures could occur.

Isolate:

A ground (or power) plane is a good idea on some projects. But a plane (sometimes called a polygon plane) increases the odds of the plane being mistakenly 'poured' onto a trace.

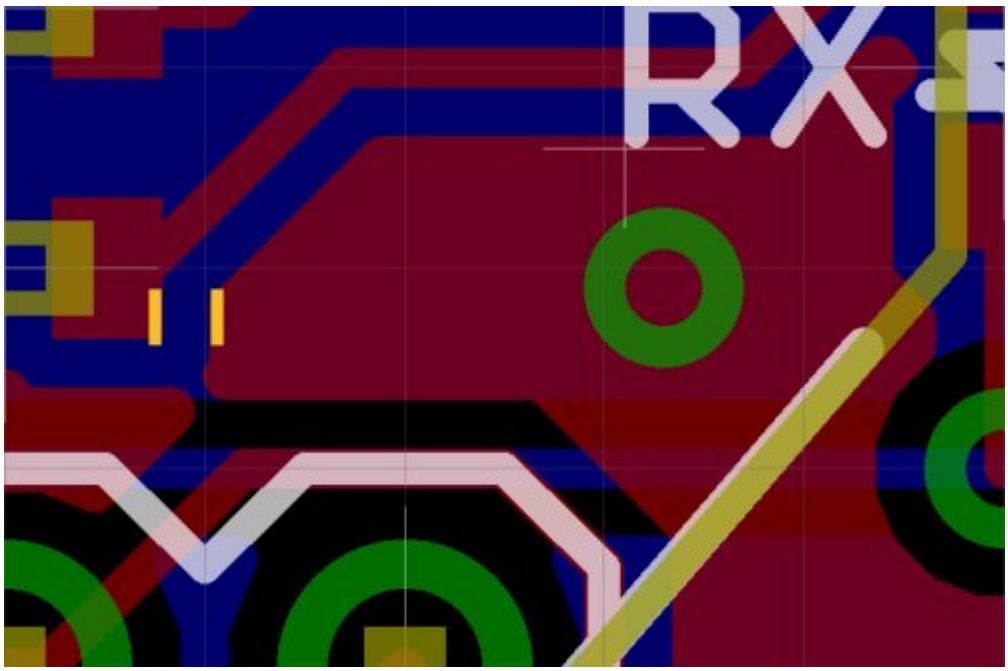


What the?! Bad ground pour. Bad!



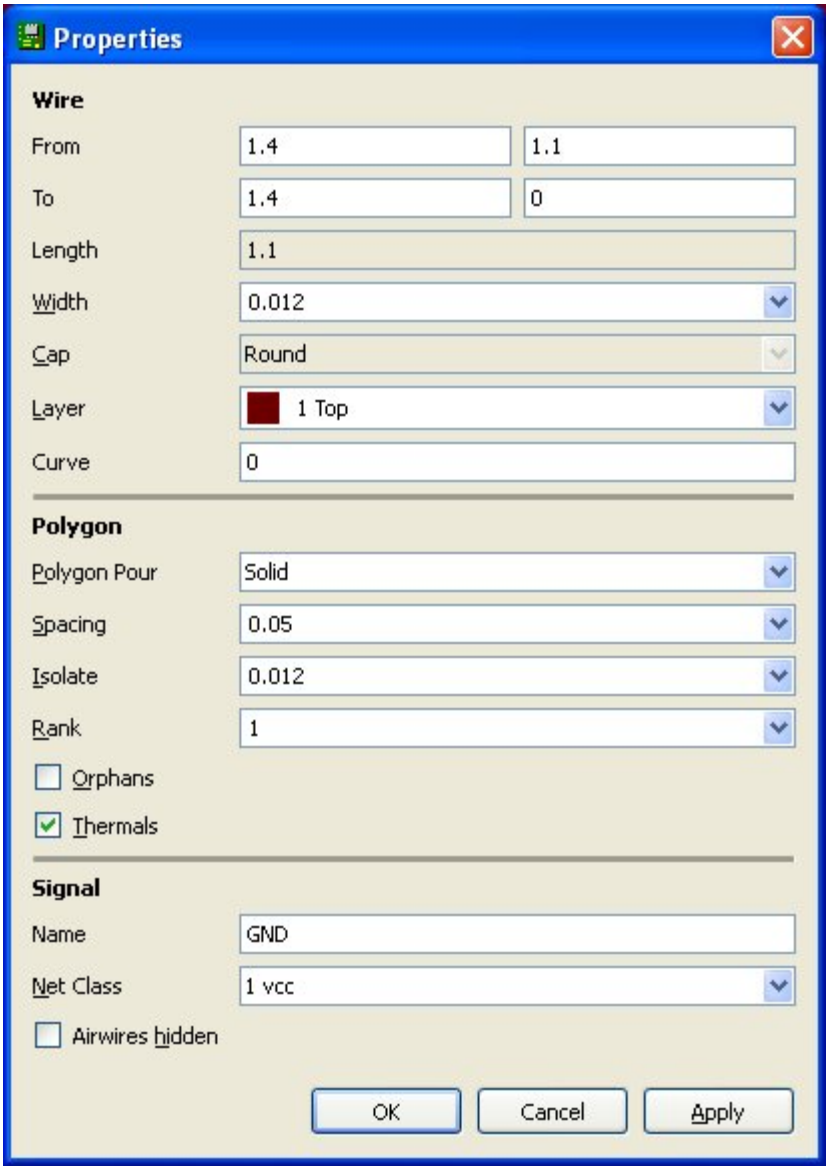
A simple board with 10mil isolation

We recommend you increase the default 10mil isolation in Eagle of a polygon pour to '0.012' or 12mil. This will pull the plane away from the signal traces, thus decreasing the odds of a manufacturing failure. This will however potentially break ground connections so be sure to check your rats nest!



Increased isolation good, ground plane break may be bad.

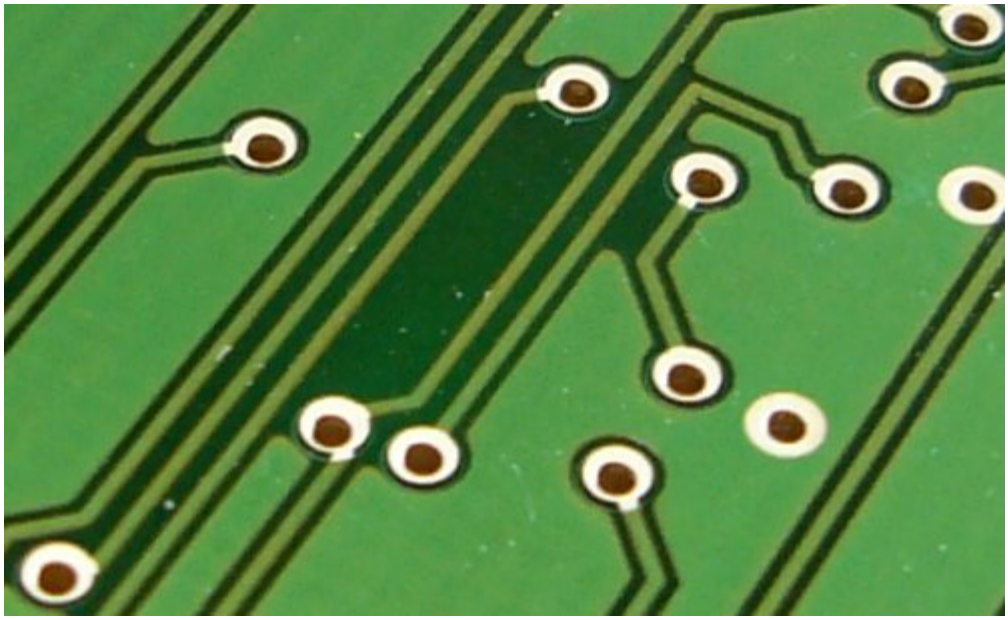
To increase the isolation on an existing polygon, click on the 'i' button for information, then click on the border of the polygon.



Then change the Isolate from a default of 0.010 to 0.012.

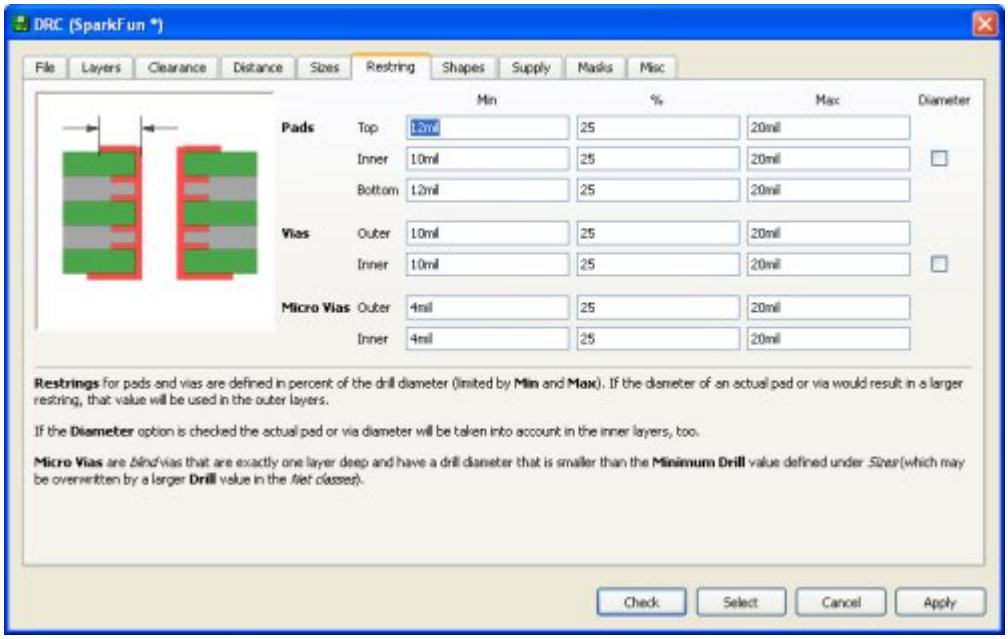
Annular Ring:

Another problem that we have found is sloppy drill hits by a fab house. To connect a trace from one side of the PCB to the other, we use a via. A via is composed of a drilled hole, two circles of copper larger than the hole on either side of the board, and connecting copper inside the hole to connect the circles on either side of the board (these are called plated through holes). Vias make PCBs work. The problem is the size of the copper circles. If the drill hit is not in the middle of the circles, the drill hole can potentially break the via and the trace connected to the via.



Sloppy drill hits in the center of the vias

All of the vias shown above work, but they are marginal. This is one board out of a run of many and the other boards could be even worse. If the drill hit is too far off center, it can cut through the trace connecting to the via. To help protect against this, we increase the size of the annular ring around the vias. To do this, we edit the Eagle DRC rules (click on menu Tools->DRC).



Restring tab of the Eagle DRC rules

Click on the tab labeled 'Restring'. The default for pads on the top and bottom is 10mil. We change this to 12 mil to increase the annular rings by 20%. This will increase the chances that our prototype PCB will work. This DRC setting is set to 12mil in the SparkFun DRC file.

Gerber File Generation:

Generating good gerber files of your PCB is the final step that causes

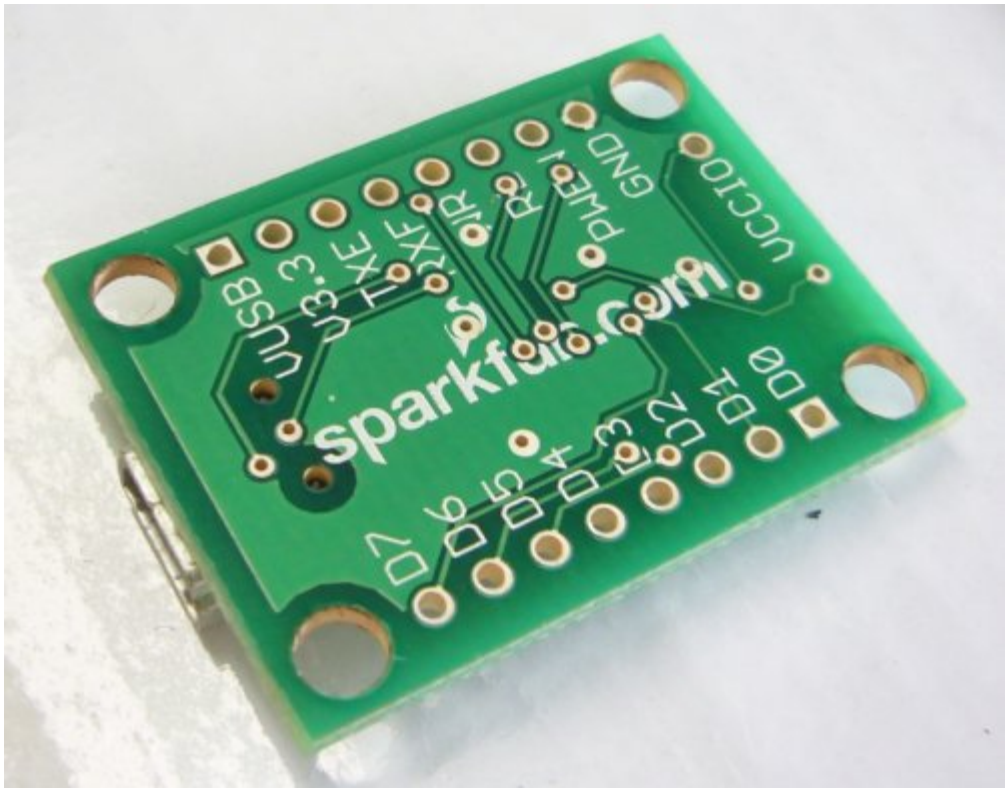
many people to fail. Eagle uses a CAM file to create the gerber files to have a PCB made. We have seen tons of people create horribly defective gerber files. Please start with our CAM file – and modify if you really need to. We've used this CAM file thousands of times without problems.

We've changed the default Eagle CAM file so that it *does not* mirror any of the bottom layers (number one problem with gerber submissions!), it outputs a standard Excellon drill file (second most common error is a missing drill file), and captures only the tPlace layer onto the silkscreen layer (this will cause all part identifiers and values to *not print* on the silkscreen). Put all text and labels onto the tPlace layer that you want to see printed on the board.

Tenting:

Tenting refers to

the soldermask and vias. The vias on a board may be left exposed or covered up by the soldermask. We've found that covering up the vias (or 'tenting' them) decreases the chances that the silkscreen labels will be broken and gives the overall board a much better look. Don't worry, you can still probe a tented via for voltage and continuity with a multimeter – the soldermask will break down when you insert the probe into the hole. However, it will be much more difficult to solder to a tented via.



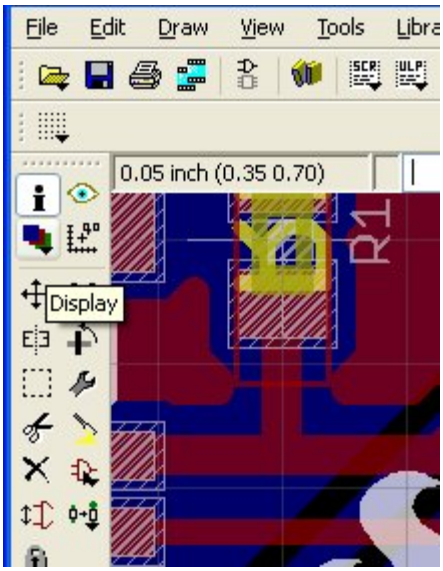
Untented vias. Ugly silkscreen. Small 10mil isolation on plane.

The bottom of the FT245RL breakout is shown above. The pin labels are completely un-readable because an untented via falls right in the middle of ‘WR’ and ’RE'. Is that ’RE'... I can’t remember.

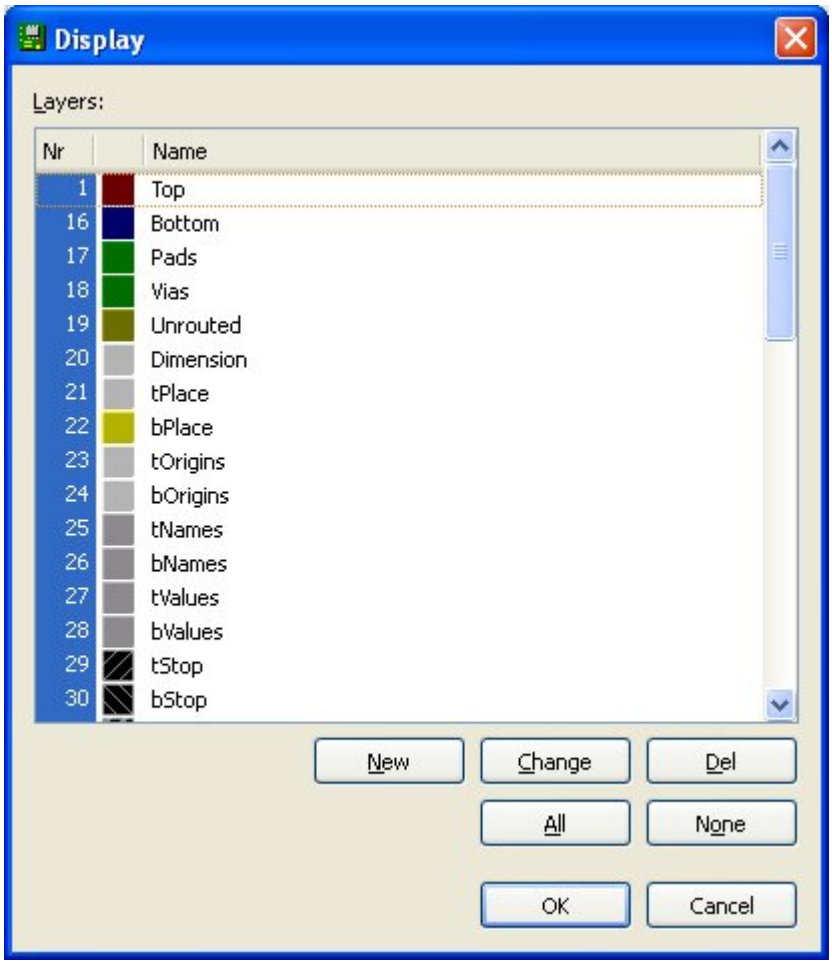
Tented vias. Happier silkscreen. 12mil isolation on polygon pour.

Bottom view of the XBee-Explorer product. I have been known to move a via to avoid a label as well, but that's just me.

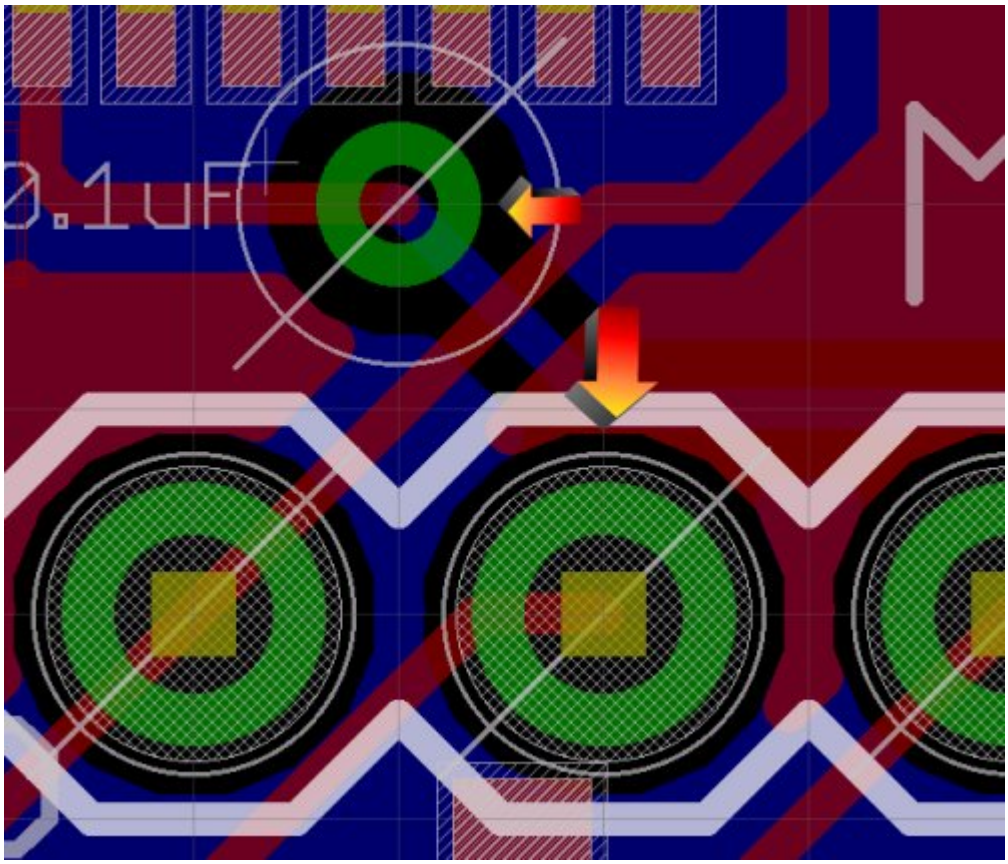
Tenting is taken care of in Eagle by modifying the DRC rules. To see if the vias will be tented or not, turn on all the layers by clicking on the display button:



The Display button is below the 'i' button.

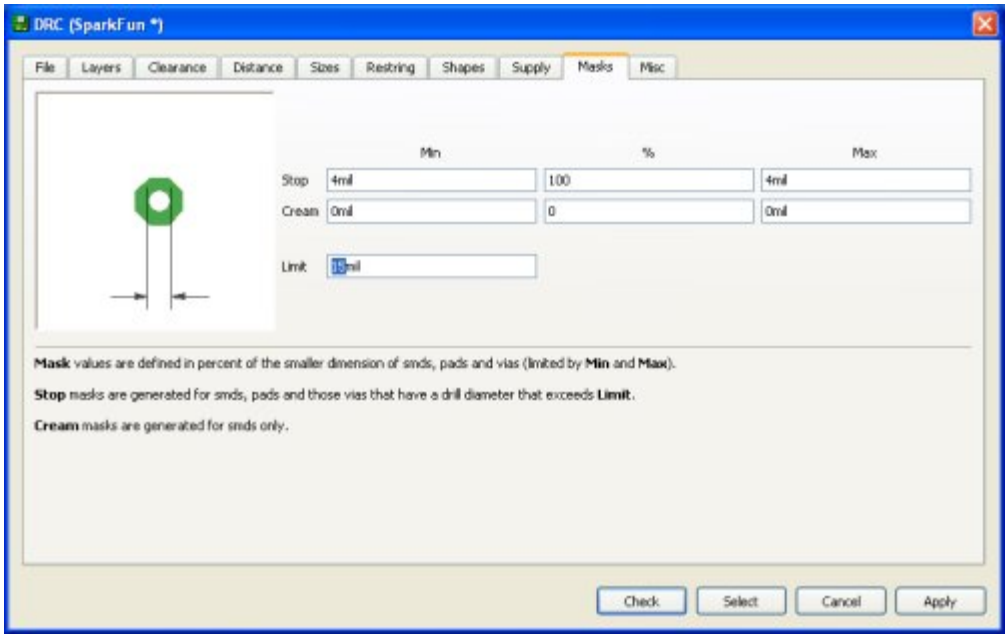


Click on ‘All’ then OK.



Turning on all the layers will create a lot of noise in the display of the board. What you are looking for is the white hatch marks indicating where the will be a *lack* of solder mask. The upper arrow points to a via that has no hatch marks, indicating there will be *no lack of soldermask* on that via (tenting it). The lower arrow points to a large hole with a white hatch mark on top of it. This is a solder point that needs to be exposed. The white hatch marks indicate there will be a *lack of solder mask* over this hole, exposing it so that we can solder to it.

To tent your vias, open the DRC rules on your current design (Tools->DRC menu).

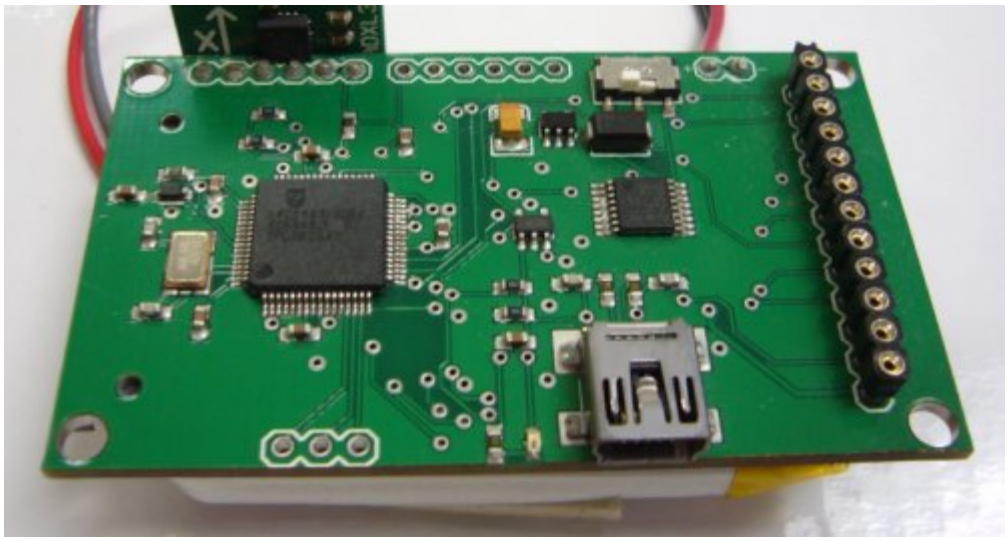


DRC Rules – Masks tab

Then increase the limit value to larger than the vias you are using. For instance, if the vias on your board are the default 0.023mil, then change the limit to 25mil and all drill hits under 25mil (0.025) will be covered in soldermask. Be careful! Don't set this number too high or you will cover important holes, like those meant to solder on connectors. The DRC setting is set to 25mil in the SparkFun DRC file.

Label everything, all the time:

This is another cosmetic issue I see so often it hurts. You should label every button, switch, LED, pin, and especially power connectors on your board. Every one of them!



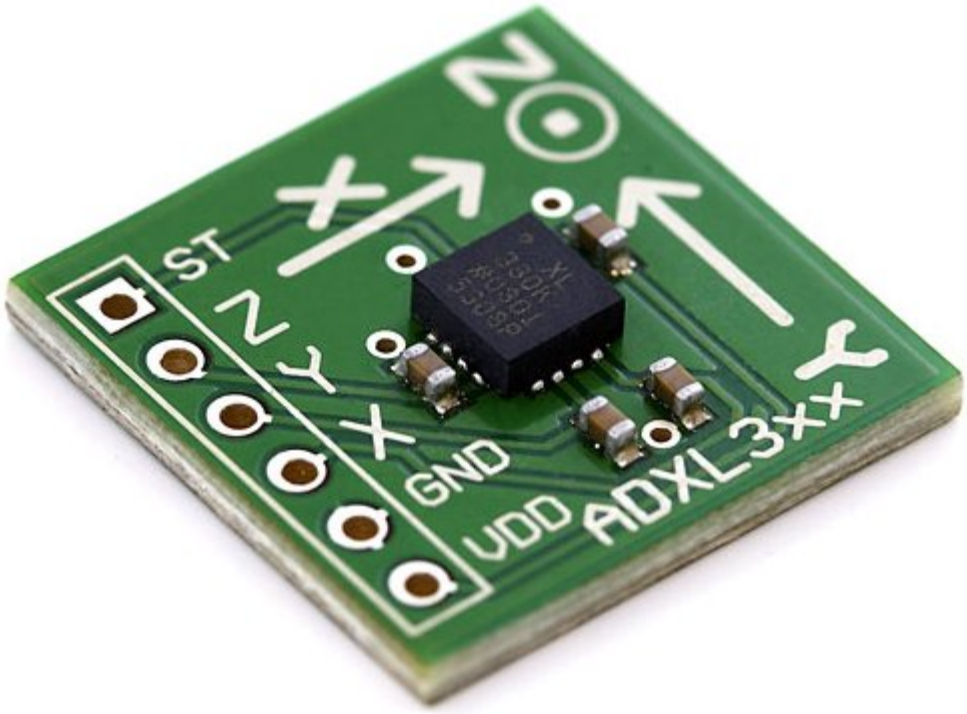
Labels! They are so easy, but so often overlooked.

1. What does the LED next to the USB connector mean? Is it a power LED? Or a status LED?
2. There's a slide switch, next to the power connector in the upper right corner. Is it a power switch? If so, which way is on?
3. There's lots of pins on this board – none of which are labeled. Why not? Silkscreen is free!
4. The one good thing about this board is the small, but apparent '+' and '–' where the battery connects. This is good! But an acceptable voltage range would have been helpful. '3-7V' or some such indicator is extremely useful.

Sure, you might remember what the LED means today, but what about 3 months from now when you dig it out of your parts bin?

I personally do not put any part indicators on my boards. When assembling the board, sure, I need to know where the 10k resistors go, the 0.1uF caps, and the LED colors. But that's all part of the assembly sheet. Once the device is built, I most likely will never need to know that a given capacitor is '22pF' and certainly I don't need to know that the big IC on the board is labeled 'U1' (what help is that anyway?). If I'm really troubleshooting a board, I will have the schematic and layout open anyways.

On the flip side, it would be nice to know what the pin functions are – right there, clearly labeled, so I don't have to guess. Every time I connect power, it would be really nice *not* to say a prayer and hope I don't hook power up backwards. And if I do hook power up backwards, is that LED supposed to come on? Or is that just a link connection LED? Oh shoot!



The ADXL330 Breakout

Here is a good example of clear pin labels as well as worthy functional labels. When playing with this accelerometer, you will probably want to know what axis is where. Yes, you could look up the datasheet but why not put the information right there on the board?

We hope these basic rules help you prevent as many mistakes as possible! We certainly have our share of coffee coasters and hope you have one less.

Cheers!
Nathan Seidle

▼ Comments 41 comments

Login or register to post comments.

- aa7jc | about 5 years ago 3

  You guys ROCK!
  thanks for the tutorial

- IvoN | about 5 years ago 3

Thanks for yet another great tutorial !
I'd like to know more about BatchPCB Outline and the Mill job in the CAM. BatchPCB allows me to upload a "outline" file. Can you give us some hints how to generate such a file ?
The Eagle CAM file mentioned above generates a .GML file which uses the "Milling" layer (46) in Eagle. For the outline i'd expect it to generate a file based on "Dimension" (20).
Also, previous tutorials mentioned using a cleaned up version of the silkscreen "_tPlace" (121) (generated after running "silk_gen.ulp"). The script removes silkscreening on solderable areas. This tutorial doesn't mention it and the CAM uses the "tPlace" (21) only. In the pictures I see pin labels, do you add other layers to the silkscreen as well ?
Thanks again, Ivo

-  Nate | about 5 years ago 1

  Thanks for the kind feedback!
  It's very important that you have some sort of an outline for your board. Using our CAM file, the Dimension layer will be outputted to the top copper layer. Sounds odd that the PCB border should be in copper, but here at SparkFun/BatchPCB, we really just need some indicator of where your board border is. Top Silk is also an acceptable place for your border.
  We do not use, and I do not recommend using, the silk_gen.ulp. We only use our CAM file to generate the correct silk. This works because I do not want part indicators or values to print on my PCBs.
  Oh – always always remember to turn on vector fonts!
  (http://www.sparkfun.com/commerce/tutorial_info.php?tutorials_id=109)

  - michael_earthmine | about 4 years ago 1

    Thanks for the tutorial! I umderstand the problem with the layers silk_gen.ulp uses, but does the CAM file do anything to correct the silkscreen line width? If not, how do you address this issue?

  - jago lee | about a year ago 1

    Great quality photos! What camera do you guy's shoot?

-  rbthursby | about 5 years ago 2

Awesome!
Once again, you guys freely impart another chunk of hard earned wisdom for the betterment of the public.
Thank you for the tutorial. I will put it to good use.

- Jeronimo Avf | about 5 years ago 2

  Cool tutorial. Great contribuitionn for the hobbysts and other persons moving from starting experimenting with electronics to the next level of building devices
  Jeronimo
  www.blogdoje.com.br
  Arduino, Avr & ARM

- mperks | about 5 years ago 2

  Good tutorial. I have a few comments.
  If you change the isolation to 12mil that is sufficient to break pours that occur between standard 0.1" headers. This may or may not affect your board. I have also never seen a problem yet from Gold Phoenix (used by batchpcb). In fact if you receive a board with a pour into a signal, I would suggest you return it and ask for a replacement because that is sloppy quality control. Because Gold Phoenix can do down to 7mil for a two-sided board it shows that their masks have quite good resolution. Some other low cost manufacturers can only do 10 mil and these are the ones I would be more concerned about.
  My personal preference is not to tent the vias, especially if it is a prototype board. This is because I sometimes use the vias to help with testing.
  I also either move the via or silkscreen to ensure that the silk screen is not over a hole.

- Dr. Bogger | about a year ago 2

  The “SparkFun Eagle Rules” in the link at the top of this page is outdated.

  Can you update to the newest?

- Ondo88 | about a year ago 2

  I know the tutorial it’s kind of old by now, but anyway, I’ve some extra tips that might help someone.

- Tenting: It's not only about having a better silkscreen on the board, soldermask will also protect your precious vias from rust and aging. It's almost mandatory on RF and analog precision circuits. Without them CuO (copper oxide) will form a thin layer over your vias and pads, ruining your impedance adaptations. Pads are protected in part by solder additives, but it's not a bad idea to use proper spray isolators on harsh enviroments.

- Some PCB software offer "tear" connections for pads and vias. http://dangerousprototypes.com/forum/download/file.php?id=6979&t=1 That is an example of what I'm talking. This reduces mechanical stress around the via connection, avoiding possible rupture of the traces. Again, it's also useful for RF applications, as it makes a better Z matching (it behaves as a tamper used in micro-wave circuits). In PCB software without this kind of feature, you can made your own tear connections manually if you're concerned about some of that issues.

- It's a good practice to place holes around the boards, joining top and bottom ground layers. That makes the board more similar to a Faraday cage, reducing greatly effects from EMI (Electro-magnetic Interference). I had a board with that kind of problems, nothing worked ok until I placed the holes, it worked like a charm since then. If you like to make beautiful boards as I do, you'll probably place that holes equidistant on the perimeter, but to be truth, randomizing the distance between the holes makes a better isolation as no single frequency gets benefited form constructive interference.

- Get to know what you're building. Before getting serious about PCB design, you should learn what is everything you're using on them. I've always said you can know if someone is a good PCB designer by asking him to give you FR4 permitivity, solder fusion temperature and the like (without checking wikipedia ;D). When you make electronic design sometimes you can forget about physics, so be sure you know them well.

- Another common mistake is not taking account of thermal activity on the board. Make sure your temperature sensitive components (like oscillators, and almost any analog circuit) are far from your heat generating circuits (regulators and the like). If your board fits in a box, be sure to have cooling paths that keep the things ok. Remember that heat goes up! (so don't put your sensitive devices on the top if you can avoid that).

- Some chips may have two Vcc or GND pins one to each other. On SMD

packages it's tempting to just join them straight, avoid that if you're using oven soldering (very likely on production). That will unbalance the thermal forces your chip may suffer, moving it from its original position, and possibly making it tombstone.

- I've found very useful to place a couple of squares on silkscreen, with an E (Error) and a T (Tested) on the side of each one. That allows you to mark easily your boards with anything you may have at hand, from a pen to a screwdriver.
- The last one is the more ethereal of the advises, "follow your ground paths". Your signal propagates from your Vcc to your GND, mainly through the shortest path, if two signals share that ground path, they'll interfere each other. Try to make that paths as short and trouble free as you can.

and most important, Have fun with your PCBs :D

-  Nate | about a year ago 2

  All very good points! Thanks!

-  ndrew | about 9 months ago 2

Can the Eagle rule check and CAM processor be updated so that they give the proper output for Batch PCB (which is a part of sparkfun as far as i can tell).

-  pburgess | about 5 years ago 1

I'm intrigued by that first picture...should we be expecting a new PIC32 board in the near future?

-  Nate | about 5 years ago 1

  Yep. Working with Brian Schmalz. It's a simple dev board for the new PIC32 chip. Should be available by end of 2009.

-  Nate | about 5 years ago 1

  Sorry – End of 2008. It's up: http://www.sparkfun.com/commerce/product_info.php?products_id=8971

- scicior | about 5 years ago 1

  Thanks for the helpful tips!
  Has anyone had luck with Tented Vias when using Advanced Circuits (www.4pcb.com)? Their www.FreeDFM.com web site says they can't fix (to their liking) tented vias...
  Thanks,
  – Steve

- Oleg | about 5 years ago 1

  SparkFun Eagle Design Rules mentions that "23)Use thicker traces for power lines where applicable. 12mil=100mA max, 16mil=500mA, and so on."
  Where can I see complete table for these values?

  - Nate | about 5 years ago 1

    This one looks pretty good: http://www.hardwarebook.info/PCB_trace

- Lee | about 5 years ago 1

  You mentioned PCB123 in the opening paragraph, do you use it at Sparkfun?

  - Nate | about 5 years ago 1

    Nope. We only use BatchPCB. I believe you have to use PCB123 software to layout the PCB. This sounds great (free software!) initially, but you are then locked into using only that company. Good PCB layout software outputs gerbers that can be sent to any fab house.

- doctek | about 5 years ago 1

  First, thanks for these guidelines and for sharing your Design Rules. Great Stuff!
  Here's a concern: Your SF Design Rules say to use a 0.05 inch grid. But for the DFN design I did recently I found that I needed to use Metric (millimeter) mode to be able to define my footprint and to place and route it correctly. Would this be a violation of your design rules? I used 0.2mm line and space rules for routing – slightly under 8 mil. The boards I got back were perfect as near as I could tell.
  What guidance would you have for future similar designs?

Thanks.

- Nate | about 5 years ago 1

  Right! Good question. The 0.05" grid rule (found within the Eagle doc) applies to the component centers. Many component footprints are hard metric (for example 0.5mm spacing or 1x1.2mm pad sizes) and it is completely ok to layout pads and parts on the mm grid. However, when placing components I recommend the component centers stay ‘on grid’. This will help with routing and overall component alignment.

- josheeg | about 5 years ago 1

  the error was:
  Less than 2 files found! Something is missing, please check your upload package.
  I am using kicad…
  All of the gerber files look ok in a viewer I zipped them in windows and ubunu before nether worked.

- rsbohn | about 4 years ago 1

  Thanks for running these tutorials. They really help.
  I put a date code in the bottom copper layer, but the BatchPCB robot rejected the board. I’ve changed it to a larger graphical date code (boxes for year, circles for board version). Perhaps a macro could encode the date in some standard (in the community) representation?
  Also, how do you set the default trace width? These 8 mil traces seem a little small, but I don’t want to replace every individual trace segment.
  Thanks again! SparkFun rocks!

  - Nate | about 4 years ago 1

    Hi, Checkout the Eagle.scr file. That’s where you can change all the defaults.
    Set WIRE_BEND 1; #Route with 45 degree angles
    Set Drill 0.02; #Make vias 0.02"
    Change Shape Round; #Make vias round
    Change Width 0.01; #Routing width default to 10mil

- AnotherNate | about 3 years ago 1

The DRC and CAM files linked above appear to be missing. Anyone have them elsewhere? Or any chance someone at Sparkfun could get them back up here?

- AnotherNate | about 3 years ago 1

  Magically they're up today. Weird.

- Loaflawl | about 3 years ago 1

  So awesome!

- SteveChamberlin | about 3 years ago 1

  As a noob designing my first PCB, I found this tutorial incredibly helpful. Restrings? Tenting? It's all beginning to make sense. My first board is now off to BatchPCB. Awesome job, thank you!

- mrmark | about 3 years ago 1

  I'm new to eagle and have been searching around your tutorials and none of them say how to create a ground pour or tips and tricks on the real nitty grittys on how to create a good board, maybe a new eagle tutorial is in order.

- Paddypaddy | about 3 years ago 1

  Thanks, and dont forget a version number

- trygvis | about 2 years ago 1

  It would be nice if these files where a part of the Sparkfun Git repository for Eagle files: https://github.com/nseidle/SparkFun-Eagle-Library, just to keep all the files together. It will also be easier to know when new updates are available.

- Member #224608 | about 2 years ago 1

  do the .dru and .cam files provided hold true for a 4-layer design in Eagle v.5? if not, where should I look for comparable help?

-  rben13 | about a year ago 1

  I'm trying to use Eagle 6.1.0 and when I try to view the gerber files using ViewMate or ViewPlot, I don't see any holes. ViewPlot complains that it can't load a drill file with drill tools, whatever that means. (I'm a newb.) The labels, which I moved to tPlace, are all missing, too. Has anyone used the CAM file with Eagle 6.1.0? Any suggestions as to what I'm doing wrong?

  Thanks!

-  silverfox | about 9 months ago 1

  BatchPCB keeps failing my boards because of traces being too narrow (0.0039000000 < 0.0081000002). I am using AutoRouter and I don't see where to change trace size. You suggest 10 mils but don't ever say where to set that value. I tried changing the Routing grid value, but no matter what I enter there, the traces are always 8 mil so I guess that is not where to set it. Please advise!

  -  Kamiquasi | about 9 months ago 1

    Edit > Design Rules... > |Sizes|

    You should be able to set the minimum trace width there. Note that the appropriate values are also in BatchPCB's DRU (Design RUles) file which you can load from that dialog. BatchPCB's should have a DRU file available, or hit up Google for some variants.

    -  silverfox | about 9 months ago 1

      I am using Eagle 6.2.0 Light edition and there is no Design Rules item in the Edit menu.

      -  Kamiquasi | about 9 months ago 1

        Are you sure? It should be near the bottom; http://i.imgur.com/P1a42.png

        -  silverfox | about 9 months ago 1

          I am using a netbook with a low resolution screen and it

turns out that menus containing a long list of items do not scroll vertically as I assumed they would, but wrap onto an extra column of items. I never saw this behavior before and so missed the last few items in the menu, including Design Rules. Thanks for your help.

- Kamiquasi | about 9 months ago 1

  Ahhh – yeah, that would make it easy to miss :) Glad I could help.

Sharing Ingenuity

- GitHub
- YouTube
- Vimeo
- Google Plus
- Facebook
- Flickr
- Twitter
- RSS

SparkFun?

SparkFun is an online retail store that sells the bits and pieces to make your electronics projects possible. Whether it's a robot that can cook your breakfast or a GPS cat tracking device, our products and resources are designed to make the world of electronics more accessible to the average person. In addition to products, SparkFun also offers classes and a number of online tutorials designed to help educate individuals in the wonderful world of embedded electronics.

Resources

- Feeds
- Forum
- SparkFun Education
- SparkFun IRC Channel
- Jobs @ SparkFun
- Sell Your Widget on SparkFun
- Become a SparkFun Distributor

- Request SparkFun Sponsorship
- Take the SparkFun Quiz
- Tell us about a project
- SparkFun Kickstarter Projects
- Chat With Us

Feedback

What's on your mind?

For which department?

General

Please include your email address if you'd like us to respond to a specific question.

email address

Submit

SparkFun Electronics ® | Boulder, Colorado | Customer Service