MANUFACTURING DESIGN GUIDELINES

INDEX

1.0 PURPOSE

The purpose of these guidelines is to establish the required standards for the design of printed circuit boards. These guidelines are intended to serve as a best practice guide to customer and suppliers to aid manufacture and process.

2.0 SCOPE

This document provides information on CPI Electronics Ltd design guidelines for the application of electronic components to all printed circuit boards designed using CAD systems. Wherever possible the specifications given conform to IPC-SM-782 Surface Mount Design and Land Pattern Standard

3.0 BOARD TYPE

Details such as board thickness, solder finish, and solder resist should be specified on the Detail Drawing. However, the following are the preferred specifications, and are recommended to be used whenever possible.

3.1 Preferred basic elements are:

Solder Finish: Lead Free HASL for circuits incorporating 0.6mm or grater pitch devices. For fine pitch and BGA's Gold flash is preferred.

Tooling Holes: Two 4 mm (+ 0.5 / – 0) tooling holes must be located in each corner (bottom left and right), positioned 5mm in from the edge of the PCB, See Fig 1

Fiducial Mark: A 1 mm (+/- 0.1) circle or 2 mm (+/- 0.1) cross is the preferred pattern. A clear area devoid of any other circuit features or markings should surround the fiducial patterns where possible. See Fig 2. Global or panel fiducial location is preferred to be set at a right angle to each other and at minimum 7 mm from the board edge, See Fig 1. The best performance contrast is achieved when a consistent high contrast is present between the fiducial mark and the PCB base material, therefore all fiducials should be clear of solder mask/ resist. The flatness of the surface of the mark should be within 0.015 mm (0.0006 in) (particularly with HASL finish PCB's.

Fig 1

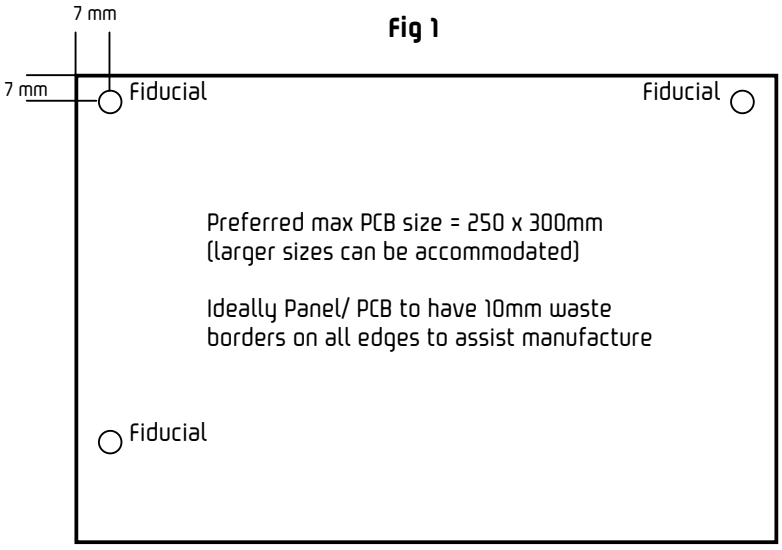
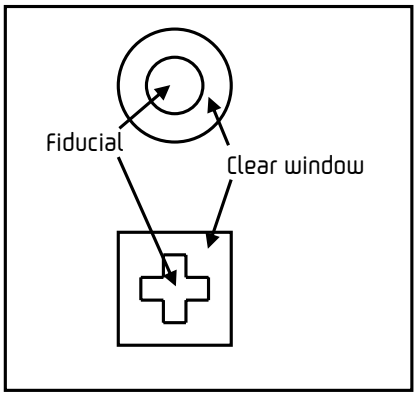


Fig 2



It is recommended that all new boards or panels to be manufactured for CPI be submitted for approval to the prior to ordering by purchasing.

4.0 COMPONENT/PROCESS CONSIDERATIONS

The choice of component types, i.e. conventional or SMD, will determine the assembly and soldering processes required by the Production Department.

4.1 SMD'S ONLY

4.1.1 Preferred method. All components should be placed on one side of the board if possible.

4.1.2 PCB designs that incorporate component placement on both sides will require re-flow on both sides.

4.1.3 It is recommended that PCB designs, which incorporate SMD IC devices that require wave soldering should contain larger end pads to act as solder thieves. It is preferred that both ends of the device have this, as an option to run the PCB through wave either way. See Fig 3

4.1.4 If SMD QFP devices require wave solder then there orientation should be such that they are placed at 45° to allow the solder to flow evenly onto the pins / pads reducing the risk of shorts. See Fig 4

Fig 3 Component Foot Print SOIC 14 and 28 Pin QFP

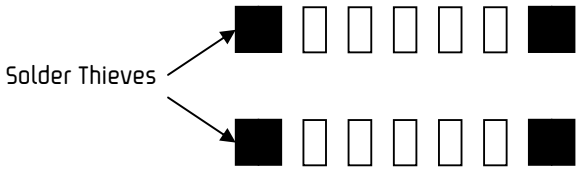
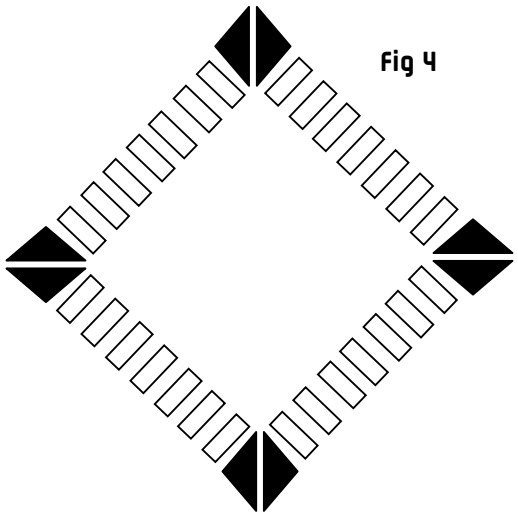


Fig 4



4.2 SMD'S AND CONVENTIONAL COMPONENTS

4.2.1 Preferred method. With conventional components on one side and SMD on the same side or on both sides, wave and re-flow soldering will be necessary.

4.2.2 When conventional components are placed on one side of the board and all SMD on the other, then bonding of SMD using glue will be required and then sent through the wave for soldering, assuming all SMD components are suited to wave solder technology.

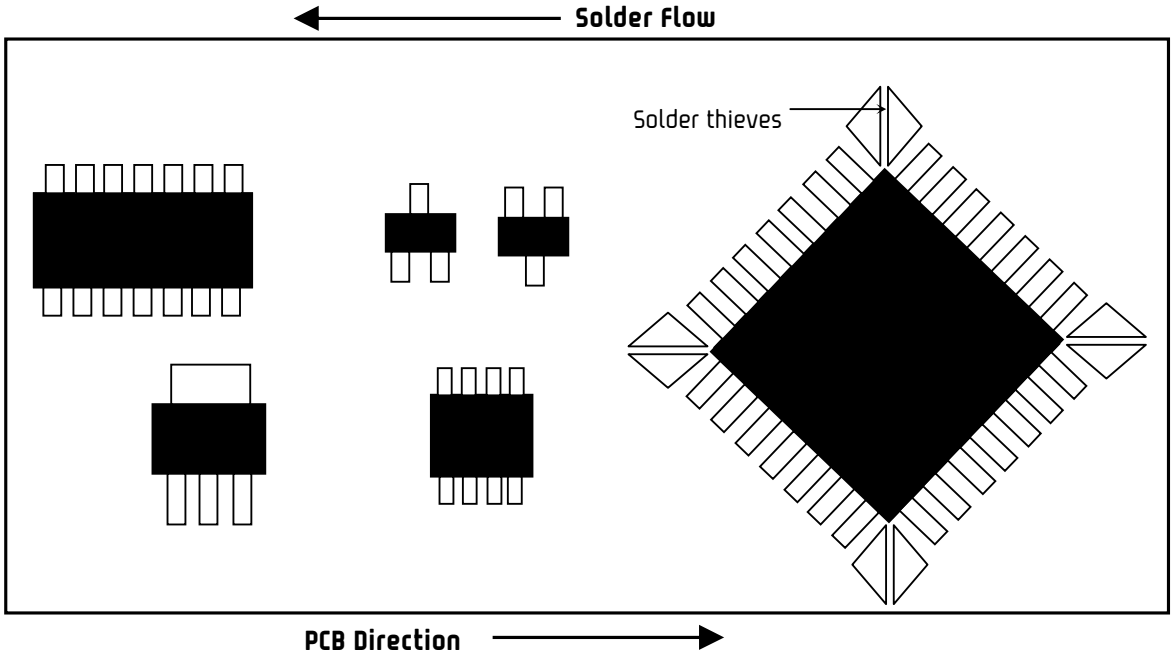
4.3 SELECTION OF COMPONENTS

4.3.1 SMD should be used in preference to conventional components unless the price increase is significantly more than the saving in assembly costs.

5.0 COMPONENT LAYOUT

5.1 For wave soldering, some components, such as DIL's and most SMD's, must be aligned correctly to achieve optimum soldering quality. The correct orientation of such components is shown in Fig 7. Soldering quality from re-flow soldering is not dependant on the orientation of components.

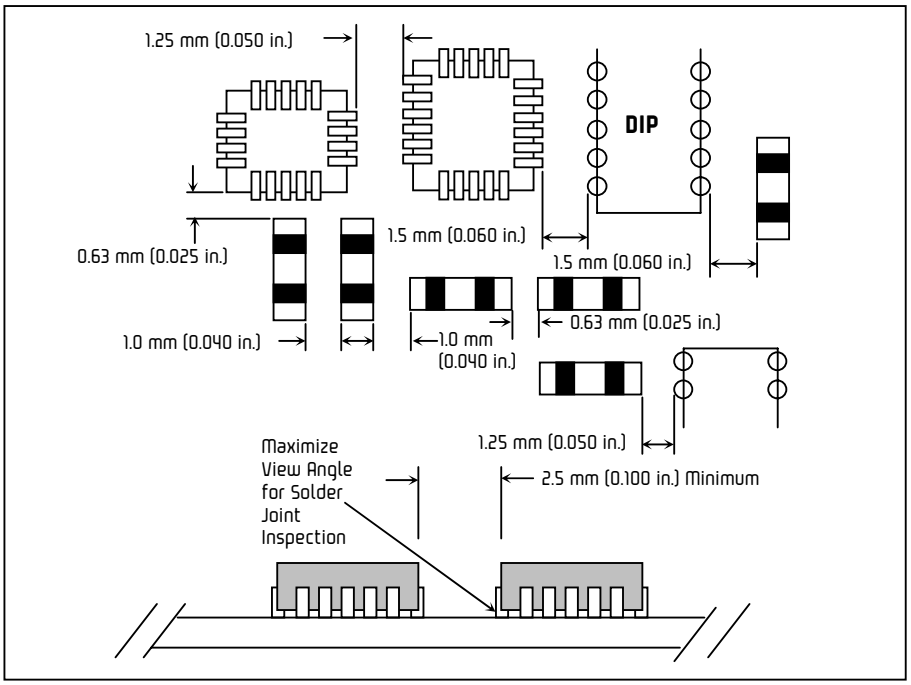
Fig 7 Component Alignment



5.2 It is preferred that all similar components are aligned in the same direction, and pin 1 of all IC's at the same end.

5.3 The spacing between components must be sufficient to allow the use of automated assembly equipment, and to avoid soldering problems such as short-circuits, shadowing, etc., especially with SMD during wave soldering, for the minimum recommended pitches for SMD see Fig 8.

Fig 8 Recommended SMD Pitch



5.4 Hand-soldering should be avoided where possible. Therefore components should be positioned to permit wave or re-flow soldering.

5.5 Space must be specified to CPI Electronics Ltd on the conventional (or topside) of the board for the following labels, and their positions shown on the assembly drawing:

5.5.1 Sub-assembly number and issue label (20mm * 6mm). If required

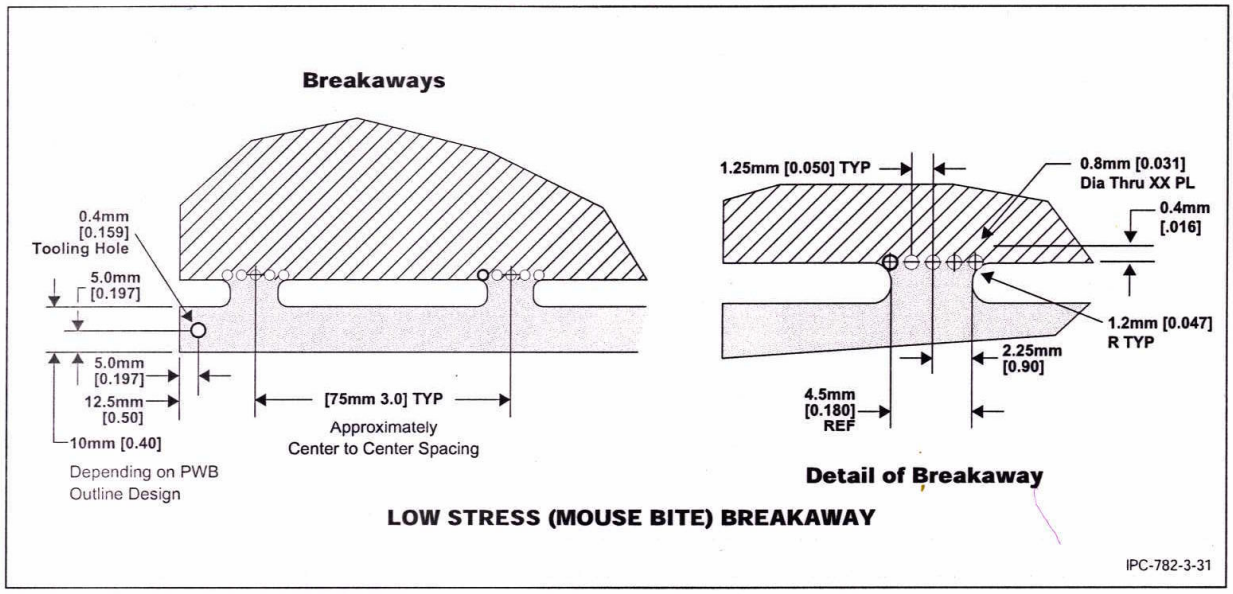
5.5.2 Bar-code serial number label (30mm * 6mm). If required

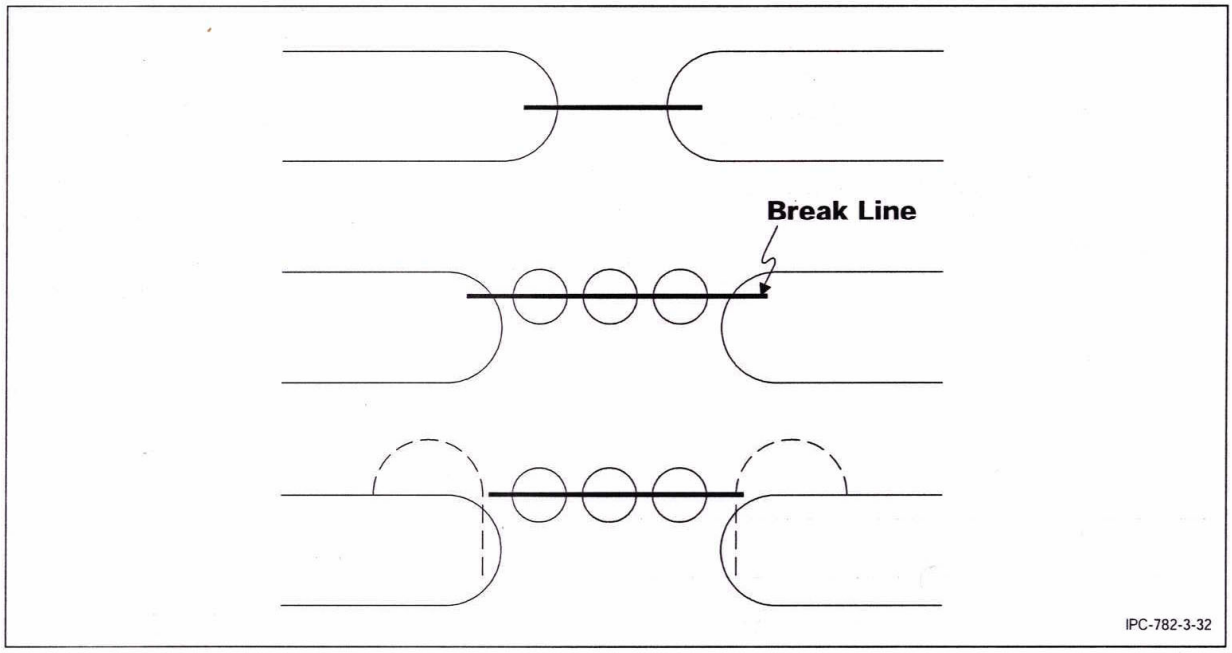
5.5.3 Test status label (30mm * 6mm). If required

5.5.4 No components (except connectors) must be placed within 5mm of the edge of the board. However, if the leading (or trailing) edge of the board through the wave solder machine is also the leading (or trailing) edge of the motherboard, no components (except hand-soldered) must be placed within 10mm of that edge.

6.0 PCB Breakout/ panelisation

6.1 CPI's preferred PCB breakout from panels is using the "Mouse bite" as shown. However "V" scoring is also acceptable where routing of the PCB is not required.





7.0 CAD / GERBER DATA OUTPUT and FORMATS

7.1 Format

All Cad or Gerber data should arrive at CPI Electronics Ltd in one of the following formats

*.GBX Embedded
*.GWK
*.GDO
Any Gerber data format
Component X-Y co-ordinates (to component centres. (CSV, Xls)

7.2 Required Layers

Pad, Paste, Spot mask, Silk Screen, Panel Details, Fiducial Markings and copper layers.

8.0 SMD LAND PATTERN DESIGN

8.1 Where ever possible IPC Design guidelines be observed

9.0 RECOMMENDED TRACK WIDTHS & TRACK POSITIONING

9.1	Minimum track width	0.25mm (0.010in)
9.2	Minimum spacing between tracks	0.25mm (0.010in)
9.3	Minimum spacing between solder pads	0.25mm (0.010in)
9.4	Minimum spacing between track and board edge	3mm (0.120in)
9.5	Minimum spacing between track and fastenings	3mm (0.120in)

10.0 Via Location Guidelines

10.1 Size of the via holes should be selected based upon the printed board thickness vs. hole diameter or aspect ratio limits as defined by printed board fabricator. In addition, specific via lands and holes can be accessed for automatic in-circuit test (ICT).

10.2 Via holes must be located away from component lands to prevent solder migration off the component land during re-flow soldering. This migration will cause insufficient solder fillets on components. (Solder drain) The solder migration can be restricted by providing a narrow bridge between the land area and via or prevented by using the solder mask over bare copper circuitry. Solder mask should be used on via holes when access for test points is not required, See Fig 11 and 11a.

Fig 11

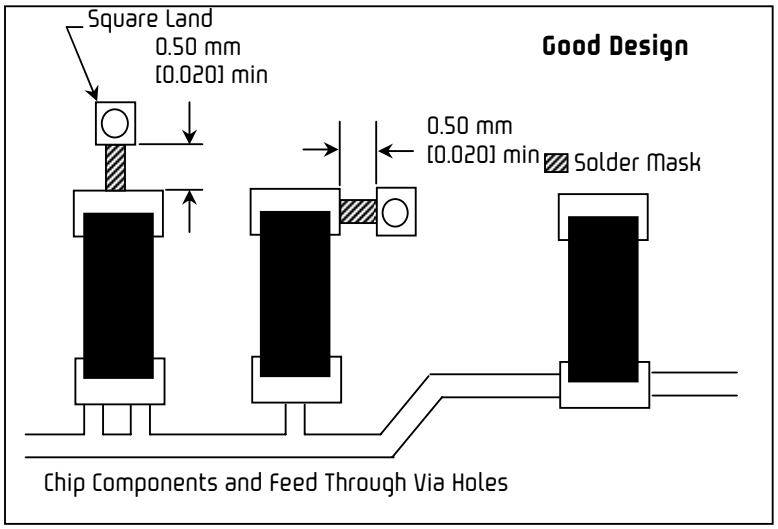
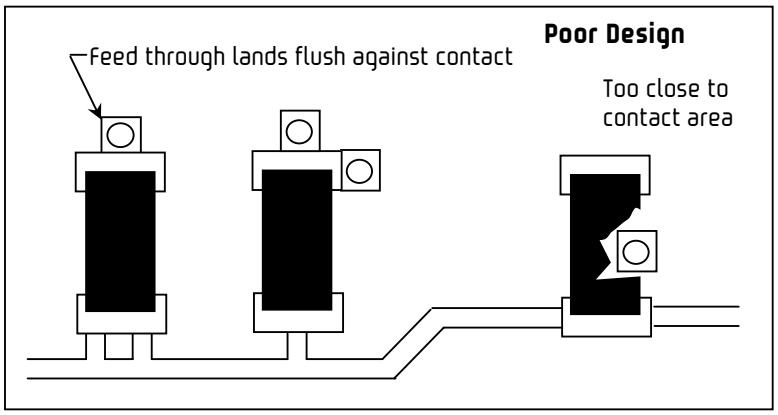


Fig 11a



12.0 Masking

12.1 CPI Electronics Ltd recommend that, any areas requiring spot, peel able mask or masking should form a complete flow of masking where possible with no breaks. This will aid in the reduction of handling time within the product, see Fig 12 and 12a.

Fig 12

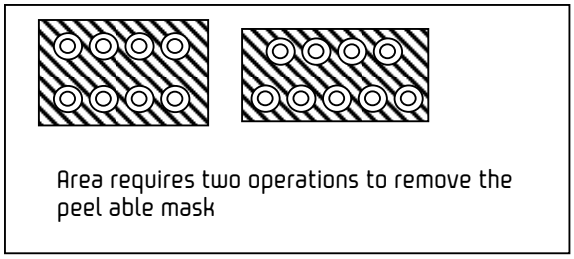
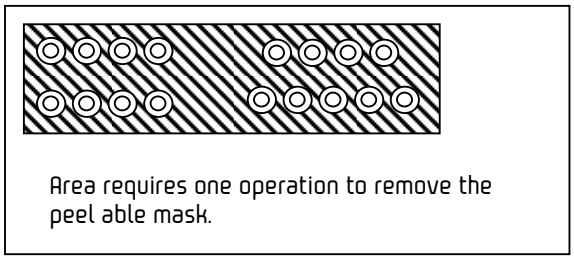


Fig 12a



13.0 Temperature Differential

13.1 If a PCB design is such that a large part of the circuit has a copper layer running through, there may be potential for board warp age, due to the copper layer acting as a heat sink. To reduce this either spread the copper layer out as even as possible across the circuit or hatch the layer reducing its heat absorbing capabilities, see Fig 13.

Fig 13 PCB with large copper layer