Study of Mutual Coupling on Mobile Phone PCB with Shielding using FDTD

Chung-Huan Li [#1], Jari Jekkonen [#1], George Tudosie [2], Nicolas Chavannes [2], and Niels Kuster [#1]

[#] *IT'IS Foundation, ETH Zurich*
Zeughausstrasse 43, CH-8004, Zurich, Switzerland
[1] ed@itis.ethz.ch
[2] jekkonen@itis.ethz.ch
[5] kuster@itis.ethz.ch

[*] *Schmid & Partner Engineering AG (SPEAG)*
Zeughausstrasse 43, CH-8004, Zurich, Switzerland
[3] tudosie@speag.com
[4] chavanne@speag.com

***Abstract*—The coupling mechanisms on a commercial mobile phone PCB with different shielding configurations has been investigated with FDTD simulation in this paper. A modified PCB based on the commercial PCB was manufactured for validation purposes prior to the simulation. Good agreement between simulation and measurement was obtained. The coupling performance of the commercial PCB was then reproduced with numerical simulations. A simplified PCB model was developed to investigate the phenomena observed in the simulation results of the commercial PCB. The investigation explains the difference of the coupling mechanisms with and without shielding and the effect of perforated shielding on the coupling.**

I. Introduction

Practical EMC problems at the PCB level are always massive and complicated. It is common to design and solve EMC problems by following guidelines based on practical experience or studies [1]–[5]. In addition to measurement, simulation can play an important role in these problems as it can reduce the number of prototypes. Simulation is able to provide information which is difficult to measure or is even not measurable. This is helpful in optimizing and debugging the design. However, simulation of real-world PCBs for EMC problems was until now not practical as it requires great computational resources and long simulation time. Thus, most numerical PCB-level EMC studies are only conducted with greatly simplified models [6]–[8]. Although those studies can serve as a knowledge base, the simulation results may not be able to reflect the real situation.

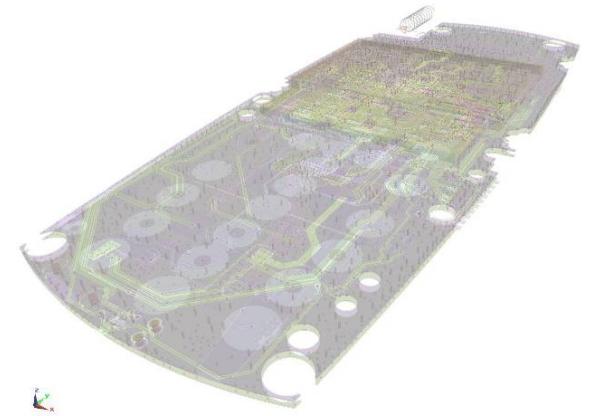
Nevertheless, recent big advances in Finite-Difference Time-Domain (FDTD) using hardware acceleration changes the situation. FDTD is frequently used to obtain the time-domain information and the EM field distribution [3], [7]–[9]. FDTD is particularly suitable for simulating EMC problems in realistic scenarios because of its good performance in highly inhomogeneous environments [10]. Besides, thanks to the rapid advance in integrated circuit technology and hardware acceleration [11], simulation of a real-world EMC problem without simplifying the scenario becomes possible and can be done in reasonable time [12]. An EMC problem of a commercial mobile phone PCB was investigated using FDTD in this paper. The commercial PCB is shown in Figure 1. It is a four-layer PCB with shielding. There are 16 active *traffic traces* and a passive *victim trace* all below the shielding. The traffic traces are the transmission lines for baseband signals and the victim trace is a part of the RF chain on this board. Each traffic trace has two locations on the top and bottom layer connected to ground via 27pF capacitors to filter the noise from the traffic traces to the LCD. Two victim ports are connected on each side of the victim trace. The harmonics generated by the traffic traces can be coupled to the victim trace so the signal-to-noise ratio (S/N) in the RF chain is decreased. On the other hand, the RF chain experiences different coupling levels with the presence of shielding. Shielding is one of the most common and effective approaches of suppressing EMI [13] and increasing the isolation between different modules on a PCB [14]. However, shielding may significantly influence the coupling between the traces underneath the shielding. The objective of this study is to investigate the effect of the shielding on the coupling of harmonics at RF from the traffic traces to the victim trace. Because the source region of the traffic traces is so small (about $1 \times 1cm^2$), measuring the coupling is not practical and so simulation was applied.

Validation of the simulation by measurement is necessary before simulating the commercial PCB to ensure reliable simulation results. Thus, a modified board was manufactured based on the PCB to validate FDTD simulation in this scenario. After the validation, the coupling behaviors on the commercial PCB were simulated with different configurations of shielding. Based on the observations of the simulation results of the commercial PCB, the coupling behaviors requiring investigation were addressed. A simplified model was then built to investigate these behaviors.

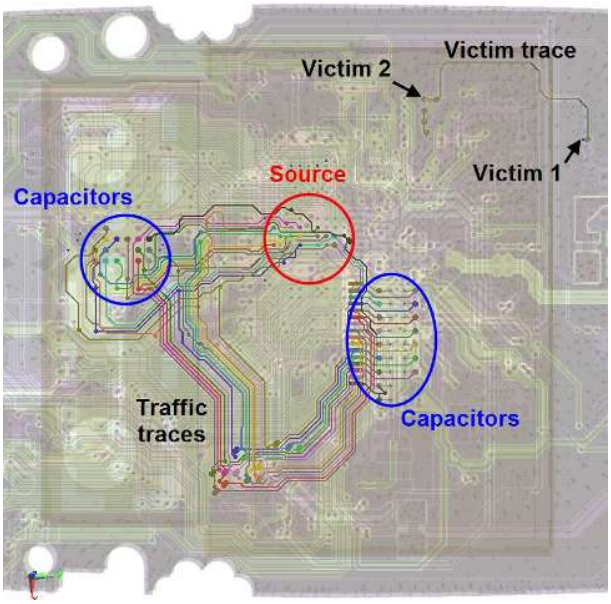
II. Validation

As mentioned above, the source region of the commercial PCB is too small to connect 16 coaxial cables to feed the

978-1-4244-6307-7/10/$26.00 ©2010 IEEE



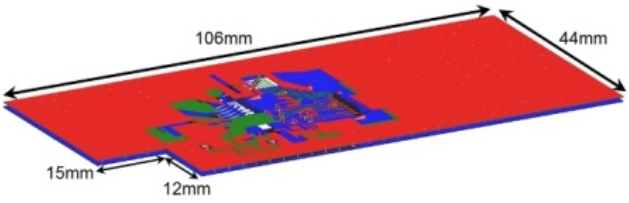
(a)



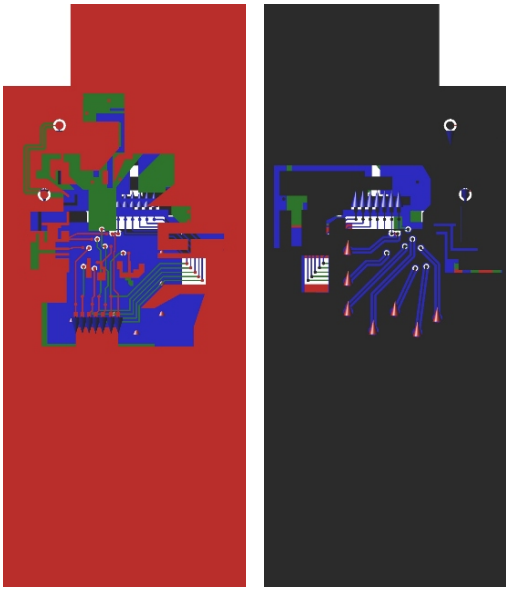
(b)

Fig. 1. The real mobile phone PCB model simulated and studied in this paper. There are 16 active traffic traces inside the shielding fed in the source region and a victim trace with two victims, one inside and one outside the shielding.

traffic traces. For the validation, a modified PCB was built as shown in Figure 2. It has four layers and the distances between each layer are 0.1 mm, 0.7 mm and 0.1 mm, respectively. The materials of the prepreg and center layers are IS410 and S6018 from Isola and Guandong Shengyi Sci. Tech., respectively ([15], [16]). Each metal layer is 30μm and there are seven traffic traces instead of 16. On the bottom layer, seven voltage sources (or coaxial cables in measurement) feed the transmission lines which connect to the traffic traces on the top layer by the through-vias. The capacitors connected on each trace are 0402, 27pF capacitors from Murata [17]. The RLC series equivalent circuit of the capacitors was used in the simulation. Two voltage sources were connected on each side of the victim trace as the victim ports. The PCB was manufactured and measured as seen in Figure 3.

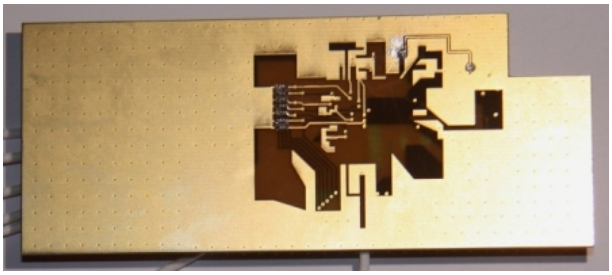


(a)

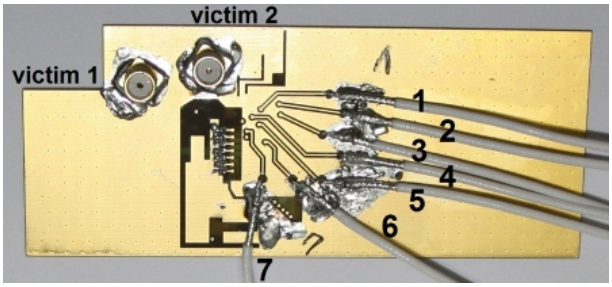


(b) (c)

Fig. 2. (a) The dimensions of the numerical model of the PCB for validation, and its (b) top and (c) bottom view. The red and blue arrows are the voltage sources and lumped elements, respectively. (red: top layer, green: mid-layer 1, blue: mid-layer 2, black: bottom layer)



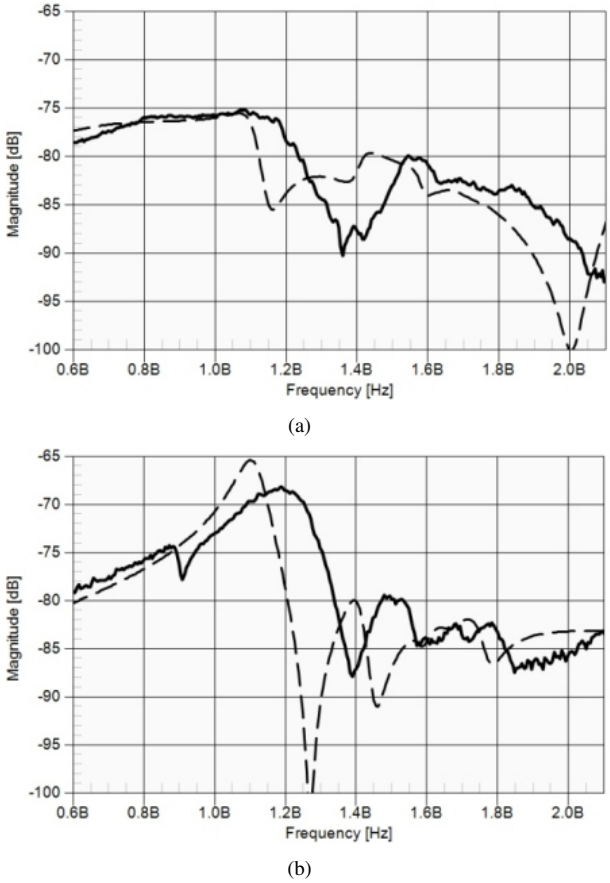
(a)



(b)

Fig. 3. The physical PCB for validation in (a) top and (b) bottom view.

Figure 4 shows the mutual coupling between (port 1, victim 1) and between (port 7, victim 1). The simulation results agree with the measurement results. The slight frequency shift (about 6%) could be due to the uncertainty of the permittivity of the substrates. As the level of mutual coupling is very low (around -80 to -85 dB), orientations of the feeding coaxial cables may significantly vary the coupling level at a frequency higher than 1 GHz. The good agreement obtained in the validation proves that simulating PCB-level EMC problems on a realistic PCB with FDTD is a reliable approach.



(a)

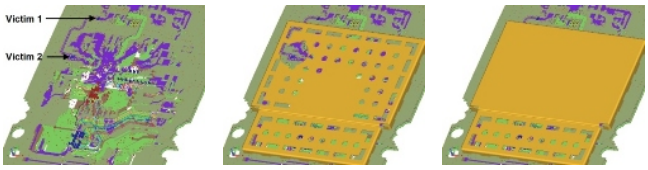
(b)

Fig. 4. The simulation (dashed) and measurement (solid) results of the mutual coupling (a) between (port 1, victim 1) and (b) between (port 7, victim 1).

III. Simulation of the Commercial Mobile Phone PCB

The 16 traffic traces on the commercial PCB were fed independently by voltage sources in the FDTD simulation. The capacitors on the traffic traces were also modeled as RLC series equivalent circuits of the 27pF capacitors from Murata. The two victim ports are 50 Ohm resistors. Three scenarios for different shielding (full shielding, perforated shielding and no shielding) were simulated, as described in Figure 5. The shielding is grounded on the top layer of the PCB.

For the purpose of this study, a parameter called *isolation* was defined to analyze the coupling between the traffic traces and victims:



(a) (b) (c)

Fig. 5. The three different configurations of the shielding on the real phone PCB; (a) no shielding, (b) perforated shielding and (c) full shielding.

$$\text{Isolation (dB)} = 10 * log(P_{v,k}/P_{in}), \qquad k = 1, 2 \qquad (1)$$

$P_{v,k}$: the real part of the power received at victim k

P_{in}: the summation of the real part of the input power of all the traffic traces.

This definition will be applied in the rest of this paper to quantify the coupling between the traffic traces and the victims.

The isolation (defined in Equation 1) at victim 1 and 2 for the three different shielding cases is shown in Figure 6. The simulation parameters and performance of both the validation and the commercial PCB are shown in Table I. The simulation time correlates to the resolution of the model and the number of time steps. The structure with a higher quality factor usually needs a longer simulation time (in periods) to obtain accurate results. FDTD with hardware acceleration using CUDA technology with four NVIDIA Tesla C1060 graphic cards, called S1070, was used in the simulations [11], [18].

TABLE I
Simulation parameters and performance of the validation and the commercial mobile phone PCB (M: million).

Parameter (unit)	Validation PCB	Commercial PCB
Frequency (GHz)	0.5 - 2.3	0.3 - 2.1
Grid size (cells)	55.5 M	55.5 M
Min. resolution (μm)	30	37
Time step	0.5 M	1.6 M
Simualtion speed (cells/sec)	1320 M	1080 M
Simulation time (hours)	6	26

The observations from the simulated isolation can be summarized as follows: victim 1 and 2 have similar isolation for the 2 shielded cases, while the isolation of victim 1 and 2 is quite different without shielding. The coupling mechanisms with and without shielding are therefore also significantly different. Furthermore, the PCB with the perforated shielding offers better isolation than the full shielding (approximately 6 - 8 dB over the frequency band). This suggests that the perforation can significantly influence the coupling. These two observations were studied with a simplified PCB in the following section.

IV. Analysis with a Simplified Model

A simplified PCB model, as depicted in Figure 7, was developed to explain the difference in isolation between victim

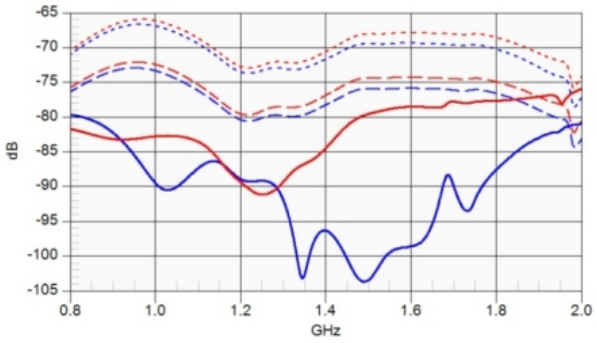
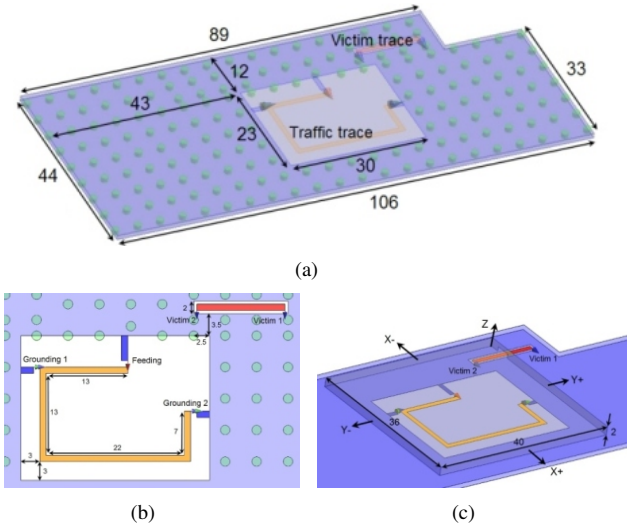


Fig. 6. The simulated isolation between the victims and the traffic traces with the real phone PCB model. (dot: full shielding, dash: perforated shielding, solid: no shielding) (blue: victim 1, red: victim 2)

1 and victim 2 with different configurations of the shielding. The simplified PCB has only one voltage source and one traffic trace. The simplified model with shielding is shown in Figure 7. As in the real phone PCB, victim 1 and victim 2 are outside and inside the shielding, respectively.

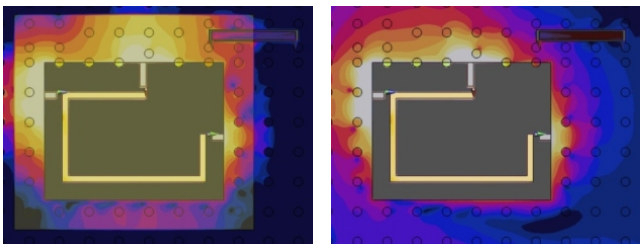


(a)

(b) (c)

Fig. 7. The simplified PCB built for investigating the coupling behaviors observed on the commercial mobile phone PCB.

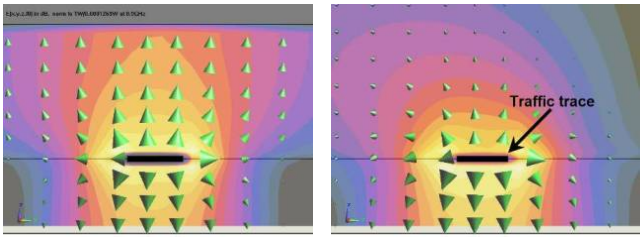
The currents at feeding and grounding 2 act as the coupling sources to the victims. The current distribution on the top layer with and without shielding is shown in Figure 8. When the PCB has no shielding, the traffic trace couples to both victims. The shielding confines the current to in the shielding only. Therefore, only victim 2 receives power coupled from the traffic trace, and the power is shared with victim 1 through the victim trace. The isolation of victim 1 and victim 2 is thus very close to each other with shielding. Besides, although the current around grounding 1 is not significantly coupled to the victims, the location can still influence the isolation. As grounding is a boundary condition for the traffic trace, the grounding location affects the total current distribution on the traffic trace. Thus, the isolation can also be changed by moving the location and load of grounding 1. The shielding does not change the current at these locations, but significantly changes the current distribution on the PCB and consequently the isolation.



(a) (b)

Fig. 8. The current distribution on the top layer (a) with shielding and (b) without shielding.

Reducing the shielding height makes the traces behave more like striplines than microstrip lines. Therefore, the shielding could enhance the coupling path via air between the traffic trace and the victims. The E-field distributions with the two different heights of shielding (Figure 9) show that, compared to the infinite high shielding, traffic trace with the 1.8 mm high shielding acts like a stripline instead of the original microstrip line. Consequently, shielding increases the power above the PCB. Moreover, there are vias in the substrate between traffic trace and victim trace, so coupling through air is the most important path between the two traces.

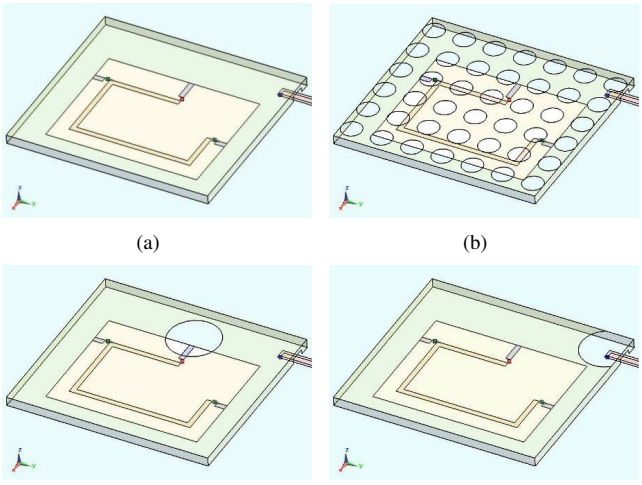


(a) (b)

Fig. 9. The E-field distributions on the traffic trace (transverse view) with the simplified PCB when the shielding has (a) 1.8 mm height and (b) infinite height.

To understand the influence of the perforated shielding, four different configurations of holes were simulated (Figure 10). The simulation results in Figure 11 show that the isolation can only be improved significantly when there is one big hole above the victim (Figure 10(d)). As mentioned above, the traffic trace behaves like a stripline with shielding, and the most important coupling path is through the air inside the shielding. Having a big hole above the victim breaks the stripline effect around the victim, so the hole significantly reduces the coupling from the traffic trace to the victim.

In the real phone model, the perforated shielding also has a big hole (3.5 mm radius) above the victim. The Poynting vector distributions of the real phone model in Figure 12 show significantly less power transmitted to the victim with the perforated shielding than with the solid shielding.



(a) (b) (c) (d)

Fig. 10. The four different configurations of shielding used to investigate the influence of perforated shielding: (a) full shielding, (b) shielding with an array of small holes (2mm radius), one big hole (5mm radius) above (c) the feeding location and (d) victim 2, respectively.

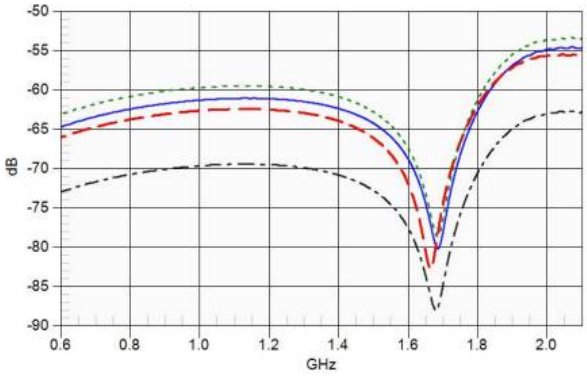
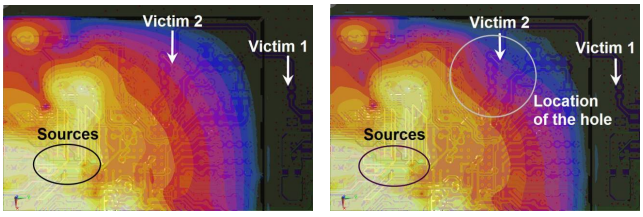


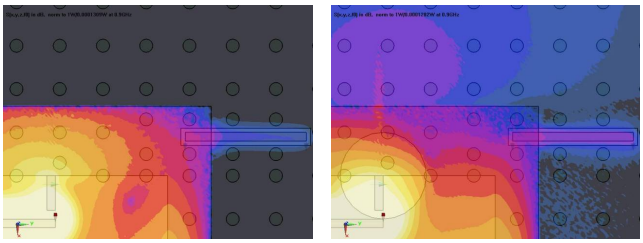
Fig. 11. The corresponding isolation of the models in Figure 10. (solid: full shielding, dash: shielding with an array of small holes, dot: one big hole above the feeding location, dash-dot: one big hole above victim 2)



(a) (b)

Fig. 12. The Poynting vector distributions at 880 MHz on 1 mm above the real phone PCB with (a) full shielding and (b) perforated shielding.

In addition, it can be observed in Figure 11 that when the shielding has a big hole above the feeding, the isolation is weaker than with full shielding. This can also be illustrated by the Poynting vector distribution shown in Figure 13. The big hole can slightly reduce the coupling power from the feeding location inside the shielding. However, EM power also leaks significantly from the shielding through the hole. Part of the leakage is coupled by the victim trace from outside the shielding. Consequently, the isolation with this shielding may be worse than that with full shielding. With regard to perforation, having one big hole above the victim appears helpful in improving isolation if the leakage is well controlled.



(a) (b)

Fig. 13. The Poynting vector distributions 1 mm above the simplified PCB at 900 MHz with (a) full shielding and (b) perforated shielding. The perforated shielding also has a big hole (3.5 mm radius) above the feeding location.

V. Conclusion

The effect of the shielding on the coupling between the traffic traces and the victim trace on a commercial mobile phone PCB was studied in this paper using FDTD. Before the simulation of the commercial PCB, a modified PCB was manufactured to validate FDTD simulation of PCB-level EMC problems on a realistic board. After obtaining good agreement between simulation and measurement from the validation, the commercial PCB was simulated with different configurations of the shielding. The simulation of the commercial PCB provides information that the shielding may significantly influence the coupling behavior and level between the traffic traces and the victim trace. A simplified PCB model was developed to gain more insight into the effect of shielding on the trace coupling.

The investigation found that, firstly, only the victim port inside the shielding is coupled from the traffic traces while both victims are coupled without shielding. Also, as the traces inside a shielding behave as striplines, the coupling to the victims is significantly increased. A big hole above the victim should be able to enhance the isolation if the leakage from the hole is low. The results of this shielding investigation can be incorporated into the knowledge base on design considerations of shielding. Furthermore, this paper shows that numerical simulation of PCB-level EMC problems for real-world models is a practical approach for cost and design considerations.

References

[1] M. Montrose, *Printed Circuit Board Design Techniques for EMC Compliance*. IEEE press, 1996.

[2] C. R. Paul, *Introduction to Electromagnetic Compatibility*. Wiley, 2006.

[3] H. Chen and J. Fang, "Effects of 20-H rule and shielding vias on electromagnetic radiation from printed circuit boards," in *IEEE Conference on Electrical Performance of Electronic Packaging*, 2000, pp. 193–196.

[4] S. Muralikrishna and S. Sathyamurthy, "An overview of digital circuit design and PCB design guidelines - an EMC perspective," *10th International Conference on Electromagnetic Interference and Compatibility*, pp. 567–573, Nov. 2008.

[5] W. Pan, D. Pommerenke, S. Xu, and J. Jia, "PCB ground fill design guidelines for radiated EMI," *IEEE International Symposium on Electromagnetic Compatibility*, pp. 1–6, Aug. 2008.
[6] F. Xiao, K. Murano, and Y. Kami, "The use of via holes for controlling the crosstalk of nonparallel microstrip lines on PCBs," in *IEEE International Symposium on Electromagnetic Compatibility*, vol. 2, Aug. 2002, pp. 633–638 vol.2.
[7] C. Schuster and W. Fichtner, "Parasitic modes on printed circuit boards and their effects on EMC and signal integrity," *IEEE Transactions on Electromagnetic Compatibility*, vol. 43, no. 4, pp. 416–425, Nov 2001.
[8] M. Rizvi and J. LoVetri, "Modeling and reduction of crosstalk on coupled microstrip line structures and multichip modules: An FDTD approach," *Microwave and Millimeter-Wave Computer-Aided Engineering*, vol. 6, no. 1, 1996.
[9] E. R. Pillai, "Coax via-a technique to reduce crosstalk and enhance impedance match at vias in high-frequency multilayer packages verified by FDTD and MoM modeling," *IEEE Transactions on Microwave Theory and Techniques*, vol. 45, no. 10, pp. 1981–1985, Oct 1997.
[10] A. Taflove and S. C. Hagness, *Computational Electrodynamics: The Finite-Difference Time-Domain Method, Third Edition*. Artech House.
[11] "Acceleware, http://www.acceleware.com/."
[12] "SEMCAD X: EM/T Simulation Platform. www.semcad.com."
[13] N. Oka, C. Miyazaki, T. Uchida, and S. Nitta, "Effect of a shielding plane connected to ground plane of a PCB in EMI reduction," *IEEE International Symposium on Electromagnetic Compatibility*, pp. 204–207, 1999.
[14] K.-D. Kim, J. Park, J.-G. Lee, J. Kim, and J.-H. Lee, "Grounded-moating and shielding for noise-coupling reduction between adjacent packages and MCMs," *Microwave and optical Technology letters*, vol. 45, no. 6, June 2004.
[15] "Isola Group, http://www.isola-group.com/."
[16] "Guangdong Shengyi Sci. Tech Co., http://www.syst.com.cn/."
[17] "Murata manufacturing Co., Ltd., http://www.murata.com/."
[18] "NVIDIA, http://www.nvidia.com."

Knowledge-based Approach to Interference Mitigation for EMC of Transceivers on Unmanned Aircraft *

Ilteris Demirkiran [1], Donald D. Weiner [2], Andrew Drozd [3] and Irina Kasperovich [3]
[1] Electrical, Computer, Software, and Systems Engineering, Embry-Riddle Aeronautical University
600 South Clyde Morris Blvd., Daytona Beach, FL 32114, USA.
demir4a4@erau.edu
[2] 960 E. Bunkerhill Dr., Terra Haute, IN, 47802 USA.
[3] ANDRO Computational Solutions, LLC, Rome, NY, 13440 USA.
adrozd@androcs.com
ikasperovich@androcs.com

Abstract- *This paper discusses the results of exploratory research and development to apply and demonstrate a heuristics, knowledge-based approach for analyzing the electromagnetic compatibility (EMC) of co-located radio frequency (RF) spread spectrum frequency hopping transceivers mounted on an unmanned airborne vehicle (UAV) platform. In particular, an expert system pre-processor is used to set up the initial problem and assure the availability of a valid geometry model which is used to compute geodesic losses in the frequency domain. A knowledge base is constructed to contain essential modeling rules and "scripts" describing the steps involved in a validated, bottoms-up/top-down EMC analysis methodology. Problem reasoning is first performed on the system geometry in the pre-processing stage. An expert system based post-processor is then used to "monitor" the signal environment in the time domain and select the interference rejection scheme(s) appropriate for mitigating the effects of interferers present at a victim receptor port. Various interference rejection schemes are considered based on the interferer type and signal environment characteristics. This is necessary since a single interference rejection scheme cannot realistically be expected to suppress all types of interference that may be present.*

Index Terms- *Interference rejection, Spread spectrum, Knowledge-based signal processing, EMC, Unmanned aircraft.*

* Research sponsored by USAF Rome laboratory under contract no F30602-97-C-0162

I. INTRODUCTION

The relevant EMC problem solving domain generally centers on predicting multiplatform RF radiated coupling and interference for several types of co-located electromagnetic sources and nearby jammers associated with battlespace sensor-to-shooter deployments. Systems and deployment scenarios include, but are not limited to: Global Hawk, Comanche, other Tier-2 class unmanned airborne vehicles (UAVs), as well as a number of advanced tactical systems and surveillance platforms. The latter includes modern composite airframe vehicles, sophisticated wireless or mobile telecommunications systems, global positioning satellites, AWACS radars, and so on. The electromagnetic sources consist of advanced military-critical radio and surveillance technologies, and state-of-the-art computing and signal processing systems. The ability to model, simulates, and assesses the various inter/intra-system electromagnetic interactions for multiple platforms, sensors, and radiators in the battlespace engagement scene is therefore, of immediate interest. This is the generalized electromagnetic environment effects (E^3) problem to be solved.

The E^3 problem is concerned with self-generated electromagnetic interference (EMI) and the effects of incident energy on systems due to jammers. The electromagnetic environments are comprised of continuous wave (CW) signals, broadband modulation noise, harmonics, nonlinear frequency components, average as well as non-average (i.e., time-domain) power signals, and filter impulse noise generated in RF receivers due to incident interference. Co-located spread spectrum frequency hopping transceivers operating simultaneously, for example, can produce such composite electromagnetic environments. This environment may adversely impact the operation of the co-located transceivers and cor-

978-1-4244-6307-7/10/$26.00 ©2010 IEEE

rupt signal information integrity. Spread spectrum radios are being installed on many advanced military platforms. These include UAVs and their ground-based command, control, communications, computers, and intelligence (C^4I) counterparts that communicate. These, in turn, communicate with a variety of other aerial/avionics and global broadcast systems, and RF links utilizing mobile military radios, personal communications systems, and so on. Of immediate concern is the efficient management of interference interactions and effects for a collection of co-located transceivers mounted on UAVs. Computer modeling and simulation is one means of achieving this. Effect of nonlinearities on the performance of spread spectrum communications systems are analyzed in detail and demonstrated by means of computer simulations by Demirkiran, Weiner, and Drozd [1].

The goal of the computer modeling and simulation task is to assure overall EMC, operability, and availability of systems and electronics packages in their intended mission environment(s). The ultimate objective is to maintain Air Force information dominance in the tactical theater as well as over the global grid. Efficient management of the EMC problem for a complex system is not readily or easily achieved with a high degree of condolence based on the present state of available E^3 analysis and prediction tools, although a few exceptions can be cited depending on the type of problem to be solved and the accuracy desired. Moreover, to perform a comprehensive analysis requires the joint application of several diverse tools and techniques in order to obtain complete, meaningful predictions. Further, top-down and bottoms-up modeling approaches are often required involving an iterative, building block approach as part of the computer modeling task. Collectively, these considerations can exacerbate the modeling and simulation task. If not approached cautiously, numerical inaccuracies and/or misinterpretations may arise which could defeat the purpose of the detailed analysis task.

II. SPREAD SPECTRUM ENVIRONMENT AND PLATFORM-DEVELOPMENT SCENARIOS

Spread spectrum communications systems send and receive both coded voice modulated RF signals and digital pulse information. Consequently, a spread spectrum transceiver is both an emitter and a receptor of electromagnetic energy. As indicated above, the problem scenario of immediate concern involves the co-location of a large suite of these electromagnetic transceivers on UAVs. The spread spectrum transceivers must be able to communicate in the presence of each other, on a non-interference basis, with similar systems located external to the UAV platform. The UAV functions as an inexpensive ”surrogate” host relaying spread spectrum coded information to/from other ”nodes” in a communications network. While it is primarily used for military airspace dynamic information exchange purposes, it can provide satellite broadcast services to alliance and third-world countries which cannot afford to install a dedicated information exchange infrastructure. It can also provide a key ”mobile battlefield internet” link to support various types of information exchanges or for communications purposes. In particular, UAVs are being deployed to provide a useful link to facilitate communications among other assets or systems located within or over the military battlespace. A typical deployment scenario involves the UAV circling over the battlespace area for extended time periods to provide range extension and act as a cross-link relay for ground/air mobile radios, cellular and personal communications systems used in the vicinity of the fly zone [2].

The UAVs are populated with advanced electronics systems that are used to communicate with corresponding ground-based and airborne assets. These systems include the Army’s Single Channel Ground-to-Air Radio System (SINCGARS) radios and other spread spectrum, frequency hopping transceivers. Thus, the E^3 associated with the UAVs and assuring information integrity are of major concern. Spread spectrum systems mounted on these UAVs are not normally intended to communicate with each other over any given hop cycle. Again, these systems send and receive voice or data signals to/from ground stations and for other airspace vehicles. A collection of pseudo-random frequency hoppers produces a very complex electromagnetic environment which in general, is comprised of CW and wideband modulation noise, nonlinear signals (e.g., receiver and transmitter intermodulation, crossmodulation products, etc.), and harmonics thereof including noise impulse responses in RF receiver front-end filter stages. Undesired coupling of signals produced by these co-located spread spectrum frequency hopping systems may compromise information integrity and desired signal processes between intentional communications nodes. Preserving the operation and information dominance roles of the UAVs are of extreme importance.

The complex and random nature of this problem presents a challenge to the system designer and EMC analyst. The computer modeling and simulation task for this type of problem is a formidable undertaking. To address this, a knowledge base approach was developed, by ANDRO Computational Solutions, LLC, Rome, NY, implemented as a state-of-the-art pre/post-processor called E^3EXPERT [2].

III. KNOWLEDGE-BASED INTERFERENCE CANCELATION

The successful design of a complex electronic system working in a congested EM environment constitutes a formidable task. Even after careful positioning of emitters

and receptors and judicious frequency assignments, it is likely that unintended signals capable of causing interference will be present at one or more receptor ports. In such situations, successful operation depends upon effective employment of interference rejection techniques. Although a variety of techniques for suppressing interference is found in the literature, no single scheme is effective for all possible interference types [2,3]. When complete information regarding the interference is unavailable, our expert system approach provides the receptor with a knowledge-based capability to monitor the environment and determine the interference process along with all necessary parameters. Based on a set of expert system rules, the knowledge-based processor selects one or more suitable interference rejection schemes. The selection is made from a library of preselected techniques. In effect, the system reacts to the electromagnetic interference environment so as to maximize performance. This approach is illustrated by the following example which was simulated using the Signal Processing Work (SPW) software package.

Example # 1: The interference to a direct sequence spread spectrum receiver is an ON-OFF frequency hopped sinusoidal carrier whose frequencies and transition times are chosen randomly. As shown in Fig. 1 (S4), the interference is sufficiently large such that significant errors occur in the decoded message stream. The details of the interference were assumed to be unknown at the receiver input. However, as shown in Fig. 2, the knowledge-based monitoring system used a power estimator/comparator to determine when the interference was ON and an Fast Fourier Transform (FFT) to estimate the value of the jammer frequency during each ON interval. Based on expert system rules, the knowledge-based processor decided to reject the interference by inserting during each ON interval a simple notch filter whose center frequency tracked that of the interferer. When the interferer was OFF, the notch filter was bypassed and the received signal was fed directly to the demodulator. As seen Fig. 1 (S1) and (S3), the interference rejection scheme resulted in a significantly low bit error rate at the demodulator output.

An expert system is needed to monitor the environment and take action on what is learned. One candidate for this purpose is the Integrated Processing and Understanding of Signals (IPUS) expert system which was developed with support from Rome Laboratory by Victor Lesser of the University of Massachusetts and Hamid Nawab of Boston University. IPUS is intended for applications where uncertainties exist about the signal environment [2,3,4]. When the environment is unknown, attempts at measuring properties and/or parameters of signals can result in distorted outputs. For example, use of an FFT with inadequate resolution will result in the incorrect detection of two signals that are closely

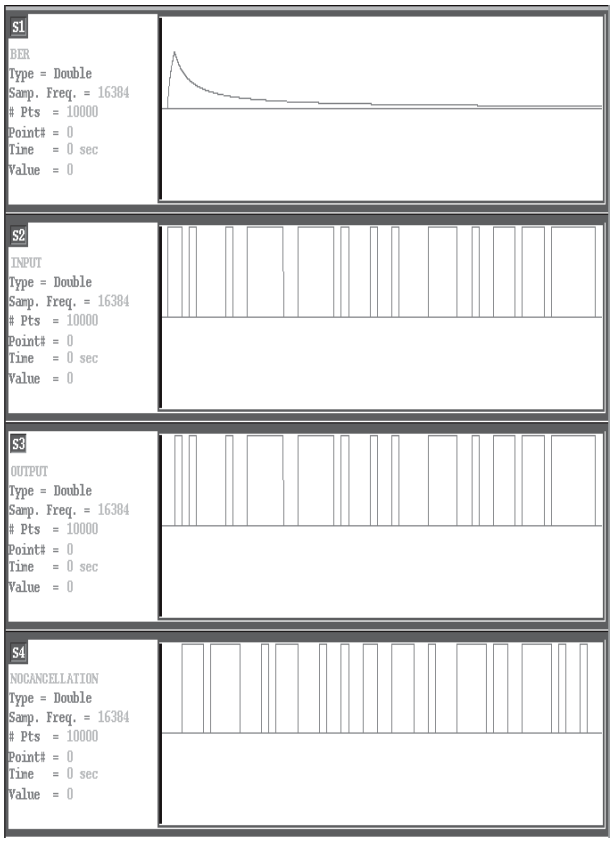


Fig. 1. S1:Cumulative Bit error rate with interference rejection, S2:Input message data, S3: Output data with interference rejection, and S4:Output message data without interference rejection.

spaced-in frequency as a single signal. Use of an amplifier with inadequate dynamic range will result in distortion of a strong signal due to nonlinear effects. Use of a receiver with inadequate bandwidth will result in distortion of a signal whose spectrum is wider than the receiver bandwidth. Nevertheless, traditional signal processing systems typically accept measured signals without questioning whether or not they may have been distorted by the front-end stages of the receiver. IPUS not only allows the receiver to interpret the essential characteristics of monitored signals, but also recognizes when uncertainties and/or distortions exist and reprocesses the monitored signals so as to reduce the uncertainties and/or distortions [3]. IPUS achieves its objective by detecting one or more of the three kinds of discrepancies defined below:

- **Violation:** A violation occurs when a monitored signal is identified as having characteristics different from those included in the class of possible signals chosen a prion for the application domain. For example, assume that only linear and sinusoidal modulations appear in the application domain for frequency modulated signals. A violation occurs when an FM signal is detected whose

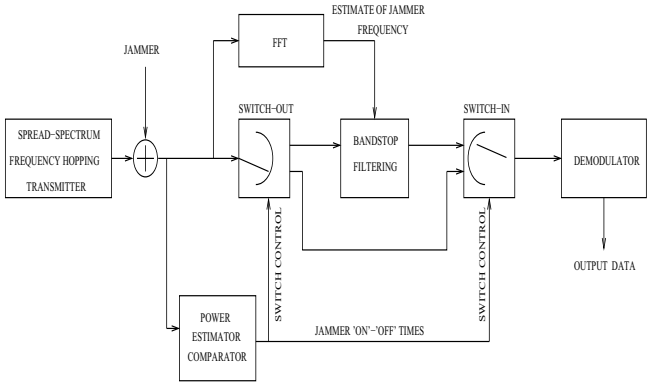


Fig. 2. Block diagram of knowledge-based intereference rejection system.

modulation appears to be neither linear or sinusoidal.

- **Conflict:** As PUS monitors signals in a particular time interval, various expectations are created for the next time interval. For example, suppose that CW interferers with frequencies at 208 MHz and 274 MHz were detected in previous time intervals. If data in the current time interval is observed to contain only a single CW interferer with a frequency of 274 MHz, a conflict is declared.
- **Fault :** A fault occurs when two different signal processing algorithms applied to the same observed data result in different conclusions. For example, suppose that a wavelet analyzer and a short-time Fourier Transform are both used to process the monitored data. A fault results should the wavelet analyzer indicate the presence of a signal in a particular time- frequency bin, but the short-time Fourier Transform does not.

Once discrepancies are detected, IPUS selects strategies to reprocess the data by changing the parameters of the signal processing algorithms and/or selecting new algorithms. The process iterates until interpretations have been generated that resolve the discrepancies. This approach is well suited to determining the characteristics of incompletely known interfering signals. The IPUS-based strategy relies on an iterative procedure guided by local and global constraints on the time-frequency characteristics of the narrow-band interference signals. This procedure, which is outlined in Fig. 3, begins by predicting the time-frequency evolution of narrow-band interference signals from the previous processing segment to the current one. The bandwidths of the analysis filters in a uniform filterbank are then adjusted on the basis of the predicted narrow-band interference. An iteration in the adaptation procedure commences with the processing of the signal data in the current analysis interval using the adjusted filterbank. Spectral peaks are picked from the output and fed to a Kalman tracker [5] that hypothesizes time-frequency trajectories corresponding to partials. We refer to these trajectories as ”tracks”. Discrepancy detection is carried out in order to search for ”distortions” that cause mismatches between the predictions and the tracks. Examples of such distortions include the absence of a track where one has been predicted and mismatch in frequency modulation rates between a prediction and a corresponding track. Following discrepancy detection, the identified distortions are explained through a process of discrepancy diagnosis. The diagnostic process is aided by knowledge regarding the possible time-frequency interactions between narrow-band interference signals. We were able to determine these interactions by means of a thorough analysis of all possible scenarios with the types of jammers considered in our research. Time- frequency information extracted from the data, such as the frequency modulation rate and the on-time of ON-OFF jammers, are utilized within diagnosis to identify the relevant interactions within the current signal context. The identified interactions form the basis for attributing causes such as low frequency resolution and low time resolution to the distortions in the processed data. A set of reprocessing plans are then retrieved for removing each distortion by erasing its causes. Execution of the reprocessing plans result in an adaptation of the analysis filters and also (if necessary) a refinement of predictions in the current processing interval. This leads to the end of an iteration in our knowledge-based strategy. Reprocessing of the data followed by the formation of fresh tracks marks the start of the new iteration. The iterative procedure involving discrepancy detection, discrepancy diagnosis, reprocessing planning, and reprocessing is repeated until all distortions are either eliminated or an iteration limit is reached. Problem-solving in an IPUS-based system takes place on a data blackboard which is operated upon by a variety of knowledge sources. It is implemented in the C++ environment which provides a convenient facility for developing IPUS applications. IPUS could also be used to simplify the implementation of computational EM codes and to improve interpretation of their results. For example, one could be the analysis of a complex EM problem using a minimal number of patches and/or wires and, with the aid of IPUS to resolve discrepancies, increase the complexity only as needed. Similarly, the same problem could be analyzed using two different analytical approaches and by resolving discrepancies with IPUS, iterate the software to converge on the correct interpretation. The above discussion focused on situations where incomplete information is available concerning the interference. Even when the interference is completely known at the receptor, the knowledge-based processor can be used to select an appropriate interference rejection scheme. This is illustrated by the following example.

Example #2: To illustrate the performance of our system, we provide the simulation results for a scenario consisting of

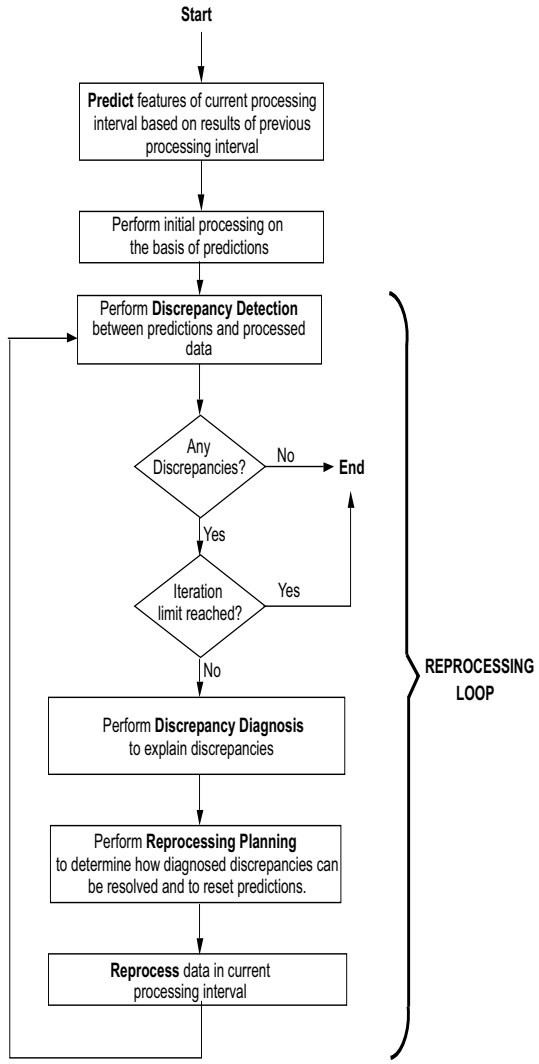


Fig. 3. IPUS model.

four linear chirp interfering signals contaminating the transmitted spread-spectrum signal. Each linear chirp contributes an interfering signal power of approximately 30 dB over the interfering signal power that can be handled by the system processing gain. Upon analyzing the received interference corrupted data, the IPUS-based interference isolation stage indicated the presence of four linear chirp interferers and provided time-frequency tracks for each interfering chirp. In Fig. 4, we show time-frequency tracks corresponding to one of the linear chirp signals. The frequency estimates are then used to adaptively control the center frequency of bandstop filters. The frequency location and time profile of each interferer are updated every 16 samples in order to avoid having to adjust the bandstop filter parameters too frequently. The error, introduced by updating the frequency estimates every 16 samples, is compensated by adjusting the stopband of the bandstop filters. In Fig. 5, we show the bit error rates obtained by our cancellation scheme and the bit error rate resulting from employing a Least Mean Squared (LMS) adaptive filter of order 20 with an error-signal formed to estimate and cancel the narrowband interference [3]. We see, by utilizing our approach, that we achieve a bit error rate which is about one fifth of the bit error rate achieved using the transversal filter.

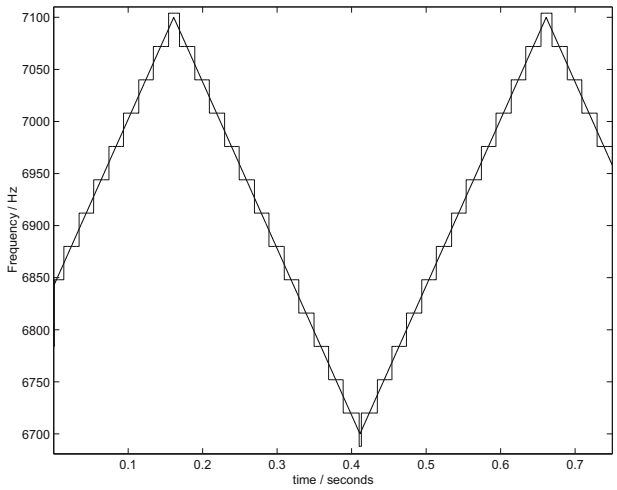


Fig. 4. Actual and Estimated Time-Frequency Track of One LFM Jammer

IV. SUMMARY AND CONCLUSIONS

We have presented a knowledge-based approach to interference rejection for EMC. IPUS is employed to monitor the signal environment so as to identify individual interfering signals and their pertinent parameters. The time-frequency tracks corresponding to the isolated interferers are utilized in a subsequent cancelation stage to adapt notch filters for

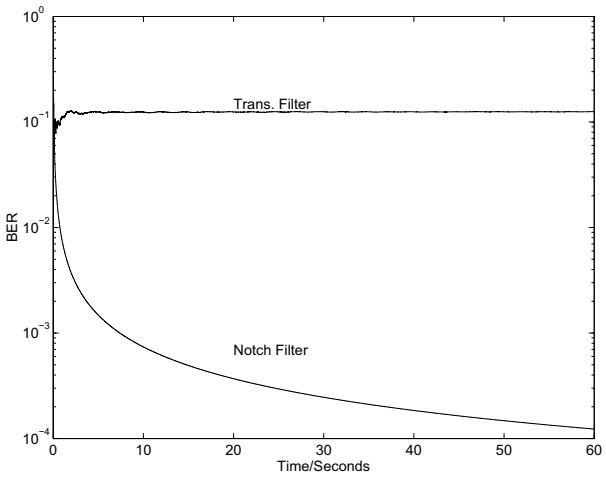


Fig. 5. Performance Comparison

removing the interference. SPW simulations conducted on a prototype Direct Sequence Spread Spectrum (DSSS) system have demonstrated the superiority of our knowledge-based interference rejection scheme over conventional interference rejection schemes in terms of both bit error rate performance and reduction in receiver design complexity.

REFERENCES

[1] I. Demirkiran, D. D. Weiner, and A. L. Drozd, 'Effect of In-band Intermodulation Interference on Direct-Sequence Spread Spectrum (DSSS) Communication Systems for electromagnetically Diverse Applications', IEEE International Symposium on EMC, Hawaii, July 2007.

[2] A. L. Drozd, C. E. Carroll, J. R. Miller, D. D. Weiner, P. K. varhsney, and I. Demirkiran, 'ANDROS's Electrimagnetc Enviromental Effect Expert Processor with Embedded reasoning tasker (AE3EXPERT)', AF97-043 CLIN003 Final Technical report , US Air Force Research Laboratory Information Directorate Rome Research Site, Rome, New York, March 1998.

[3] P. K. Varshney, D. D. Weiner, S. H. Nawab, I. Demirkiran, and V. N. Samarasooriya, 'A Knowledge-Based Interference Rejection Scheme for Direct-Sequence Spread-Spectrum Systems', AFRL-IF-RS-TR-1999-53 Final Technical Report US Air Force Research Laboratory Information Directorate Rome Research Site, Rome, New York, March 1999.

[4] V. R. Lesser, S . H. Nawab, and F. I. Klassner, 'IPUS: An Archtecture for the Integrated Processing and Understanding of Signals', Artificial Intelligence, vol. 77, pp. 129-171, 1995.

[5] Y. Bar-Shalom and T. E. Fortmann, 'Tracking and Data Association', Academic Press, 1988.

New Insights on Loop Radiation Efficiency

Dheena Moongilan
Bell Laboratories, Alcatel-Lucent
Murray Hill, NJ 07974
Dheena.Moongilan@alcatel-lucent.com

***Abstract*-Circuit loop area reduction is a frequently used EMC technique for minimizing differential mode current radiations and improving the overall immunity of products from electrical noise. The efficiency characteristics of loop radiation are studied and new facts on loop radiation are described. The relationship of the radiation amplitude efficiency and frequency of the first radiation-peak with the size and shape of the loop area is explained. A mathematical model is presented for calculating radiations first peak and its frequency from the loop area. The effect of loop area shape on peak radiation frequency is experimentally verified. Experimental data is also provided to demonstrate that the radiation amplitude efficiency peak shifts to higher frequencies when the loop area is minimized.**

I. INTRODUCTION

The loop area is an important parameter that must be controlled in every EMC design to reduce radiated emission levels and improve the overall electrical immunity of products. Circuits with a large loop area not only radiate higher field levels but also act as a more effective receptor of unwanted noise. Cost effective EMC design typically requires that the loop area of all sensitive circuits must be reduced as far as practicable before applying other interference reduction techniques. Unlike antenna designers, EMC designers must consider the numerous shapes and sizes that form the circuit's loop area. The properties of loop areas are generally derived for circular and square shapes and there is very little published literature available for other loop area shapes. The circular or square loops are usually classified as either electrically small or large based on the loop circumference or perimeter wavelength. Any circular loop that has a circumference less than $\lambda/10$ is considered a small loop while any loop that has a circumference greater than λ is considered a large loop. For any small loop, the circular and square loop radiation characteristics are similar.

The loop radiation efficiency (R_η) is defined as "the ratio of total RF power radiated and net RF power input accepted by the loop". The value of R_η is generally measured in dB. The far field radiated by electrically small loops is proportional to the loop area and the square of the frequency [1]. Hence, R_η can be derived from the loop area and the square of the frequency. In this paper resulting R_η values measured in a GTEM are presented for circular, square and rectangular shaped loops. The loop radiation characteristics based on shape, area and frequency are discussed as well. In addition, the relationship between the loop radiation peak harmonics amplitudes and its corresponding occurring frequency and the loop area is investigated. Based on R_η a mathematical equation is provided for calculating the frequency of the first peak amplitude and occurring loop area.

Key Assumptions:
In this work, it is assumed that loops do not form a transmission line. This implies that the capacitance between any loop conductors is negligible. The words "perimeter", "loop length" and "circumference" are interchangeably used.

II. THEORY

If the perimeter of the loop is very small as compared to the wavelength of interest and the loop is excited by a differential mode current, a uniform in-phase current flows on the loop. Generally, when the loop circumference or perimeter approaches $\lambda/12$, some of the current will be out-of-phase [2]. For each point in a loop (at any frequency), there is a diametrically opposite point in which the current flow is in the opposite direction [3]. Therefore certain radiated fields from these points cancel.

Radiation efficiency (R_η) and Radiation Resistance (R_r): The R_η of an antenna is defined as a function of radiation resistance (R_r) and the sum of the losses in the antenna (R_ℓ).

$$R_\eta = R_r/(R_r + R_\ell) \quad \text{..... (1)}$$

Equation (1) can be rewritten as

$$R_\eta = 1/(1 + (R_\ell/R_r))$$

When R_ℓ/R_r is large, $R_\eta = R_r/R_\ell$. …….(2)

Loss Resistance (R_ℓ): Any radiator can be modeled as an antenna. The primary contributors to R_ℓ are the loop resistance (ohmic) loss, the loop inductance and the loop mismatch. The ohmic losses are proportional to the loop length (ℓ) and are inversely proportional to skin-depth. The skin depth is inversely proportional to the square root of frequency ($\sqrt{f}$) and this value is lower for high frequencies therefore there is higher resistive loss at higher frequencies. The net loop inductance is dependent on the loop shape. It is proportional to the loop area, and inversely proportional to the loop length. For similar loop shapes, the self and mutual inductance will be proportional. If the loops are small, the net loop inductance will be a constant ratio. Since R_r is typically low ($< 3\Omega$) for small loops, then the loop mismatch variations can be ignored for the cases where the input power is from a 50 ohm source [4] or higher.

Current flow in Small loops: When small loops are examined at low frequencies, the current flow is uniform and it is in-phase. The frequency at which the out of phase current flow commences is dependent on the loop shape and its area. In smaller area loops, the out-of-phase current appears at a

978-1-4244-6307-7/10/$26.00 ©2010 IEEE

higher frequency while in larger area loops the out-of-phase current appears at a lower frequency. Ampere circuital law states that the line integral of field intensity (H) about any closed path is exactly equal to the forward current (I) enclosed by the path (L). This law apparently applies to loops having uniform and symmetrical current [5].

$$\oint \boldsymbol{H}.d\boldsymbol{L} = \boldsymbol{I} \quad \ldots\ldots (3)$$

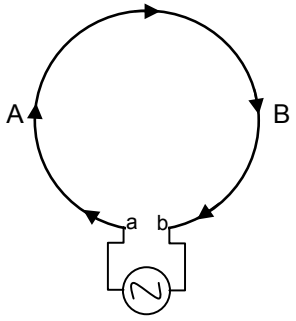


Figure 1 - Current flow in a short loop.

Applying Ampere's circuit law for a circular loop shown in Figure 1 gives the field intensity produced at any point 'A' in the loop perimeter. There is a corresponding point 'B' in the loop perimeter in which the field intensity is equal but in the opposite direction to the field produced by point 'A'. At any specific low frequency, the net field radiated by the loop is proportional to loop area and inversely proportional to the proximity of points A and B [1]. Hence, the radiated fields cancel effectively if points A and B are very close.

First peak amplitude Frequency: The radiation amplitude of any loop increases with increasing frequency until it reaches its peak; beyond this frequency the amplitude falls. At this frequency the out-of-phase current flow commences with a decreasing in the value of R_η. Subsequent increases in frequency causes in-phase or out-of-phase currents depending upon the loop area. Therefore, the radiation field vectors either add or subtract depending on the phase angles of the current around the loop. This causes several very distinct peaks and valleys in R_η. Let us call the first transition point of R_η as the "first peak amplitude frequency" and subsequent peaks as harmonic peaks. The first peak amplitude frequency is also a "transition point for Ampere's circuital law" beyond which the current distribution on the loop is no longer symmetrical. For the same loop shape, while the first peak occurs at a lower frequency for larger loops and at a higher frequency for smaller loops, the loop radiation efficiency is unchanged. The loop radiation efficiency follows a linear to logarithmic transition up to the first peak, so the calculation of R_η is trivial to that point. However, after the transition of the first peak, R_η cannot be established using trivial mathematical equations. The R_η calculation is provided in several references.

The R_r *and GTEM Radiation:* The R_r of equation (2) is derived from the total average radiated as far field power where the angular phase difference of power between any radius from the antenna is considered negligible. In a GTEM, the radiated power (P) is measured at the apex (see Figure 3) $= (E \times h)^2/R$

Where h is the septum height,

E is the electric field, and R is the 50Ω GTEM termination.

The GTEM provides an accurate representation of maximum field levels, even though the angular phase differences of the radiated field from any point on the loop is certainly not negligible. Therefore, when deriving R_r it is appropriate to consider the radiated field levels rather than the total radiated power. A simplified equivalent circuit of a Loop in a GTEM is shown in Figure 2. From Figure 2, the loop current $i = \boldsymbol{v}/R_\ell = e/R_r$

Therefore, $R_r/R_\ell = e/\boldsymbol{v}$ …. (4)

But 'e' is proportional to the electric field 'E × h'. If 'h', the septum height, is constant, then 'e' is proportional to 'E'.

According to reference [1] 'E' is proportional to (A/λ^2) … (5)

Where λ is the wavelength of the loop's input power in meters and A is the loop area in m^2.

Surface Resistivity (R_s*):* The Surface Resistivity, R_s, of an electrically conductive material increases with the conductor length ($\boldsymbol{\ell}$) and the square root of frequency ($\sqrt{f}$). Small loops are normally made from short length of conductors (less resistance) while large loops are made from longer conductors with higher resistance. Since the first peak frequency occurs at a higher frequency for short loops, then short loops operating at higher frequencies will have relatively higher losses due to skin effect. For large loops, with lower first peak frequency, the resistive loss due to skin-effect will be less [6]. The overall effect results in the surface resistivity of both short and long loops to be essentially the same order of magnitude. However, for an accurate estimation of R_η the ohmic losses must also be considered.

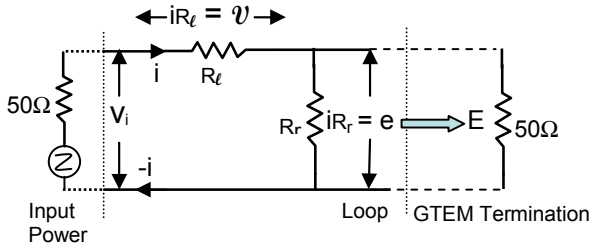


Figure 2- Simplified Equivalent Circuit of a Loop in GTEM

Loop Area (A) and First Peak Amplitude Frequency: If R_η of two loops are equal, then the following relationships can be deduced from Equation (2), (4) and (5).

$(A_1/\lambda_1^2)/ R_{\ell 1} = (A_2/\lambda_2^2)/ R_{\ell 2} = k_1$ (constant) …. (6)

Recall that R_ℓ is proportional to R_s which is proportional [7] to the loop perimeter ($\boldsymbol{\ell}$) and ($\sqrt{f}$).

Substituting $\boldsymbol{\ell}$ and $\sqrt{f}$ in (6) and taking the logarithm on both sides results in:

$\log_{10} (A_1/(\lambda_1^2\, \boldsymbol{\ell}_1\, f_1^{½})) = \log_{10} (A_2/(\lambda_2^2\, \boldsymbol{\ell}_2\, f_2^{½})) = \log k_1$

The experiments show that loops of the same shape produce equal R_η at the first peak amplitude frequency; however the occurring frequency of these peaks changes with loop area.

Therefore for any loop shape and its first peak amplitude, the generalized equation will be

$= \log_{10} (A_1/(\lambda_1^2\, \ell_1 f_1^{½})) = \log_{10} (A_2/(\lambda_2^2\, \ell_2\, f_2^{½})) =$

$\log_{10} (A_3/(\lambda_3^2\, \ell_3\, f_3^{½})) \ldots\ldots = \log_{10} (A_n/(\lambda_n^2\, \ell_n\, f_n^{½})) = k$ … (7)

Therefore,

$\log_{10} A - 2 \log_{10} \lambda - \log_{10} \ell - ½ \log_{10} f = k$

Rewriting with frequency f in MHz units to wavelength λ in cm units yields:

$\log_{10} A - 2 \log_{10} \lambda - \log_{10} \ell + ½ \log_{10} \lambda - ½ \log_{10} 30{,}000 = k$

$= \log_{10} A - 1.5 \log_{10} \lambda - \log_{10} \ell - ½ \log_{10} 30{,}000 = k$ ….. (8)

If the constant (k) is determined, the relationship between loop area (A), first peak amplitude wavelength (λ) and the loop perimeter (ℓ) can easily be calculated. Furthermore the equation can be reduced to simple two variable (A and λ) equations for simple loop shapes by translating length ℓ in terms of area.

Circular loops:

$½ \log_{10} A - 1.5 \log_{10} \lambda - 2.78816 = k_c$ ……. (9)

Square loops:

$½ \log_{10} A - 1.5 \log_{10} \lambda - 2.8406 = k_s$ ……. (10)

Rectangular loops:

When the length (L) >> width (w), then the perimeter is 2L, and

$\log_{10} w - 1.5 \log_{10} \lambda - 2.53956 = kr$ …… (11)

III. EXPERIMENTAL VERIFICATION AND PREDICTIONS

Radiated emissions tests were performed in a 75cm high septum to bottom ground plane GTEM using a Network Analyzer. The Network Analyzer was calibrated before use. The calibration procedure adjusts the measured amplitude readings of the cable losses of the Network Analyzer to the GTEM. Each of the test loops was attached to a 50Ω BNC connector with one end of the loop connected to the center pin and the other end to the connector shell. The output port of the Network Analyzer was connected to the test sample loop that was attached to BNC connector and the other port was connected to the apex of the GTEM. The test setup is shown in Figure 3. A reasonable input power level (0 or 5dBm) was selected from the Network Analyzer. The test loop samples were rotated in their upright position so that the maximum reading was recorded on the Network Analyzer. Generally the maximum readings were observed when the plane of the loop is placed perpendicular to the length of the septum (see Figure 3) and parallel to the side ground planes. The radiation efficiency, the difference between GTEM radiated emissions and the Network Analyzer input power level is plotted in dB (Graphs 1 to 9). The test sample loop areas were selected such that influence of the sample connectors was very low. Similarly, excessively large area samples were avoided to facilitate accurate measurements at higher frequencies. All test loop samples were made from 30AWG Litz wire.

The following configurations were tested:

1. Circular loops: Three loops having areas of 100cm^2, 50cm^2, and 10cm^2
2. Square loops: Three loops having loop areas of 79.2cm^2 (8.9cm x 8.9cm), 39.7cm^2 (6.3cm x 6.3cm) and 7.8 cm^2 (2.8cm x 2.8cm). The square loops are constructed from the same length of wire used in circular loops.
3. Rectangular loops: Two loops having loop areas of 16.7cm^2 (16.7cm x 1cm) and 1.7cm^2 (5.3cm x 0.32cm). The length and width ratio of loops are approximately equal.

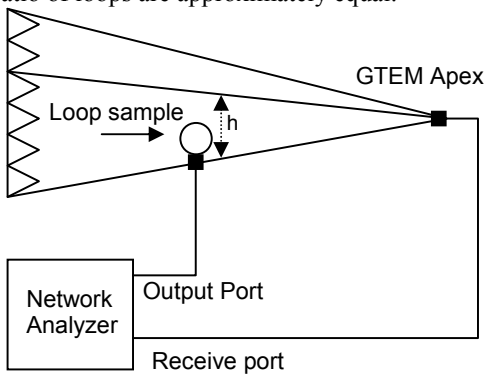


Figure 3 - Test Measurement setup in GTEM

IV. RESULTS

The Graphs 1, 2, and 3 provide plots of radiation loop efficiency for 100cm^2, 50cm^2, and 10cm^2 circular loops. Graphs 4, 5 and 6 provide radiation loop efficiency plots for 79.2cm^2 (8.9cm x 8.9cm), 39.7cm^2 (6.3cm x 6.3cm) and 7.8 cm^2 (2.8cm x 2.8cm) square loops. Graphs 7 and 8 provide radiation loop efficiency plots for 16.7cm^2 (16.7cm x 1cm) and 1.7cm^2 (5.3cm x 0.32cm) rectangular loops. For Graphs 1 and 4, a 35.5cm long wire was used. For Graphs 2 and 5, a 25.2cm long wire was used. For Graphs 3 and 6, an 11.2cm long wire was used. Table 1 summarizes first peak amplitude frequencies and loop efficiencies. As can be seen from Table 1, the loop efficiencies are almost equal for loops of same shape but their occurring frequencies are different.

TABLE 1: LOOP SHAPE, AREA AND LOOP EFFICIENCY AT THE FIRST PEAK FREQUENCY

Loop Shape	Graph No	Loop Area cm^2	First Peak Frequency MHz	λ cm	Loop Efficiency dB
Circular	1	100.0	87.1	344.4	-39.3
	2	50.0	107.4	280.0	-39.7
	3	10.0	176.6	169.9	-39.2
Square	4	79.2	88.8	337.8	-38.2
	5	39.7	109.6	275.2	-38.5
	6	7.8	179.4	167.2	-38.3
Rectangle	7	16.7	104.7	286.6	-37.7
	8	1.7	207.6	144.5	-38.0

The author has verified several other loop areas and obtained the same relationship. Table 2 summarizes the logarithmic relationship between loop area and wavelength of the first peak. The last column in Table 2 shows the logarithmic relationship between loop area, loop perimeter and wavelength of the first peak varies depending upon the loop shape. The loop area indicated in the Table 2 is less than the

actual values because the loop area formed by the test sample connections (area below 'a b' of Figure 1) to the BNC connectors is not included. This "additional" loop area influences the test results when the actual loop area is small. This also prevents testing of much smaller loop areas. The last column of Table 2, provide approximate values of constants k for Equation 8. From this value Equations 9, 10 and 12 are rewritten as Equations 12, 13 and 14. For all practical purposes, the approximate relationships (Equation 12, 13, and 14) provide good agreement when other loops and shapes tested. However for loop area less than 0.5 cm^2, the test loop terminal connection area must be accounted for in order to achieve accurate results.

TABLE 2: LOOP SHAPE, LOGARITHMIC RELATIONSHIP OF LOOP AREA (A) AND FIRST PEAK FREQUENCY WAVELENGTH

Loop Shape	Loop Area (A)		First Peak Frequency		Loop Perimeter	log (A)- 1.5 log λ – log ℓ
	A cm^2	log A log-cm^2 (1)	MHz	1.5 log λ (2)	(log ℓ) (3)	- ½ log (30000)= (1) –(2)–(3)–2.2386
Circular	100.0	2.0	87.1	3.80	1.55	-5.59
	50.0	1.7	107.4	3.67	1.40	-5.61
	10.0	1.0	176.6	3.35	1.05	-5.63
Square	79.2	1.89	88.8	3.79	1.55	-5.68
	39.7	1.59	109.6	3.66	1.40	-5.72
	7.8	0.89	179.4	3.33	1.05	-5.73
Rectangle	16.7	1.22	104.7	3.69	1.55	-6.26
	1.7	0.23	207.6	3.24	1.05	-6.29

Circular loops:

$$\tfrac{1}{2}\log_{10} A - 1.5\log_{10}\lambda = -2.80 \quad \text{..... (12)}$$

Square loops:

$$\tfrac{1}{2}\log_{10} A - 1.5\log_{10}\lambda = -2.84 \quad \text{.... (13)}$$

Rectangular loops, when length (L) >> width (w)

$$\log_{10} w - 1.5\log_{10}\lambda = -3.69 \quad \text{..... (14)}$$

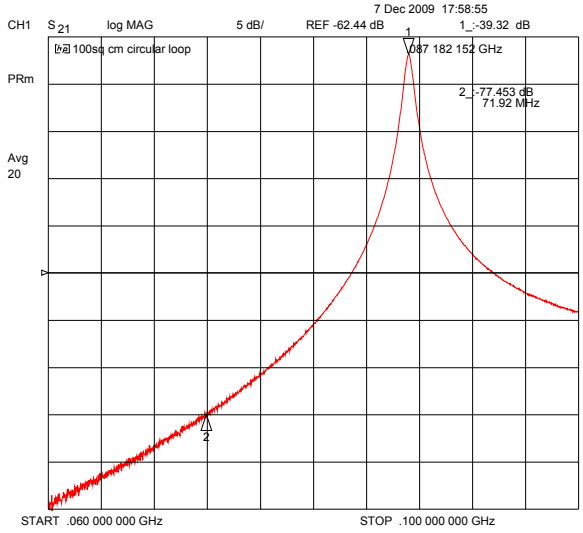
Where the loop area A is in cm^2.
The wavelength λ is in cm.
and the Loop width w is in cm.

There exists a frequency ratio relationship between similar loops at equal loop efficiency points. (Example: Graphs1 and 2, the ratio of first peak frequencies is 1.7 and the frequency ratio is same at other equal loop efficiency points).

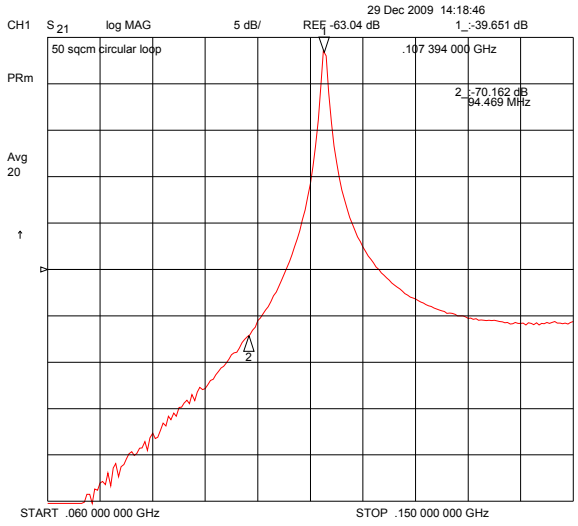
Graph 9 provides a plot of R_η up to 2GHz for a 79.2 cm^2 (8.9cm x 8.9cm) square loop. The plot indicates peaks at the harmonics of the first peak and also at some other peaks. It appears that there are other resonant frequencies present as well. The other resonant frequencies also appear to be lower when loop area is very large. When the loop area is very small, the capacitance formed between the connector and loop connecting location affects the results. The peak frequencies are not affected due to loop rotation in GTEM.

V. CONCLUSION

The results of Table-1 show that the first peak radiation efficiency amplitude occurs at different frequencies. When loop area is small, the first peak occurs at a higher frequency. For similar shape loops, the first peak amplitude is nearly constant and independent of loop area. Therefore, other conditions being equal, it's concluded that the loop radiations amplitude does not change with the loop area reduction but shifts the amplitude to a higher frequency. Also, there exists a frequency ratio relationship between similar loops at equal loop efficiency points. A comparison of Graph-9 and other Graphs shows that up to first peak, the modeling of the radiation efficiency amplitude is trivial; beyond the first peak a comprehensive modeling is required. The first peak is an indicator of the frequency transition point for in- phase to out-of-phase currents. The results of Table-2 demonstrate that existence of a logarithmic relationship between loop area and wavelength for the first peak radiation efficiency amplitude.



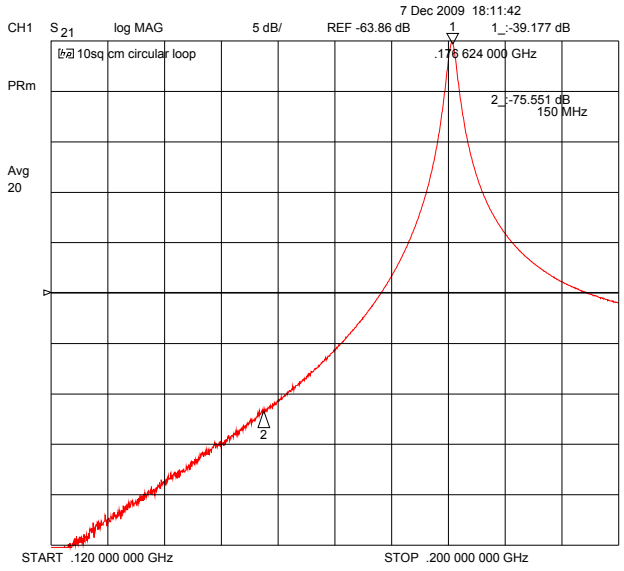
Graph-1: 100 Sq cm Circular Loop



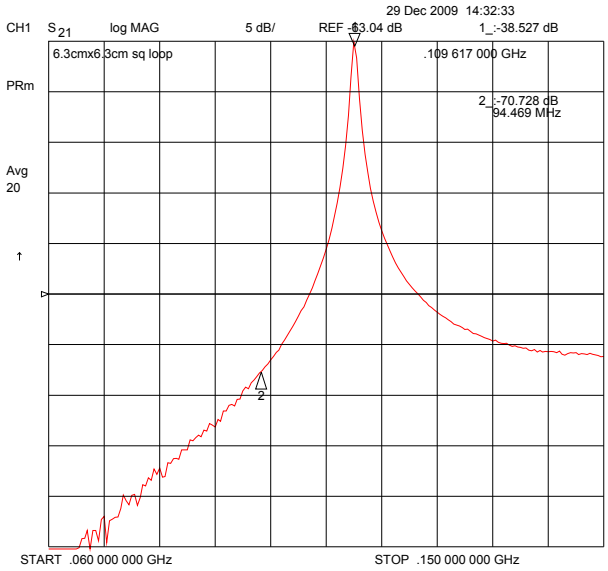
Graph-2: 50 Sq cm Circular Loop

REFERENCES

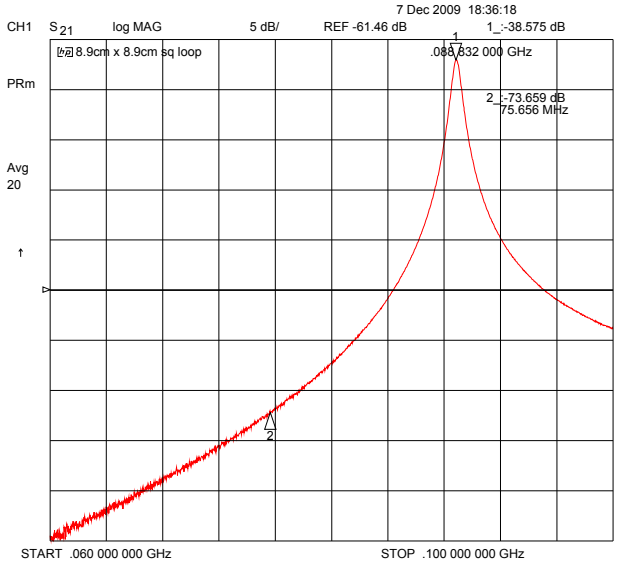
[1] J. D. Krauss, "Antennas", 2nd Ed, McGraw-Hill, 1988, pp 242-259.
[2] D. Moongilan " Radiation Characteristics of Short Unterminated Transmission Lines" 2009 IEEE International symposium on EMC, pp. 57 - 62
[3] J. R. Wait, "Electromagnetic radiation from cylindrical structures" Peter Peregrinus Ltd, London, UK 1998, pp182-184
[4] R. C. Johnson, "Antenna Engineering Handbook", 3rd Ed, McGraw-Hill, 1993, pp 5-3.
[5] S. Gartenhasus, "Physics Basic principles", Holt Rinehart and Winston, Inc., 1975 pp775.
[6] K. Fujimoto and J.R. James, "Mobile Antenna System Handbook", Artech House, Inc, 1994, pp-190.
[7] C. A.Balanis,"Modern Antenna Handbook", John Wiley &Sons Inc., 2008, pp 37.



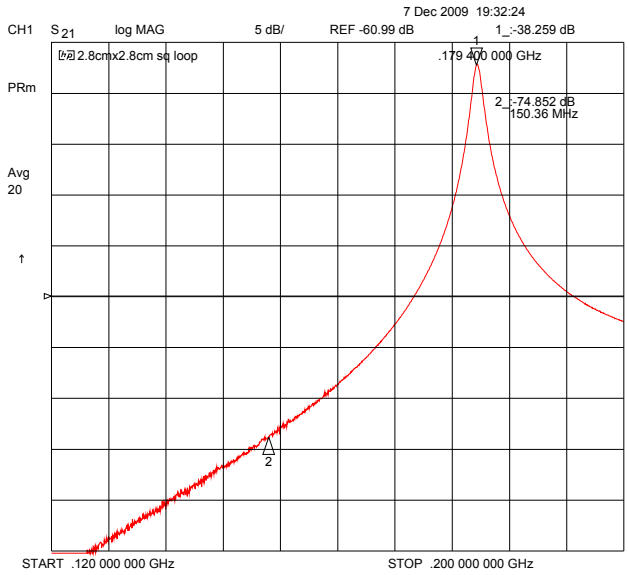
Graph-3: 10 Sq cm Circular Loop



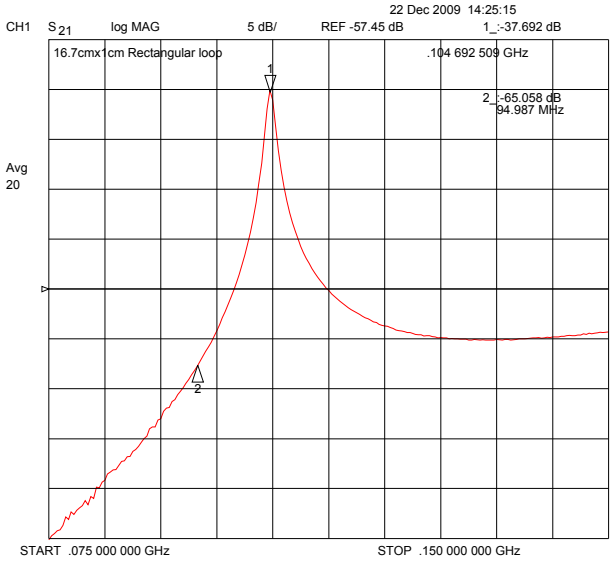
Graph -5: 39.7 Sq cm (6.3cm x 6.3cm) Square loop



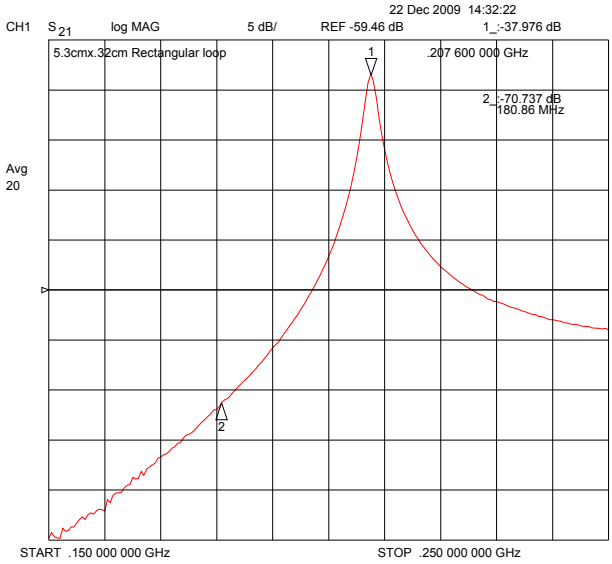
Graph -4: 79.2 Sq cm (8.9cm x 8.9cm) Square loop



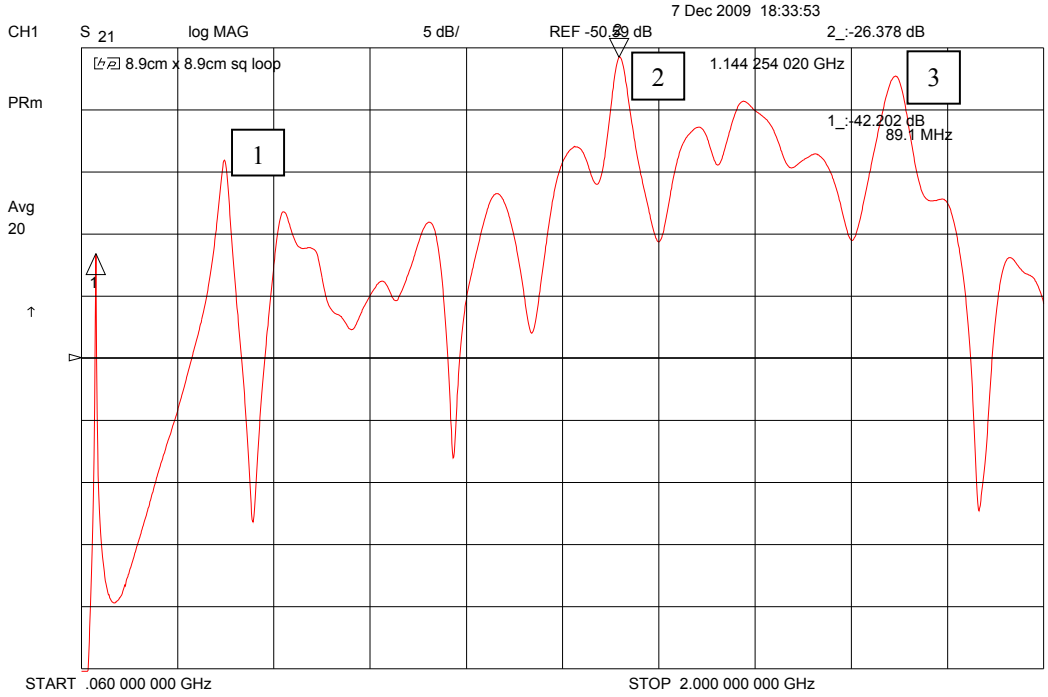
Graph -6: 7.8 Sq cm (2.8cm x 2.8cm) Square loop



Graph -7: 16.7 Sq cm (16.7cm x 1.0cm) Rectangular loop



Graph-8: 1.7 sq cm (5.3cm x 0.32cm) Rectangular loop



Notes: In the Graph (1) is 4th Harmonic, (2) is 13Th Harmonic and (3) is 19th Harmonic

Graph -9: 79.2 Sq cm (8.9cm x 8.9cm) Square loop showing Harmonic and Non-Harmonic Peaks

Polarization Extraction Through the Linear Component Method

J. A. Nascimento[#1], G. Fontgalland[#2], R. M. Valle[#3]

LEMA (Laboratory of Electromagnetism and Microwave Applied)

UFCG (Federal University of Campina Grande)

Campina Grande – Brazil

[1]jobson.nascimento@ee.ufcg.edu.br

[2]fontgalland@dee.ufcg.edu.br

[3]rvalle@dee.ufcg.edu.br

Abstract – In this article is proposed a measurement technique to the electromagnetic polarization for completely polarized waves, using the linear component method, in order to obtain the magnitude and phase of the radiated electric field by one or many sources. Through these parameters the characteristics of the electromagnetic wave emitted by antennas, including the type and miniaturized RFID, will be defined more precisely.

Index Terms – Electromagnetic polarization, electric field, electromagnetic interference, miniaturized antenna, RFID

I. INTRODUCTION

The importance of the study of new techniques to achieve the decrease of the damage caused by the electromagnetic interference (EMI) in electronic devices [1] and [2], has increased in the last few years. Through the study of electromagnetic waves polarization, we could identify the radiated electric field behavior.

The knowledge of the electric field amplitude and phase [3], allows us to identify the pattern of a polarized wave. Using the techniques of measuring the polarization, [4] and [5], we can find the unknown polarization of one or more sources. With the antenna polarization information, it is possible to determine the operation efficiency and others parameters.

The most used equipment measure the electric magnitude field only. Therefore but the way to characterize the electromagnetic wave is an effective tool, for it will provide the field phase as well, and therefore, the characteristics of the radiated electric field will be determined with more precision.

By knowing the electric field phase, it is possible to estimate more precisely the direction of the field and the part of the equipment that is under electromagnetic interference is more affected, intending to propose to the manufacturer solutions that will diminish the effects caused by the interference.

The necessity to reduce the physical size of devices, especially the antennas, is essential in many applications such as radar systems, mobile and RFID. Thus, the use of miniaturized antennas has been extensively studied because they also have low cost, low weight, are easy to manufacture, have formability, and are versatile in terms of resonance frequency and polarization [6] - [7].

The RFID application, very used recently, is utilized to identification of products, people and animals, monitoring the production process, product traceability, control of access, among others; an example is cited in [8]. The characteristics of this application, such as fault tolerance, real-time operation, security, robustness, operation without the need for physical contact, has made this a useful tool employed in several areas, such as tolls, medical applications and biometrics, access control, protection personnel, logistics, industrial assembly lines.

The polarization extraction is not an obvious task, since the dimensions of the antenna are much smaller than the wave length, and a conventional structure, in which the active circuit, irradiator and remaining parts of the circuit are integrated, wherefrom comes the importance of knowing the wave polarization in these antennas.

The methodology to measure amplitude and phase of the irradiated electric field, as well as

978-1-4244-6307-7/10/$26.00 ©2010 IEEE

the obtaining of complete polarization profile, as it can be seen in [9], is proposed in this article.

II. METHODOLOGY

The method of the linear component consists to fix two $\lambda/2$ dipoles separated by a $\lambda/2$ distance; so there will be no coupling among them. The dipoles are arranged in a right angle. The first dipole is in the horizontal plane and the second in the vertical plane, as shown in Fig. 1(a). The wave issued by the source is usually propagated to out of the page. The first part of the experiment consists in obtaining the axial ratio, which is defined as the ration between the axis, biggest and smallest of the polarization ellipsis.

Initially the receiver is connected to the dipole terminals in the vertical, and the amplitude of field E_1, showed by the electric field measurement equipment, is collected. Next, the receiver is connected, now in the dipole terminals in the horizontal, and the amplitude of the electric field E_2, is noted. Then, the axis ratio is found by the equation:

$$AR = \frac{E(greater\ axis)}{E(smaller\ axis)} \quad (1)$$

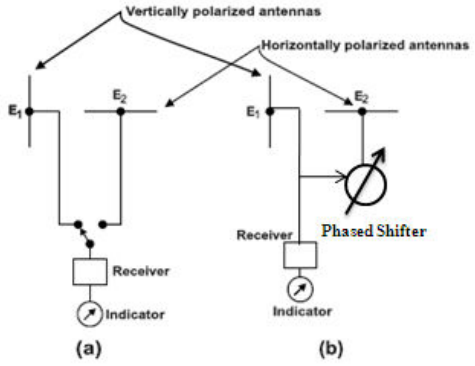


Figure 1. (a) Set for the axis ratio measurement, using the *linear component method.*

Figure 1,(b) Set for the phase difference measurement ψ, using the linear component method.

In this relation, the component of the electric field with greater amplitude refers to the greater axis of the ellipsis polarization.

The second part of the measurement is the measurement of the phase difference between the fields collected by the dipoles, using the field collected by the dipole placed in the vertical, as a reference.

The dipole placed in vertical is connected to the one slotted line, through at dipole placed horizontally, the model proposed by Kraus [9] or a phase comparator circuit in place of these transmission line and both connected to a receiver, as shown in Fig. 1(b). The model described by Kraus [9], he suggests using an attenuator which has only the function of protected the measurement equipments against haut levels of the tension, not interfering at the measurement process.

In this part of the experiment, we will have a wave formed from the two fields with the phase information. Considering the lossless medium, the complex equation for the electric field becomes equal to

$$E_R = E_1 e^{-j\beta z_1} + E_2 e^{-j(\beta z_2 + z_0)} \quad (2)$$

When the appropriate displacement in the slotted line, described by Kraus [9] is done, until the maximum signal amplitude is obtained, the value of the distance z_0 is found, and using the field captured by the vertical dipole, as a reference, the phase difference will be approximately equal to βz_0. The value of the constant of the electromagnetic wave β is given by:

$$\beta = \frac{2\pi}{\lambda} \quad (3)$$

Where, λ is the wavelength of the signal.
After the calculation of the wave phase constant, the value will be given by:

$$\psi = \beta z_0 \quad (4)$$

Once known, the axis ratio (AR) and the lag between the fields (ψ), the ellipsis polarization [10] can be determined. The rotation direction can also be calculated. Since we have the axis ratio, calculating the angle that defines the circle, in the Poincare sphere, through a reference point, is given by:

$$\gamma = tg^{-1}E(smaller\ axis)/E(\ greater\ axis) \quad (5)$$

And finally the calculation of the half latitude angle in the Poincare sphere is given by:

$$\epsilon = \frac{1}{2} arcsin[sin(2\gamma).sin(\psi)] \quad (6)$$

If $\epsilon > 0$, the polarization is to the left; if not, to the right. Another possibility to find the rotation direction of the ellipse polarization is by

analyzing the value of ψ. Since the angle signal ϵ has the same signal as $sin(\psi)$, if $sin(\psi) > 0$, necessarily $\epsilon > 0$, so the ellipse rotation is to the left; if not, to the right.

During the second part of the measurement system to find the phase of the electric field, it is possible that the amplitudes collected in the first part of the experiment are identical, i.e., $E_1 = E_2$. If this happens, there may be doubts about the polarization of the wave. If the polarization is linear prone described 45° or move right or left, that have equal amplitudes of the field. The information circular polarization has an average value of the signal is not zero, which does not happen in linear polarization inclined at 45°.

Another methodology for the second part of the experiment is to replace the line split by a delayed circuit for high frequencies. The main advantage of using a circuit or even a delayed digital or analog is the size reduction of circuit. The main disadvantage is to build a circuit lagged at higher frequencies to ensure a continuous response lagged. According to the phase difference, we characterize the polarization of the wave.

III. CONCLUSIONS

In this article was verified that through the polarization measurement method, using the linear component, it is possible to have access to the magnitude and phase of the electric field irradiated by an electromagnetic wave that is completely polarized. With these parameters it is possible to characterize the wave polarization state.

Future studies look forward to proposing, with the knowledge of the wave polarization, techniques that will diminish the damages caused by electromagnetic interference, especially due to polarization antennas with RFID technology. In order to validate the proposed technique, experimental results are included in the next steps.

ACKNOWLEDGMENT

I thank the program CAPES/ COFECUB by supporting scientific research.

REFERENCES

[1] Zhao Yang, See Kye Yak, Li Shijin, Luo Yongchao, "Fast Diagnosis, Prediction and Signal Characterization of Radiated Eletromagnetic Interference (EMI) Noise", *Lab. Of Millimeter Waves, Southeast University*, China, 2008.

[2] Hirata, E. Taillefer, H. Yamada and T. Ohira, "Handheld direction of arrival finder with electronically steerable parasitic array radiator using the reactance – domain Multiple Signal Classification algorith", *IET Microw. Antennas Propag*., pp. 815 – 821, 2007 1, (4).

[3] Peter Kohns, Yuri Machekhin, "Measurement of Polarization and Applications", *LFNM* , pp. 188 - 196, Kharkiv, Ukraine, 2002, 3 -5 June.

[4] P. Hallbjörner, "Retrieving field magnitude and polarisation ellipse from phaseless measurements of linear polarisations including error analysis", *IEE Proc. Microw. Antennas Propag*. Vol. 150, n° 1, pp. 28 -33, Febuary 2003.

[5] George H. Knittel, "The Polarization Sphere as a Graphical Aid Determining the Polarization of Antenna by Amplitude Measurement Only", *IEEE Transaction on Antennas and Propagation*, Vol. Ap – 15, n° 2, pp. 217 - 221 March 1967.

[6] N. A. Zakaria, A. A. Sulaiman and M. A. A. Latip, "Design of a Circular Microstrip Antenna", *IEEE International RF and Microwave Conference Proceedings*, pp. 289 – 292, December 2-4, 2008.

[7] Wanchu Hong, Chin – Ting Chenq, Yu – De Lin, Toshihide Kitazawa, "A novel Dual Circularly Polarized Microstrip Antenna", *Proceedings of the 36 th European Microwave Conference*, pp. 1629 - 1630 , September 2006.

[8] Wout Joseph, Leen Verlock, and Luc Martens, "Reconstruction of the Polarization Ellipse of the EM Field of Telecommunication and Broadcast Antennas by a Fast and Low – Cost Measurement Method", *IEE Transactions on Eletromagnetic Compatibility*, Vol. 48 n º. 2, pp. 385 - 296 May 2006.

[9] John D. Kraus, Antennas, 1ª ed. McGraw – Hill book Company, 1950, pp. 480 – 481.

[10] John D. Kraus, Keith R. Carver, Eletromagnetismo 2ª ed. Guanabara, pp. 400 – 415, 1986.

Improved Target Impedance and IC Transient Current Measurement for Power Distribution Network Design

Jingook Kim[#1], Songping Wu[#2], Hanfeng Wang[#3], Yuzou Takita[*4],
Hayato Takeuchi[*5], Kenji Araki[*6], Gang Feng[&7], and, Jun Fan[#8]

[#]*EMC Laboratory, Missouri University of Science and Technology, Rolla, MO 65409, USA*
[*]*Sony Corporation, Gotenyama Tec. 5-1-12 Kitashinagawa Shinagawa-ku,Tokyo, 141-0001 Japan*
[*]*Research In Motion, 440 Phillip Street,RIM 14B, Waterloo, ON, N2L 5R9, Canada*

[1]kimjing, [2]swhv7, [3]hw3h6, [8]jfan@mst.edu
[4]Yuzou.Takita, [5]Hayato.Takeuchi, [6]Kenji.Araki@jp.sony.com
[7]gfeng@rim.com

***Abstract*—An improved definition of target impedance is proposed in this paper, which is derived from the time-domain waveforms of the IC transient current and the allowable voltage fluctuation. The proposed target impedance removes the unnecessary constraint in the original definition and allows for more cost-effective power distribution network (PDN) designs for consumer electronic products. A measurement procedure to obtain IC transient current waveforms is also developed for the PDN designs utilizing power traces. The proposed target impedance and the measurement procedure have been validated using practical functioning designs.**

I. INTRODUCTION

Modern integrated circuits (ICs) operate in an internal clock frequency of more than several gigahertz and consume a current of up to tens of amperes. The switching current flowing from power to ground through the logics and buffers results in significant drop and ripple in the supply voltage, seriously affecting power and signal integrity (PI & SI) as well as causing electromagnetic interference (EMI) problems [1]. For EMI and SI concerns, not only the magnitude of the voltage ripple or drop but also its time-domain waveform determines the spectral components of electromagnetic emissions and noise. However, for power integrity, the maximum fluctuation of the power level seen by an IC is critical. Too much voltage fluctuation could cause serious functioning issues such as logic malfunction and timing jitter in signals. The waveform of the voltage drop/ripple has very little effect in terms of power integrity as long as the maximum drop does not exceed the allowable limit. Therefore, one of the important design objectives of a power distribution network (PDN) is to supply enough charge for IC switching so that the maximum voltage drop seen by the IC is lower than the specified allowable limit, which is usually defined as a percentage of the supply voltage.

A very convenient criterion for PDN design is target impedance. As long as the IC switching current is somehow known, the voltage drop seen by the IC is a product of the switching current with the input impedance of the PDN in the frequency domain. Target impedance is defined as the input impedance that results in the maximum allowable voltage drop. Then, the objective of the PDN design becomes to achieve an input impedance lower than the target impedance, which supposedly ensures a voltage drop lower than the limit [1]. Based on the discussions, it is clear that the target impedance is a frequency-domain concept.

Originally, target impedance is defined as

$$Z_{\text{target}} = \frac{(\text{power supply voltage}) \times (\text{allowed ripple \%})}{\text{current}}. \qquad (1)$$

This definition is very straightforward and intuitive. However, both the voltage ripple and the switching current change with time, but the target impedance is a frequency-domain concept. To resolve this conflict, the peak values of the ripple and current are used. This definition is then extended to the entire frequency range of interest as a constant value. As it will be discussed later, it is actually based on the assumption that the PDN is purely resistive.

The actual impedance of a PDN seen by an IC is not constant, but dependent on frequency as shown in Fig. 1, where the PDN utilizes power traces instead of power planes. Using power traces is fairly common in compact consumer electronic devices for various reasons. Several capacitors such as bulk, local, and on-chip ones are employed to lower the impedance value in different frequency ranges. Bulk capacitors work well from approximately 1 kHz to 1 MHz. High-frequency ceramic local capacitors are effective from approximately 1 MHz to several hundred MHz. On-chip and on-package decoupling capacitors are used for the frequencies above several hundred MHz.

The original target impedance definition requires that the input impedance of a PDN needs to be lower than a constant value in the entire frequency range of interest. As seen in Fig. 1, various parasitic inductances existing in a PDN make the low-impedance objective more difficult to achieve at higher frequencies. In other words, the original target impedance has too much constraint at high frequencies, which could result in an over-design. In consumer electronics, product cost plays a critical role. Therefore, improved target impedance is desirable to allow for more cost-effective PDN solutions.

978-1-4244-6307-7/10/$26.00 ©2010 IEEE

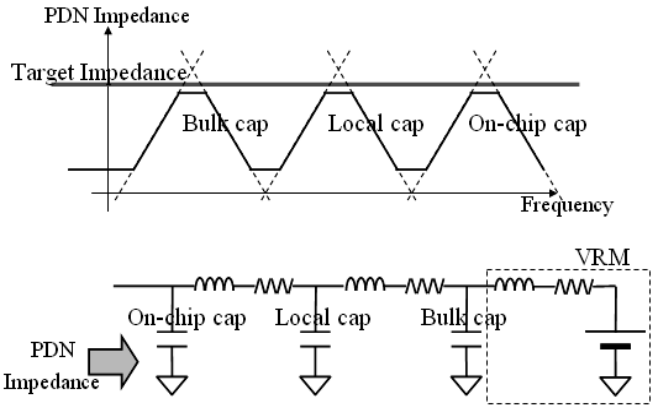


Fig. 1. Input impedance of a PDN utilizing power traces.

From the earlier discussions, target impedance is defined as a function of IC switching current. The knowledge of the switching current is a key for effective PDN design. However, in most situations, proprietary SPICE models or even IBIS behavior models of ICs are not available to PCB designers. A measurement procedure is desirable to accurately measure the transient current waveforms, which are also necessary to design a cost-effective PDN for consumer electronic devices.

In this paper, an improved definition of target impedance is proposed to relate the IC switching current waveforms to the allowable voltage drop waveforms in the time domain. As a result, target impedance becomes a group of impedance curves, and the input impedance of a PDN only needs to be lower than one of the curves to satisfy the design objective. Also, a measurement procedure is presented in this paper to measure the transient current of a decoupling capacitor. In a PDN design utilizing power traces, the capacitor current is approximately the same as the IC transient current. Combined with the improved target impedance, an optimal PDN design is possible in terms of both performance and cost. The proposed approaches are validated with measurements.

II. Improved Target Impedance

To understand how improved target impedance is defined, a simple model of PDN as shown in Fig. 2 is studied first. Again the PDN under study is assumed to have power traces instead of power planes. The connection between an IC and a nearby local decoupling capacitor is modelled as a series resistance and inductance. The inductance comes from the interconnections (such as bond wires, BGA balls, package/PCB traces and vias) and the equivalent series inductance (ESL) of the capacitor package. The resistance may dominantly result from the contact resistance of IC pins, interconnects, and the equivalent series resistance (ESR) of the capacitor. Most high frequency current drawn by the IC is provided by the local decoupling capacitor, since the input impedance into the rest of the power distribution network including the bulk capacitors and VRM is much higher at the high frequencies due to the parasitic inductances whose values are much larger than the one between the IC and the local decoupling capacitor. Therefore, it is reasonable in this case to approximate the high-frequency IC transient current using the high-frequency current that flows through the decoupling capacitor. It is well known that the waveform of the switching current is similar to a rounded triangular shape in most IC chips; therefore, IC switching current is assumed to have a triangular shape herein for simplicity.

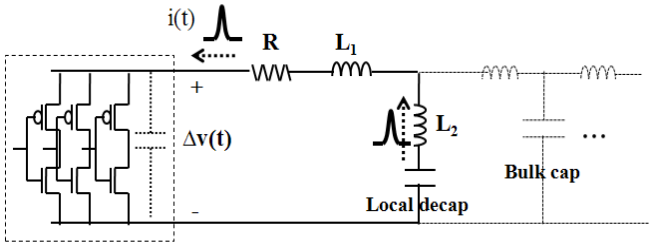


Fig. 2. A simplified PDN model that shows the high-frequency current of the local decoupling capacitor is approximately the same as the IC switching current when power traces are used.

In the simplified PDN model shown in Fig. 2, it can be further approximated that the voltage fluctuation seen by the IC results from the switching current flowing through the parasitic resistance (R) and inductance (L_1 and L_2). The capacitance of the decoupling capacitor is assumed to be large enough to supply the high-frequency switching current, and its contribution to the voltage fluctuation is negligible. In other words, the self resonant frequency of the decoupling capacitor is assumed low enough, and thus the capacitor has an inductive behavior in the frequency region of interest. This assumption is true for most practical designs.

When a triangular current pulse shown in Fig. 3 (a) flows through the parasitic resistance and inductance, the resistive component results in a voltage drop with the same shape as the current pulse, while the inductive components generate a voltage ripple that is proportional to the derivative of the current pulse. As shown in Fig. 3 (b), the total voltage fluctuation seen by the IC is the sum of the resistive drop and the inductive ripple. The exact shape of the overall voltage fluctuation varies with different values of the parasitic resistance and inductance. But it can be shown that the maximum voltage drop always occurs when the current pulse goes to the peak value.

As discussed earlier, for power integrity, a critical design criterion is the maximum voltage drop. The effect of the actual waveform of the voltage fluctuation is less important as long as the drop is less than an allowable limit. Obviously, different weightings of the parasitic resistance and inductance can result in the same maximum voltage-drop values, although the waveforms are different. As an example, four cases with different resistance and inductance weightings are shown in Fig. 4. They result in the same maximum voltage drop but with different waveforms of voltage fluctuation. The case shown in Fig. 4 (a) is purely resistive, while the one shown in Fig. 4 (d) is purely inductive. The other two cases shown in Fig. 4 (c) and (d) have both parasitic resistance and inductances, but with different values.

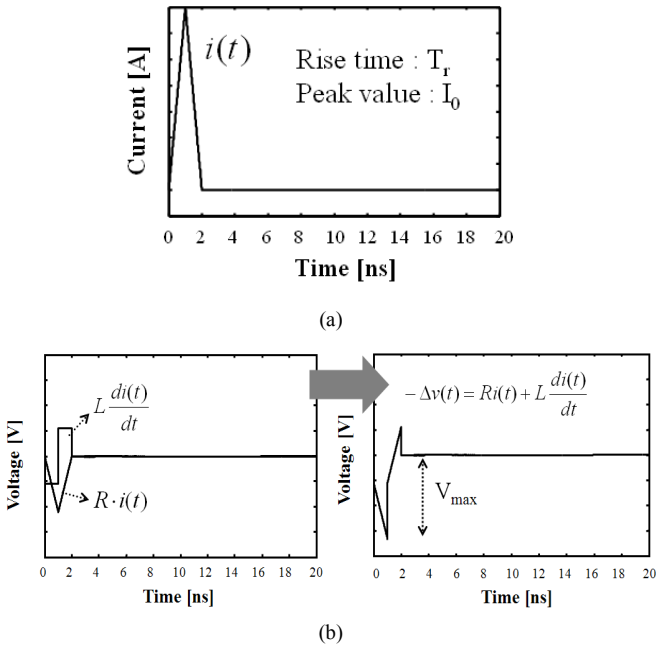


Fig. 3. (a) A triangular current pulse representing IC switching current; (b) voltage fluctuation seen by IC caused by the triangular current pulse in (a), including both resistive drop and inductive ripple.

Mathematically, the triangular current pulse can be expressed as

$$i(t) = \frac{I_0}{T_r}\left(tu(t) - 2\times(t-T_r)u(t-T_r) + (t-2T_r)u(t-2T_r)\right), \quad (2)$$

where T_r is the rise time of the pulse; I_0 is the peak value of the current; and, $u(t)$ is the unit step function. The overall voltage fluctuation as a sum of the resistive drop and the inductive ripple can be derived as

$$\Delta v(t) = -Ri(t) - L\frac{di(t)}{dt} \quad (3)$$

$$= -R\frac{I_0}{T_r}\left[tu(t) - 2(t-T_r)u(t-T_r) + (t-2T_r)u(t-2T_r)\right],$$

$$-L\frac{I_0}{T_r}\left[u(t) - 2u(t-T_r) + u(t-2T_r)\right]$$

where L is the sum of L_1 and L_2 shown in Fig. 2. Then the maximum voltage drop can be calculated as

$$V_{\max} = -\Delta v(T_r) = I_0\left(R + \frac{L}{T_r}\right). \quad (4)$$

It is clear from (4) that the maximum voltage drop increases when R, L, or I_0 increases, or T_r decreases. This is consistent to the physical understanding that larger values of parasitics as well as larger and faster switching currents generate larger voltage fluctuations.

According to the definition of target impedance, it equals to the input impedance seen by IC that generates the maximum allowable voltage drop. In other words, target impedance can be calculated from (4) by setting V_{max} as the allowable limit (a few percentage of the supply voltage). In other words,

$$Z_{\text{target}}(f) = R + j2\pi fL, \quad (5)$$

where the values of R and L satisfy the condition that V_{max} equals to the allowable voltage-drop limit.

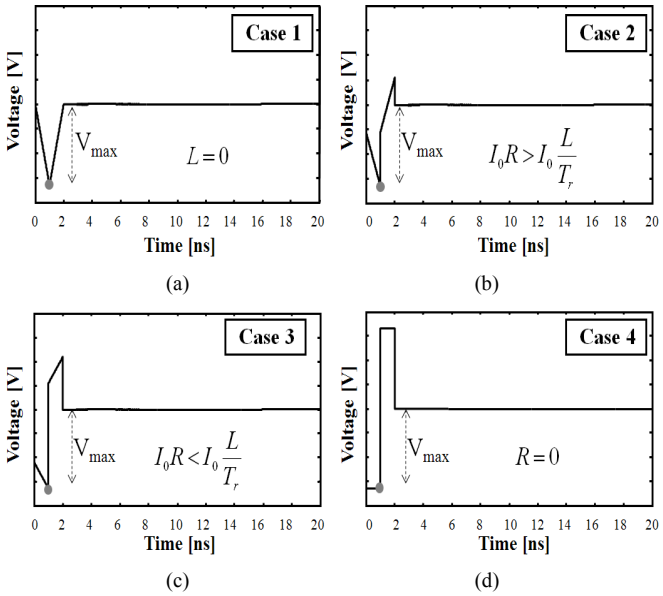


Fig. 4. Four different combinations of R and L that can generate the same V_{max}. Voltage fluctuation is: (a) comprised of purely resistive drop; (b) dominated by resistive drop; (c) dominated by inductive ripple; and, (d) comprised of purely inductive ripple.

Obviously there are many possible solutions since different R and L combinations can result in the same V_{max}. Four target impedance curves corresponding to the four cases shown in Fig. 4 are shown in Fig. 5, where the allowable voltage-drop limit is assumed to be 5% of 3.1 V. All the target impedance values generate the same 0.155 V of the maximum voltage drop in the time domain assuming linear phase. As long as the actual magnitude of the input impedance of a PDN is lower than one of the target impedance values, the voltage drop due to the IC switching current is guaranteed to be lower than 0.155 V, again assuming linear phase.

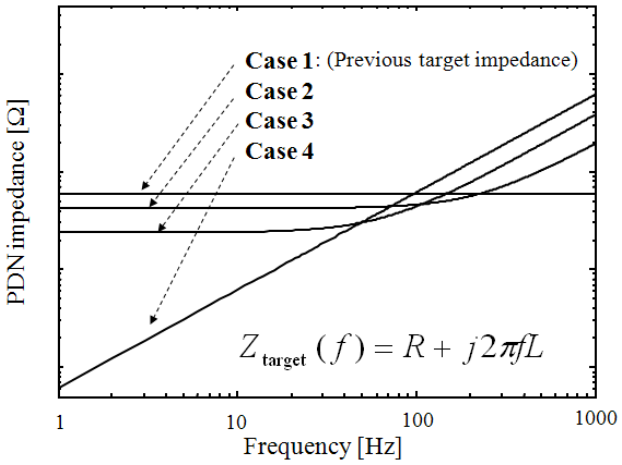


Fig. 5. Target impedance values calculated from the four different R and L combinations shown in Fig. 4. Cases 1 to 4 correspond to Fig. 4 (a) to (d), respectively.

A closer examination of Fig. 5 reveals that Cases 1 and 4 actually serve as the two bounds for all the possible target impedance curves. Case 1 is actually the original target impedance discussed in Section I. Its value is constant at the frequencies of interest. Obviously, it is difficult to meet this target impedance at high frequencies due to the parasitic inductances as discussed earlier. Case 4 is the other extreme. It has the least constraint at high frequencies, but with a price paid at the low frequencies. Fortunately, the other cases provide some degree of compromise between the high- and low-frequency impedance constraints.

The main advantage of the improved definition of target impedance is the reduced constraint at high frequencies. PCB designers can easily calculate the two bounding cases and choose the most suitable target impedance curve in between for the specific design. Thus, over-designs can be avoided, and design optimization in terms of cost becomes possible.

In summary, the overall procedure for obtaining the improved target impedance curves is illustrated in Fig. 6. As discussed earlier, the accurate information of IC switching current in the time domain is necessary. It can be simulated using IC models such as SPICE, IBIS, and so on, when they are available. Otherwise, the current waveform can be obtained from measurements. Then the target impedance values are calculated using (5) based on the allowable voltage-drop limit.

In this paper, the IC switching current was measured using an approach presented later. After the target impedance curves were obtained, they were validated using the measurements of the actual input impedance of the PDN in the frequency domain and the power-bus noise in the time domain from an existing functioning design.

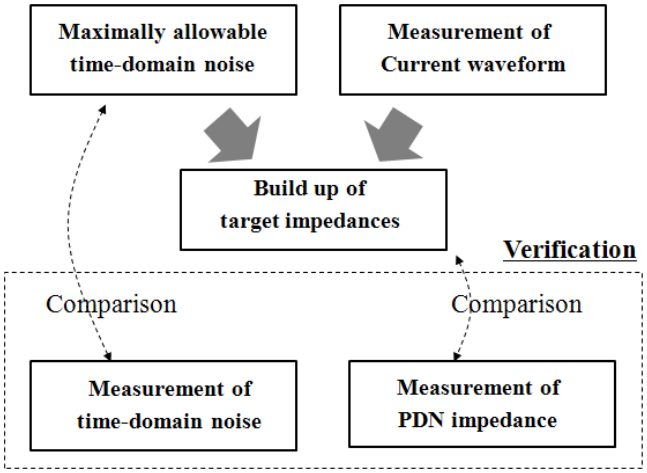


Fig. 6. Overall procedure for extraction of the proposed target impedance and its verification

III. Transient Current Measurement and Validation of Target Impedance

A. Measurement of IC Transient Current

As discussed earlier, in a PDN utilizing power traces that is common for compact consumer electronic devices, the high-frequency IC switching current can be approximated using the high-frequency current flowing through a local decoupling capacitor. A measurement approach is then developed herein to obtain the high-frequency capacitor current using a magnetic-field loop probe. Because the size of the local decoupling capacitors is small and the circuit components are densely placed, a differential probe with a loop size of 7 × 5 mils manufactured using the flex PCB technology was used, which has a very good spatial resolution and sensitivity. As shown in Fig. 7, the voltage induced in the current probe was high-pass filtered, amplified, and then measured in the time domain using an oscilloscope.

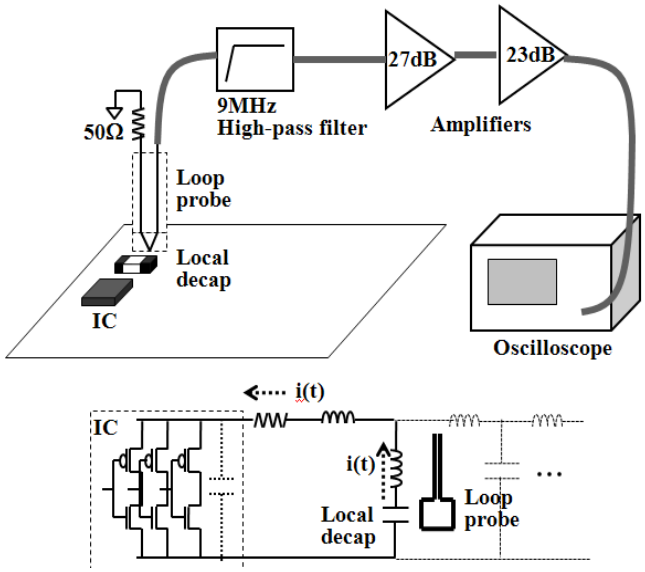


Fig. 7. Experimental setup for decoupling capacitor current measurement.

The induced probe voltage measured on the top of a local decoupling capacitor is shown in Fig. 8. The oscilloscope was triggered by the large peak, and averaging was performed to reduce the random noise. The large peak was then used to calculate the target impedance.

What was measured from the loop probe is the induced voltage. To obtain the transient current of interest, generally speaking, a de-convolution procedure is needed. In this particular case, since the transfer function of the loop probe can be approximately described using a mutual inductance, de-convolution becomes an integration of the measured voltage over time. Specifically, a local integration procedure was performed around the large peak shown in Fig. 8 to estimate the decoupling capacitor current.

Mathematically, the unknown transient current can be calculated from the induced voltage as

$$i(t) = \frac{1}{Gain \cdot M} \int v(\tau) d\tau , \qquad (6)$$

where *Gain* represents the overall gain of the measurement system including the gain of the amplifiers and the loss of the cables; and, *M* is the mutual inductance between the current probe and the decoupling capacitor under measurement. The *Gain* and *M* values were measured in the frequency domain using a vector network analyser (VNA) as 46 dB and 6 pH, respectively. From (6), it is found that the peak value of the

current can be obtained by integrating the positive part of the induced voltage pulse. Since the positive voltage waveform of the large peak is similar to a triangle, the peak value of the transient current can be estimated as

$$I_0 \approx \frac{1}{2}\frac{\Delta V \cdot T_r}{Gain \cdot M}, \quad (7)$$

where T_r is the rise time of the current pulse, which approximately equals to the duration of the positive part of the large pulse in the induced probe voltage. For the induced voltage shown in Fig. 8, the peak magnitude I_0 and the rise time T_r of the high-frequency switching current can be estimated as 66.4 mA and 1.7 ns, respectively, using the local integration method introduced here.

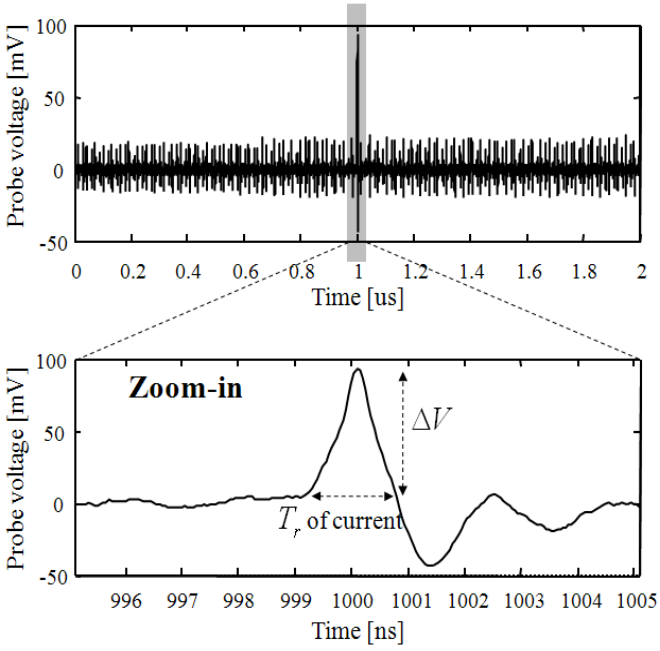


Fig. 8. Induced voltage measured using a loop probe on the top of a local decoupling capacitor.

B. *Validation of Target Impedance*

Since the IC transient current is assumed to have a triangular waveform, it is fully determined as soon as T_r and I_0 are obtained. Then the target impedance curves can be plotted using the approach discussed earlier. Three different cases with allowable voltage-drop limits of 5%, 0.5%, and 2% of the 3.1V supply voltage are shown in Fig. 9 (a)-(c), respectively. Each set of the target impedance curves are compared with the measured actual input impedance of the PDN in each figure. Four different combinations of the R and L values, all satisfying (5), are used to represent each set of the target impedance curves. In Fig. 9 (a), the measured input impedance is clearly lower than at least one of the target impedance curves, while it is clearly higher than any of the target impedance curves in Fig. 9 (b). The intermediate case is shown in Fig. 9 (c), where the measured input impedance is close to the values of the target impedance.

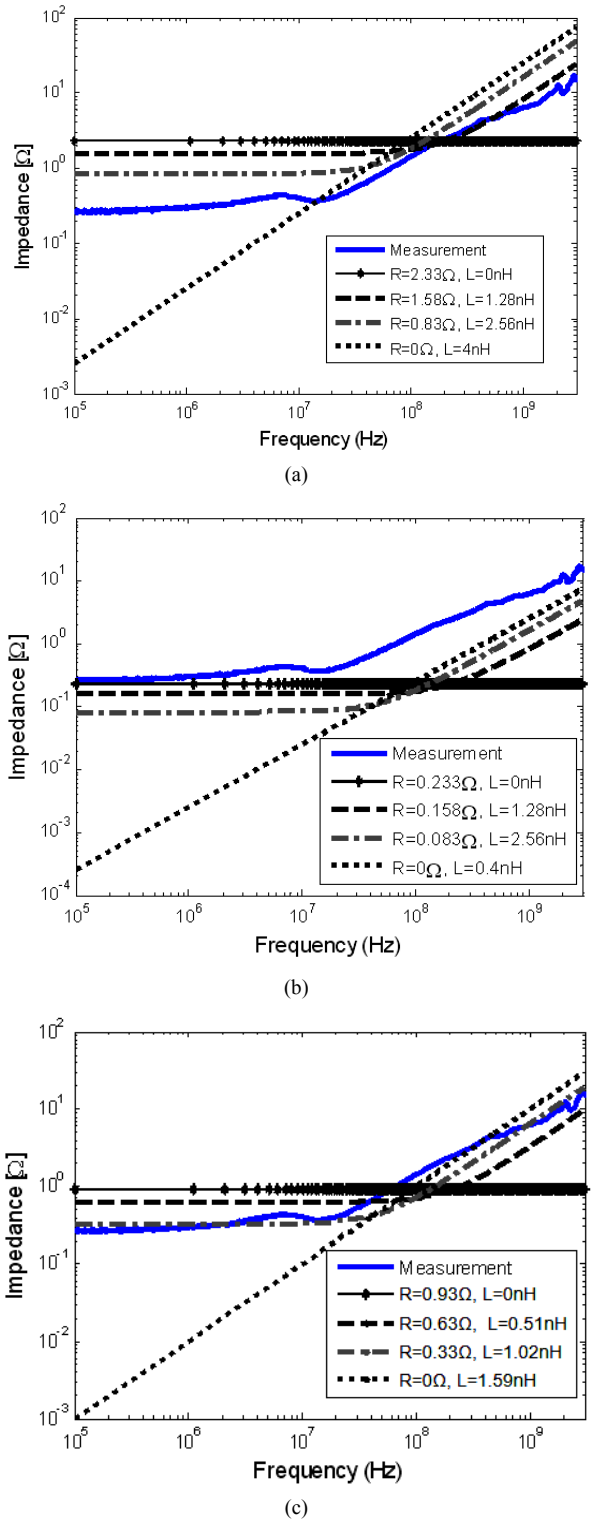


Fig. 9. Comparisons of the target impedance curves with the measured input impedance of the PDN. The allowable voltage-drop limit used to calculate the target impedance curves is: (a) 5% of 3.1 V; (b) 0.5% of 3.1 V; and, (c) 2% of 3.1 V. The IC transient current is assumed to be a triangular pulse with T_r = 1.7 ns and I_0 = 66.4 mA.

From the concept of target impedance, it can be concluded from Fig. 9 that the actual voltage drop seen by the IC should be lower than 155 mV (5% of 3.1 V), higher than 15.5 mV (0.5% of 3.1 V), and close to 62 mV (2% of 3.1 V). To verify whether this prediction is correct, time-domain power-bus noise voltage was measured using an oscilloscope at the exact same location where the input impedance was measured. A 9 MHz high-pass filter was used to filter out the low frequency noise from other components such as DC-DC converters. Also, an 18 dB amplifier was used to increase the signal to noise ratio.

The measured noise voltage is shown in Fig. 10. The measured maximum voltage drop is approximately 155 mV in the oscilloscope. Considering the gain of the amplifier, the actual maximum voltage drop is approximately 19.5 mV. This value correlates well with the prediction in Fig. 9, considering the fact that the phase is always assumed to be linear in the target impedance calculations. Although the measured value is still between 15.5 mV and 155 mV, it is much less than 62.5mV. This indicates that the new target impedance proposed in this paper, although greatly improved, is still not a very accurate design criterion. One common issue in all the target impedance related concepts is the lack of phase information. Notice impedance is a frequency-domain concept, while voltage and current waveforms are time-domain quantities. To relate them together, the Fourier transforms require both magnitude and phase information of the impedance. In the previous discussion, linear phase is always assumed. However, in practical PDN designs, phase is never linear due to the existence of the inductive and capacitive components.

It should be noted that, in Fig. 9, the measured input impedance of the PDN violates the original target impedance criterion in the frequency range of interest for all the cases, demonstrating the unnecessary constraint it imposes at high frequencies. The improved target impedance proposed in this paper removes most of this constraint.

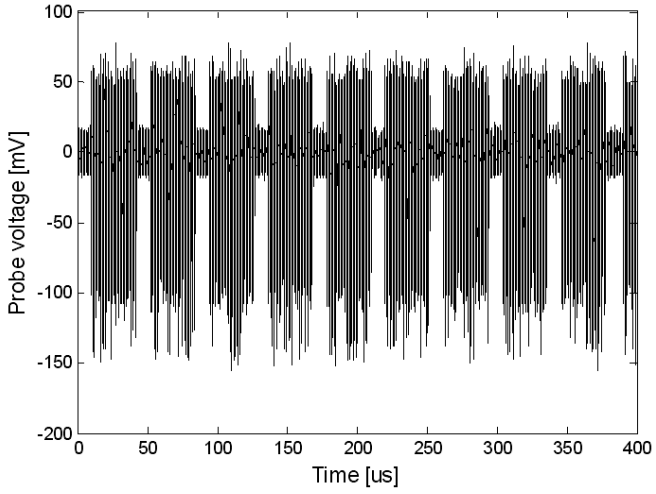


Fig. 10. Measured time-domain power-bus noise voltage.

IV. CONCLUSION

Target impedance is a commonly used criterion for power distribution network design. However, the original target impedance definition imposes too much constraint at high frequencies, which often results in over-designs. An improved concept of target impedance has been proposed in this paper. It was developed from a simple model of the PDN designs using power traces; however, the concept can be extended to the PDN designs using power planes as well. The improved target impedance can have a set of different values between two outer bounds with a variable degree of compromise between the low- and high-frequency impedance requirements. Thus, a PDN design can be optimized for cost, which is critical for modern consumer electronic products.

Target impedance is always based on the knowledge of IC transient current. A measurement approach has been presented in this paper to measure the high-frequency transient current using a loop probe. Simple local integration methods have been developed to estimate the peak magnitude and rise time of a triangular current pulse from the measured induced voltage in the probe.

The proposed target impedance has been validated using the measurements from an existing functioning design. Clear advantage of the new definition has been observed, and the limitation of the approach has been discussed.

REFERENCES

[1] Larry D. Smith, Raymond E. Anderson, Douglas W. Forehand, Thomas J. Pelc, and Tanmoy Roy, "Power distribution system design methodology and capacitor selection for modern CMOS technology", IEEE Transactions on Advanced Packaging, vol. 22, no. 3, pp. 284-291, Aug. 1999.

[2] T. H. Hubing, J. L. Drewniak, T. P. Van Doren, and D.Hockanson, Power bus decoupling on multilayer printed circuit boards," IEEE Trans. on Electromagnetic Compatibility, vol. 37, no. 2, pp. 155-166, May 1995.

[3] J., Knighten, B. Archambeault, J. Fan, G. Selli, S. Connor, and J. Drewniak, "PDN Design Strategies: I. Ceramic SMT ecoupling Capacitors – What Values Should I Choose?," IEEE EMC Society Newsletter, Issue No. 207, pp. 46-53, Fall 2005.

[4] J., Knighten, B. Archambeault, J. Fan, G. Selli, L. Xue, S. Connor, J. Drewniak, "PDN Design Strategies: II. Ceramic SMT Decoupling Capacitors – Does Location Matter?," IEEE EMC Society Newsletter, Issue No.208, pp. 56-67, Winter 2006.

[5] J. Fan, W. Cui, J. L. Drewniak, T. P. Van Doren, and J. L. Knighten, "Estimating the Noise Mitigation Effect of Local Decoupling in Printed Circuit Boards," IEEE Transactions on Advanced Packaging, vol. 25, no. 2, pp. 154-165, May 2002.

[6] Istvan Novak, *Power Distribution Network Design Methodologies*. Chicago: IEC publications, 2008.

Differential Signal Via Shield with Narrow Via Pitch Partial Electromagnetic Bandgap Structure

Chulsoon Hwang, Minchul Shin, Jun So Pak, and Joungho Kim

Department of Electrical Engineering, KAIST
373-1, Daejeon, 305-701, South Korea
cshwang@kaist.ac.kr

***Abstract*— This paper presents a signal via shielding method in a printed circuit board with the narrow via pitch partial electromagnetic bandgap (NVP-PEBG) structure. The NVP-PEBG structure was developed to shield a small area such as a signal via with wideband isolation and compact size. This NVP-PEBG structure showed excellent noise isolation for a single-ended signal via. In this paper, the NVP-PEBG structure is applied to a differential signal via and its performance with the differential signal via is demonstrated in coupling against the noise in a power and ground plane.**

I. INTRODUCTION

Recently, differential transmission lines become a popular interconnection for RF/analog signals due to their high immunity to the crosstalk and electromagnetic interference (EMI) as well as common-mode power/ground noises [1]. Differential lines should be carefully designed to take these advantages over GHz, but in the practical design, inevitable electrical parasitic elements from the circuits and asymmetric signal routing cause the discontinuities and unbalances of differential line. These discontinuity and unbalance generate undesirable mode-conversion (differential-mode to common-mode or vice versa) and signal integrity of differential line is also disturbed by the noise converted from the common-mode noise [2]. One of the major common-mode noise sources is power/ground noise such as simultaneous switching noise (SSN) generated from the switching digital circuits. The SSN is coupled to a signal mainly through the signal via when the signal changes its reference plane. Therefore, it is important to shield a differential signal via in common-mode propagation as well as differential-mode propagation.

To shield a signal via, coaxial or quasi-coaxial arrangements using a ground shield via can be employed [3]. However, this conventional shielding technique can hardly be applied to a multi-layer board because of numerous power planes with various voltage levels and separated ground planes. In a multi-layer board, a signal via can be shielded by locating an electromagnetic bandgap (EBG) structure, which has been exploited to suppress SSN coupling in a power/ground plane. The EBG structure for shielding specific small area such as the signal via is called partial EBG structure, where a few EBG cells are partially located around victim or aggressor to reduce the occupied area by the EBG structure.

EBG structures have evolved to achieve a wide stopband because the digital circuits generate the SSN across a wide frequency spectrum [4]-[7]. The EBG structures for a wide stopband have been implemented using cascaded structures [4], [5], high-dielectric thin films [6], multi-via structures [7]. However, the previous efforts for a wide stopband are not suitable for the partial EBG structure due to not enough number of cells. Because of limited area, the partial EBG structure is composed of only a few cells, thereby having lack of periodicity.

The narrow via pitch partial EBG structure (NVP-PEBG) was recently proposed in [8], where its structure was explained in detail and verified for the suppression of the SSN coupling to a single-ended signal via in a multi-layer board. The NVP-PEBG structure enhanced the stopband with a compact size by adopting the geometry for narrow via pitch array to reduce effective unit cell size and the vertical stacked structure to increase number of unit cells without increasing area. In this paper, the NVP-PEBG structure is applied to a differential signal via. And its performance is demonstrated for the common-mode propagation and differential-mode propagation, respectively. The NVP-PEBG structure for differential signal via, embedded in a 6-stack multi-layer board, also has a remarkable stopband compared with the conventional PEBG structure.

II. NARROW VIA PITCH PARTIAL ELECTROMAGNETIC BANDGAP (NVP-PEBG) STRUCTURE

Fig. 1 presents the NVP-PEBG structure embedded in a 6-layer board. The NVP-PEBG structure (in gray) is composed of en eight-via array with a narrow via pitch and eight planar patches forming EBG cells surrounding the shielding point. Arrangement of EBG via is similar to that of the coaxial shield via. The EBG via is connected to the patch at the vertex of the patch to decrease via pitch with adjacent EBG via, thereby the via pitch is reduced by px in x-direction and py in y-direction. Each patch has one EBG via. The patches in L3 layer are connected to plane in L5 layer, and the patches in L4 layer to plane in L2 layer. The patches in different layers (L3 and L4) overlap each other in the footprint, i.e. vertically stacked structure, so as to increase the number of EBG cells while maintaining a narrow via pitch (px by py), as shown in Fig. 1 (b). All of patches have the same size.

978-1-4244-6307-7/10/$26.00 ©2010 IEEE

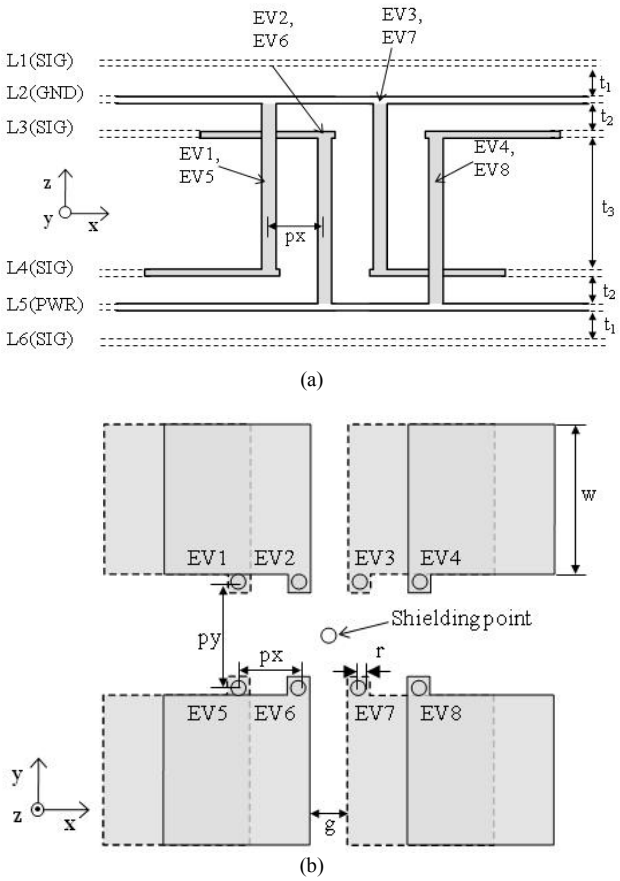


Fig. 1. (a) The cross-sectional view of the NVP-PEBG structure embedded in a 6-layer board (b) the top view of overlapping patches with periodic narrow pitch via array.

When a mushroom-type EBG structure has one via per one patch, the effective unit cell size of the EBG structure can be determined by the periodic via pitch [9]. Therefore, the effective unit cell size of the NVP-PEBG structure can be reduced than that of the conventional mushroom-type EBG structure. In the conventional mushroom-type EBG structure, the minimum effective unit cell size should be larger than the patch size in single layer structure, half of patch size in vertical stacked structure. The smaller the unit cell has, the smaller EBG via inductance becomes [10] and the narrower cross section the power/ground plane per unit cell has. Narrower cross section of the power/ground plane means higher characteristic impedance of the power/ground plane. Since lower EBG via inductance and higher characteristic impedance of the power/ground plane make stopband increase [9], the NVP-PEBG structure has enhanced stopband comparing to the convention mushroom-type EBG structure. Since the capacitance between patch and power or ground plane is not affected by the narrow via pitch and vertically stacked structure, the capacitance remains the same. The parasitic capacitance between overlapped patches is negligible because its value is much smaller than the capacitance between patch and power or ground plane. Since the stopband

TABLE I
PARAMETERS OF THE NVP PEBG STRUCTURE

Parameter	Unit (mm)	Parameter	Unit (mm)
px	0.8	t1	0.1
py	2.1	t2	0.1
g	0.4	t3	0.56
w	5	r	0.1

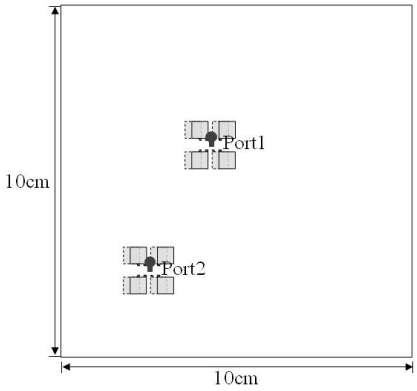


Fig. 2. The simulated structure for the noise coupling between two ports in the power/ground plane with/without the NVP-PEBG structure.

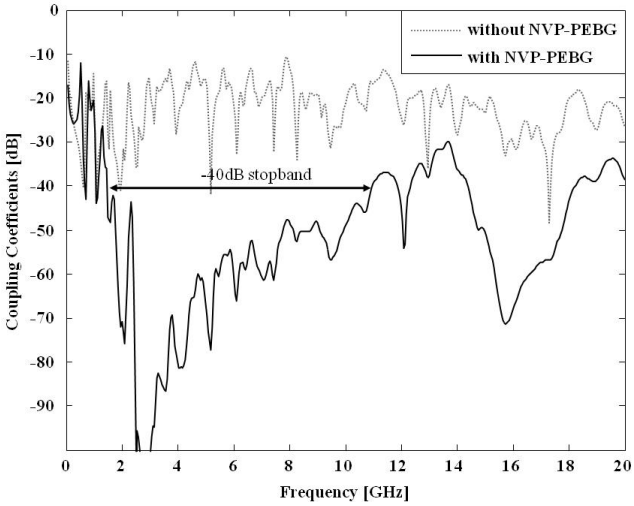


Fig. 3. Simulated noise coupling coefficients between two ports assigned in the power and ground plane with/without the NVP-PEBG structure.

is inversely proportional to the via pitch, wider stopband can be achieved by using narrower via pitch. But minimum via pitch is regulated by two requirements. Via pitch should not violate the minimum via pitch design rule of PCB process and affect signal via impedance.

Fig. 2 describes the simulated structure for the noise coupling between two ports in the power/ground plane with/without the NVP-PEBG structure. Port1 is used to excite the noise between the power and ground plane, coupled noise is probed at port2. Reference board has no shield structure whereas, in the board with a shield structure, both port1 and

port2 are surrounded by the NVP-PEBG structure. Dielectric is FR4, metal is copper. The dimensions of the NVP-PEBG structure are listed in TABLE I. Ansoft SIwave, a 2.5D field solver [11], is used to simulate the structure.

Simulated coupling coefficients are shown in Fig. 3. The dotted line is the reference board without the NVP-PEBG structure, and the solid line the board with the NVP-PEBG structure. Graph shows stopband of 9.5 GHz from 1.5 GHz to 11 GHz (below -40 dB). However, the cut-off frequency determined by certain isolation level can be different depend on the board circumstances. The measured cut-off frequency of the stopband depends on not only the EBG structure, but also the structure where the EBG structure embedded because the cavity resonances are not suppressed enough by the partial EBG structure within its stopband due to lack of periodicity.

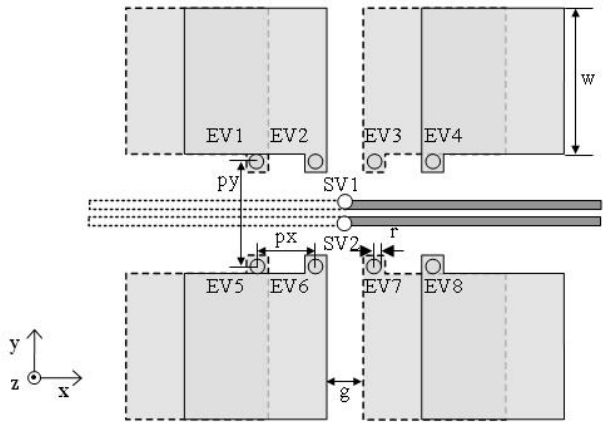


Fig. 4. The top view of overlapping patches with periodic narrow pitch via array.

III. Differential Signal Via Shield

Three types of test vehicles (TVs) were fabricated to verify the performance of the NVP-PEBG structure in shielding the differential signal via. Fig. 4 depicts the NVP-PEBG structure applied to a differential signal via. The test vehicles were fabricated using the FR4 PCB, through-hole via process. A differential micro-strip transmission line is routed from the top layer to the bottom layer through differential signal via. The lines are designed to have differential impedance 100 Ω. The each signal line of differential signal on the bottom layer is terminated with a high-frequency 50 Ω resistors, respectively, to prevent the reflection. TV A has a conventional via transition without a shielding structure, while TV B has a via transition with the PEBG structure and TV C has a via transition with the NVP-PEBG structure as shown in Fig. 5. Although through-hole via is used in the fabrication, via is depicted as buried via in Fig. 5 for simplicity. The dimensions of the NVP-PEBG structure are same as listed in TABLE I. In the TV B, EBG via is located at the center of patch, whose size is 5mm, and gap between patches is 1mm. Port1 is used to excite the noise between the power and ground plane, while differential port2 is designated to measure coupled noise at the end of differential signal on the top layer.

The mixed scattering parameters [12] of the TVs were measured using an Agilent N5230 vector network analyzer and a Picoprobe 250 um-pitch microprobe from 10 MHz to 20 GHz. Microprobe was used to reduce the parasitic effect of probing pad on signal impedance. For common-mode coupling, single-to-common mixed mode parameter Scs21 is measured, and for differential-mode, single-to-differential mixed mode parameter Sds21 is measured.

Fig. 6 and Fig. 7 show the measured coupling coefficients from the power/ground noise to the differential signal line in common-mode and differential-mode, respectively. The NVP-PEBG structure shows the excellent noise suppression for the differential signal via in both propagation modes. And the stopband of NVP-PEBG structure is much wider than that of conventional PEBG structure occupying the same area. The coupling level of Fig. 7 is much lower than that of Fig. 6

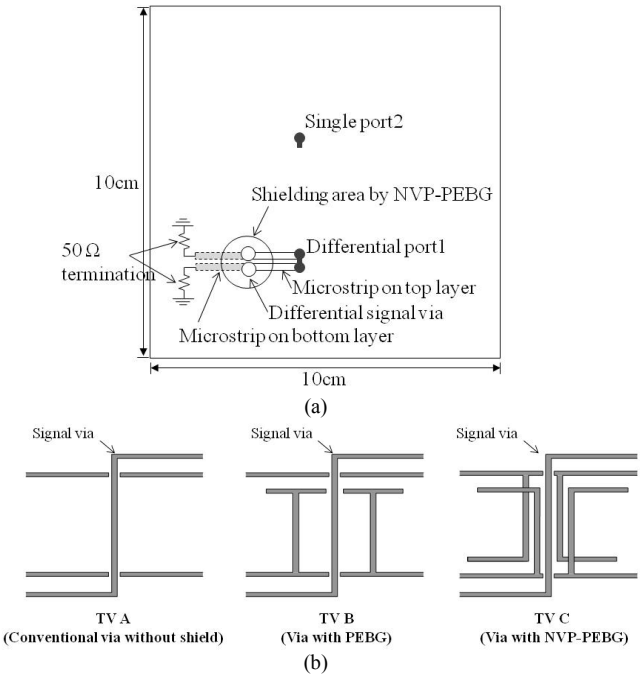


Fig. 5. (a) Top view of the test vehicles (b) the cross-sectional structure of the test vehicles.

because the coupled noise to each signal vias are added in common-mode but cancelled by each other in differential-mode. The stopband of Fig. 3 is overlaid to compare the stopband of the NVP-PEBG structure itself and applied effect.

The stopband of the NVP-PEBG structure applied to differential via is difficult to define based on certain level such as -30dB or -40dB because the noise coupling depend on not only PEBG structure performance, but also noise coupling between signal via and power/ground plane. Moreover, as mentioned before, comparing to the stopband of the EBG structure, that of PEBG structure is more influenced by the cavity resonances due to lack of periodicity.

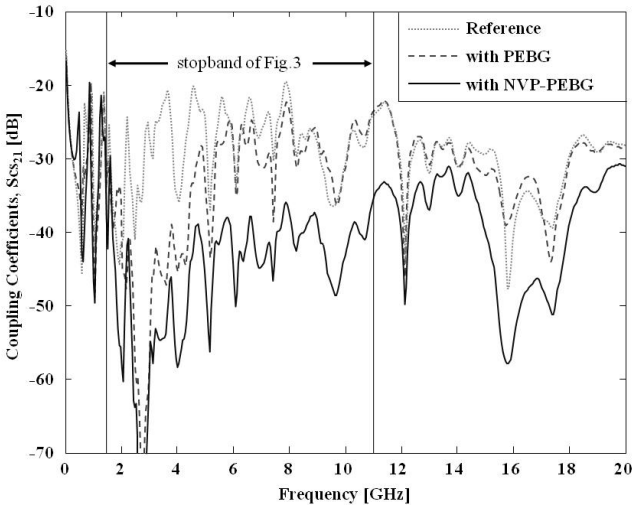


Fig. 6. Measured noise coupling coefficients between differential line with via transition and the power/ground plane in common-mode.

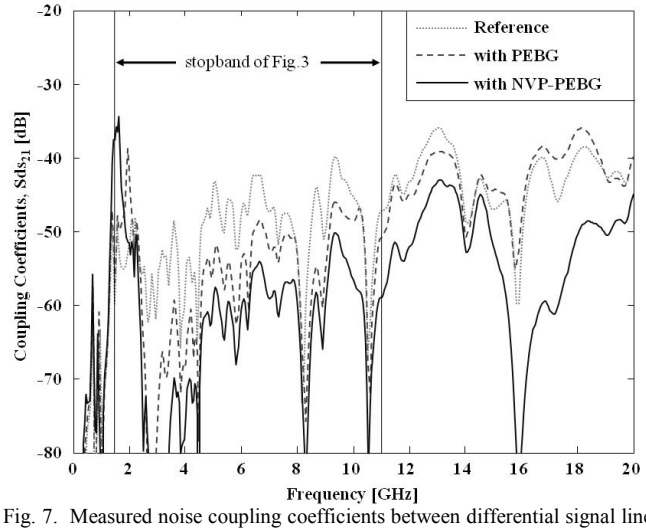


Fig. 7. Measured noise coupling coefficients between differential signal line with via transition and the power/ground plane in differential-mode.

IV. CONCLUSION

In this paper, the excellent differential signal via shield using the NVP-PEBG structure has been demonstrated for both common-mode and differential-mode propagations. The designed NVP-PEBG structure had the stopband of 9.5GHz in simulation and applied to the differential via. The measurement results showed that the applied NVP-PEBG structure suppressed noise coupling within its stopaband for both propagation modes, and could be an efficient method to isolate analog/RF signals against the power/ground noise for not only single-ended signal via but also differential signal via.

REFERENCES

[1] J. Lee, J. Kim, J. Kim, A.C.W. Lu, W. Fan, and L.L. Wai, "Efficiency of differential signaling on cavity noise suppression in applications with reference plane change," in *IEEE Int. Symp. Electromagnetic Compatibility*, Aug. 2004, pp. 203-208.

[2] S. Baek, S. Ahn, J. Park, J. Kim, J. Kim, J.H. Cho, "Accurate high frequency lossy model of differential signal line including mode-conversion and common-mode propagation effect," in *IEEE Int. Symp. Electromagnetic Compatibility*, Aug. 2004, pp. 562-566.

[3] E.R. Pillai, "Coax via-A technique to reduce crosstalk and enhance impedance match at vias in high-frequency multilayer packages verified by FDTD and MoM modeling," *IEEE Trans. Microwave Theory Tech.*, vol. 45, no. 10, pp.1981-1985, Oct. 1997.

[4] S. Shahparnia and O.M. Ramahi, "Simultaneous switching noise mitigation in PCB using cascaded high-impedance surfaces," *Electronics Lett.*, vol.40, no.2, pp. 98-100, 22 Jan. 2004.

[5] J. Park, A.C.W. Lu, K.M. Chua, L.L. Wai, J. Lee, and J. Kim, "Double-Stacked EBG Structure for Wideband Suppression of Simultaneous Switching Noise in LTCC-Based SiP Applications," *IEEE Microwave Wireless Components Lett.*, vol. 16, no. 9, pp. 481-483, Sep. 2006.

[6] J. Lee, H. Kim, and J. Kim, "High dielectric constant thin film EBG power/ground network for broad-band suppression of SSN and radiated emissions," *IEEE Microwave Wireless Components Lett*, vol.15, no.8, pp. 505-507, Aug. 2005.

[7] M.S. Zhang, Y.S. Li, C. Jia, and L.P. Li, "A Power Plane With Wideband SSN Suppression Using a Multi-Via Electromagnetic Bandgap Structure," *IEEE Microwave Wireless Components Lett*, vol.17, no.4, pp.307-309, Apr. 2007.

[8] C. Hwang, J. Kim, E. Song, Y. Shim, and J. Kim, "A Wideband and Compact Partial Electromagnetic Bandgap Structure Using Narrow Via Pitch for Signal Via Shield," *IEEE Trans. electromagnetic compatibility,* submitted for publication.

[9] W. McKinzie and S. Rogers, Circuit and method for suppression of electromagnetic coupling and switching noise in multilayer printed circuit boards, U.S. Patent Applicat. 10/794,185, filed Mar. 3, 2004.

[10] S. Clavijo, R.E. Diaz, and W.E. McKinzie, "Design methodology for Sievenpiper high-impedance surfaces: an artificial magnetic conductor for positive gain electrically small antennas," *IEEE Trans. Antennas Propag.*, vol. 51, no. 10, pp. 2678-2690, Oct. 2003.

[11] Ansoft SIwave 4.0 [online] Available: www.ansoft.com.

[12] D.E. Bockelman, W.R. Eisenstadt, "Combined differential and common-mode scattering parameters: theory and simulation," IEEE Trans. *Microwave Theory Tech.*, vol. 43, no. 7, pp.1530-1539, July 1995.

Equivalent Transmission-Line Model for Vias Connected to Striplines in Multilayer Print Circuit Boards

Siming Pan[#1], Jianmin Zhang[*2], Qinghua B. Chen[*3], and, Jun Fan[#4]

[#]*EMC Laboratory, Missouri University of Science and Technology, Rolla, MO 65409, USA*
[*]*Cisco Systems, Inc., 170 West Tasman Dr., San Jose, CA 95134, USA*
[1]spmq3, [4]jfan@mst.edu
[2]jianmin, [3]billchen@cisco.com

***Abstract*— Vias are typical discontinuities for high-speed signal transmission in printed circuit boards. Previous work has studied the through-hole via connections from the top layer to the bottom between microstrip traces and proposed an equivalent transmission-line model for impedance matching between traces and vias. In this paper, the equivalent transmission-line model is extended for the via structures connected to striplines based on modal decomposition. Both single-ended and differential cases are discussed, and the effects of the model parameters on the performance of signal transition are also investigated. The extended equivalent transmission-line model is accurate and fast to be embedded in circuit simulators for via and link-path analysis. Further, it could provide straightforward criteria to design and optimize via structures for better signal integrity.**

Key words: Via structures, stripline connection, modal decomposition, equivalent transmission-line model, signal integrity.

I. Introduction

High-speed digital systems require high performance in signal links for data communications. Off-chip interconnects often limit the maximal achievable data rate as they introduce frequency-dependent distortions. Modeling the passive components in a signal link path in print circuit board becomes critical to help designers balance the tradeoffs between cost and performance in practical engineering designs. Different modeling approaches in previous studies have addressed this issue. Most of them are based on numerical methods [1], [2]. However, the computational burden of numerical methods, namely memory and time cost, grow rapidly when the geometry under study is complex. Analytical techniques have been introduced as well, especially for relatively simple structures such as the parallel plane pairs in power distribution network (PDN) [3] [4] and the transverse electromagnetic (TEM) structures.

As common discontinuities in printed circuit boards, via structures have been extensively studied [5] [6]. For those connected to striplines, the signal propagates through them excites the parallel plane cavity formed by the two reference planes of the striplines and causes the two reference planes at different potential levels. As a result, the striplines cannot be considered as pure transmission-line structures anymore. Thus, a modal decomposition approach has been proposed in [7] [8], to model the signal transitions between vias and striplines.

In this paper, the prior work in [6] to model via structures as equivalent transmission lines is extended to include the stripline connections for both single-ended and differential cases based on the modal decomposition approach. The equivalent transmission-line model is based on physical geometry, and can provide design insights for engineering issues such as back drilling, via placement, and impedance matching. The equivalent transmission-line model is first extended for the via structures connected to striplines based on the modal decomposition approach inside a parallel plane cavity in Section II. In Section III, the extended equivalent transmission-line model is validated using the comparisons with other published approaches. Potential applications of the extended equivalent transmission-line model are discussed in Section IV from the perspective of signal transmission through the geometry under study.

II. Extended Equivalent Transmission-Line Model for Vias Connected to Striplines

A. Mode Decomposition Inside a Parallel Plane Pair

A typical geometry with coupled striplines connected to signal vias is shown in Fig. 1. The cross sectional view is shown in Fig. 2. The thickness of the strip conductors is assumed negligible. The spacings from the strip conductors to the top and bottom planes are h_1 and h_2, respectively. When the top and bottom planes are at the same potential level, only the TEM waves can propagate in the striplines inside of the plane pair, and the striplines can be modeled as a coupled multi-conductor transmission line (MTL). Thus the voltage and current waves in the striplines can be described in the telegraph equations as:

$$\begin{aligned} \frac{\partial}{\partial z} V_{strip} &= -RI_{strip} - L\frac{\partial}{\partial t} I_{strip} \\ \frac{\partial}{\partial z} I_{strip} &= -GV_{strip} - C\frac{\partial}{\partial t} V_{strip} \end{aligned} \tag{1}$$

The per-unit-length RLGC matrices can be obtained from 2-D cross sectional analysis. The TEM waves described in (1) are also denoted stripline mode waves.

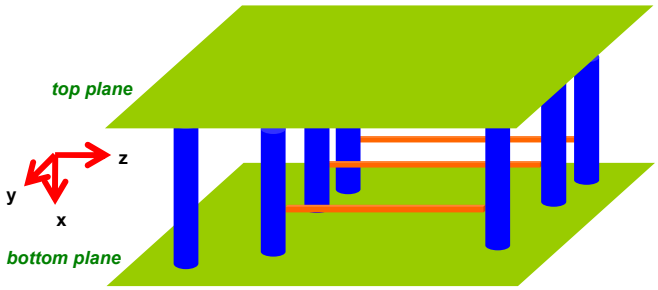


Fig. 1. Coupled striplines connected to vias between two parallel metal planes.

When signal flows though the vias, the parallel plane cavity formed by the two reference planes is excited and the electromagnetic waves in the parallel-plane modes are generated. When the dielectric substrate between the two planes is thin, only the x-directional electric field and the horizontal (y and z-directional) magnetic field components are dominant. In other words, the TM_{z0} modes dominate in such parallel plane cavities. Under this assumption, voltages and currents can be defined at the parallel-plane ports defined between the two planes as shown in Fig. 3. These parallel-plane voltages and currents can be related as

$$V_{pp} = Z_{pp} \cdot I_{pp}, \tag{2}$$

where Z_{pp} is the impedance matrix of the parallel plane pair, which has been extensively studied [10], [11].

It can be shown that the stripline mode and the parallel-plane modes are orthogonal. In other word, the physical voltages and currents defined in Fig. 4 can be expressed as the supposition of the stripline mode and the parallel-plane mode voltages and currents, as

$$\begin{bmatrix} V_{st1} \\ \vdots \\ V_{st\frac{n}{2}} \\ V_{sb1} \\ \vdots \\ V_{sb\frac{n}{2}} \end{bmatrix} = [T_v] \cdot \begin{bmatrix} V_{strip1} \\ \vdots \\ V_{strip\frac{n}{2}} \\ V_{pp1} \\ \vdots \\ V_{pp\frac{n}{2}} \end{bmatrix}, \tag{3}$$

$$\begin{bmatrix} I_{st1} \\ \vdots \\ I_{st\frac{n}{2}} \\ I_{sb1} \\ \vdots \\ I_{sb\frac{n}{2}} \end{bmatrix} = [T_i] \cdot \begin{bmatrix} I_{strip1} \\ \vdots \\ I_{strip\frac{n}{2}} \\ I_{pp1} \\ \vdots \\ I_{pp\frac{n}{2}} \end{bmatrix}, \tag{4}$$

where

$$[T_v] = \begin{bmatrix} 1 & \cdots & 0 & k & \cdots & 0 \\ \vdots & \ddots & \vdots & \vdots & \ddots & \vdots \\ 0 & \cdots & 1 & 0 & \cdots & k \\ 1 & \cdots & 0 & 1+k & \cdots & 0 \\ \vdots & \ddots & \vdots & \vdots & \ddots & \vdots \\ 0 & \cdots & 1 & 0 & \cdots & 1+k \end{bmatrix},$$

$$[T_i] = \begin{bmatrix} 1+k & \cdots & 0 & -1 & \cdots & 0 \\ \vdots & \ddots & \vdots & \vdots & \ddots & \vdots \\ 0 & \cdots & 1+k & 0 & \cdots & -1 \\ -k & \cdots & 0 & 1 & \cdots & 0 \\ \vdots & \ddots & \vdots & \vdots & \ddots & \vdots \\ 0 & \cdots & -k & 0 & \cdots & 1 \end{bmatrix},$$

and, $k = \dfrac{-h_1}{h_1 + h_2}$.

Fig. 2. Illustration of the stripline mode ports and voltages.

Fig. 3. Illustration of the parallel-plane mode ports and voltages.

Fig. 4. Illustration of the physical ports and voltages.

B. Circuit Model for Single-Ended Case

For single-ended signal transition from a signal via to a stripling, as shown in Fig. 5, (4) and (5) can be reduced to

$$\begin{aligned} V_{st} &= V_{strip} - k_1 \cdot V_{pp} \\ V_{sb} &= V_{strip} + k_2 \cdot V_{pp} \\ I_{st} &= k_1 I_{strip} + I_{pp} \\ I_{sb} &= k_2 I_{strip} - I_{pp} \end{aligned} \tag{5}$$

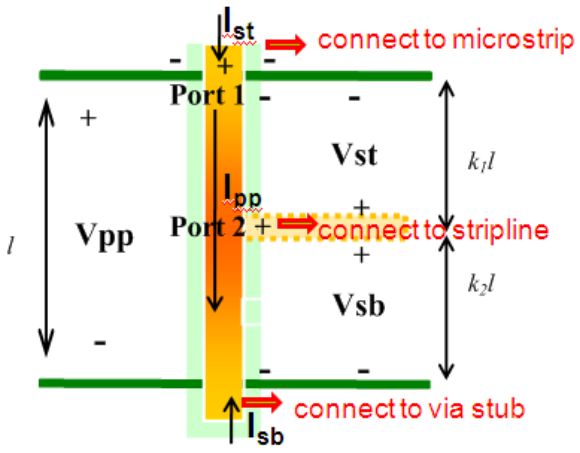


Fig. 5. A single-ended signal via connects to a single-ended stripline.

The equivalent circuit model for the structure shown in Fig. 5 is illustrated in Fig. 6. The signal via inside the cavity is modeled as an equivalent transmission line with a characteristic impedance of

$$Z_0 = \sqrt{Z/Y} \tag{6}$$

where Z and Y are the per-unit-length impedance and admittance, respectively, and their analytical expressions are given in [12]. All the ports are clearly defined in Fig. 5. Two additional current sources are added in the model so that all the voltages and currents can satisfy (5).

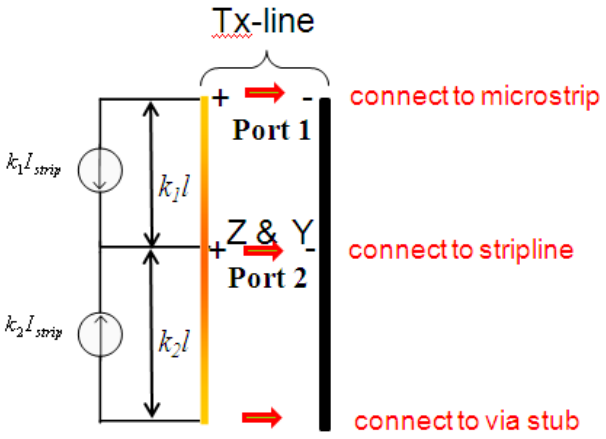


Fig. 6. An equivalent circuit model for the structure shown in Fig. 5.

All the circuit parameters in Fig. 6 are related to certain geometrical dimensions. When signal flows from the top of the via to the stripline, the via stub underneath Port 3, if any, can be treated as a load Z_{load}. The value of the load is the input impedance of the via stub looking at Port 3, which can be calculated using the analytical expression given in [13]. In addition, the current sources in Fig. 6 can be further converted to two impedances, as shown in Fig. 7, as

$$Z_1 = \frac{k_1 Zl(Z_c + k_1(Z_{load} // (k_1 l / Y)))}{k_2((Z_{load} // (k_1 l / Y)) + k_2 Zl)}$$
$$Z_2 = \frac{-k_2 Zl(Z_c + k_1(Z_{load} // (k_1 l / Y)))}{k_1((Z_{load} // (k_1 l / Y)) + k_2 Zl)} \tag{7}$$

where Z_c is the characteristic impedance of the stripline.

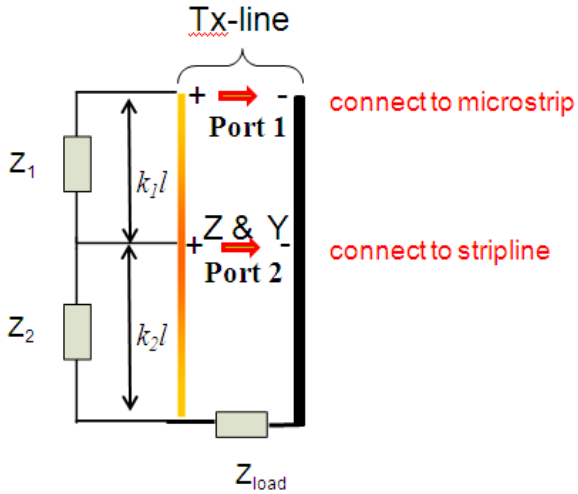


Fig. 7. Equivalent circuit model including the via stub effect for the structure shown in Fig. 5. The current sources in Fig. 6 has been replaced with equivalent impedances.

C. Circuit Model for Differential Case

The geometry of the differential case under study with a differential signal flows through two symmetric signal vias to two coupled striplines is shown in Fig. 8. For differential signals, (4) and (5) become:

$$\begin{bmatrix} V_{st1} \\ V_{st2} \\ V_{sb1} \\ V_{sb2} \end{bmatrix} = \begin{bmatrix} 1 & 0 & -k_1 & 0 \\ 0 & 1 & 0 & -k_1 \\ 1 & 0 & k_2 & 0 \\ 0 & 1 & 0 & k_2 \end{bmatrix} \cdot \begin{bmatrix} V_{strip1} \\ V_{strip2} \\ V_{pp1} \\ V_{pp2} \end{bmatrix}, \tag{8}$$

$$\begin{bmatrix} I_{st1} \\ I_{st2} \\ I_{sb1} \\ I_{sb2} \end{bmatrix} = \begin{bmatrix} k_2 & 0 & -1 & 0 \\ 0 & k_2 & 0 & -1 \\ k_1 & 0 & 1 & 0 \\ 0 & k_1 & 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} I_{strip1} \\ I_{strip2} \\ I_{pp1} \\ I_{pp2} \end{bmatrix}. \tag{9}$$

For differential signals of balanced signal paths,

$$I_{pp1} = -I_{pp2} \tag{10}$$

Similar to the single-ended case, the equivalent circuit model for the geometry shown in Fig. 8 is developed as shown in Fig. 9. Only the differential mode is considered in deriving the circuit parameters. The analytic expressions to calculate the per-unit-length impedance matrix **Z** and the admittance matrix **Y** can be found in [6], and

$$Z = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix}$$

The differential-mode input impedance looking into the via stubs, if any, beneath the bottom plane is Z_{load_diff}, which can be obtained using the expression given in [13]. Similar to the single-ended case, in Fig. 9, the parallel impedances Z_{up} and Z_{down} are converted from the extra current sources as

$$Z_{up} = \frac{k_1 Z_{11} l (Z_{dd} + k_1((Z_{load\_diff}/2)//(k_1 l / Y_{11})))}{k_2((Z_{load\_diff}/2)//(k_1 l / Y_{11})) + k_2 Z_{11} l)}$$
$$Z_{down} = \frac{-k_2 Z_{11} l (Z_{dd} + k_1((Z_{load\_diff}/2)//(k_1 l / Y_{11})))}{k_1(((Z_{load\_diff}/2)//(k_1 l / Y_{11})) + k_2 Z_{11} l)} \quad (11)$$

where Z_{dd} is the differential-mode characteristic impedance of the coupled striplines.

The mutual impedance of via above and below the stripline changes from Z_{12} to Z_{up12} and $Z_{bottom12}$ respectively, with

$$Z_{up12} = \frac{-k_1 Z_{12} l (Z_{dd} + k_1((Z_{load\_diff}/2)//(k_1 l / Y_{11})))}{1 - k_2(((Z_{load\_diff}/2)//(k_1 l / Y_{11})) + k_2 Z_{11} l)}$$
$$Z_{bottom12} = \frac{Z_{12} l (-Z_{dd} + k_1((Z_{load\_diff}/2)//(k_2 l / Y_{11})))}{-Z_{dd} + k_1(2((Z_{load\_diff}/2)//(k_2 l / Y_{11})) + k_2 Z_{11} l)} \quad (12)$$

The per-unit-length self impedance of the via remains the same as the diagonal terms in the matrix **Z**. Z_{load_diff} is the differential-mode input impedance looking from the cavities below the bottom plane. We assume differential port 2 is matched with differential striplines. The equivalent transmission line model shown in Fig. 9 satisfies equation (2), (8), (9) and (10).

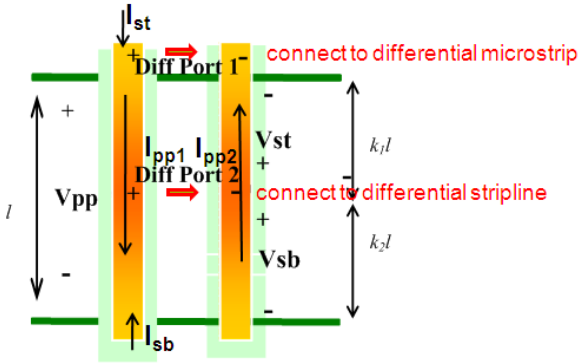


Fig. 8. Two differential signal vias connects to two coupled striplines.

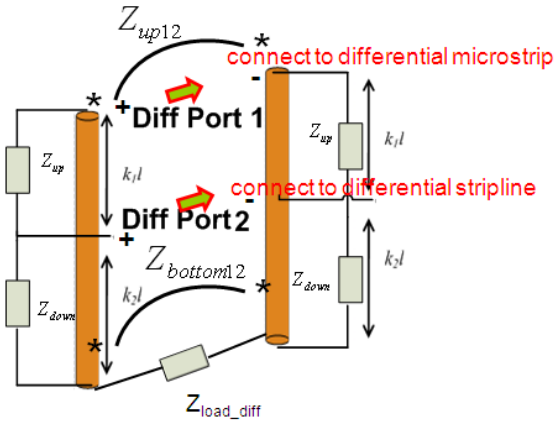


Fig. 9. Equivalent differential transmission line model including the via stub effect for the structure shown in Fig. 8. The reference plane is omitted.

D. Equivalent Transmission-Line Model

For both the single-ended and the differential cases, the equivalent circuit models developed earlier can be further simplified using an equivalent transmission line terminated with a load, as shown in Fig. 10.

Fig. 10. A simplified model using an equivalent transmission line with terminations for both single-ended and differential cases. For differential cases, the reference plane is omitted

For the single-ended case shown in Fig. 7, the per-unit-length impedance Z' and admittance Y' in the simplified model in Fig. 10 can be obtained as

$$Z' = Z//(Z_1/(k_1 l))$$
$$Y' = Y \quad (13)$$

The value of Z_{load_port2} can be calculated from the circuit parameters in Fig. 7 as

$$Z_{load\_port2} = (Z_2 // Zk_2 l + Z_{load}//(k_2 l / Y)). \quad (14)$$

Similar derivations can be applied for the differential case, as

$$Z_{diff\_load\_port2} = 2(Z_{down} // Z_{11} k_2 l - Z_{down12} + (Z_{load\_diff}/2)//(k_2 l / Y_{11})) \quad (15)$$

III. Validation of the Proposed Model

A test geometry shown in Fig. 11 including a single-ended signal via connected to a stripline in a multi-layer PCB is used as a validation example. Signal flows from a microstrip trace in the top layer to a stripline trace in a middle layer. The two traces are assumed short enough so that the ports are approximately defined at the via-trace intersections. Two ground vias are placed surrounding the signal via. The radii of the via drills and the anti-pads are 10 mils and 30 mils, respectively. The thickness of the copper planes is 1 mil. The dielectric layers have a dielectric constant of 3.84 and a loss tangent of 0.033. The other geometrical details can be found in Fig. 11.

The geometry is modeled layer by layer. In the fourth parallel-plane cavity where the via connects to the stripline, the equivalent transmission-line model proposed in this paper is used. In all other cavities, a standard equivalent transmission-line model introduced in [12] is used instead.

The simulated S_{11} and S_{12} magnitudes between Ports 1 and 2 defined in Fig. 11 using the method described above are compared with those obtained using a physics-based equivalent circuit model combined with modal decomposition [8] in Figures 12 and 13. Good agreements between the two methods are observed up to 40 GHz.

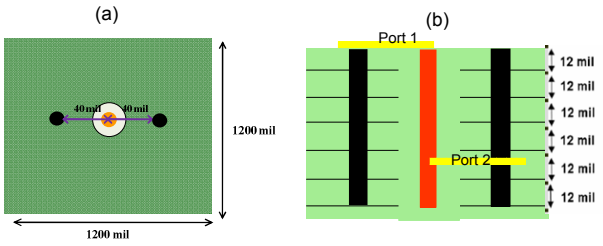


Fig. 11. (a) Top view; (b) side view of a single-ended test case.

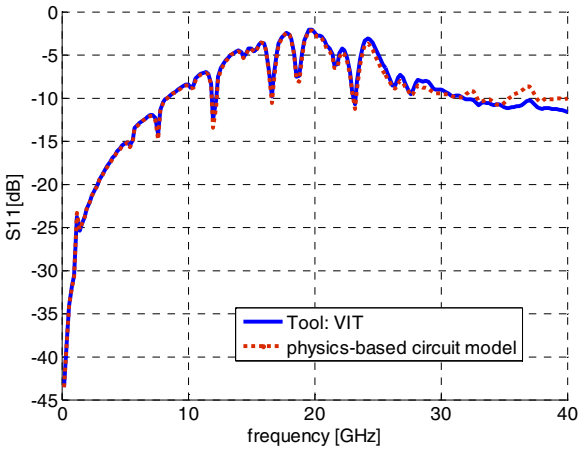


Fig. 12. Comparison of the S_{11} magnitudes for the single-ended case shown in Fig. 11.

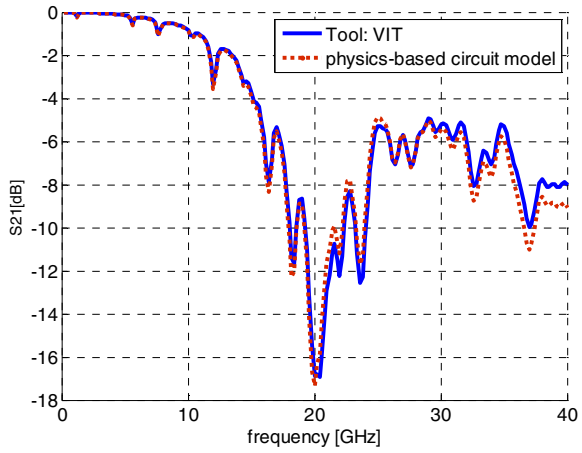


Fig. 13. Comparison of the S_{12} magnitudes for the single-ended case shown in Fig. 11.

A differential validation example is shown in Fig. 14. Two pairs of differential signal vias are connected though a differential stripline embedded in the cavity. The ports are defined at the top of the vias. The differential stripline is modeled using an HSPICE W-element model assuming a homogeneous and constant cross section.

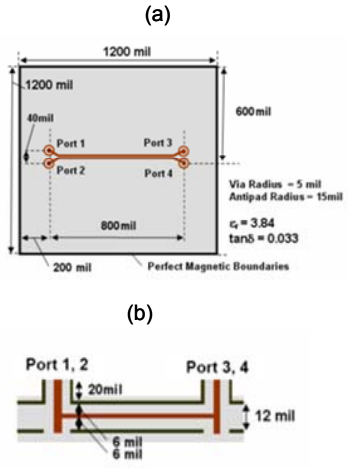


Fig.14. (a) Top view; (b) side view of a differential test case.

The differential mode S_{dd11} and S_{dd21} magnitudes are calculated using the equivalent transmission-line model proposed in this paper, and are compared with those obtained using a physics-based equivalent circuit model with modal decomposition [8] and using HFSS, a full-wave finite element method, in Figures 15 and 16. The differential Port 1 is comprised of the single-ended Ports 1 and 2 defined in Fig. 14, and the differential Port 2 is comprised of Ports 3 and 4. It can be clearly seen that the equivalent transmission-line model proposed in this paper has a good accuracy compared with the other methods. The unique advantage of the proposed method is that via analyses and designs can rely on some conventional transmission-line concepts such as the characteristic impedance for impedance matching.

IV. Design Implications

Smooth transitions between vias and traces are desirable for high-speed signal transmission in multi-layer PCBs. Impedance matching is important when signal transits from trace to via and vice verse. The simplest design philosophy is to ensure that the characteristic impedance of the equivalent transmission line in Fig. 10 representing vias is the same as the characteristic impedance of the traces that connect to the vias.

The effects of via stubs are also critical to the signal transmission through the vias. The value of Z_{load_port2} in Figure 10 describes the effects of via stubs. Ideally, Z_{load_port2} should be desired to be infinitely large, which means the electrical length of the via stubs shall be zero. If Z_{load_port2} becomes relatively small at the frequencies of interest, the via stubs can impose adverse effects on the signal transmission, and back drilling may be necessary. Therefore, Z_{load_port2} can be used to determine when a back drilling is needed.

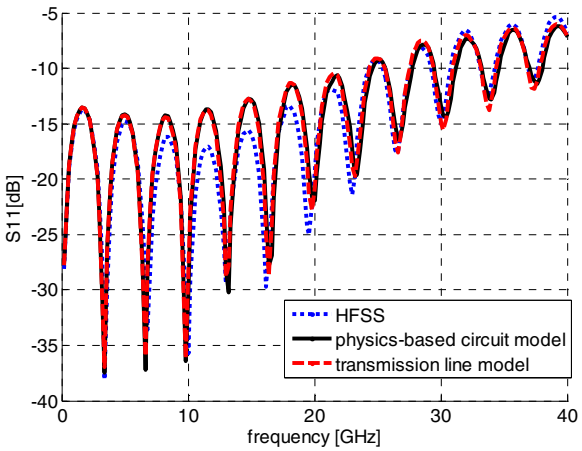


Fig. 15. Comparison of the S_{dd11} magnitudes for the differential case shown in Fig. 14.

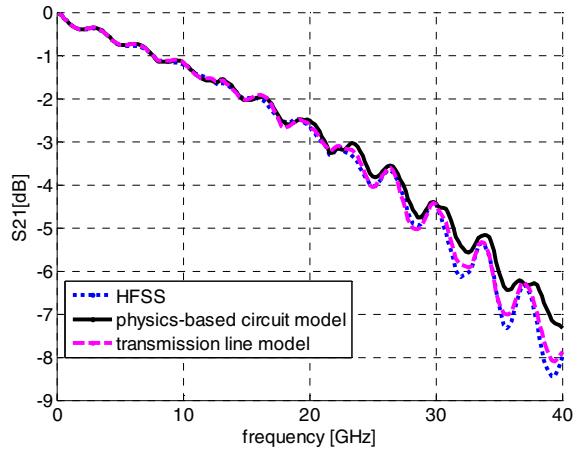


Fig. 16. Comparison of the S_{dd11} magnitudes for the differential case shown in Fig. 14.

V. Conclusion

An equivalent transmission-line model is extended in this paper for the via structures connected to striplines based on the modal decomposition approach, which has been validated with other methods. As a result, the characteristic impedance of the equivalent transmission line can be used for impedance matching between the vias and the traces. In addition, the value of the load impedance representing the effects of via stubs can be used to determine when a back drilling is necessary.

References

[1] A. E. Engin, K. Bharath, M. Swaminathan, M. Cases, B. Mutnury, N.Pham, D. N. de Araujo, and E. Matoglu, "Finite-difference modeling of noise coupling between power/ground planes in multilayered packages and boards," in Proc. 56th Electron. Compon. Technol. Conf., Jun. 2006, pp. 1262–1267.

[2] S.-G. Hsu and R.-B. Wu "Full-wave characterization of a through hole via in multilayered packaging," IEEE Trans. Microw. Theory Tech., vol. 43, pp. 1073, May 1995.

[3] N. Na, J. Jinseong, S. Chun, M. Swaminathan, and J. Srinivasan, "Modeling and transient simulation of planes in electronic packages," IEEE Trans. Adv. Package., vol. 23, no. 3, pp. 340–352, Aug. 2000.

[4] M. Xu, Y. Ji, T. H. Hubing, T. P. Van Doren, and J. L. Drewniak, "Development of a closed-form expression for the input impedance of power-ground plane structure," in Proc. IEEE Int. Symp. Electromagn. Compat. Washington, DC, Aug. 2000, pp. 77-82.

[5] X. Gu and M. B. Ritter, "Application of Foldy-Lax Multiple Scattering Method To Via Analysis in Multi-layered Printed Circuit Board", DesignCon 2008, Santa Clara, CA USA, Feb. 4 - Feb. 7, 2008.

[6] S. Pan, J. Fan. "Equivalent Mixed-mode Characteristic Impedances for Differential Signal Vias," IEEE International Symposium on Electromagnetic Compatibility, Austin, Texas, August 17 - 21, 2009.

[7] A. Ege Engin, Werner John, Grit Sommer, Wolfgang Mathis, and Herbert Reichl, "Modeling of Striplines Between a Power and a Ground Plane," IEEE Trans. Adv. Package, VOL. 29, NO. 3, AUGUST 2006.

[8] Renato Rimolo-Donadio, Xiaoxiong Gu, Young H. Kwark, Mark B. Ritter, Bruce Archambeault, Francesco de Paulis, Yaojiang Zhang, Jun Fan, Heinz-Dietrich Brüns, and Christian Schuster, "Physics-Based Via and Trace Models for Efficient Link Simulation on Multilayer Structures Up to 40 GHz," IEEE Trans. Microw. Theory Tech, VOL. 57, NO. 8, AUGUST 2009

[9] S.-G. Hsu and R.-B. Wu "Full-wave characterization of a through hole via in multilayered packaging," IEEE Trans. Microw. Theory Tech., vol. 43, pp. 1073, May 1995.

[10] G.T. Lei, R. W. Techentin, P. R. Hayes, D. J. Schwab, B. K. Gilbert, "Wave Model Solution to the Ground/Power Plane Noise Problem", IEEE Trans. Instrumentation and Measurement, Vol. 44, No. 2, April 1995

[11] R. Chadha, K.C. Gupta, "Segmentation Method Using Impedance Matrices for Analysis of Planar Microwave Circuits", IEEE Trans. Microw. Theory Tech, Vol. MTT-29, No.1, January 1981.

[12] S. Pan, J. Fan. "Equivalent characteristic impedance and propagation constant for multi-layer Via Structures," 2009 International Symposium on Electromagnetic Compatibility, Kyoto, Japan, July 20-24

[13] H. Wang, W. Cheng, J. Zhang, J. Fisher, L. Zhu, J. L. Drewniak, and J. Fan, "Investigation of mixed-mode input impedance of multi-layer differential vias for impedance matching with traces," in Proc. IEEE International Symposium on Electromagnetic Compatibility, Austin, USA, Aug. 2009, pp.203-207

Off-Phase Crosstalk Behaviour and Design Considerations for High-Speed Memory Buses

Amy J. Chen, Hao Wang

Intel Corporation

2200 Mission College Blvd.
Santa Clara, CA 95054-1549
USA

amy.j.chen@intel.com

hao.wang@intel.com

***Abstract*— The interconnect margins shrink rapidly at higher speed due to reduced bit width and increased noise level. Crosstalk impact remains the biggest concern for the single-ended memory busses such as DDR3 and GDDR5 interconnect. The phase relationship of the xtalk coupling plays an important role on interconnect performance. This paper outlines several types of off-phase crosstalk and their impact to system margin. It also provides the methodology to analyse their effects and design considerations to mitigate their impact.**

I. Introduction

The DDR memory bus is the interconnect between the memory controller and Dual In-line Memory Module (DIMM) cards. The speed target for DDR3 is in range of 1GT/s to 2GT/s. The GDDR memory bus is the interconnect between Graphic Processing Unit (GPU) and Synchronous Graphics Random Access Memory (SGRAM) devices. The speed target for GDDR5 is in range of 3GT/s to 6GT/s.

Both memory interfaces utilize single-ended signaling technology. As the speed increases, bus timing margin is challenged due to the reduction in available time window and increased jitter; bus voltage margin is as well challenged due to higher loss and elevated crosstalk levels.

Crosstalk remains the biggest risk factor in designing the DDR3 and GDDR5 interfaces to meet design targets. The existing analysis methodology captures in-phase crosstalk effects fairly well in examining the signals within a byte group in the bus. However, the conventional methodology breaks down when a signal group interfaces with other types of signals in the physical design, such as between data and address/command signal boundary, and at the byte and channel boundaries. Since there is no strict phase relationship between different types of signals and between channels, off-phase crosstalk has to be considered in the design practice. Their design considerations are very different than that from the in-phase crosstalk.

The off-phase crosstalk effects examined in this paper include phase noise, all-phase crosstalk, and read-write crosstalk. Phase noise usually exists within and between memory byte groups due to driver skew and channel length variations. All phase crosstalk has to be considered in the GDDR5 bus due to per-bit tuning and absence of length matching requirements (to facilitate physical design). Read-write crosstalk needs to be accounted for in channel boundary and signal group boundary, such as between data and address/command groups. Lack of consideration for read-write crosstalk can cause catastrophic failure in design.

This paper also outlines an analysis methodology to account for off-phase crosstalk in High Volume Manufacturing (HVM) environment. The case study examines read-write crosstalk within a GDDR5 channel, but is applicable to any other interface with similar concern.

The off-phase crosstalk behaviour is usually complicated and requires significant analysis effort to understand the impact. One's best offense is to design it out by minimizing off-phase crosstalk effects. This paper demonstrated several design considerations in package and board designs to mitigate the impact. These examples may serve as references, though the appropriate constraints for each design will need to be tailored after careful analysis and examination by the designer.

II. Channel-to-Channel Crosstalk in DDR3

In memory bus routing and pin map design practices, it is not uncommon to route data signals from two different channels next to each other, mainly due to large numbers of signals and relatively small routing space. As illustrated in one example in Figure 1, the data signal D22 in Channel 1 is surrounded by five data signals from Channel 0. These practices work fine for DDR2 and low speed DDR3, whose data rate is no higher than 800 MT/s. Such design practices, however, pose great risks when the data rate reaches 1066 MT/s and beyond. The risks are further exacerbated due to the popular trend of adaptation of sockets at junctions between memory controllers and motherboards for desktop and server products. Large amounts of lab data reveal that when multiple channels are toggling, the victim channel could have noticeably degraded margins or even fail completely. The culprit is believed to be the channel to channel crosstalk, as it is always the signals at the channel to channel boundary which have the lowest margins and worst performance.

978-1-4244-6307-7/10/$26.00 ©2010 IEEE

Ch1_D13	Ch1_D14	Ch0_DS2 P	Ch0_DS2 N
Ch1_D18	VSS	Ch0_D6	Ch0_D20
Ch1_D19	Ch0_D3	Ch1_ D22	Ch0_D1
VSS	Ch1_DSP	Ch0_D5	VSS

Fig. 1. An Example of DDR3 Controller Pin Map

Channel to channel crosstalk can be categorized as write-write, read-read, and read-write crosstalk, all of which are all-phase crosstalk as the channels operate independently. Among the three types of crosstalk, read-write crosstalk has the most pronounced impacts for two reasons. First, contrary to write-write and read-read crosstalk, of which far-end crosstalk (FEXT) plays predominant roles, the read-write crosstalk is determined by near-end crosstalk (NEXT) that typically has higher magnitudes even for a short interleaving distance. Second, despite being effective on suppressing FEXT, the stripline routing practices cannot tame NEXT as well [1].

This section depicts the procedures aimed at quantitatively analysing the impacts of read-write crosstalk on voltage and time margins. It evaluates each contribution factor and its potential risks along the whole signal path. And it presents the approaches which can effectively alleviate or even design out the channel-to-channel crosstalk.

A typical DDR3 bus, running at 1600 MT/s and with 2 DIMM-per-channel is used here as the test vehicle. Four aggressor signals are included in analysis, with half of them in the read channel and the other half in the write channel. Peak Distortion Algorithm (PDA) tool is used to extract eye diagram at receiver [2]. One can perform the analysis as a 3-step process:

1) Force the write channel quiet while exciting read channel, and obtain the pulse responses at the victim receiver pad in the read channel. The purpose of this step is to obtain Inter-Symbol-Interference (ISI) response and within-channel crosstalk.

2) Force the read channel quiet while exciting write channel, and obtain the pulse responses at the same victim receiver pad. This step will extract crosstalk from the write channel to read channel.

3) Use the PDA tool to add the crosstalk contributions from 1) and 2). It is critical to define the step 1)'s results as in-phase crosstalk and step 2)'s results as all-phase crosstalk, as the two channels are running independently.

Using the non-interleave in-phase crosstalk as the baseline, Table 1 shows the eye diagram results with read-write crosstalk when two channels are interleaved at various areas. For example, as shown in Case 2, if the two channels are interleaved at the package only, the eye height and eye width will lose 40 mV and 10 pS, respectively.

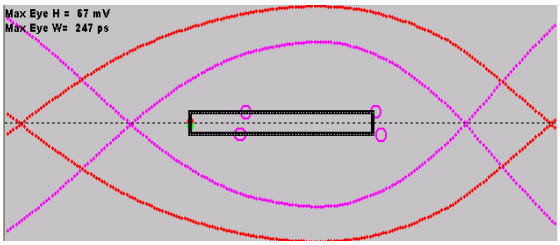
The worst scenario happens when the two channels interleave all the way covering the package, socket and motherboard, as shown in Case 6. The eye height and eye width losses reach as high as 170 mV and 110 pS, respectively.

TABLE I

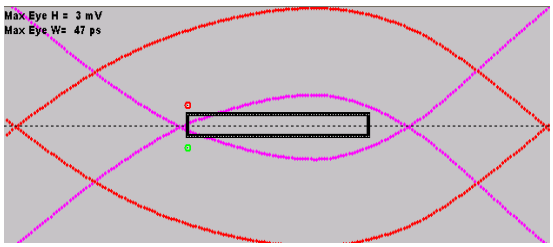
RECEIVER EYE DIADRAM WITH VARIOUS INTERLEAVING SCENARIOS

Cases	Interleaved Area	Eye Height (mV)	Eye Width (pS)
1	Non-interleave baseline	291	378
2	Interleave at package Tline only	256	369
3	Interleave at socket only	260	369
4	Combined impact of package and socket	212	328
5	Interleave at PCB Tline only	210	344
6	Interleave at package, socket and PCB	119	260
7	Mitigation effort #1: isolate channels in pin map	199	334
8	Mitigation effort #2: 2X spacing at Ch2Ch boundary	328	437

Figure 2 compares the eye diagrams of victim signal at receiver with and without CH2CH Xtalk. The inner eyes in the plots showed the receiver eye with crosstalk impact. Apparently, the voltage and time margin losses are disastrous and it demonstrates lack of consideration for read-write crosstalk can cause catastrophic failure in design.



(a) Eye Diagram of Non-Interleaved Design



(b) Eye Diagram of CH2CH Interleaved Design

Fig. 2. Eye Diagrams Of Initerleaved And Non-Interleaved Design

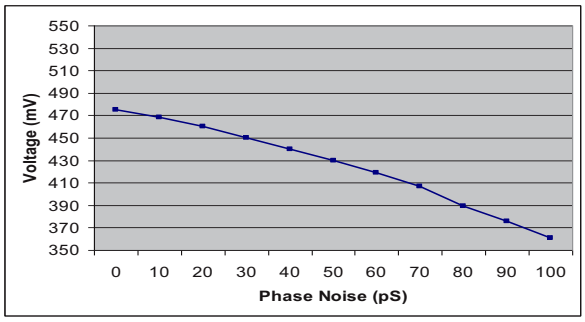
Cases 7 and 8 in Table I show two approaches to effectively mitigate the channel to channel crosstalk. If the pin map is changed to isolate two channels in socket, and interleaving still exists in the package and board routing, voltage and timing margins will recover 80 mV and 74 pS, respectively. If, for better isolation, the spacing between the two channels is doubled in package and board routing, the channel-to-channel crosstalk impacts will be removed completely.

Another effective approach not covered in Table I, but popularly applied in the real design, is to route the two channels in different routing layers to isolate their signals.

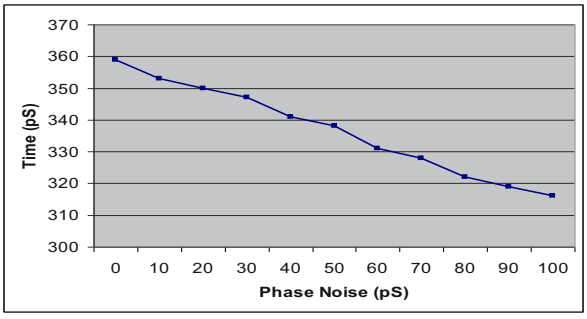
III. Byte-to-Byte Phase Noise Impact in DDR3

Phase noise exists between DDR3 byte groups mostly due to driver skew and routing length difference. The phase noise impact is significant and cannot be neglected in the high speed memory bus design. Exploiting the same DDR3 bus as shown in the last section as the test vehicle, running at 1600 MT/s, the phase noise is swept from 0 ps (in-phase) to 100 pS to investigate the impact on the data signal straddled at the byte–to-byte boundary. In this simulation, 3 aggressors from within byte and 3 aggressors from the neighboring byte are taken into account.

From Figure 3, it is observed that timing and voltage margin continuously degrade as the phase noise increases. The eye height and eye width will lose 114 mV and 43 pS, respectively, when the phase noise is at 100 pS. The margin loss of this magnitude is intolerable in any design and needs to be resolved.



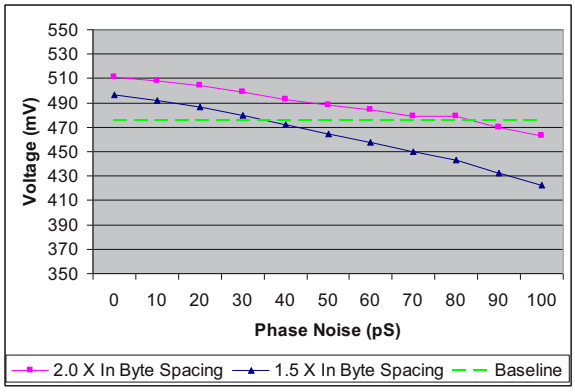
(a) Eye Height Trend



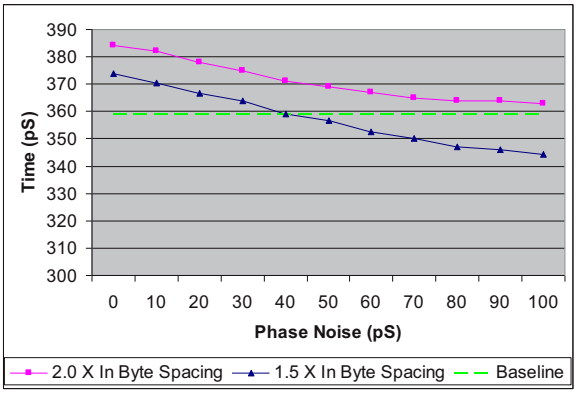
(b) Eye Width Trend

Fig. 3. The Impact Of Phase Noise on Voltage And Timing Margins

Although increasing routing spacing is well known as the most effective way to alleviate the phase noise crosstalk, delicate simulation effort is still worthwhile in finding the adequate separation distance to make it neither too small to alleviate the crosstalk sufficiently, nor too big to waste precious routing space. Using the in phase crosstalk level as the baseline, Figure 4 clearly indicates that by doubling the routing spacing between bytes, the phase noise impact, even at 100 pS, is well managed.



(a) Eye Height Trend



(b) Eye Width Trend

Fig. 4. Byte-to-Byte Spacing Increase to Mitigate Phase Noise Impact

IV. Within Channel Interleaving and DOE Analysis Method in GDDR5

Section II focuses on the channel-to-channel crosstalk, which requires larger separations at the channel boundaries in DDR3 interface. For GDDR5, similar issue also exists within the channel as well as in channel boundary, and needs to be considered. With a faster speed (3-6GTs) and faster transition (7-12V/ns driver edge rate), the crosstalk noise is aggravated and often causes problem for certain sensitive signals even within the channel.

Figure 5 shows the signal groups in a typical SGRAM device [3]. As seen in the plot, different signal groups have different transaction directions. For instance, DQ/DBI lanes are bi-directional; EDC signals are input only to controller;

WCK, CK, address, and command signals are output only to controller. The signals could have simultaneous transactions that cause read-write crosstalk. This is defined as within-channel interleaving, which could lead to catastrophic failure if not designed carefully.

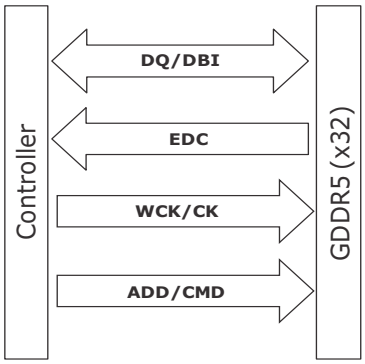


Fig. 5. GDDR5 Signal Groups Within A Channel

One of the sensitive signals is the Error Detection Code (EDC) signal. In GDDR5, the EDC signal is used to provide error detection on the data bus to improve system reliability. One EDC signal is assigned to each byte and is usually routed together with other DQ/DBI signals within the same byte. As one can see from Figure 5, when DQ/DBI signals travel outbound from controller, and EDC travels inbound into controller, read-write crosstalk from all the aggressors will couple directly into the EDC receiver at controller. This scenario is even worse than the channel-to-channel crosstalk, as coupling occurs on both sides of the victim signal.

A typical GDDR5 channel, running at 4GT/s and with 6 aggressor signals, is used here as the test vehicle. The 3-step process as shown in Section II is used to account for crosstalk effects. In addition, Design-of-Experiment (DOE) method [4] is used to capture interconnect variations, such as length and impedance. A Response-Surface-Model (RSM) [4] is built to identify the worse case in High-Volume-Manufacturing (HVM) environment.

All-phase crosstalk needs to be examined here due to two reasons: 1) GDDR5 bus does not have phase matching for all signals and utilizes per-bit skew to center the eye; 2) interleaved victim and aggressors usually don't have phase relationship constraints in real application.

Figure 6 illustrates the 2-D routing as well as 3-D PTHs and adjacent ground PTHs in a multi-layer package. 2-D interleaving refers to the off-phase crosstalk at the 2-D routing sections, while 3-D routing refers to the off-phase crosstalk at the PTHs, which are routing the signals from top-side down to back-side by going through multi-layers in the length of 800 um- 1000 um vertically. Normally, GND PTHs to signal PTHs distances are minimized within 200 um to provide good return paths.

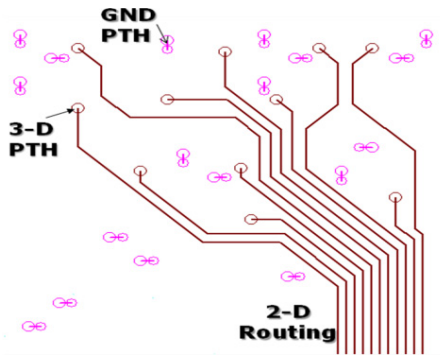
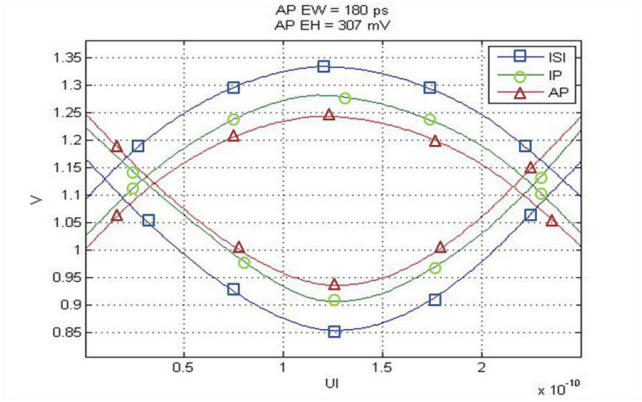
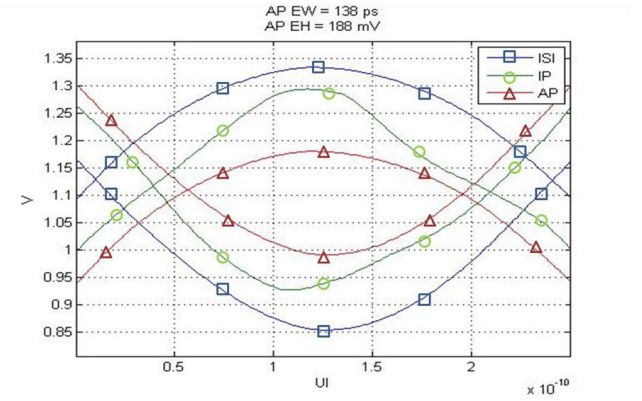


Fig. 6. 2-D and 3-D Interleaving in Package

Figure 7 shows the eye diagram comparison for interleaving in package 2-D routing section only. As one can see from Figure 7b), the in-phase (IP) eye looks distorted and it is due to artificially fixed phase relationship in read/write transactions in simulation. When all-phase (AP) is considered, the eye clasps with worst case phase relationships that could happen. Interleaving in package routing causes 119mV eye height loss and 42ps eye width loss, respectively. The impact is significant due to the smaller bit width at 4GTs speed.



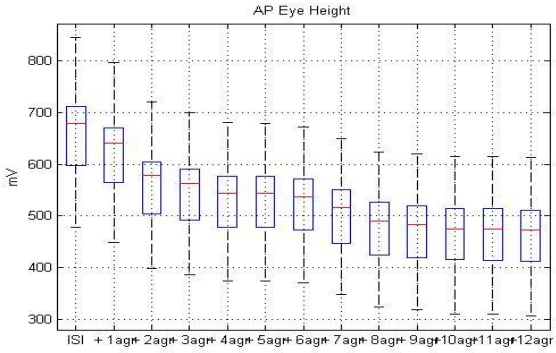
a) Non-Interleaved Eye



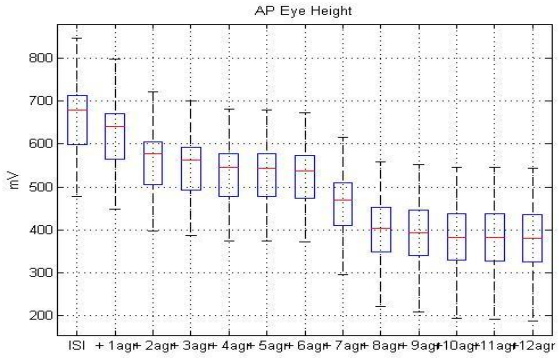
b) Interleaved Eye

Fig.7. Receiver Eye Comparison with Package Interleaving

To further understand the interleaving impact, the aggressor contribution to eye height is plotted out in Figure 8. In this figure, each vertical box represents the DOE margin spread in HVM, and moving from left to right, one can see the ISI eye height, and distribution change adding one aggressor at a time, till max of 12 aggressor nodes. The first 6 aggressor nodes are FEXT nodes from non-interleaved sections. The next 6 nodes (7-12) are defined differently depending on interleaving status - In the non-interleaved design, they are FEXT nodes from target section in read transaction. In the interleaved case, they are NEXT from target section in write transaction. As one can see, aggressor nodes 7-12 (NEXT) have far bigger impact to eye height in the interleaved design, and therefore cause the big voltage margin degradation.



a) Without Interleaving

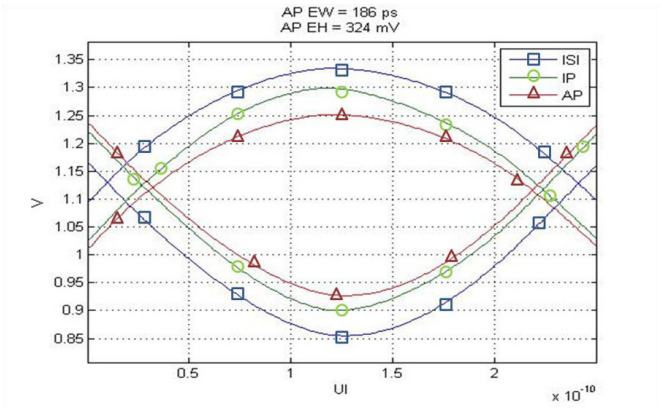


b) With Interleaving

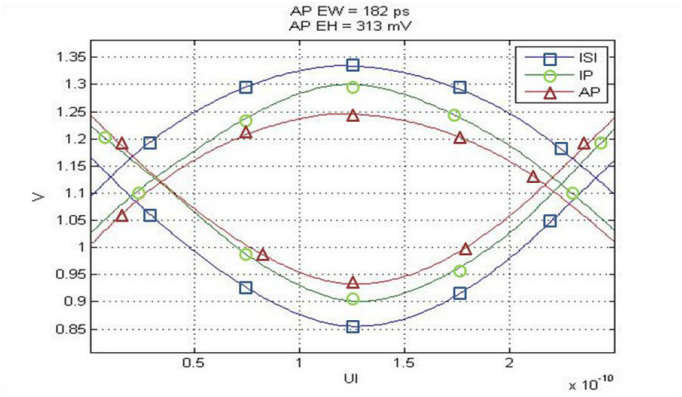
Fig. 8. AGGRESSOR IMPACT FROM PACKAGE INTERLEAVING

Using same approach, similar analysis is done for the package and board 3-D Plated-Through-Holes (PTHs) to compare with the package 2-D interleaving.

Figure 9 shows the comparison for non-interleaved and interleaved 3-D PTH sections. Interestingly, interleaving in the 3-D vertical PTH section does not produce significant margin loss as compared to package interleaving. The eye height and eye width loss are merely 11mV and 4ps, respectively.



a) Non-Interleaved Eye



b) Interleaved Eye

Fig. 9. PDA EYE COMPARISON FOR 3-D VERTICAL INTERLEAVING

Table II summarized the eye margin comparison for the two interleaving scenarios in GDDR5 interconnect. To alleviate the impact due to package 2-D interleaving, better isolation is implemented between EDC lines and all other data signals. The spacing is chosen so that the NEXT from aggressors is reduced to an acceptable level. With this approach, the adverse effect of interleaving is eliminated.

TABLE II

MARGIN COMPARISON SUMMARY FOR GDDR5 CASE STUDY

Cases	Interleaved Area	Eye Height (mV)	Eye Width (pS)
1	Non-interleaved package 2-D	180	307
2	Interleaved package 2-D	138	188
3	Non-interleaved 3-D vertical path	186	324
4	Interleaved 3-D vertical path	182	313
5	Mitigation effort: Interleaved package 2-D with design change	192	347

V. Design Considerations to Mitigate Interleaving Impact

Interleaving options affect product definition such as package layer count, package stackup, pin map definition, and PCB design, etc. Even though interleaving effects can be well captured in DOE analysis as demonstrated by above section, this type of analysis is usually much more complicated and time consuming than the traditional analysis process. One may not always have the luxury to perform the analysis for each design, as critical decisions usually need to be made early in the design phase before thorough analysis can be performed.

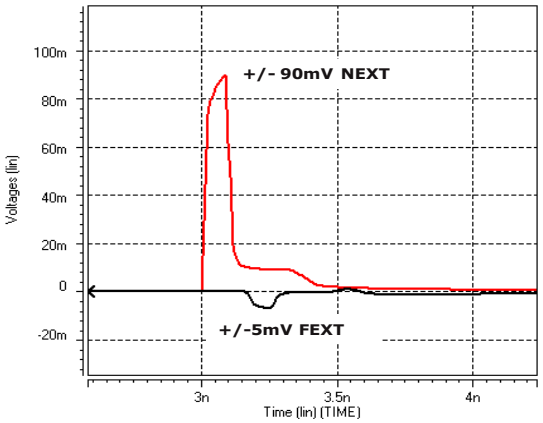
Due to this reason, the designers must understand: 1) when interleaving becomes an issue; 2) how to design it out.

To address the first question, one may consider the 2-D and 3-D interleaving comparison in previous section again. It may not be apparent why interleaving is big problem in package 2-D routing, but not in 3-D PTH sections. One has to examine the crosstalk behaviour for these sections to gain better insight.

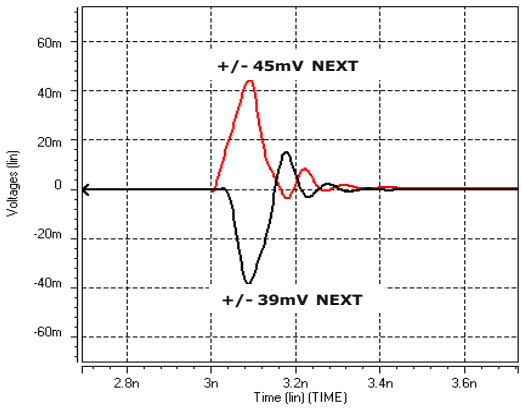
Figure 10 shows the NEXT and FEXT comparison for the package 2-D routing and the 3-D vertical path. As shown in figure 10a), the FEXT is very small, +/-5mV p-p; however, the NEXT amplitude is very large, +/-90mV p-p. This is the typical behavior in package stripline routing, which has symmetric stackup. In addition, the NEXT has much longer duration than FEXT that span across multiple bits. Both of these effects will degrade margin significantly.

In contrast, NEXT and FEXT from the vertical 3-D section have similar amplitude and duration, as shown in 10b). Even though the crosstalk has relatively large magnitude (compare to package FEXT), the difference between FEXT and NEXT is small. This is the reason why interleaving in this particular 3-D structure doesn't produce much degradation compared with non-interleaved case.

In summary, 2-D routing in stripline does not contribute too much to in-phase crosstalk, but causes dramatic degradation when interleaved; while 3-D routing (PTH) produces appreciable in-phase crosstalk, but does not causes extra degradation even when interleaved.



a) Crosstalk from Package 2-D Routing



b) Crosstalk from 3-D PTHs

Fig. 10. NEXT/FEXT Comparison for 2-D/3-D Interleaved Sections

In similar fashion, one could study the crosstalk behaviour for any given section in the interconnect, in order to assess the rough interleaving impact. Based on analysis work and comparison, a given section should not be interleaved if: 1) NEXT has much larger amplitude than FEXT; 2) NEXT has much longer duration than FEXT. If either condition is true, further analysis is needed to quantify the impact of interleaving.

In summary, this section provides a straightforward method to assess the interleaving impact by comparing the NEXT and FEXT for any given section in the interconnect. The example is from GDDR5 interconnect, but the general approach is applicable for any other parallel interface as well as serial interface.

VI. Summary of the Learning and Methods

This paper comprehensively examined the severe impacts of off-phase crosstalk on high speed DDR and GDDR memory buses. It outlined the procedures to quantitatively analyze the impacts due to read-write crosstalk and phase noise. It also originally provided a method to assess the interleaving impact by comparing the NEXT and FEXT for any given section in the interconnect. In addition, this paper demonstrated the design approaches to effectively alleviate or even design out the off-phase crosstalk. These analysis methods and considerations are crucial in design to achieve faster speeds for single-ended memory busses.

Bibliography/References

[1] Howard W. Johnson, Martin Graham, "High-Speed Digital Design", New Jersey: Prentice Hall PTR, 1993.

[2] Stephen H. Hall, Howard L. Heck, "Advanced Signal Integrity for High-Speed Digital Design", New Jersey: John Wiley & Sons, Inc., 2009.

[3] JEDEC GDDR5 SGRAM specification, ballot template version draft revision G, 2005.

[4] Meyers, Raymond H., and Montgomery, Douglas C., Response Surface Methodology: Process and Product Optimization Using Designed Experiments, J.W. Wiley, 1995.