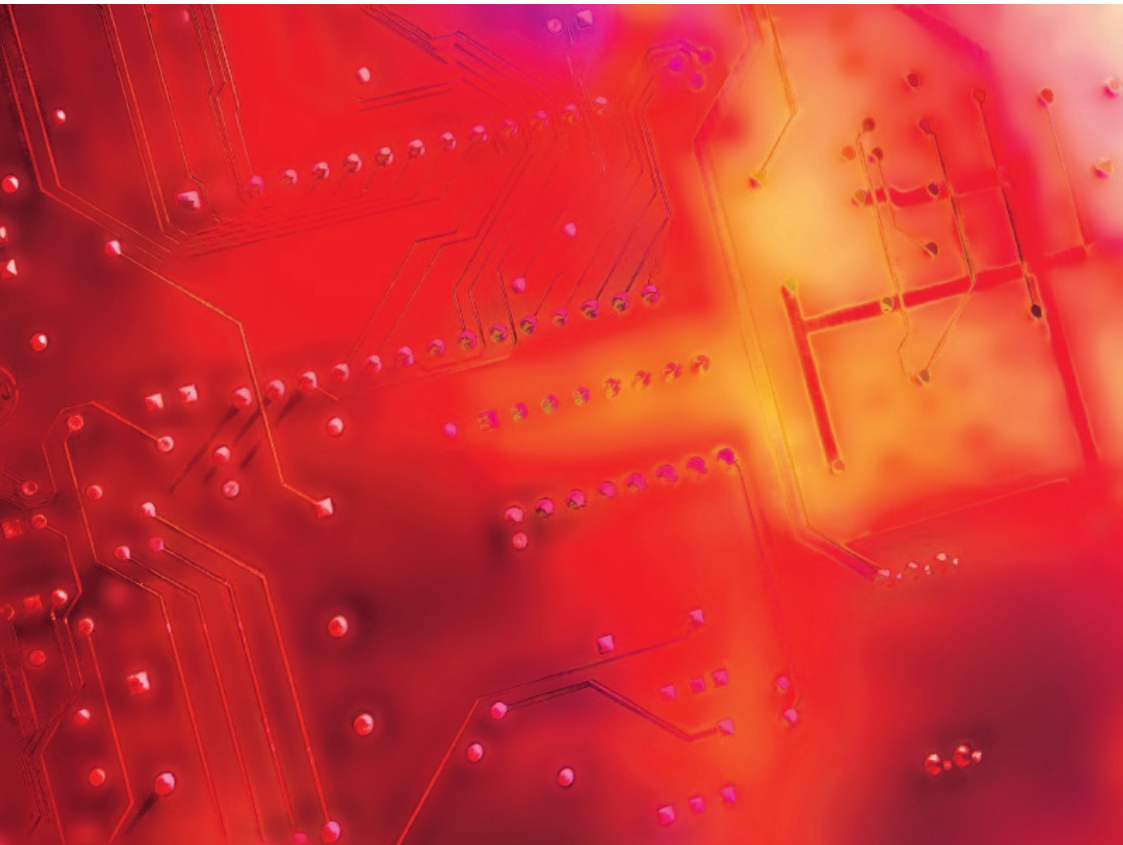
intellect
REPRESENTING THE UK TECHNOLOGY INDUSTRY

# PCB data design guide

## A guide for PCB designers placing an order with a fabricator



## A guide for PCB design data

PCB fabricators have, for some time now, struggled with how to encourage designers and customers to ensure that the data they provide is always complete and accurate. Poor data at any point in the process can at best slow it down, and at worst lead to end products that are not fit for purpose. To help mitigate this risk, Intellect's PCB Fabricators and Suppliers Group has developed this checklist to help ensure that the design data provided for PCB manufacture is as clear, accurate and comprehensive as possible. This guide is intended to help designers consider all the issues and questions that need addressing to enable the PCB Fabricator to produce the product they require.

## Preferred input formats (these are displayed in order of preference)

**Board Layers**

1. ODB++
2. Gerber 274x
3. Gerber 274d
4. Dpf

**Drawing Layers**

1. HPGL
2. PDF
3. DXF
4. Gerber 274x
5. Paper

**Drill Tapes**

1. Excellon II
2. Gerber 274x
3. EIA
4. Sieb Meyer

**Nelists**

1. IPC-356
2. Mentor
3. Meyer

## How to supply data effectively

### First check

- ☐ Is the data you are supplying in the format shown above?
- ☐ Does the data you are supplying contain a layer that has an accurate board outline or a dimensioned drawing that references a drilled hole?
- ☐ Can the data you are supplying be used to create a rout tape?
- ☐ Does the data you are supplying contain a drill report with finished sizes with tolerances and counts, which tie up with the supplied drill layer?
- ☐ If the data you are supplying is not ODB++, does it contain a text file with layer order and build information, as well as a netlist file in one of the above-mentioned formats?
- ☐ If the data used is old Gerber 274d, is the associated aperture table included within the data package?

## Now, more specifically

- ☐ If there are any differences between the data and the supplied netlist (star points or links), have you identified their positions in the Readme file so the fabricator will be aware of their presence?

- ☐ If the design contains controlled impedance tracks, have you supplied a drawing or text file with the required impedance value and tolerance along with reference plane details? In the Gerber file, make sure the impedance tracks are a unique track width to allow for easy adjustment.

- ☐ Where impedance is used, have you allowed for structure adjustment, line width and dielectric separation to ensure the fabricator can fine-tune the impedance?

- ☐ Have you specified whether there is a TDR test requirement?

- ☐ Are any mechanical drawings dimensioned in one format (metric is preferred, but imperial may be used, but not both)?

- ☐ When outputting plane layers to Gerber 274x, have you ensured that the surfaces option is not used?

- ☐ If plane layers are being outputted as a positive image, has a unique line size for creating the draw/fill been used?

- ☐ Have you avoided using line filled plane layers (these increase CAM time significantly) and used contourised block data or negative fill instead? Or, where line fill must be used, have you used the largest feature possible and provided a unique value?

- ☐ Have you avoided using cross hatching (it will increase the volume of DRC violations, thereby slowing the engineering process and increasing sliver risks)? Or, where cross hatching must be used have you ensured that the line width chosen is unique?

- ☐ If scoring is required have you ensured that there are no tracks or pads closer than 20 thou to the edge of the circuit. A solder mask clearance should be introduced (The proximity of the surface features to the top of the angled cut edge is critical. This will be in-board, as the true board edge is the base of the score. It is imperative that the surface features are protected.)?

- ☐ On silk screen legends have you ensured that there are no line widths smaller than 5 thou and no character widths/heights of 40 thou or greater?

- ☐ Have you checked that oversize solder mask clearances are not oversized by too much? (This causes additional CAM processing. The resist needs only to be increased by 5 thou (127um) minimum, so long as it does not cause slithers of less than 3 thou between surface mount pads.)

- ☐ If you have a solder resist clearance on one side with a hole drilled through it, have you ensured that there is a resist clearance on the other side? (otherwise you will get solder resist trapped down the holes creating a chemical trap with potential corrosion damage).

- ☐ If the PCB contains surface mount devices and will be automatically assembled, have you supplied a solder paste layer? (Although this is not required for manufacture, if the fabricator has to step the PCB in a frame, the paste screen manufacturer will need the fabricator to supply the stepped paste along with step and repeat instructions as appropriate.)

- ☐ Have you ensured that holes are not placed close to adjacent BGA land? (Small pitch component via holes will be close to solder sites. There must be room to create a solder mask barrier to the solder joint. If not, the via hole must be filled with resin.)

- ☐ If slots are included in the design, have you ensured this is noted on the drill drawing or drill report (as some design stations will output slots as two drills, one at either end of the slot, but unless this is noted it is not understood how to convert these holes into the required slot size)?

- ☐ Have you identified the plating requirements of holes and slots and where features are to be un-plated noted this? (Tolerances should be set against the finished feature size. Via holes should be shown with a large lower tolerance, e.g. 0.3 mm +0.05 / -0.3.)

- ☐ If it is required that the PCB be supplied in a panel, have you supplied information about the following?

    - ☐ Panel size
    - ☐ Number of PCBs in the panel
    - ☐ Number and size of fiducials and positions
    - ☐ Number and size of fixing holes and positions
    - ☐ Details and positions of breakout pips
    - ☐ Whether the fabricator can add copper thieving to the waste areas of the panel

- ☐ Have you listed acceptable modification to the data set? (This might include non-functional pad removal, addition of teardrop connections, thermal rotation, inclusion of fabrication tooling within the support biscuit, soldermask adjustment, copper trimming from board edges, pin hole and sliver filling.)

- ☐ If you require the fabricator to supply you with the stepped solder paste, or if you require the step to be approved before manufacture, have you informed the fabricator?
- ☐ Have you provided e-mail addresses and phone numbers for the designers, as well as the buyer?
- ☐ If your job or a similar job has been made before and you need the fabricator to make your new version to match this panelisation, have you provided the previous part and order number?
- ☐ If you are working on an up issue, have you incorporated DFM feedback from the previous design?
- ☐ Have you listed acceptable data modifications that can be achieved without formal authorisation?
- ☐ Have you clearly stated any minimum acceptance criteria e.g. IPC-6012 class 2? (These criteria affect cost, tooling and manufacturing time.)

**Intellect works with and for members to:**

- **develop the UK's capability to support a strong and growing technology sector**
- **improve their business performance by**
  - **providing insights into markets and supply chains and constructively influencing their development**
  - **engaging with government and regulators to create the most favourable environment for growth and employment**
  - **maintaining the industry's reputation and championing its strategic importance**
  - **sharing and promoting best practice**

**For more information visit www.intellectuk.org**

intellect
REPRESENTING THE UK TECHNOLOGY INDUSTRY

Intellect
Russell Square House
10-12 Russell Square
London
WC1B 5EE

T 020 7331 2000
F 020 7331 2040
E info@intellectuk.org
W www.intellectuk.org