HOW TO CHOOSE & PLACE DECOUPLING CAPACITORS TO REDUCE THE COST OF THE ELECTRONIC PRODUCTS

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With the edge rates of high-speed signals on boards increasing dramatically in modern PCB designs, it becomes more challenging to manage clean power supplies. The number of decoupling capacitors used for a power delivery system keeps increasing as well. This causes two problems for board designers and layout engineers: 1) How to determine the numbers and the types of decoupling capacitors needed for a particular design; and 2) Where to place the selected capacitors on board. Without a clear set of tools and methodologies to solve these two problems, many boards would have to be treated in a pessimistic and conservative way and would end up with a lot of unnecessary decoupling capacitors, which increases design cost, reduces board reliability, and also makes it extremely difficult to place and route capacitors in a limited board space.

This paper provides a solution for board designers to choose decoupling capacitors early in the design process. It illustrates how it is not a good practice to place decoupling capacitors with fixed values at every pin of a chip with the fastest switching speed. The method described in this paper shows how a more effective decoupling can be achieved with fewer decoupling capacitors. A real design example will be given to show the savings on capacitors and board space when applying such a selection method. The paper

also presents the case that it is not always necessary to place these capacitors close to the power pins of the ICs that the capacitors are designated to associate with. The actual distance of the decoupling capacitor from the power pin varies based on the value and other characteristics of the decoupling capacitor

DESIGNING POWER DELIVERY SYSTEMS

Using target impedance to describe the behavior of a power delivery system has been widely accepted. Considering the voltage ripple budget when worst transient current occurs, target impedance has been defined as follows [1

$$Z_{t\,\mathrm{arg}\,et} = \frac{(power\_\mathrm{sup}\,ply\_voltage)\times(allowed\_ripple)}{current}$$

For reliable operation of a power delivery system, its impedance spectrum needs to be maintained below the target impedance at the frequencies from DC to $f_{max.}$ The f_{max} can be evaluated according to the edge rate of the fastest chip powered by the power supply [1].

Due to the scales of ICs, packages and board, larger values of decoupling capacitors on a board work at lower frequency range. In addition, smaller package and die capacitance is effective in the higher frequency range, and plane capacitance dominates at even higher frequencies. It is important to understand this and to look at each frequency band independently.

Based on this understanding, decoupling capacitors can be chosen first without taking into account the effects of power and ground planes. For example, the blue trace in Figure 1 shows the frequency responses of a general plane pair. The first serial resonance peak (lowest resonance frequency point which is based on the size of a regular shaped plane) does not occur until the frequency reaches f_0. To keep the distributed impedance of a power delivery system below the target impedance, decoupling capacitors are needed in the frequency range from DC to f_d. If decoupling capacitors are correctly selected, the actual response becomes what is shown as red in Figure 1. The overall distributed impedance from DC to f_0 is kept under the target impedance, while the first resonance frequency peak of the plane remains almost un-changed. This shows that, in general, we can design the power delivery systems with two separated steps.

When the physical size of a plane is large enough, its lowest resonant frequency can fall into the effective ranges of small values of decoupling capacitors. Then, these capacitors need to be carefully selected to overcome plane resonance effects

PROCEDURE FOR DEVELOPING POWER DELIVERY STRATEGY OF A PCB

Step 1. Determine the optimum number and type of decoupling capacitors needed

Traditionally, (as many IC companies still do) designers follow IC manufacturers' recommendations to use decoupling capacitors with fixed values (for example, 0.01µF) at every pin of the chip with fastest switching speed. It can be proven through a tool like SQPI that this recommendation is not only expensive, but it also introduces higher distribution impedance. This typical approach also is likely to increase the cost of components for a design (more decoupling capacitors than necessary) and adds to congestion near a high pin count components such as BGA, which can lead to higher layer count for routing. Figure 2 demonstrates the impedance peak caused by selecting too many capacitors with same value.

The design of power delivery on PCBs is realized by voltage regulators, bulk capacitors, ceramic capacitors and planes (as frequency range of operation increases). Each of these types has its own effective frequency range, as shown in Figure 3. Power and ground planes behave like a large capacitor at the working frequencies of bulk and ceramic capacitors. With proper capacitor library and analysis engine, one can use the "single node analysis method" to simulate the frequency responses of an arbitrary group of decoupling capacitors to see if the distributed impedance is under the pre-defined target impedance [1]. By adding more capacitors and changing capacitor values when repeating the simulation, a set of bulk and ceramic capacitors with determined types and values is eventually achieved.

Another important practice in selecting decoupling capacitors is to have every two neighboring resonance points apart from each other by 2 decades, to eliminate anti-resonance peaks, as shown in Figure 4. Our experience shows that choosing decoupling capacitors with the method proposed here can easily help designs save about 40% of capacitors in many cases. The gain in cost saving can be more significant if we consider that fewer capacitors mean fewer vias and more space for component placement and routing.

One problem designers often encounter is that the resonance peaks shift when decoupling capacitors are placed on boards. This is due to the effects from planes and capacitor distribution. One should not try to match the new resonance point and measure the errors between the shifting, but to ensure that the distributed impedance over the required frequency range is still under the target impedance.

A key factor to successfully select decoupling capacitors is the right set of capacitors, which has most commonly used capacitors with accurate ESR (equivalent serial resistance), ESL (equivalent serial inductance) values and mounting inductance. The ESR and ESL values provided in capacitor catalogs / datasheets may not be accurate enough for high-speed PCB power delivery system designs. Many of them do not even include ESL values in the capacitor datasheet. Decoupling capacitors with low mounting inductance is beneficial to the decoupling strategy. Figure 5 compares the frequency responses of capacitors with different mounting inductances. Mounting inductance is a function of the fan-out of surface-mounted capacitors and the layer stack up used for design. This is the main reason why single node analysis alone is not sufficient for developing the power delivery system.

A design example from Huawei Technologies illustrates the points made in this paper. A power integrity analysis was performed to the power delivery system V33 of a production board with 24 ICs. The maximum switching current was calculated as 2090.30mA. Given the 5% ripple requirement with the 3.3V voltage supply, the target impedance of this power supply network was 78.9mΩ. The original design has the following decoupling capacitors as shown in Table 1. There are 30 TAN-caps on the board.

Table 1 Capacitors of V33 system

Cap package	Cap material	Cap value	Cap number
0603	X7R	0.01uF	25
0603	X7R	0.1uF	50
0603	X7R	1000pF	16
1210	Y5V	10uF	2
	A1	330uF	1
3528	TAN	10uF	30

Using the strategy described earlier, we can analyze whether or not these 30 TAN-caps are necessary. Our measurements reveal that there is significant margin in the range of 2MHz – 10MHz, compared with that in the range of frequency higher than 50MHz. This indicates that the number of TAN-caps with working range at 1MHz – 10MHz can be reduced. Figure 6 shows the measured frequency impedance profiles of the original 30 TAN-caps from DC to 20MHz where only TAN-capacitors operate, and Figure 7 shows the measured profile with 18 of them taken out. Compared with the time domain measurement, when the number of TAN-caps is reduced, only a fraction portion of noise can see an increase. This also indicates that the power noise spectrum has more high frequency components. After taking out 18 TAN-caps, measurements show that the noise amplitude at the frequency range of 2MHz – 10MHz is increased, but is still within the budget range, while power noise at high frequency range is not affected. And more importantly, the board still works normally after these 18 TAN-caps are removed. The above comparison results are consistent with the SQPI simulation results as shown in Figure 8, i.e., reducing the number of TAN-caps at lower frequency range only affects the filtering effectiveness at low frequency, not at high frequencies.

This design example demonstrates how SQPI can be used to determine and guide decoupling capacitor selection. Similar analysis can also be applied to the other decoupling capacitors on the same board to obtain the final decoupling design.

With correct decoupling capacitor selecting strategy, a great number of decoupling capacitors can be saved, which gives the designer more freedom to place other components on board, helps increasing the board reliability and reduces product cost significantly.

Step 2. Power plane effects in power deliver system

Once decoupling capacitors are determined with single node analysis, plane effects can be investigated using multiple node analysis provided in SQPI. It is recommended to perform pure plane analysis first without any decoupling capacitor placed. For the designs of backplanes and large PCB in communication equipments, the first resonance frequency point can happen at as low as a couple of hundreds MHz with resonance amplitudes exceeding target impedance. Smaller ceramic capacitors are then needed to reduce the impedance amplitude at these frequencies. Their numbers and values can be determined by running the “multiple node analysis” multiple times [1]. In the cases that the magnitudes at resonant frequencies within required range are below the target impedance, or that the resonant frequency points with magnitudes above the target impedance are out of required range, no further work is needed.

In the designs in which one plane pair cannot provide low enough impedance in required frequency range, multiple plane pairs or reducing plane gaps have to be considered.

Step 3. Rules for placing and routing of decoupling capacitors

Placing decoupling capacitors is always a big puzzle to designers. One problem with placing and routing is fanout. The way a decoupling capacitor is fanned out is a crucial piece to the capacitor's performance. Next to the ESR, which models the capacitor's performance at the point of first serial resonance, the total inductance of the decoupling capacitor determines, together with the capacitance, the frequency at which first serial resonance emerges. The total inductance is formed by the sum of the capacitor's intrinsic inductance plus the mounted inductance, which can be seen as the inductance formed by the current loop of the capacitor's pins connecting to the power and ground plane. The relation is quite simple, the larger the area of the current loop, the larger the inductance. Knowing this, a very simple routing rule can be determined: Keep the fanout traces short and place the capacitor on that side of the PCB which is closest to the decoupled power and ground plane structure in the stack-up.

Another question to ask is whether it is necessary to place all decoupling capacitors close to power pins of fast-switching components. The origin of this requirement is to limit the lead inductance of capacitors. This is true for the capacitors with their resonance points at higher frequencies, and such capacitors are normally of smaller values. For the capacitors with larger values, such as bulk and ceramic capacitors, their resonance frequencies are at the KHz to lower MHz range. The lead inductance effects are therefore not significant. Placement rules for these capacitors should be loosened for designers to make use board space more efficiently.

SUMMARY

With a proper methodology, right simulation tools and up-to-date capacitor libraries, users can develop a power delivery system for their design that guarantees adequate power supply at all frequencies of operation while reducing the overall cost of the PCB system being designed. This paper illustrates the strategy of obtaining such power delivery systems by describing the procedure which takes into consideration different parts in a power delivery system – VRMs, bulk and ceramic capacitors – chooses the right types of capacitors, and reduces the total number of capacitors. The paper shows with a real design example that placement and routing become easier and the cost of a board can be

reduced when fewer capacitors are used. It also maintains that capacitors with large values can be placed almost everywhere on a board, which gives freedom to layout engineers to achieve more effective board layout

REFERENCE

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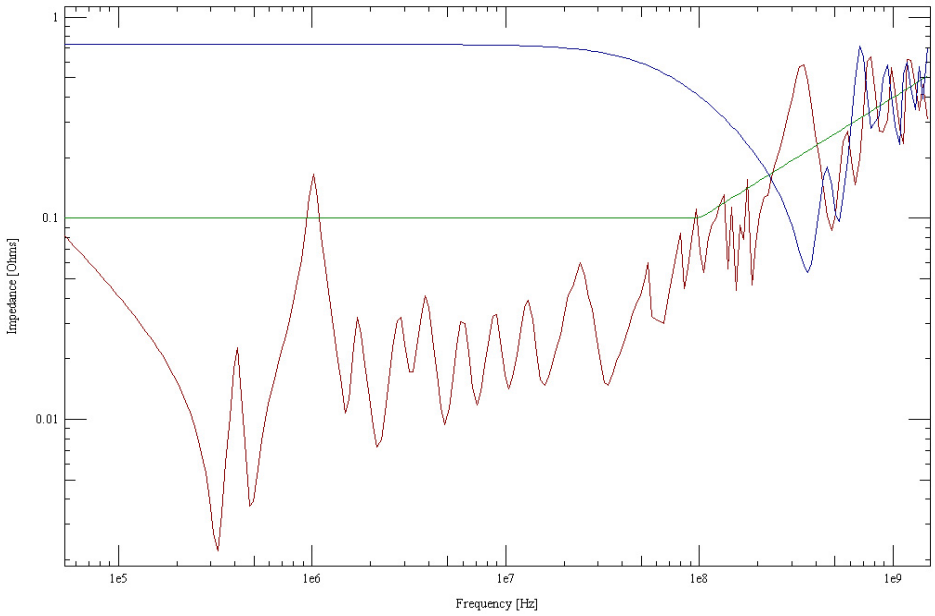

Figure 1. Frequency responses of a general plane pair with and without decoupling capacitors placed

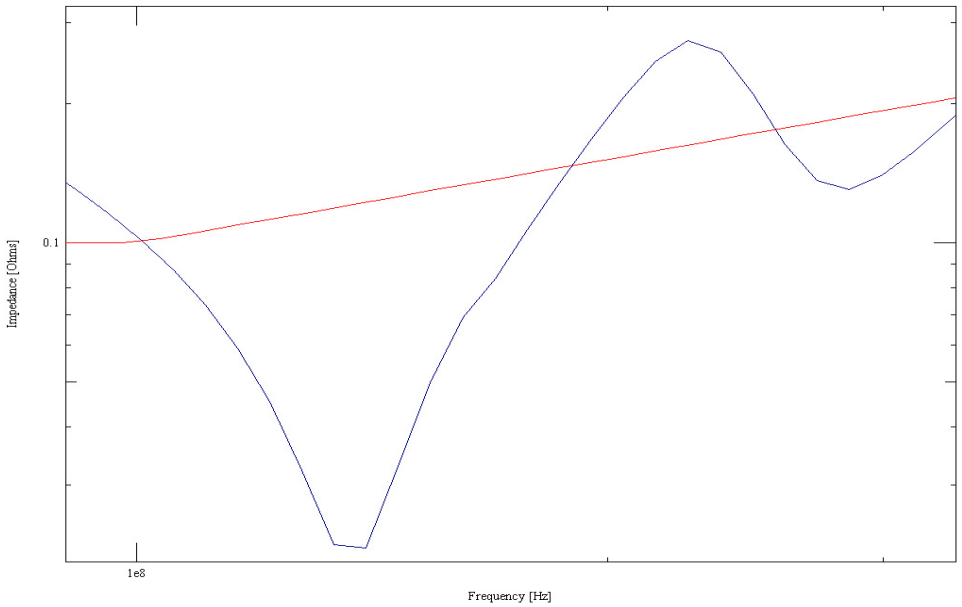

Figure 2. Impedance peak caused by wrongly selecting decoupling capacitors