

PCB Design Specifications

1.0. Introduction

Each semester, ECE477 students design PCBs using PADS or Eagle. The designs are then exported to the industry-standard Gerber file format and sent off to a fabrication house for manufacturing. There are certain manufacturing specifications that need to be met in order for your design to be manufactured correctly. The purpose of this document is to provide a list of requirements and guidelines to follow to ensure your PCBs work properly from a manufacturing and electrical standpoint.

2.0. Manufacturer Requirements

At the time of this writing, ECE477 uses [Advanced Circuits](#) for PCB fabrication. Advanced Circuits has set requirements for PCB manufacture, which are detailed at their [design specifications page](#). Relevant design specs are repeated below:

<u>Inner Layer Clearances:</u>	0.010" (10 mils)
<u>Copper to Edge of PCB:</u>	0.010" (10 mils) for outer layers, 0.015" (15 mils) for inner layers (0.020" or 20 mils is preferred)
<u>Pad Size/Annular Ring:</u>	Pad size should be +0.010" (10 mils) over the finished hole size for vias and +0.014" (14 mils) over the finished hole size for component holes
<u>Hole Size:</u>	0.008" (8 mil) minimum finished hole size, 0.015" (15 mil) or larger hole size recommended
<u>Copper Trace Width/Spacing:</u>	0.005" (5 mil) trace widths allowed, but an additional charge is assessed if design contains any features with spacing less than 0.007" (7 mils). Recommended minimum spacing: 8 mils.
<u>Minimum Silkscreen Width:</u>	0.005" (5 mils) minimum line width.

2.1. A Note About Inlaid Board Routes

Every semester, a team wants to have some sort of custom shape cut out of their circuit board, such as slots. Fabrication houses can and do offer these services, particularly to larger industry clients, HOWEVER, this is a very expensive proposition. Including board routes requires the fabrication house to retool their assembly line, and routing costs can be significant. Therefore, ECE477 does not support boards with inlaid routes. If you need to route your board, try to find a way around it, or as a last resort, silkscreen the custom shapes and cut them out carefully with a drill and rotary tool.

3.0. Power Electronics Layout Guidelines

Power circuitry often requires traces that are wider than the standard logical circuitry on a PCB. For this, it is useful to know the current-carrying capacity of PCB traces at various widths. A good resource on this is the trace current capacity table found at <http://www.armisteadtechnologies.com/trace.shtml>. Boards manufactured in ECE477 utilize 1oz. copper, so these portions of the table have been copied into figure 3.0.1.

Temp Rise	10 C	20 C	30 C
Width (mils)	Max Current (A)		
10	1	1.2	1.5
15	1.2	1.3	1.6
20	1.3	1.7	2.4
25	1.7	2.2	2.8
30	1.9	2.5	3.2
50	2.6	3.6	4.4
75	3.5	4.5	6
100	4.2	6	7.5
200	7	10	13
250	8.3	12.3	15

Fig. 3.0.1. Trace Current Capacity Guidelines
(Source: [Armisted Technologies](#))

3.1. Other Tables and Calculators

In addition to the conservative estimates provided in the table above, additional trace current tables and calculators exist for PCB design. Some of these resources are listed below:

1. Armisted Technologies: <http://www.armisteadtechnologies.com/trace.shtml>
2. CircuitCalculator Blog Trace Width Calculator:
<http://circuitcalculator.com/wordpress/2006/01/31/pcb-trace-width-calculator/>
3. ANSI IPC-2221A Trace Width Calculator:
<http://www.desmith.net/NMdS/Electronics/TraceWidth.html>
4. Advanced Circuits Trace Width Calculator:
http://www.4pcb.com/index.php?load=content&page_id=95

3.2. Other Power Layout Techniques

In some situations, current capacities need to be increased, but there is not sufficient room on the PCB to increase the width of power and other traces. To get around this problem, one common technique is to add a soldermask keepout region around the desired traces in the design layout software. Then, when the board is manufactured, these traces are left with exposed copper. Solder can then be added to the top of the trace, increasing the trace weight and thereby increasing the current-carrying capacity of those traces without making the traces wider.