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POWERING INNOVATION

Multicore Software Migration and Development – Challenges and Solutions

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Software R&D

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Agenda

- Objective
- System characteristics of a Multicore Architecture
- Challenges with Multicore Architecture
  - Application Porting Challenges from Unicore to Multicore Architecture
    - Programming Model
    - Processing Model
- Debugging Support with Multicore Architecture
  - Performance Debugging Support
  - Functionality Debugging support
- Summary

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Objective

After this presentation, you should be able to understand following:

- Challenges in effectively exploiting the Multicore SoC architecture
- Performance and functionality debugging challenges
  - Effective threading
  - Avoidance of deadlock situations
- Role of OS
  - Thread and interrupt migration across different CPUs
  - Support for thread and interrupt affinity and debugging
- Role of enhanced I/O devices in Multicore migration
  - Load Spreading
  - Data Stashing
- Debugging Support
  - Freescale proprietary debugging support
  - OpenSource debugging support

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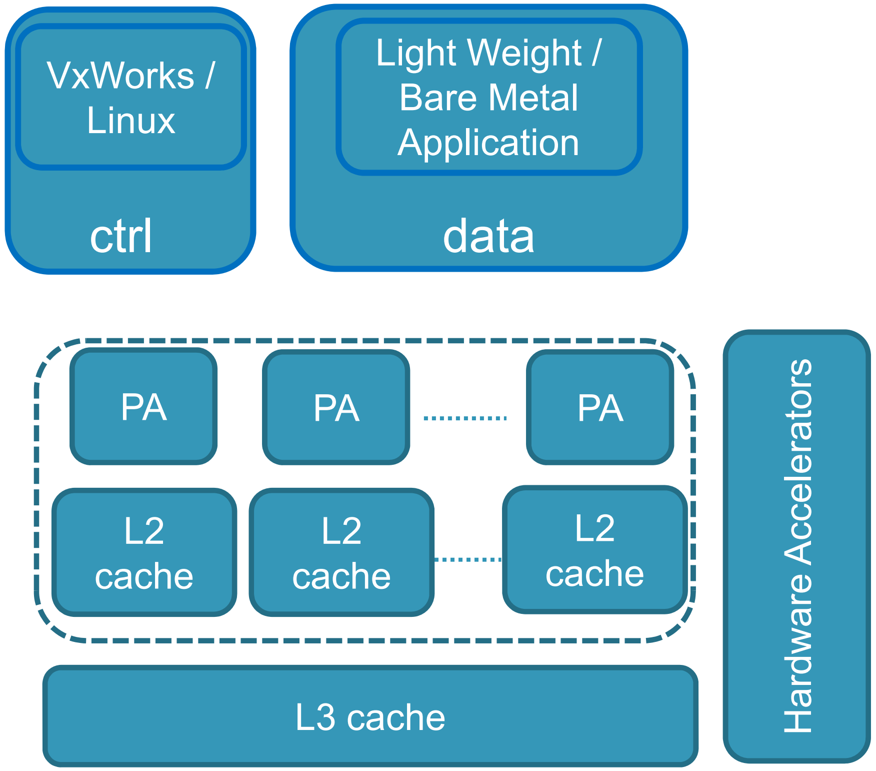
System characteristic changes in Multicore Architecture

- Homogeneous CPUs with multilevel cache hierarchy
  - Threaded cores, co-located control/data planes
  - OSes, baremetal apps running on virtual partitions
- Specialized hardware accelerators, I/O ports with support for load spreading and selective data stashing
- More powerful and complex Buses inside SoC package reduce debug application thread interaction with I/O devices



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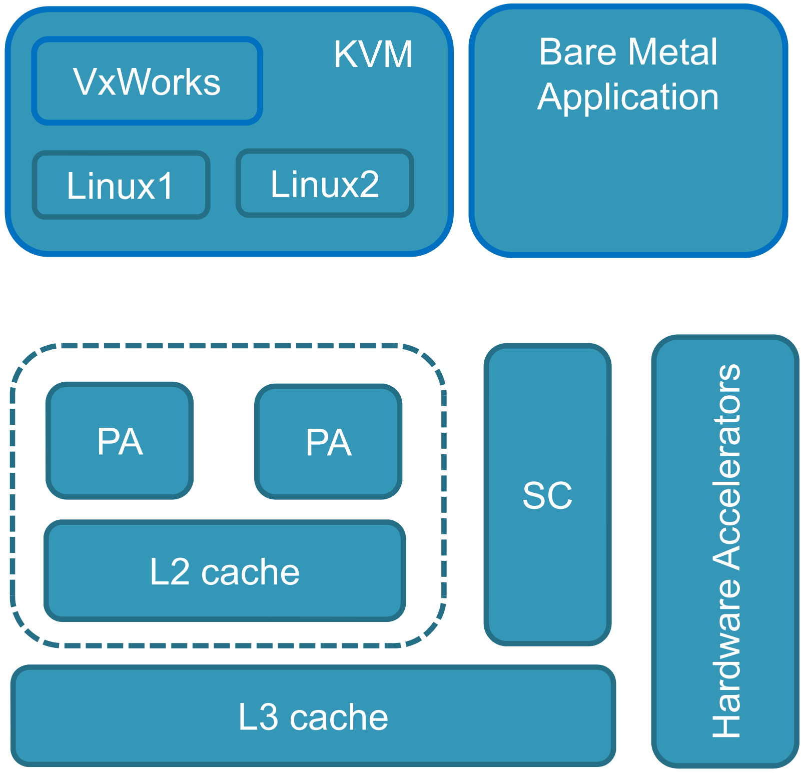
System characteristic changes in Multicore Architecture (Contd..)

- Heterogeneous CPUs with multilevel cache hierarchy
  - Threaded cores, co-located control/data planes
  - OSes, baremetal apps running on virtual partitions
- Optionally virtual machine appliance (e.g. KVM, etc.)
- More powerful and complex Buses inside SoC package reduce debug application thread interaction with I/O devices



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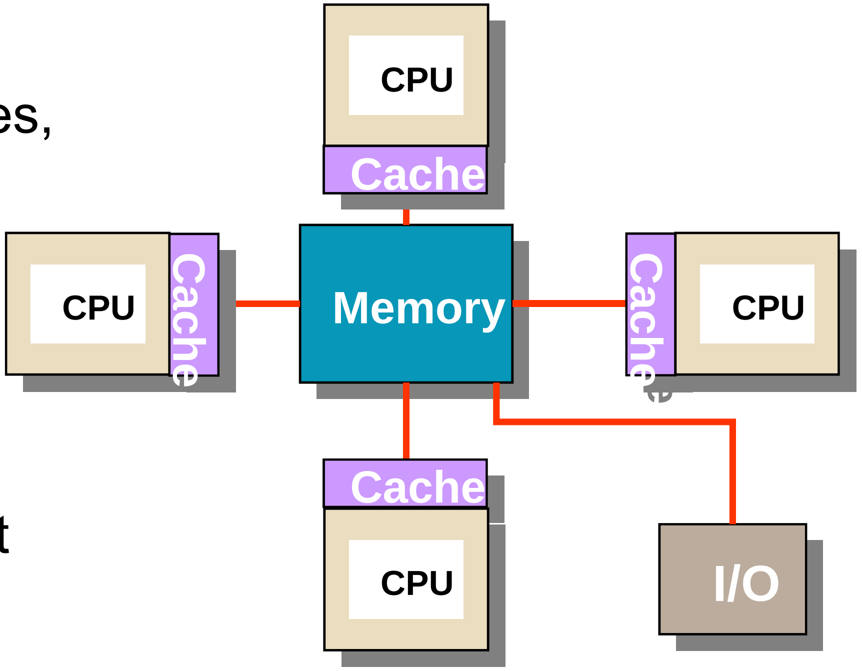
Symmetric Multi-processing (SMP)

- **SMP** is a ***multi-processor homogeneous computer architecture*** where two or more identical processors are connected to a globally shared main memory…
- Processors could be separate devices, all on 1 device or a mix
- Typically all CPUs share memory, I/O and are run one OS instance
- Each processor can run independent processes and threads
- Any idle processor can be assigned any task



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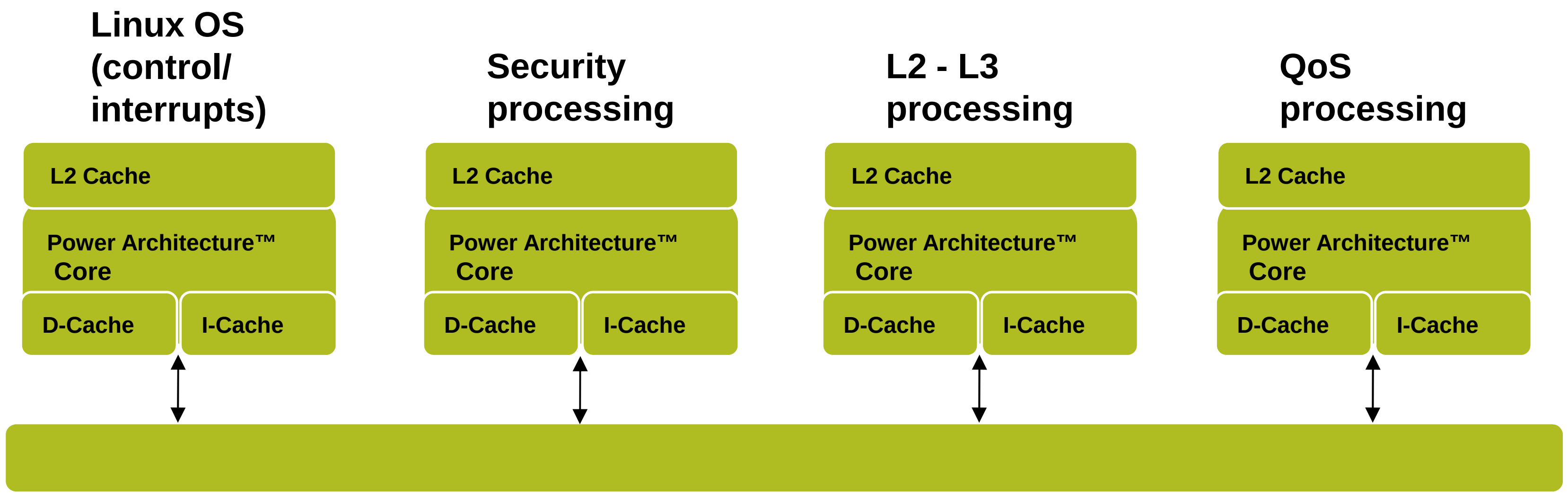
Asymmetric Multi-processing (AMP)

- A ***multi-processing usage model*** in which individual processors are dedicated to particular tasks, such as running the operating system or performing user requests
- Beware: AMP does not need to imply heterogeneous hardware! It is perfectly possible to implement a software AMP system design on SMP hardware (e.g. MPC8641HPCN Linux BSP supports both)



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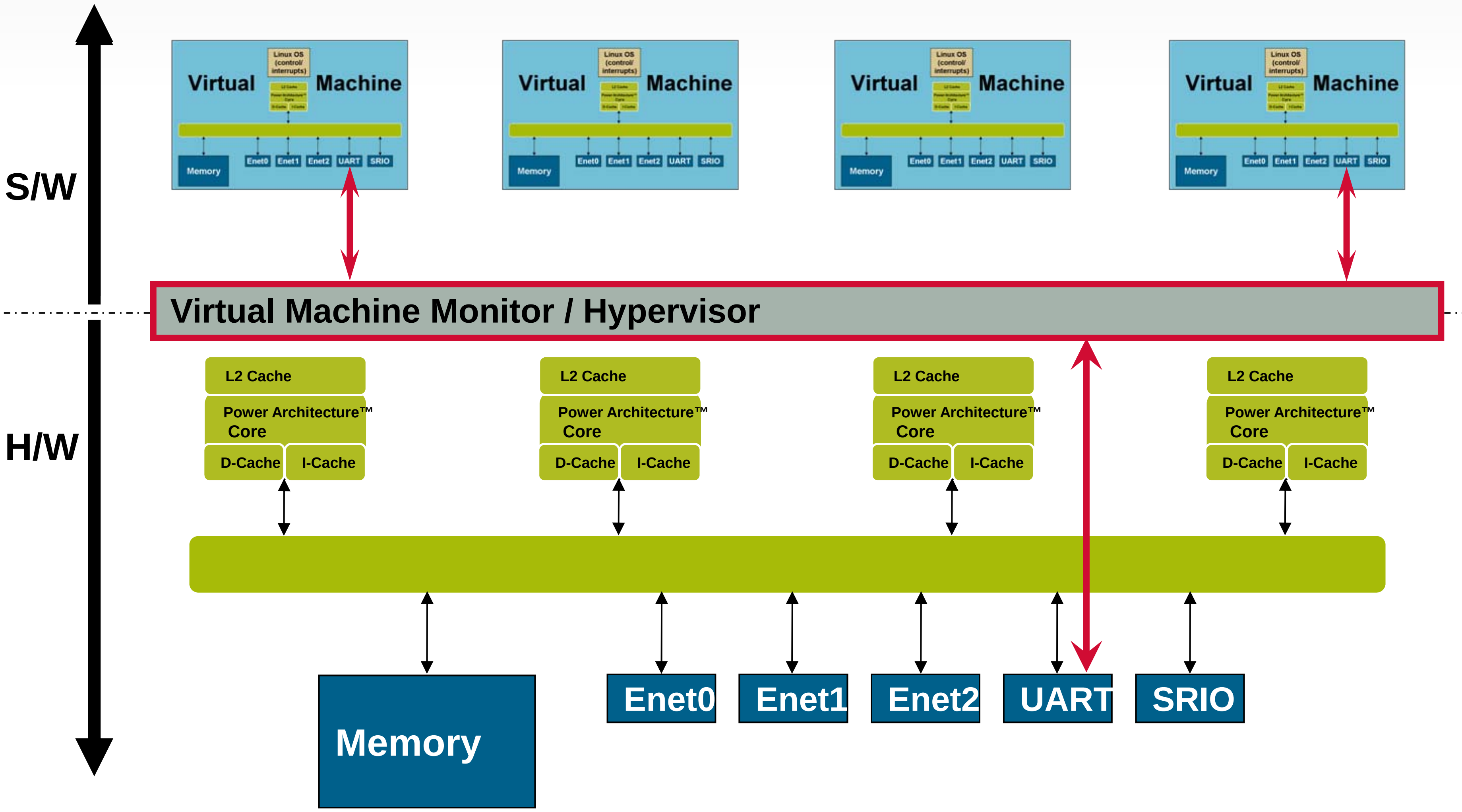
The Need for Virtualization



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Software Considerations on Multicore

- System partition (mainly cores, memory, ports resources)
- OS consideration (control plane OS, data plane bare-board or light-weighted env)
- Data plane cores working architecture (functionalities bound to each core/core-group)
- Mutext mechanism
- Data plane tables shared among all data plane cores (shared memory mechanism)
- Inter core communication mechanism
- System global variables, CPU global variables
- Rx/Tx driver
- Arch specific accelerators use
- Control plane partition and data plane partition communications

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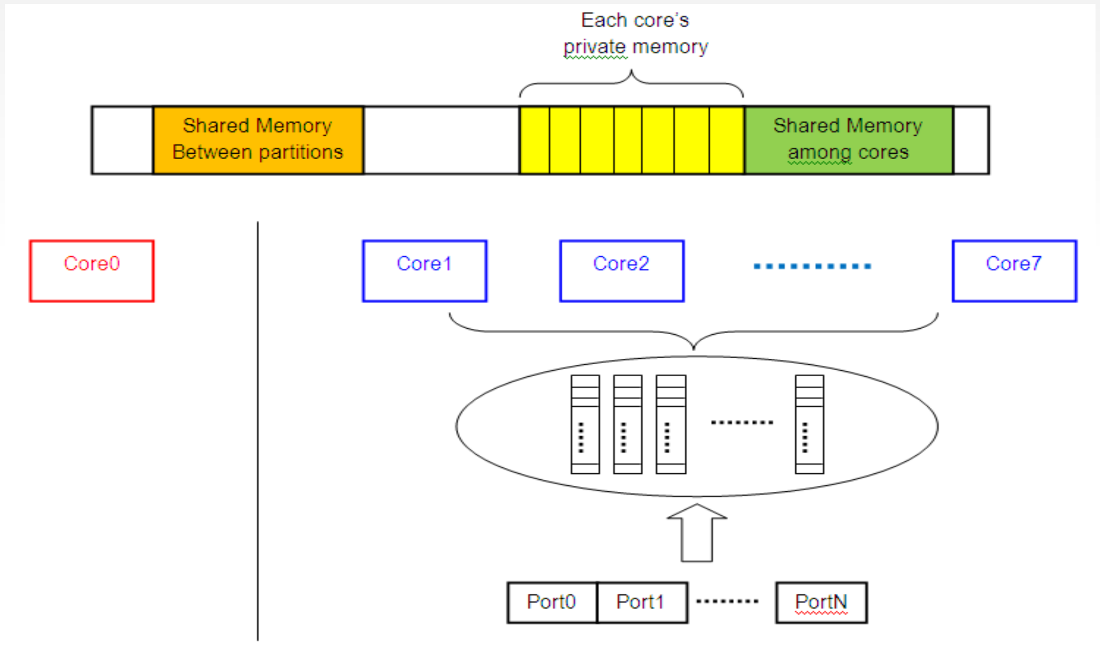
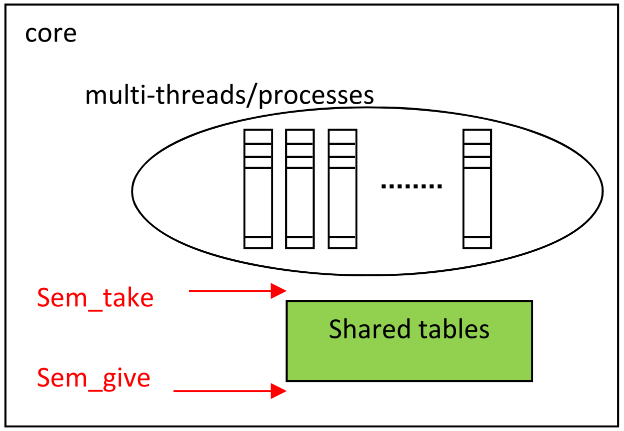
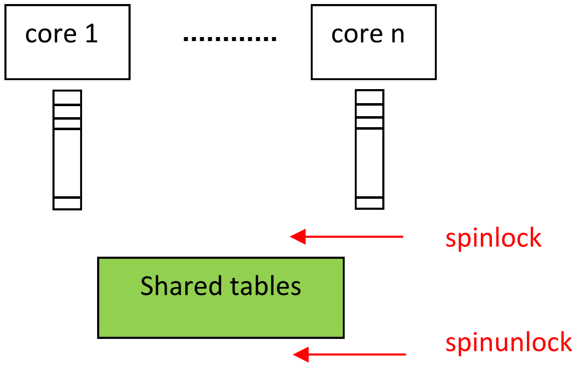
Examples


Each core's private memory
Shared Memory Between partitions
Shared Memory among cores
Core0
Core1
Core2
Core7
Port0
Port1
PortN





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Challenges with Multicore Architecture

- Legacy software written for non-SMP
  - Multithreading a must for scaling with Multicore
  - Dynamic thread migration by OS scheduler
  - Possibility to Affine application threads and interrupts to a core
  - Locks must for shared resources in multithreaded applications
    - Resource contention, priority inversion, deadlocks
- Parallel threads execution in real time
  - Latent race conditions get uncovered
  - Difficult to reproduce bugs
  - Data corruption more difficult to nail down

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Challenges with Multicore Architecture (contd…)

- Cache efficiency requires careful Software design
  - False cache line sharing
  - Cache line thrashing due to threads running on different cores
- Finding performance bottleneck
  - Core loading by scheduler
  - TLB, cache thrashing
  - Stash downgrades
  - Too many interrupts, interrupt distribution, context switches
  - Slow IPC

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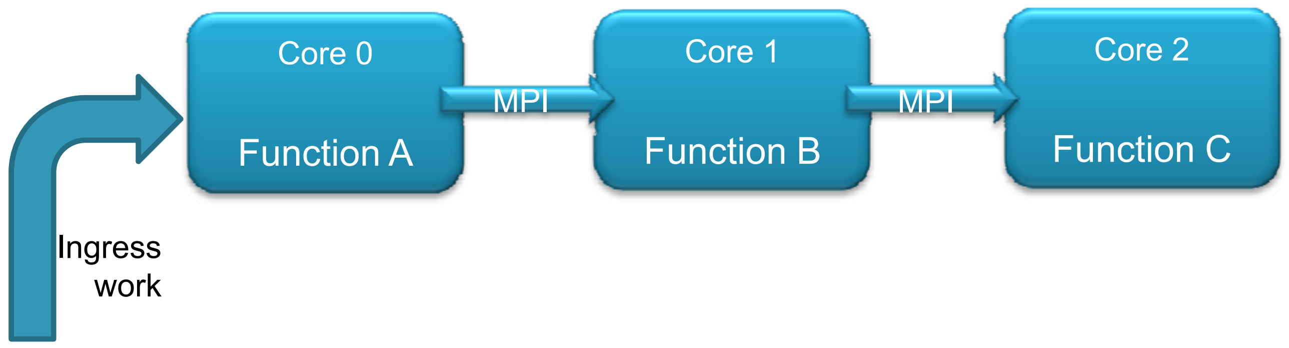
Programming Models

- Pipeline
  - Work division across the cores by the way of functionality
  - Each core executes a subset of functions on each work unit
  - Individual work units passed along functional blocks/cores



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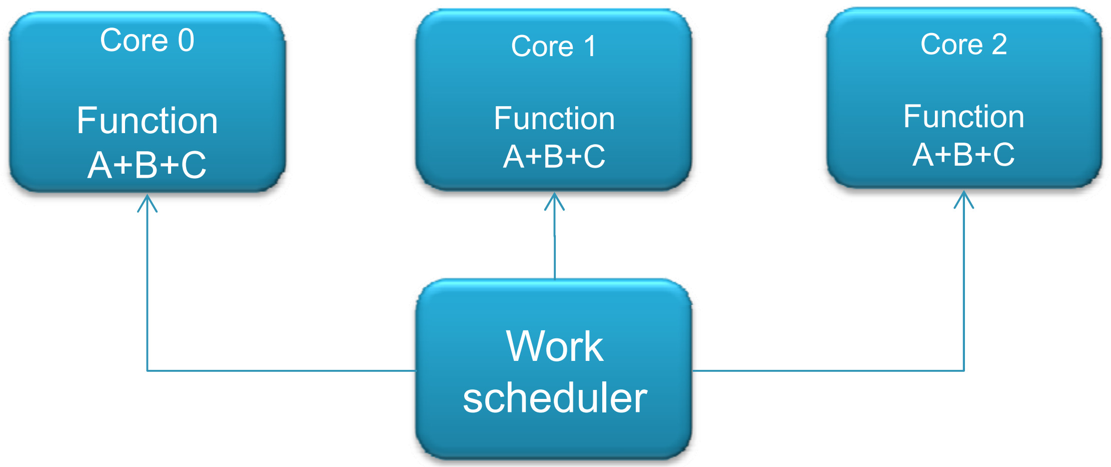
Programming Models – contd..

- Run to completion
  - Work is divided by splitting work units across cores
  - Work scheduler divides work units across cores
  - Each core executes all functions on received work units



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Programming Models - Comparison

Aspect	Pipeline	Run to completion
Programmability	Difficult to break a problem in equal chunks of work	Easy
I-Cache utilization	Good	Poor
D-cache utilization	Poor	Good
Load balancing	Poor	Easy(If hardware supported)
Fault tolerance	Poor	Good
Locks required	No	Yes
Egress work ordering	Maintained	Disturbed
Work distribution hardware	Not required	Required
IPC/MPI overhead	High	Nil
Real-time/priority work latency	Low	High
Scalability with cores	Difficult (requires redesign)	Easy

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Programming Language support

- ‘C’ does not natively support multithreading
  - Compiler assumes single flow of control
  - Protecting shared resource is responsibility of programmer
    - Locks, volatile etc
  - Parallelism cannot be expressed as an intent to compiler
    - Compiler cannot do inter thread optimization

- Relaxed ordering
  - Out of order completion of loads and stores across cores
    - Instruction/storage barriers
  - Programmers need to be closely aware of hardware

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Compiler Limitation

- The compiler may not be able to do the parallelization in the way you like to see it:
  - A loop is not parallelized
  - The data dependency analysis is not able to determine whether it is safe to parallelize or not.
  - The granularity is not high enough
  - The compiler lacks information to parallelize at the highest possible level

- **Explicit parallelization through OpenMP directives and functions are used to overcome above limitations**

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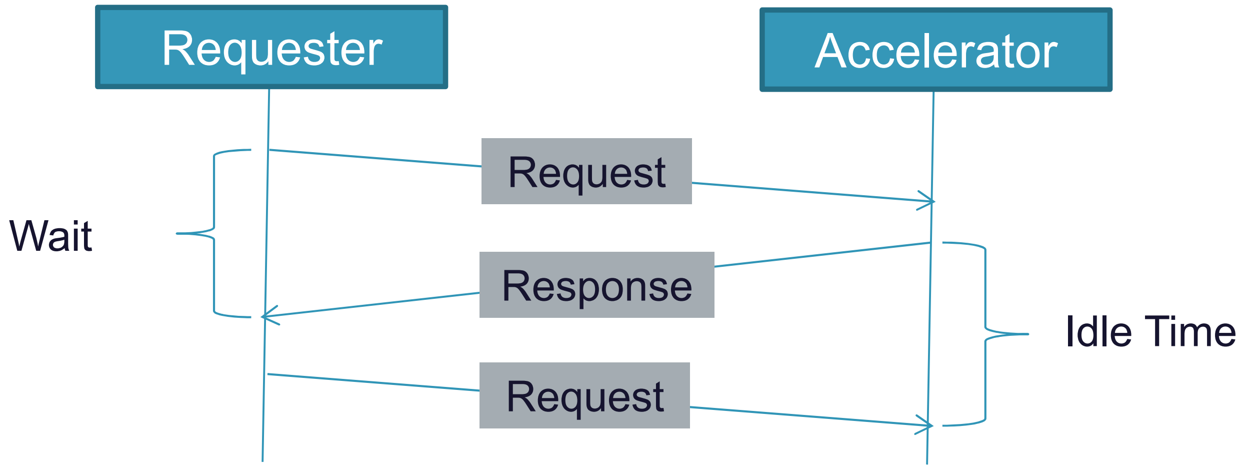
REQ/RESP processing model

- Synchronous
  - Requester waits till response arrives
  - Simplifies programming as response pending state not required
  - Only single pending request
  - Suitable for core-inbuilt offload hardware accelerators



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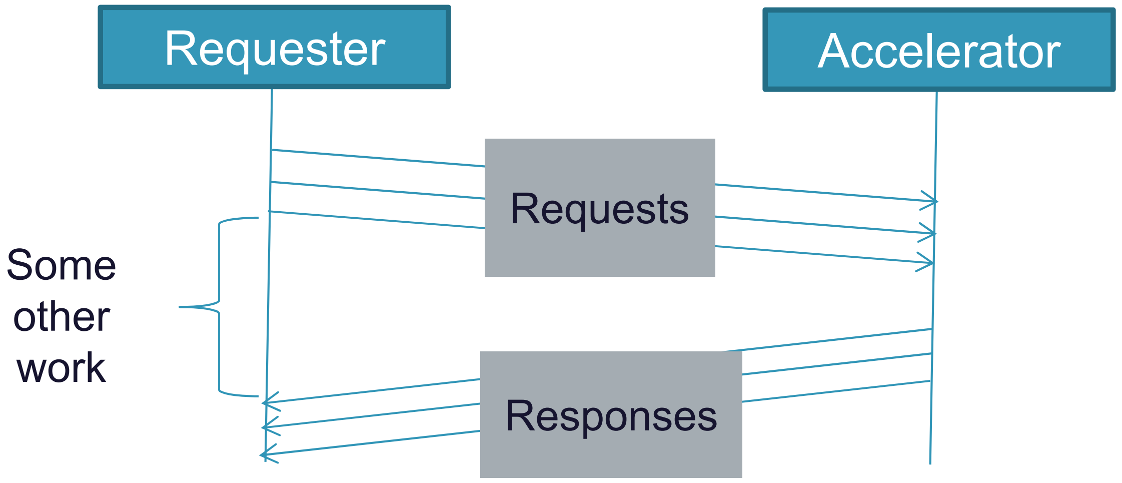
REQ/RESP processing model (contd)

- Asynchronous
  - Requesters do not wait till response arrives (fire and forget)
  - Response comes as another state machine input
  - Request & response co-relation required
  - Multiple requests can be pending
  - Suitable for core external offload hardware accelerators



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REQ/RESP processing model - Comparison

Aspect	Synchronous	Asynchronous
Programming ease	High	Low
Context switches	High	Low
Accelerator utilization	Low	High
Pending requests	Single	Multiple
Context switches	High	Low
Single flow B/W	Low	High

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  - Functionality Debugging support

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OpenSource Debugging Tools

Function trace: Kernel internal tracer

- Derived from -rt patch Latency Tracer
- Plugin tracers
  - ftrace : function tracer
  - irqsoff : interrupt disabled latency
  - wakeup : latency of highest priority task to wake up
  - sched_switch: task context switches
  - (more)
- Works with Ring buffer
- Saved traces used to save maximum latency traces

- **Gives cost-view of different context level in kernel per core**

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OpenSource Debugging Tools (Cont.)

Oprofile & Perf

- System-wide profiler (both kernel and user code)
- Sample-based profiler –Time based and event based
- SMP machine support
- Performance monitoring hardware support
- Relatively low overhead, typically <10%
- Designed to run for long times
- Perf supports recording function trace between two events

- **Gives more complete picture of where application spends time per core or process wide**

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Freescale Debugging Tools

- **Scenarios Tool**
  - Simple one click access to common performance analysis scenarios for QorIQ – including DPAA Debug IP
  - Removed need from customer to know how to configure DPAA debug IP to collect performance data from common scenarios.
- **Register Analyzer**
  - Alpha version delivered
  - Provides feedback on incorrect configuration of DPAA blocks (FM, QM, BM and SEC)
- **SPID (Major Updates for 2012)**
  - Target Side Library to access debug IP inside (instrumentation) a customer application.
  - Sample code to show how to collect trace and performance data for basic cases.
  - Extensive documentation.
  - Supports Linux and Bare Metal Applications
- **SPID Utilities (New for 2012)**
  - Applications focused on specific use-cases to improve usability of debug IP in FSL SDK Linux applications.
  - Packaged for release in SDK 1.2
  - First release 3Q 2012

- **Application Notes**
  - Performance Analysis
  - LTTng Trace
  - Application Debugging
- **qoriq-dbg (Major Updates for 2012)**
  - Easy access to QorIQ debug IP from user scripts or applications via standard file system operations.
  - Present tools in a manner that is familiar to Linux developers
- **DPAA Tools. (New for 2012)**
  - Packet Tracing tool – Allows a customer to trace a packet as it moves through system.
    - Focus for 2012
    - First version scheduled for 4Q 2012.
  - This tooling makes use of the on-board trace facility of each block.
  - DPAA Trace supporting ALU USDPAA application Alpha being delivered in CW 10.1.2 (may 2012) and Production versions (Expert mode) scheduled for CW 10.2 (June 2012)
  - **LTTng/LTTngX**
    - Linux Community standard Kernel Tracing Framework
    - LTTngX – Freescale's unique extensions to LTTng Framework to support access to Freescale QorIQ Debug IP

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Summary

- Multicore processor is like a traditional multiprocessor boards shrunk to a single chip. Additionally it may have hardware accelerators
- Application needs to be threaded to benefit from multicore but most legacy applications are single threaded
- To benefit from multicore capabilities, applications need to be careful about many aspects like core / interrupt affinity, cache thrashing, TLB management, priorities, deadlocks, etc.
- There are multiple programming models for multicore applications, with each one having its own advantages and disadvantages
- Several open source tools are available for functionality and performance debugging on multicore platforms
- Freescale supports QorIQ debug architecture to assist debug across layers of software and hardware

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Session materials will be posted @ www.freescale.com/FTF

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