Assembly and PCB Layout Guidelines for Chip-Scale Packages

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Introduction

The Chip-Scale Package (CSP) is a dual or multi-layer plastic encapsulated BT-Epoxy type substrate with copper signal and plain layers. The small form factor allows for enhanced conduction of heat to the PCB and provides a stable ground through down bonds; as well as an electrical connection through conductive, die-attached material. The design of these dual and multi-layer small body packages allows for flexibility and enhances electrical performance to high-speed operating frequency.

Microsemi offers CSPs in multiple configurations: substrate ball pitch range from 0.4 mm to 0.8 mm, with a package body size of 4 x 4 mm to 14 x 14 mm, and overall package height of 0.73 mm to 1.35 mm. The package footprint and outlines are specified in JEDEC MO-195, JEDEC MO-205, and JEDEC Design Guide 4.5 "Fine-Pitch, Square Ball Grid Array Package (FBGA)".

This application note provides general guidelines for proper board design and surface mount process.

CSP Package Overview

Figure 1 and Figure 2 illustrate how the package height is reduced to the minimum by having the die background resulting in a thinner substrate and lower-bond wire loops. Figure 3 on page 2 illustrates the detailed construction of the layer stack-up. CSPs have excellent thermal dissipation because the thinner die, due to backgrinding, enables a thinner substrate and smaller overall body.

The efficient and compact design of CSPs reduces electrical parasitics.

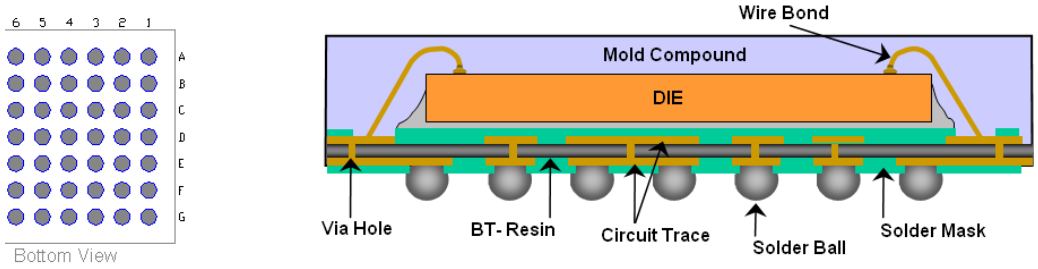

***Figure 1* • Bottom View and Cross-Section of Two-Layer CSPs**

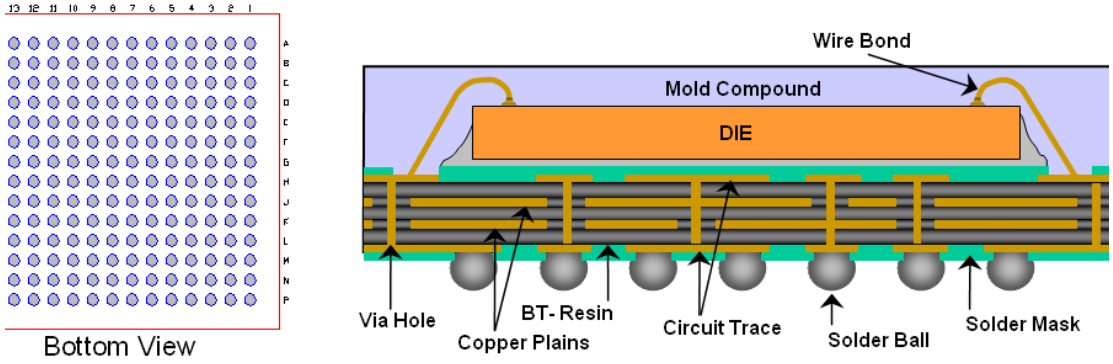

***Figure 2* • Bottom View and Cross-Section of Four-Layer CSPs**

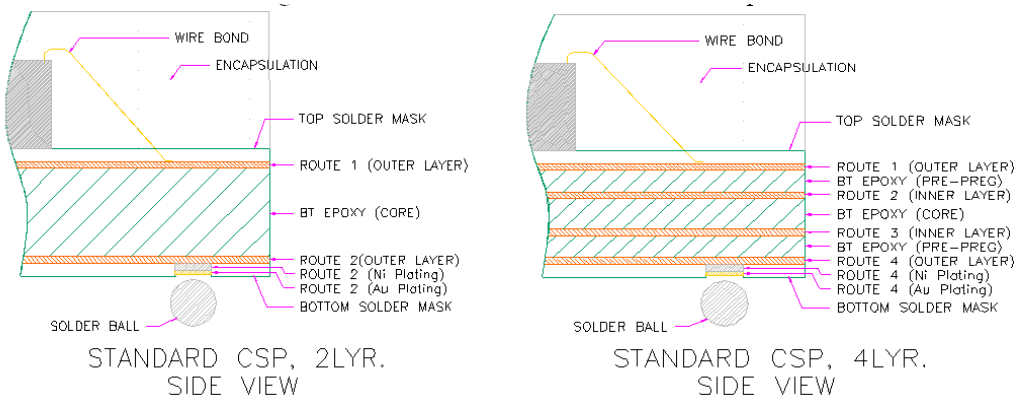

***Figure 3* • Detail of Substrate Stack-Up Construction**

Table 1 and Table 2 provide typical reliability and standard material data.

***Table 1* • Typical Reliability Data**

Moisture Sensitivity	MSL-3
Autoclave, 121°C	168 hours
Temperature Cycle, Condition Cycle	1000 cycles
Unbiased HAST, 130°C	96 hours
HSTL, 150°C	1000 hours

Note: JEDEC/JESD22-A102-C does not require autoclave test on laminate- or tape-based packages: i.e., FR4 material, polymide tape, or equivalent.

Table 2 • **Typical Standard Material Data**

Substrate	BT resin
Substrate Finish	Electrolyte plating
Die Attach	Conductive
Mold Compound	RoHS-compliant
Marking	Laser mark
Solder Ball	Standard: 62 Sn / 36 Pb / 2 Ag, or Standard: 63 Sn / 37 Pb, or Pb-free: 96.5 Sn / 3 Ag / 0.5 Cu

Surface Mount Considerations for CSPs

Special considerations are needed to properly design the motherboard and to mount the package for enhanced thermal, electrical, and board-level performance. The amount of the standoff clearance required depends on the application. The PCB footprint design should take into account dimensional tolerance due to package, PCB, and board assembly.

A number of factors may have a significant effect on how CSPs are mounted on the board and the quality of the solder joints. Some of these are the amount of solder paste coverage, stencil type, type of via, board thickness, ball finish on the package, surface finish on the board, type of solder pasted, and reflow profile.

PCB Land Pad Design Guidelines

This section provides both package and board-level routing constraints in describing the philosophy behind the recommended land pad patterns.

Solder Masking Considerations

Non-solder mask defined (NSMD) pads are recommended for CSPs because a copper etching process has tighter control than a solder masking process and improves the reliability of solder joints.

Pad Design Recommendations

The solder pad on the PCB should not be larger than the solder mask opening for the ball pad on the package. For optimal solder joint strength, Microsemi recommends a 1:1 ratio for the two pads (Figure 4).

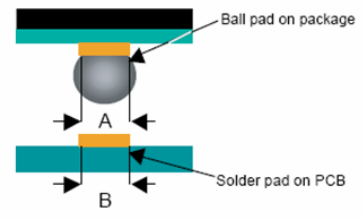

Figure 4 • **Pad Design Recommendations**

Note: A/B = 1:1 for optimum reliability

Trace and Via Design Recommendations

The dog-bone style land pad layout is recommended for 0.8 mm to 0.5 mm land pitch with a through hole or micro via structure; for the 0.4 mm land pitch use the via in pad. The via in pad should be micro via, and the through holes will need tenting, as shown in Figure 5 and Figure 6.

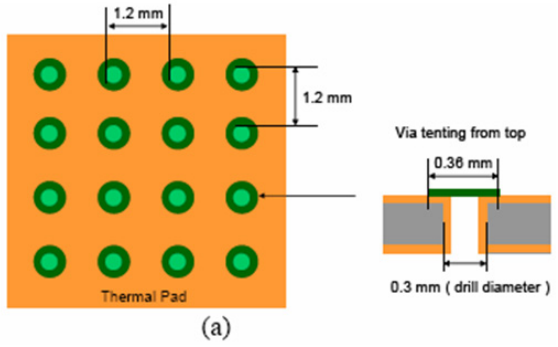

***Figure 5* • Via Tenting For In Pad Through Hole**

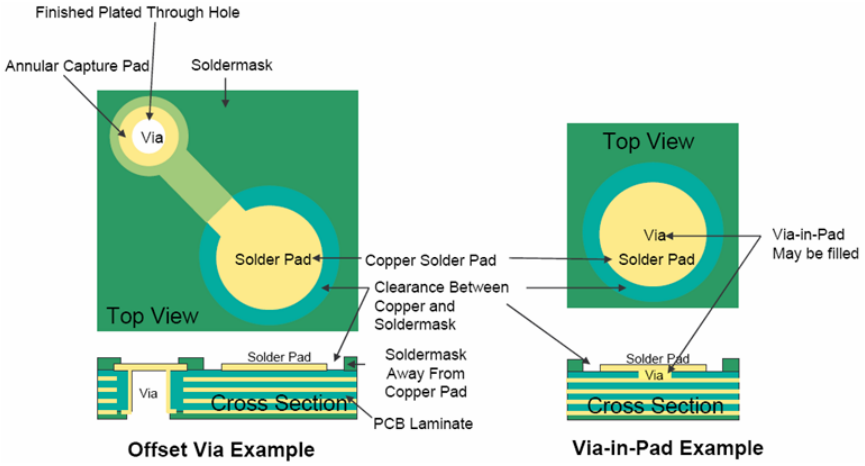

***Figure 6* • Dog-Bone Style Offset Via Through Hole (left), In Pad Micro Via (right)**

Line width should be a minimum of 0.075 mm with a spacing of 0.085 mm. See the "Detailed PCB Layout" section on page 8 for detailed dimensions and possible PCB breakout routing recommendations.

Board Mounting Guidelines

This section provides guidelines for stencil design. Due to the small land surface area on the PCB surface, care must be taken to form reliable solder joints for the CSP. Microsemi recommends using stainless steel stencils with a thickness of 0.10 to 0.20 mm and metal squeegees. If polymer squeegees are used, the minimum durometer should be 90.

Stencil Design and Thickness

Stencils should be laser cut and electropolished. The polishing helps in smoothing the stencil walls, which results in better paste release. Positive taper with a bottom opening of 25 to 50 microns larger than the top can provide better solder paste release. The stencil aperture tolerance should be tightly controlled because tolerance can effectively reduce the aperture size.

To maintain proper stencil design, do not ever exceed an area ratio of 0.66 or aspect ratio of 1.5.

Solder Paste

Since not enough space is available underneath the part after reflow, use "no clean," type 3 or type 4 paste for mounting CSPs. Nitrogen purge is also recommended during reflow, as gases entrapped in the solder joint are the main cause of voiding. There should be sufficient dwell time in the molten state to ensure gases from the solder paste have time to separate and escape from the molten solder.

Reflow Profile and Peak Temperature

Reflow profile and peak temperature has a strong influence on void formation. Microsemi strongly recommends following the profile recommendation of the paste suppliers, since it is specific to the requirements of the flux formation. However, the following two profiles in Figure 7 and Figure 8 can be used as references to fine-tuning the final profile that works for your application.

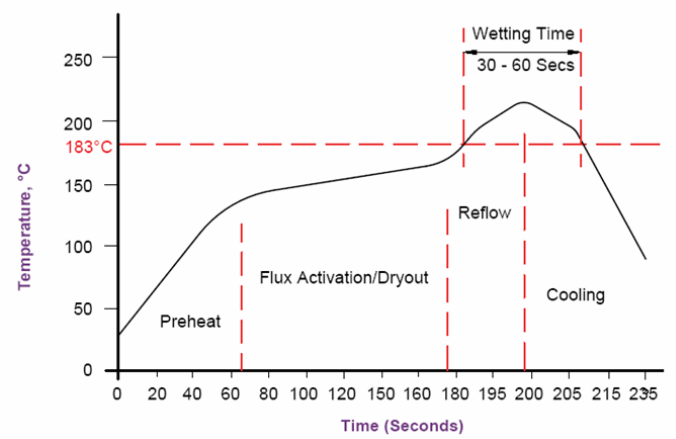

***Figure 7* • Eutectic Solder Reflow Profile**

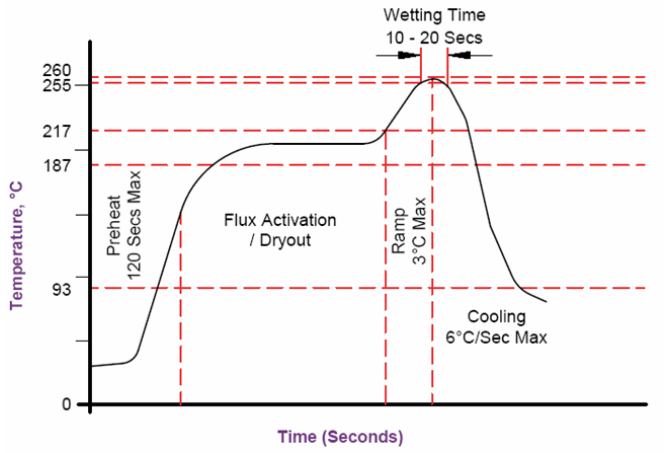

***Figure 8* • Pb-Free Solder Reflow Profile**

Assembly Process Flow

Figure 9 on page 6 shows the typical process flow for mounting surface mount packages to printed circuit boards. The same process can be used for mounting the CSP. However, Microsemi recommends including post-print and post-reflow inspection, especially during process development. The volume of paste printed should be measured either by 2D or 3D techniques. The paste volume should be around 80 to 90% of stencil aperture volume to indicate good paste release. After reflow, the mounted packages should be inspected in a transmission x-ray for the presence of voids, solder balling, or other defects. Cross-sectioning may be required to determine the fillet shape and size, and joint standoff height.

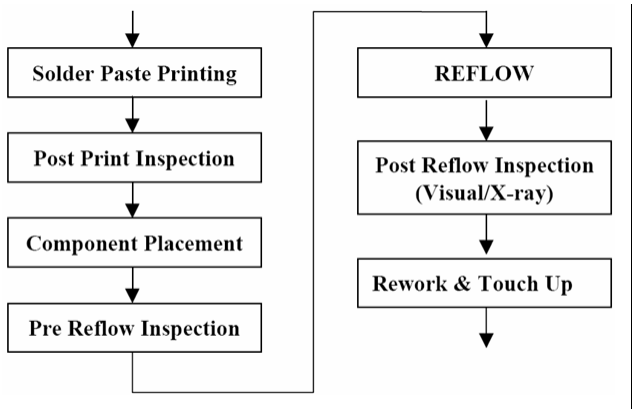

***Figure 9* • Thermal Pad Stencil Design**

Rework Guidelines

Since solder joints in CSPs are not fully exposed, any retouch is limited. For defects underneath the package, the whole package has to be removed. Reworking CSPs can be a challenge due to their small size. In most applications, CSPs are mounted on smaller, thinner, and denser PCBs that introduce further challenges due to the handling and heating difficulties. Since reflow of adjacent parts is not desirable during rework, the proximity of other components may further complicate this process.

The rework process involves the following steps:

- Component removal
- Site redress
- Solder paste application
- Component placement and attachment

Component Removal

The first step in removing a component is to make sure the PCB is dry. Microsemi recommends baking the PCB for 24 hours at 125°C to prevent moisture-induced "popcorn" damage from any moisture in the PCB or package. The second step is the reflow of solder joints attaching the component to the PCB board. Ideally, the reflow profile for part removal should be the same as the one used for part attachment. However, the time above liquid can be reduced as long as the reflow is completed.

In the removal process, Microsemi recommends heating the board from the bottom side using a convective heater and using hot gas or air on the top side of the component. Use a nozzle to direct the heating in the component area and minimize the heating of adjacent components. Avoid excessive airflow, as this may cause the CSP to skew. Microsemi recommends air velocity of 15 to 20 liters per minute. Once the joints have been reflowed, the vacuum lift-off should be automatically engaged during the transition from reflow to cool down. Because of the small joint size, the vacuum pressure should be kept below 15 in of Hg. This will prevent pad lift-off if all joints have not been reflowed.

Site Redress

After the components have been removed, and while the board is still hot, clean the site properly. It is best to use a combination of a blade-style conductive tool and de-soldering braid. The width of the blade should be matched to the maximum width of the footprint, and the baked temperature should be low enough not to cause any damage to the circuit board. Once the residual solder has been removed, the lands should be cleaned with solvent. The solvent is specific to the type of paste used in the original assembly, so follow the manufacturer's recommendations.

Solder Paste Printing

Because of the small size and finer pitches of CSPs, solder paste deposition requires extra care. However, you can achieve a uniform and precise deposition by using a miniature stencil specific to the component. Align the stencil aperture with the pads under 50X–100X magnification. Lower the stencil onto the PCB and deposit the paste with a small metal squeegee blade. Alternatively, you can use the mini stencil to print paste on the package site. Use a 125-µ stencil with the same aperture size and shape as the package land. The small standoff of CSPs does not leave much room for cleaning, so do not use a no-clean flux.

Component Placement and Attachment

CSPs are expected to have superior self-centering ability due to their small mass. Placement of this type of package is similar to that of BGA packages. As the land pads are on the underside of the package, use a splitbeam optical system to align the component onto the motherboard. This will form an image of land overlaid on the mating footprint and will aid proper alignment. Perform the alignment at 50X–100X magnification. The placement machine should have the capability of allowing fine adjustments in X, Y, and rotational axes.

Use the reflow profile developed during original attachment or removal to attach the new component. Since all reflow profile parameters have already been optimized, using the same profile will eliminate the need for thermocouple feedback and will reduce operator dependencies.

Detailed PCB Layout

This section provides the suggested board layout of soldered pads for CSPs.

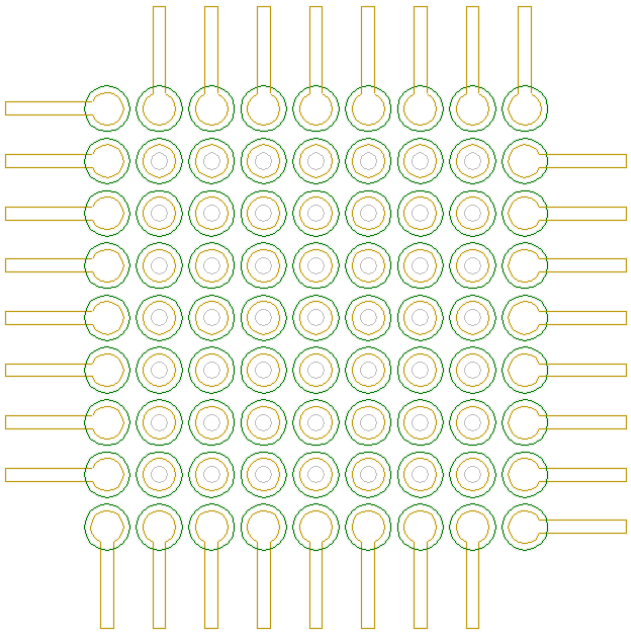

***Figure 10* • Suggested Board Layout for NSMD of Soldered Pads for µC81 CSPs (PCB Top Layer)**

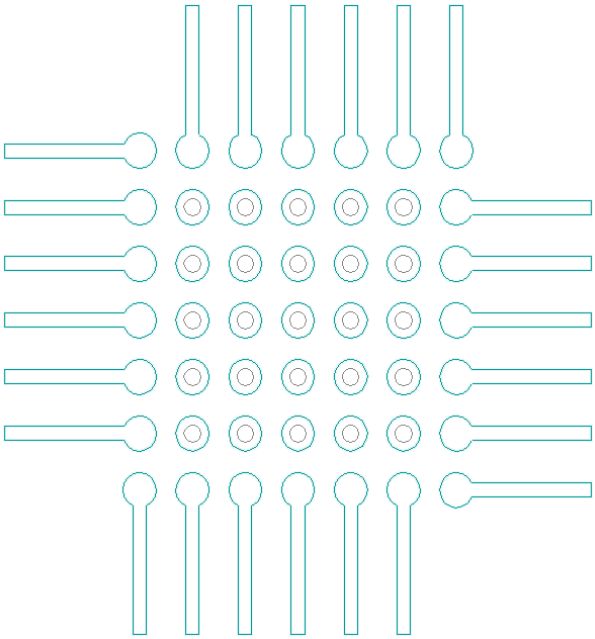

***Figure 11* • Suggested Board Layout of Soldered Pads for µC81 CSPs (PCB Lower Layer)**

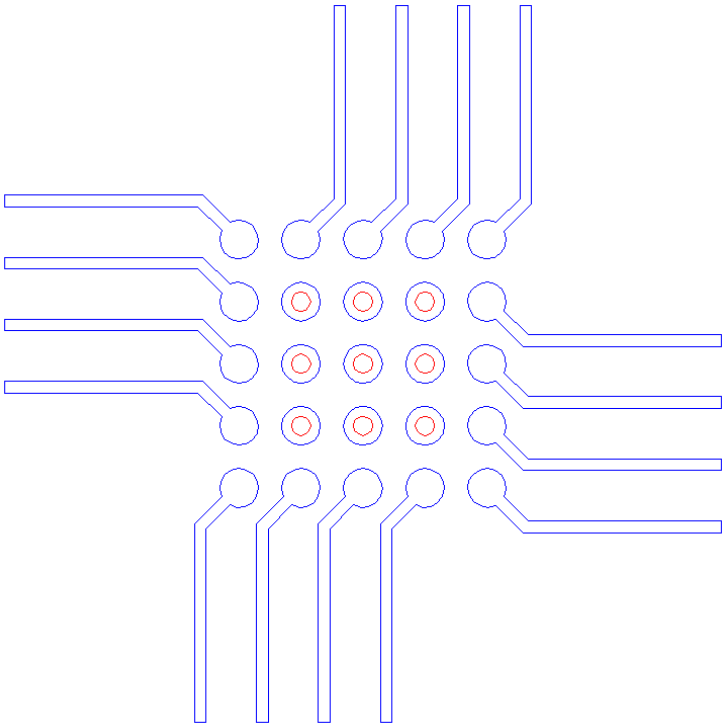

***Figure 12* • Suggested Board Layout of Soldered Pads for µC81 CSPs (PCB Lower Layer)**

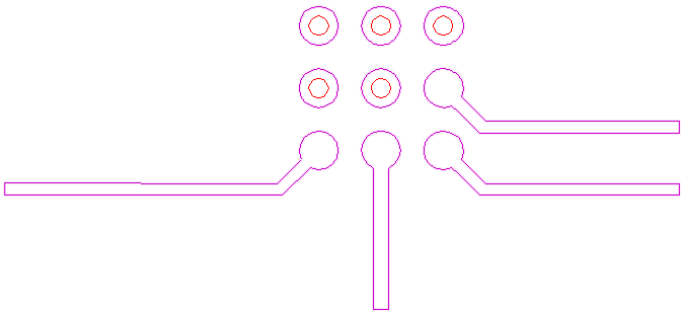

***Figure 13* • Suggested Board Layout of Soldered Pads for µC81 CSPs (PCB Lower Layer)**

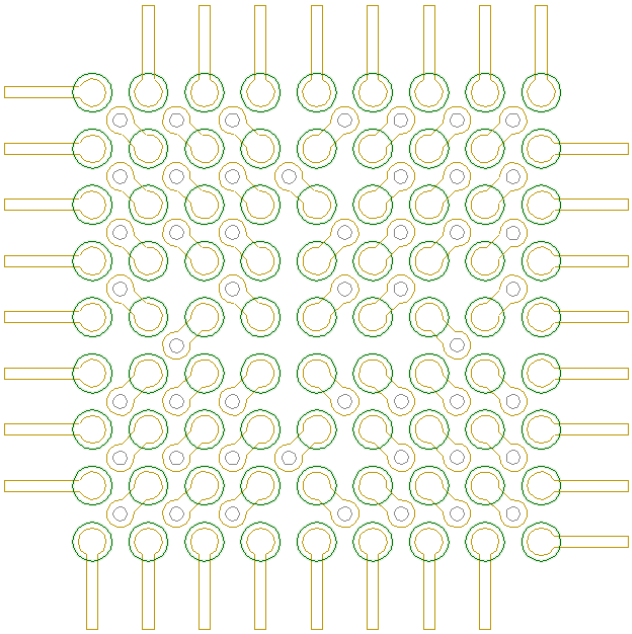

***Figure 14* • Suggested Board Layout for NSMD of Soldered Pads for CS81 CSPs (PCB Top Layer)**

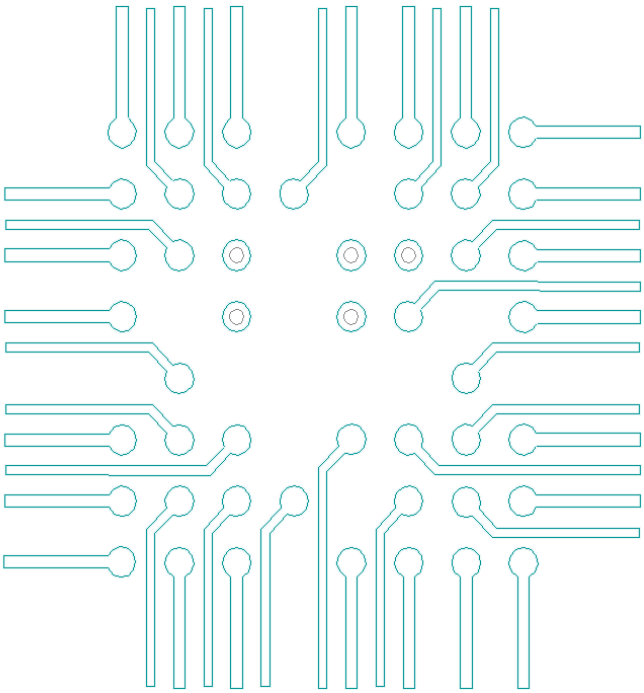

***Figure 15* • Suggested Board Layout of Soldered Pads for CS81 CSPs (PCB Lower Layer)**

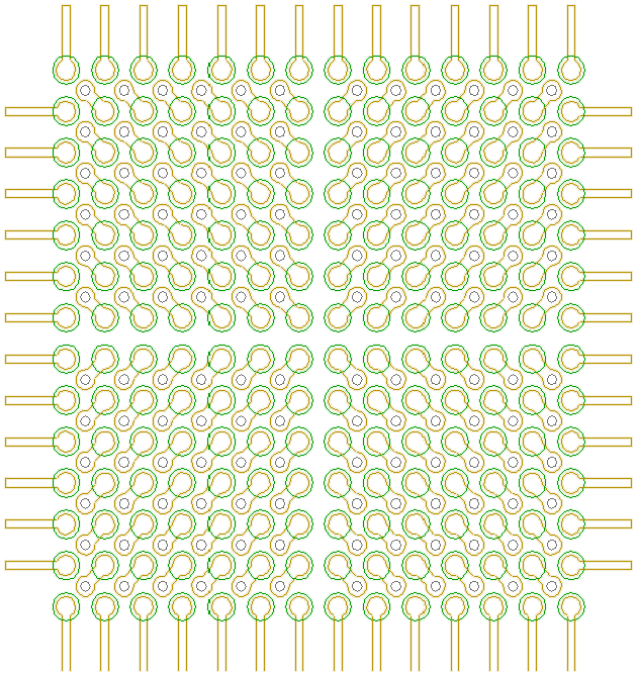

***Figure 16* • Suggested Board Layout for NSMD of Soldered Pads for CS196 CSPs (PCB Top Layer)**

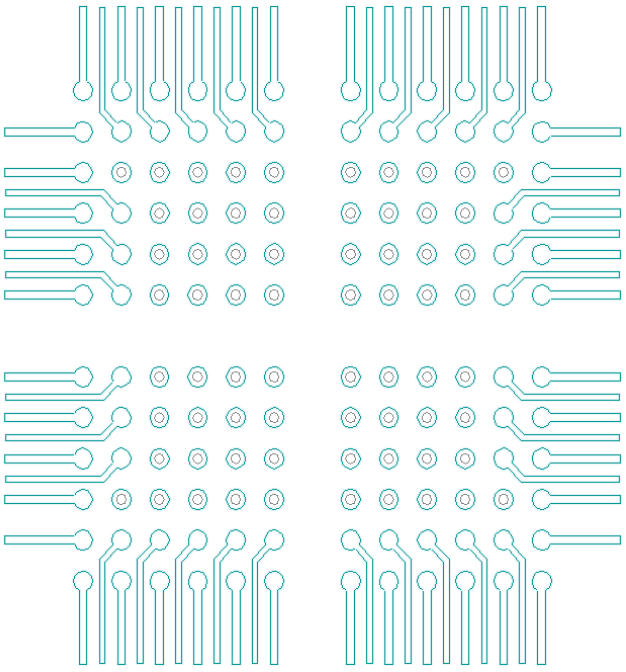

***Figure 17* • Suggested Board Layout of Soldered Pads for CS196 CSPs (PCB Lower Layer)**

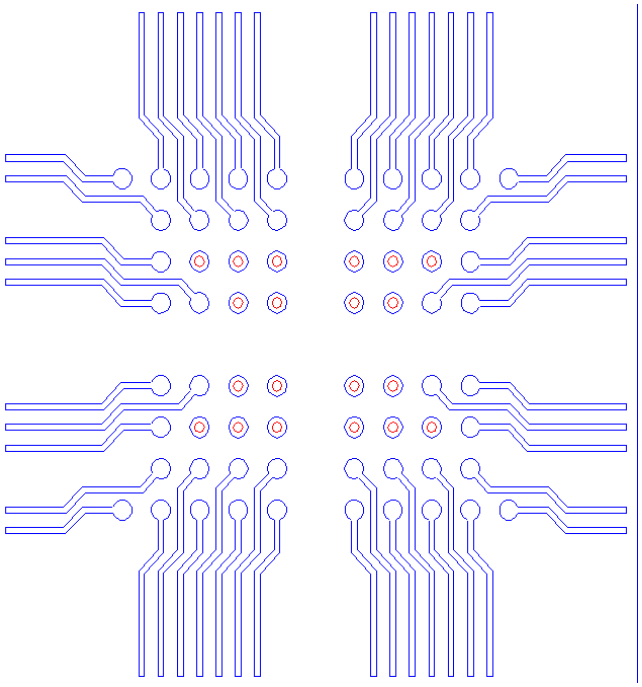

***Figure 18* • Suggested Board Layout of Soldered Pads for CS196 CSPs (PCB Lower Layer)**

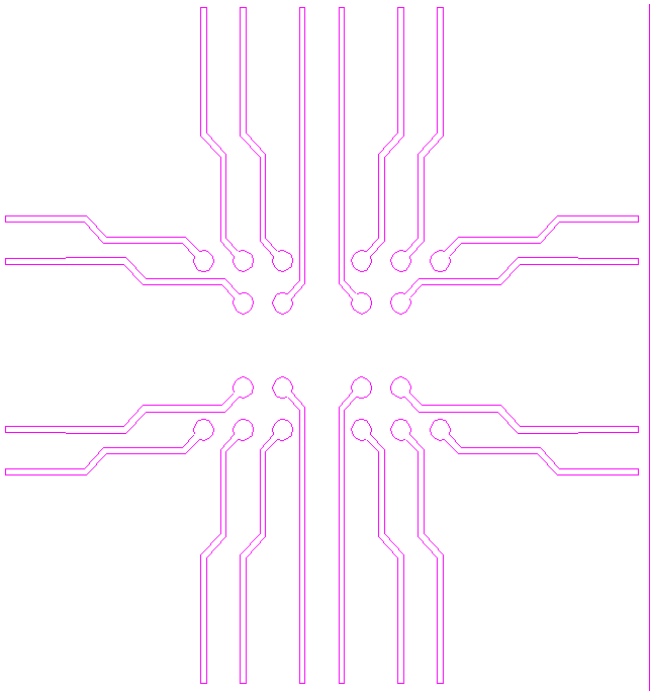

***Figure 19* • Suggested Board Layout of Soldered Pads for CS196 CSPs (PCB Lower Layer)**

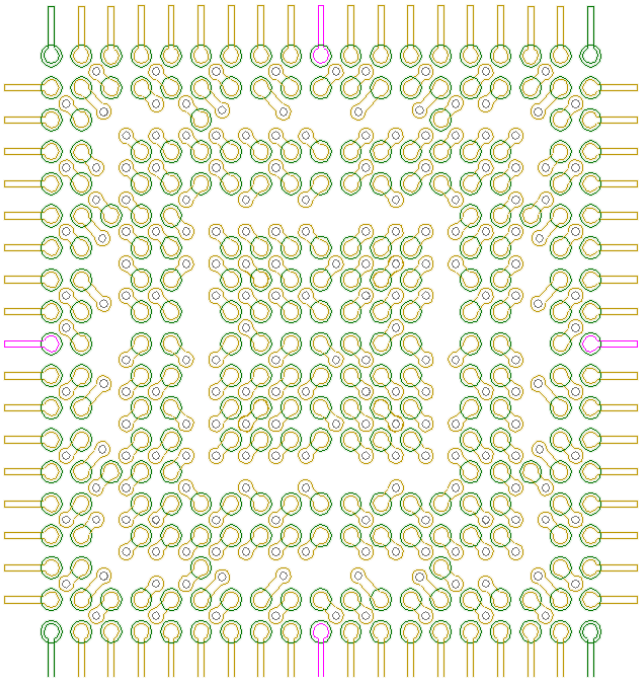

***Figure 20* • Suggested Board Layout for NSMD, 3-Layer PTH of Soldered Pads for CS281 CSPs (PCB Top Layer)**

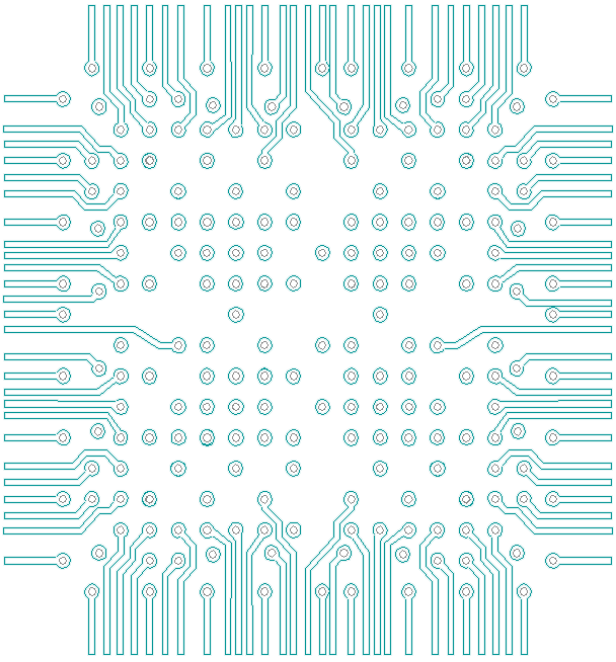

***Figure 21* • Suggested Board Layout of Soldered Pads for CS281 CSPs (PCB Lower Layer)**

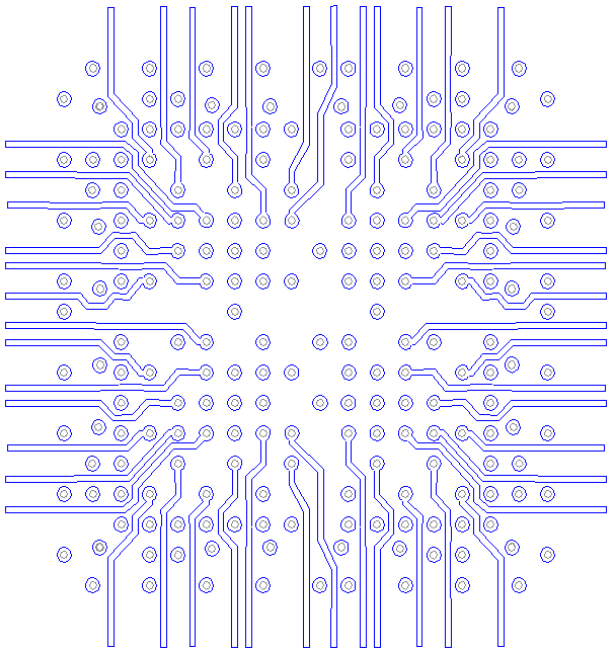

***Figure 22* • Suggested Board Layout of Soldered Pads for CS281 CSPs (PCB Lower Layer)**

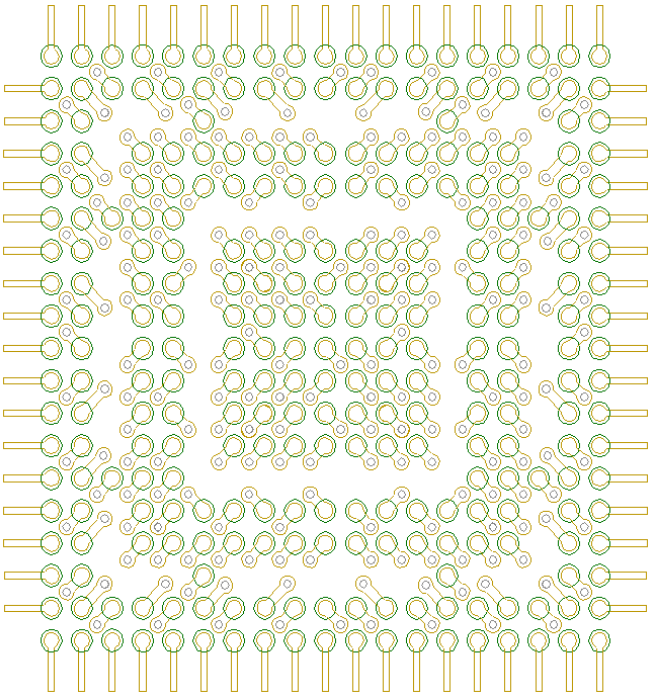

***Figure 23* • Suggested Board Layout for NSMD, Line Width 0.1 mm, of Soldered Pads for CS281 CSPs (PCB Top Layer)**

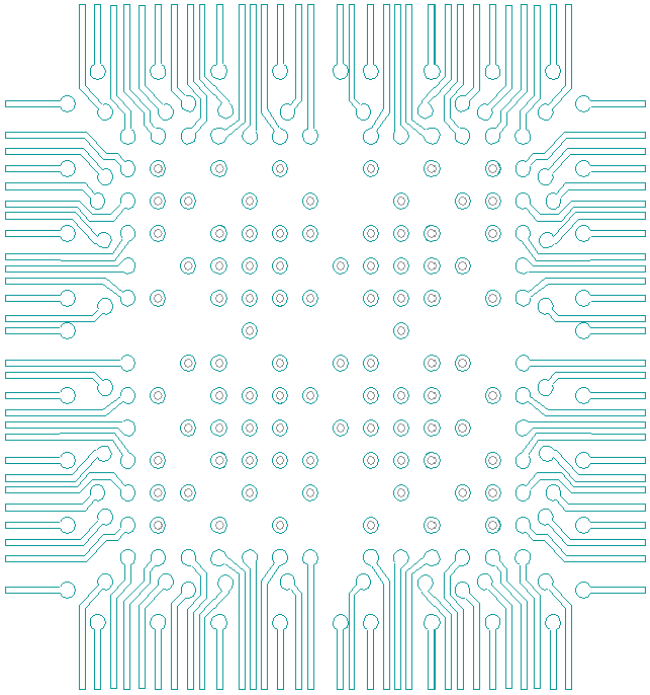

***Figure 24* • Suggested Board Layout of Soldered Pads for CS281 CSPs (PCB Lower Layer)**

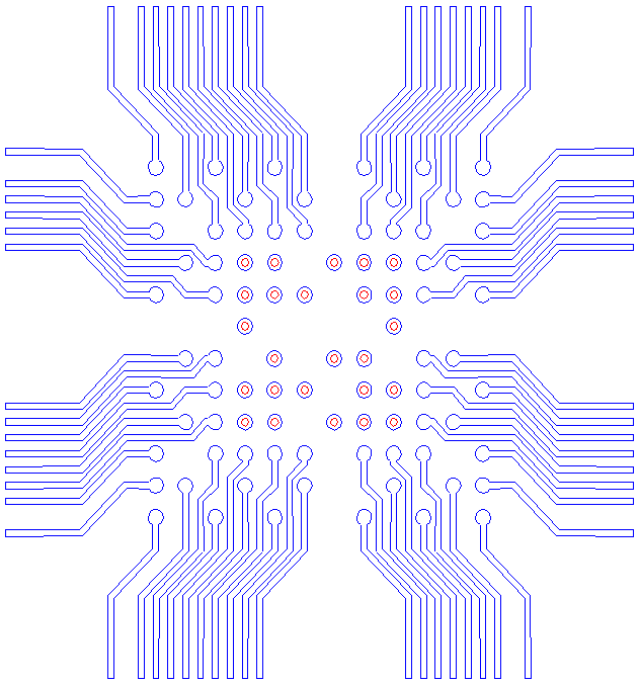

***Figure 25* • Suggested Board Layout of Soldered Pads for CS281 CSPs (PCB Lower Layer)**

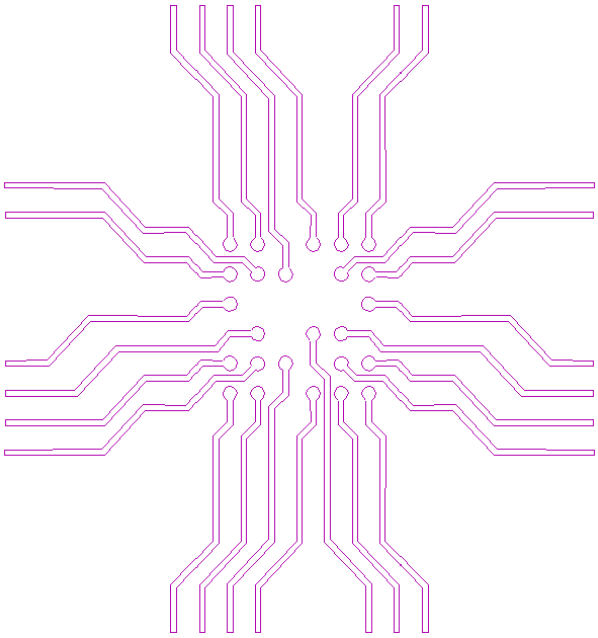

***Figure 26* • Suggested Board Layout of Soldered Pads for CS281 CSPs (PCB Lower Layer)**

EIA Standard Board Layout Drawing for BGA and CCGA Packages

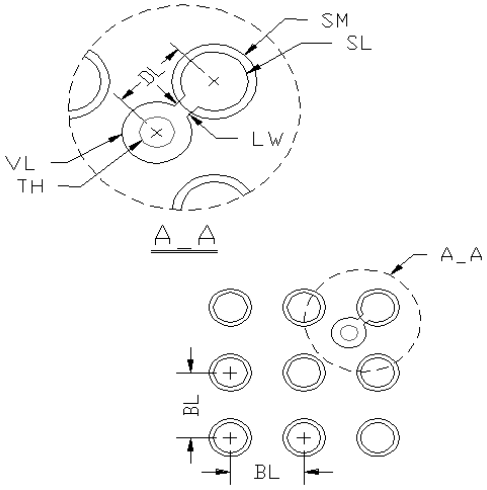

***Figure 27* • Suggested Board Layout of Soldered Pads for BGA Packages**

Table 3 on page 17 contains the recommended guidelines for board layout soldered pad dimension for Microsemi CSPs (0.4 mm to 0.5 mm Pitch CSP) only.

Table 4 on page 17 contains the recommended guidelines for board layout soldered pad dimension for Microsemi CSPs (0.8 mm Pitch CSP) only.

Table 3 • **Recommended PCB Design Guidelines for Microsemi CSPs (0.4 mm to 0.5 mm pitch BGA package)**

Diameter	uC81	CS81	CS121	CS196	CS201	CS281
Component Land Pad Diameter (SMD)	0.33	0.35	0.35	0.35	0.35	0.35
Solder Land Diameter (SL)	0.23	0.25	0.25	0.25	0.25	0.25
Solder Mask Opening Diameter (SM)	0.33	0.35	0.35	0.35	0.35	0.35
Solder Ball Land Pitch (BL)	0.40	0.50	0.50	0.50	0.50	0.50
Line Width Between Via and Solder Land (LW)	Via In Pad	0.15 to 0.20	0.15 to 0.20	0.15 to 0.20	0.15 to 0.20	0.15 to 0.20
Distance Between Via and Solder Land (DL)	Via In Pad	0.353	0.353	0.353	0.353	0.353
Via Land Diameter (VL)	See Land Diameter	0.200 to 0.250	0.200 to 0.250	0.200 to 0.250	0.200 to 0.250	0.200 to 0.250
Through Hole Diameter (TH)	0.100 to 0.125	0.100 to 0.125	0.100 to 0.125	0.100 to 0.125	0.100 to 0.125	0.100 to 0.125
Line Width (L)	0.075	0.075	0.075	0.075	0.075	0.075
Line Width (L) If Inner Outer Via's Staggered.	NA	NA	NA	NA	NA	0.10
Line Space (S)	0.085	0.085	0.085	0.085	0.085	0.085
Pad Array	Full	Full	Full	Full	Perimeter	Perimeter
Pad Matrix	9 x 9	9 x 9	11 x 11	14x14	15x15	19x19
Periphery Rows	-	-	-	-	4, 1, 5	2, 2, 7

Note: Component Land Pad Diameter (SMD):The component land pad diameter is the diameter of the solder ball. This is the diameter of the metal pad in the package or component. The opening of the metal pad in the package or component side is always solder mask defined (SMD).

Table 4 • **Recommended PCB Design Guidelines for Microsemi CSPs (0.8 mm pitch BGA package)**

Diameter	CS49	CS128	CS180
Component Land Pad Diameter (SMD)	0.35	0.35	0.35
Solder Land Diameter (SL)	0.30	0.30	0.30
Solder Mask Opening Diameter (SM)	0.45	0.45	0.45
Solder Ball Land Pitch (BL)	0.80	0.80	0.80
Line Width Between Via and Solder Land (LW)	0.15	0.15	0.15
Distance Between Via and Solder Land (DL)	0.56	0.56	0.56
Via Land Diameter (VL)	0.50	0.50	0.50
Through Hole Diameter (TH)	0.25	0.25	0.25
Pad Array	Full	Perimeter	Perimeter
Pad Matrix	7x7	12x12	14x14

Table 4 • **(continued)Recommended PCB Design Guidelines for Microsemi CSPs (0.8 mm pitch BGA**

Diameter	CS49	CS128	CS180
Periphery Rows	-	4	5
Note: Component Land Pad Diameter (SMD):The component land pad diameter is the diameter of the solder ball. This is the diameter of the metal pad in the package or component. The opening of the metal pad in the package or component side is always solder mask defined (SMD).			

List of Changes

The following table lists critical changes that were made in each revision of the document.

Revision*	Changes	Page
Revision 2 (September 2012)	Added note below Table 3 and Table 4 (SAR 34196).	17
Revision 1 (August 2008)	Table 17 · Recommended PCB Design Guidelines for Microsemi CSPs (0.8 mm pitch BGA package) was updated to include information about the CS289 package.	17

*Note: *The revision number is located in the part number after the hyphen. The part number is displayed at the bottom of the last page of the document. The digits following the slash indicate the month and year of publication.*

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Microsemi Corporation (NASDAQ: MSCC) offers a comprehensive portfolio of semiconductor solutions for: aerospace, defense and security; enterprise and communications; and industrial and alternative energy markets. Products include high-performance, high-reliability analog and RF devices, mixed signal and RF integrated circuits, customizable SoCs, FPGAs, and complete subsystems. Microsemi is headquartered in Aliso Viejo, Calif. Learn more at **www.microsemi.com**.

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