



*Professional Test Engineering*

## **PCB Design-For-Test Guidelines**

### **1. DFT General Information**

All electrical nets should have one test point on one side of the PCB, preferably on the non-component side of the PCB (Secondary side), to support In-Circuit-Test (ICT) and/or Functional Testing. Additional test points may be requested pending Professional Test Engineering evaluation. If it is not possible to place all of the test points on one side of the PCB test points may be added to the component side (Primary side) with the added risk of reduced test coverage, higher cost for test fixtures and possible false failures during test are possible.

A reduction of test points will reduce the effectiveness of ICT by reducing test coverage of the unit under test (UUT) and may affect the ability to perform FVT. Please allow Professional Test Engineering to evaluate your PCB design to insure that a thorough ICT and/or functional test is possible with the proposed design prior to PCB fabrication.

Surface mount component lands should not be used as test points.

Holes in solder mask, with acceptable trace widths, are acceptable test points.

Edge Connector fingers may be used for test points, as long as the dimensional requirements for the test point locations are satisfied.

Connectors with 0.050" or less centers require separate test points.

All IC pins that are internally connected but are not used in the circuit must have a test point. This is to allow for detection of internal and external shorts.

Critical noise sensitive areas where test points are not permitted should be designated by the customer's design engineering prior to layout. This should be noted on the UUT's schematic.

Professional Test Engineering may require the ability to "Tri-State" all busses in order to avoid back-driving signals during test and to allow testing of individual components that are connected on the bus. Access to the signals that are necessary to disable the Tri-State devices, is required.

To measure a resistance of 1.0 Ohms or less, two test points on each side of the component may be required to support 4-wire resistance measuring. Please consult Professional Test Engineering to verify this requirement prior to PCB fabrication.



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### **2. Test Points**

#### **2.1 Requirements**

- 2.1.1 All networks on the PCB require a separate test point to support ICT and FVT test coverage.

#### **2.2 Type, Shape and Size**

- 2.2.1 Test Pads are the preferred types of test points. If design constraints prohibit the use of test pads for all test points, Test Vias or Through-Hole leads may also be acceptable (see 2.7 No-Clean Process for details)
- 2.2.2 Square or Round test points are the preferred shapes although Hex shaped pads are also acceptable.
- 2.2.3 Regardless of the type or the shape, the test points should always be a minimum of 0.035" flat to flat or diameter. If Test Vias are used the minimum inside diameter of the Plated through-hole shall be 0.018".

#### **2.3 Spacing and Clearance Criteria**

- 2.3.1 Reflow or Wave Solder Process
- 2.3.2 Reflow Only Process
- 2.3.3 Low Profile, High Cost PCB Process
- 2.3.4 No-Clean Solder Flux Requirements

#### **2.4 Reference Designators**

- 2.4.1 The reference designators for test points will be marked in etch or silk screened if possible.
- 2.4.2 When marking test points the "TP" may be omitted leaving only the number for identification. (example TP101 may be referenced as 101)

#### **2.5 Surface Mount Connectors (non-power)**

- 2.5.1 Separate test points are required for all surface mount connectors.

#### **2.6 Input / Output Power Requirements**

- 2.6.1 Separate test points are required for all power connectors.
- 2.6.2 To support FVT two test points for each power signal are required at a minimum. Two for the source side and two for the return side. This requirement may change if the power through the circuit is not continuous, please consult Professional Test Engineering for clarification.

- 2.6.2.1 0.060" Diameters vias with a 0.025" diameter plated through hole are preferred but if the current through the circuits does not exceed test probe limits 0.035" vias may be used.

Note: A test probe that corresponds to the 0.060" test via is rated at approximately 2 Amps and the test probe that corresponds to the 0.035" test via is rated at approximately 1 Amp. Exceeding these rating will reduce probe life.



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### **2.7 No-Clean Flux Process**

- 2.7.1 Leaded connectors and any other leaded components cannot have the test point on the lead (where the component is physically mounted to the PCB), as No-Clean Flux on the lead can obstruct the test probes causing intermittent contact.
- 2.7.2 For hand soldered components, the test points must be 0.100" away from the component holes.
- 2.7.3 If a test point is required between components, there must be a minimum of 0.005" solder mask the end of the components and the test pad.

### **3. Test Tooling Holes**

- 3.1 PCB mounting holes, not plated through, should be used for test tooling holes as long as the mounting holes are toleranced as a tooling hole.
- 3.2 A preferred diameter of 0.125"  $\pm$  .003"/-.000" (minimum 0.100"  $\pm$  .003"/-.000") is required.
- 3.3 The tooling holes should be located on opposite ends of the board, as far away from each other as possible, diagonally.
- 3.4 An area clear of components equal to the diameter of the tooling hole  $\pm$  .080" and centered around the tooling hole must be provided.
- 3.5 Tooling holes in the tab are not to be used for test purposes.