PRINTCA AS
6.1.2000
PCB DESIGN PARAMETERS

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Design for manufacturability (DFM) is an important issue when designing PCBs. To save time and cost, it is important to have knowledge to the PCB manufacturers capability and production tolerances. The parameters in the following describe our capability and main pricing factors.
You will not find all types of PCBs mentioned in this paper; this, however, does not necessarily mean we are incapable of producing such types - you are always welcome to submit designs for our technical evaluation.

1. MATERIALS

Rigid laminate/prepreg resin systems:

FR4	GF
High Tg FR4	GFG
BT-EPOXY	GM
POLYIMIDE	GI

Glass reinforcement and Aramide (thermount®) for Polyimide is available.

Microwave materials: RO3003, RO3006, RO3010, RO3203, RO3210, R4003, RO4350, RT6002,RT6006, RT6010LM, RT5870, RT5880, TMM3, TMM4, TMM6, TMM10
DiClad 527, D522, D870, D880, CuClad 217, C233, C250, AD300, AR320, AR350, AR450, AR600, AR1000, CLTE, 25N, 25FR

Flexible laminate systems:

With adhesive:
- Butyral based
- Acrylic based
- Epoxy based

Adhesiveless

We recommend to use adhesiveless flex material, due to better dimensional and thermal properties.

All multilayer laminate is specified acc. to IPC-4101 cl II.
As you may be aware, the IPC in cooperation with DSCC has developed an IPC Specification for Base Materials for Rigid and Multilayer Printed Boards (IPC4101) that will effectively replace MIL-S-13949 and the IPC "L" series of specifications (L-108, L-109, L-112 and L-115). IPC4101 was released for publication in December 1997 as the replacement standard for both Military and Commercial purchases of Laminate and Prepreg. It contains much of the language used in MIL-S-13949, including the requirements in the familiar Group "A", "B" and "C"

COPPER FOILS

Printca stocks (12),17,35,70µ copper foil, all foil is HTE type.
( ) Only used with buried / blind vias.
To have superior surface quality, CAC foil is used.

Copper Resistivity

With designs of finer lines, distributed resistance of copper is becoming increasingly important. The formula for calculating resistivity in copper traces is given by the following equation:

$R=(0.679 \times 10^{-6}$ ohm/inch) / (width X thickness inches)

Example: In fine-line designs, using 0.5 oz. Copper, a .005 trace, 5 inches long, the resistivity will be:

$((.679 \times 10^{-6}) / (5 \times 0.7 \times 10^{6})) \times 5 = 0.97$ Ohm

STANDARD STOCK MATERIALS AT PRINTCA

FR4 Double sided (Rigid laminate)

thickness copper (h=half ounce = 17µ, 1 = one ounce = 35µ, 2 = two ounce = 70µ)

0,80mm	h-h
1,55mm	h-h
1,55mm	1-1
1,55mm	2-2
2,00mm	1-1
2,00mm	h-h
2,40mm	h-h
2,40mm	1-1
3,20mm	1-1

FR4 Multilayer (Thin laminate)

0,002	h-h
0,005	h-1
0,005	1-1
0,008	1-1
0,008	1-2
0,008	2-2
0,010	1-1
0,014	h-1
0,014	1-1
0,014	2-1

0,014 2-2
0,018 h-1
0,018 1-1
0,022 h-1
0,022 1-1
0,022 1-2
0,022 2-2
0,028 1-1
0,028 2-2
0,028 h-1
0,036 1-1

Polyimide laminate

0,005 h-1
0,005 1-1
0,008 2-1
0,008 2-2
0,008 1-1
0,010 1-2
0,010 2-2
0,022 1-2
0,022 2-2

Flexible laminates

Rogers product series 2000:

20FR-C-110 2 mils polyimide, 1 mil acrylic adhesive
20FR-C-210 2 mils polyimide, 2 mil acrylic adhesive

Dupont AP series:

AP8525 2 mils adhesiveless 17/17 copper
AP9121 2 mils adhesiveless 35/35 copper
AP9222 2 mils adhesiveless 70/70 copper

COPPER FOILS

17µ and 35µ (12µ and 70µ only used on laminates)

Glass-epoxy prepregs GFN

1080 thickness 0.0026"
2125 thickness 0.0040"
7628 thickness 0.0070"

Glass-polyimide prepregs GIL

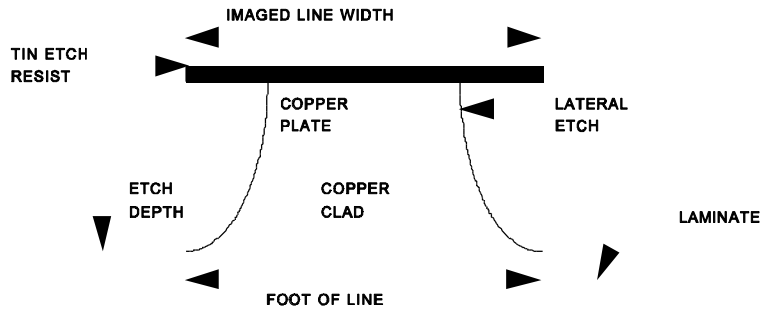
1080 thickness 0.0033"
2113 thickness 0.0043"

Glass-polyimide prepregs GIJ

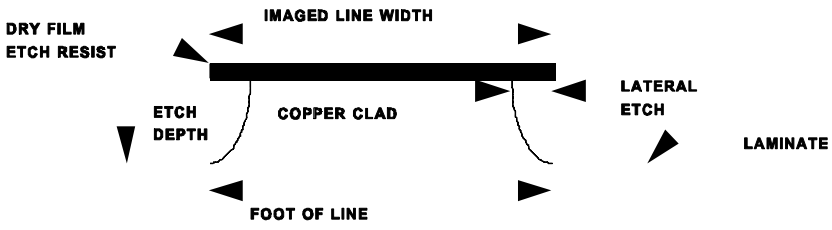
1080 thickness 0.0033"
2116 thickness 0.0046"

2. TRACK WIDTH & ISOLATION

The trace width changes due to predictable losses during the etching process. The diagram below shows a cross sectional view of the inner and outer layer trace after etching.



Outer Layer Line after Etching



Inner Layer Line after Etching

During the etching process, the etchant removes copper downward and laterally. The tin etch resist in the case of outer layers and the dry film etch resist in inner layers, establishes the original line width, but cannot avoid eventual undercut of this boundary. For outer layer, by virtue of the additional electroplated copper, the effective ratio of vertical versus lateral etch is approximately 1:1. For inner layers the etch ratio is approximately 2:1. This leads to trace profiles as shown in the diagrams shown above.

Copper clad weight is the most important factor in controlling trace width. Using 17µ copper clad reduces the total cop-per thickness etched and thereby reduces the lateral etching.

The etching process does not cause a significant change in the base line width (foot of line). The top of the line is reduced however. This is significant for electrical performance characteristics, such as impedance, since it reduces the cross sectional area and the effective (average) width of the line

Outer layers:

Minimum nominal track width:

Minimum:	0.100mm (17µ basic Cu.)
Price optimum:	0.150mm (17µ basic Cu.)

Minimum nominal isolation distance:

Minimum:	0.100mm (17µ basic Cu.)
Price optimum:	0.150mm (17µ basic Cu.)

Inner layers:

Minimum nominal track width:

Minimum std.:	0.100mm (max. 35µ basic Cu.)
Price optimum:	0.150mm (max. 35µ basic Cu.)

Minimum nominal isolation distance:

Minimum std.:	0.100mm (max. 35µ basic Cu.)
Price optimum:	0.150mm (max. 35µ basic Cu.)

PLATED THROUGH HOLES (PTH)

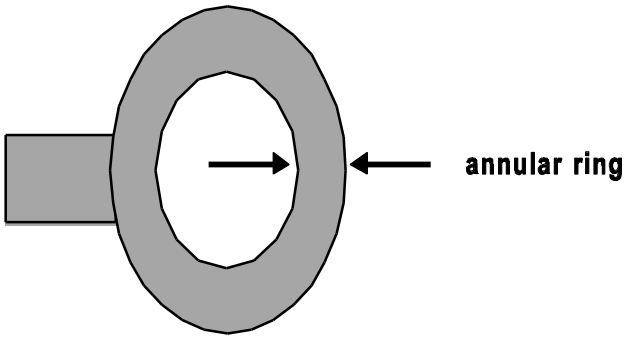
Minimum mechanical drilled through, std. production 0.30mm.
Minimum mechanical depth drilled (microvia) 0.1mm.
Laserdrilled microvias 0.075-0.15mm.
Minimum PTH diameter tolerance 0.15mm (ex: -0.05mm/+0.1mm)
PTH above 6.00mm is nibble drilled.

NON PLATED HOLES

Diameter tolerance, min. 0.05mm, up to dia. 6.00mm, above, 0.2mm dia. tol.

3. ANNULAR RING

The difference between the drill diameter and the corresponding circuitry pad diameter,divided by 2.



Specification for designed hole/pad ratio:

The pad diameter is calculated as:
Drilled hole dia. + production tolerance + (2 x annular ring)
Drilled hole is at Printca defined as: minimum hole + 0.2mm (except press-fit holes).

The production tolerance

is defined as; twice the misalignment between any hole and the corresponding pad on the PCB. The misalignment is depending on construction type, panel size, material type, etc..

Printca prod. tol. for 21" panels; price optimum

	Inner layer	**Outer layers**
Double sided PCBs	NA	+0.20mm
Multilayer, drilled through holes	+0.30mm	+0.20mm
Buried vias, two-layers	+0.20mm	NA
Blind vias, two-layers	+0.40mm	+0.30mm
Blind or buried vias between several layers	+0.50mm	+0.30mm
Multilayer with flexible inner layers +0.50mm	+0.20mm	
Micro vias capture pad size	0.35mm	0.35mm

Printca prod. tol. for 18" panels

Double sided PCBs	NA	+0.17mm
Multilayer, drilled through holes	+0.25mm	+0.17mm
Buried vias, two-layers	+0.17mm	NA
Blind vias, two-layers	+0.35mm	+0.27mm
Blind or buried vias between several layers	+0.45mm	+0.27mm
Multilayer with flexible inner layers +0.45mm	+0.17mm	
Micro vias capture pad size	0.30mm	0.30mm

Calculation of pad sizes, examples;

Pad size = drilled hole + printca prod.tol. + (2 x annular ring)

Example 1:

Pad size for **ESA PSS-01-710** spec. PCB, for a **0.9mm ±0.1mm Component hole**, designed for minimum pad sizes (higher costs) :
Prod. tol. are 0.2mm on outer layers.
(drilled hole will be min. hole + 0.2mm = 0.8 + 0.2 =1.0mm)
Annular ring demand for C-side is 250µ, S-side is 400µ.
C-side:
1.0 + 0.20 + (2 x 0.25) = **1.70mm**
S-side:
1.0 + 0.20 + (2 x 0.40) = **2.00mm**

Example 2:

Pad size for a **MIL-P-55110D** spec. PCB, to a **0.9mm ±0.1mm component hole**, designed for price optimum production.
Prod. tol. are 0.4mm on inner layers and 0.3mm on outer layers acc. To above fig.
(drilled hole will be min. hole + 0.2mm = 0.8 + 0.2 =1.0mm)
Annular ring demand for outer layers are 130µ, inner layers 51µ.
Pad size, outer layers:
1.0 + 0.30 + (2 x 0.130) = **1.56mm**
Pad size, inner layers:
1.0 + 0.40 + (2 x 0.051) = **1.52mm**

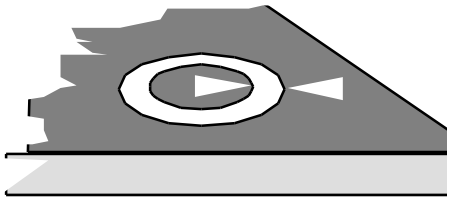
Example 3:

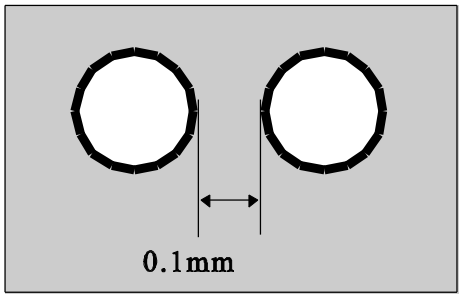
Pad size for a **industrial std**. spec. PCB, (e.g. the danish Perfag3) for a **0.9mm ±0.1mm component hole**, designed for price optimum production.
Prod. tol. are 0.4mm on inner layers and 0.3mm on outer layers acc. To above fig.
(drilled hole will be min. hole + 0.2mm = 0.8 + 0.2 =1.0mm)
Annular ring demand for outer layers are 50µ, inner layers 10µ.
Pad size, outer layers:
1.0 + 0.30 + (2 x 0.05) = **1.40mm**
Pad size, inner layers:
1.0 + 0.40 + (2 x 0.01) = **1.42mm**

Power- & ground-planes

On ground and power planes the clearance pads are the inner layer areas free of copper surrounding the finished hole diameters. It is calculated by measuring the difference between the specified drill diameter and the corresponding clearance pad diameter.

When designing planes without non-functional pads, the openings in the planes must be as follows:
Opening = required pad size + (2 x demand for isolation)
Ex: Openings in planes with conditions from example 2 above.
Inner layer required pad size was 1.52mm.
If demand for isolation is 6 mils (0.15mm) from holewall to plane, the openings must be designed:
1.52mm + (2 x 0.15mm) = 1.82mm





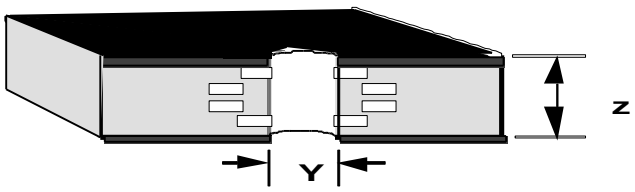
If the plane layer design leaves strips of copper between clearance pads, a minimum of 0.1mm is required between clearance pads to avoid causing shorts due to resist lifting and redepositing.

Remove copper from planes, minimum 0.4mm inside contour, and please remove copper 2.6mm outside contour. (Then our router last longer and the edge quality would be optimised)

If planes are designed with 70µ Copper we do not recommend to remove non-functional pads on the plane layers.

ASPECT RATIO

The maximum board thickness divided by the smallest selected drill diameter. The maximum board thickness is the calculated thickness over copper before plating. Additional thickness caused by plating, hot air levelling, or soldermask has no impact on aspect ratio.

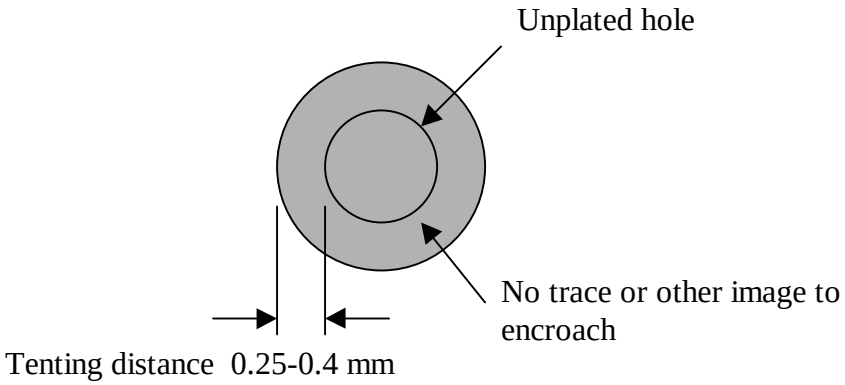


1:6 ratio is std.
From 0.4mm dia. holes, ratio 1:8 can be processed.
For depth drilled holes and micro vias, the ratio is 1:1.

TENTING OF UNPLATED HOLES

For improved locational accuracy of unplated holes, it is preferred to drill them during the initial plated through hole drilling set-up. In order to avoid plating of etch resist into these holes., it is required that the unplated holes be tented with dry film during the outer layer imaging process, overlapping the hole edge for a minimum distance. Before the etching process, this tent is removed. This allows the removal of copper from the hole walls during the consequent etching process.

Maximum hole diameter to be tented is 5mm, tenting dia. is hole dia. + 0.8mm.
For holes below 3mm, the tenting dia. is hole + 0.5mm.



4. FINISH

Electroless Nickel/Immersion Gold (99.9% Gold)

- Typical thickness: 0.1µ Gold over 5µ Nickel
- Excellent corrosion resistance
- Excellent for fine-pitch technology
- Excellent solderability
- Good for Aluminium wire bonding
- Excellent shelf life

HAL (Eutectic 63% Tin - 37% Lead)

- Typical coating thickness: 2-50µ, design dependent.
- Excellent solderability
- 0.63mm Pitch capability
- 0.8mm minimum board thickness capability
- Good shelf life

Reflowed Tin/lead

- Typical coating thickness: 8-15µ, after reflow.
- Excellent corrosion resistance
- Excellent solderability
- Qualified for SPACE
- Excellent shelf life

Nickel - Hard Gold

- Typical thickness: 1.5µ Gold (99.7%) over 5µ Nickel

- Excellent corrosion resistance
- 130 to 220 Knoop harness
- Excellent wear resistance, best for surface rotary switches, on-off contacts, and edge connectors
- Excellent shelf life

Nickel - Soft Gold

- Typical thickness: 2-4µ Gold (99.9%) over 5µ Nickel
- Excellent corrosion resistance
- Less than 90 Knoop hardness
- Good for pressure contacts and Aluminium or Gold-wire bonding
- Fair wear resistance

Organic Solderability Preservative (OSP)

- Typical coating thickness: 0.2µ to 0.5µ
- Excellent solderability
- Excellent surface coplanarity and hole size uniformity
- Excellent for use in Fine-pitch technology
- Improved surface contrast - assembly vision capability
- Board not subjected to thermal shock (as with HAL)
- Good shelf life (12 months)

Edge Connector Plating

The preferred manufacturing process for gold plating of edge connectors is Tab Plating. This process does not require the extra labour and materials associated with double image plating.
The maximum length of the gold plated tab is 30mm.
The annular ring of a through hole must be a minimum of 2mm from the edge of the gold plated area to prevent "black holes", resulting in solderability problems.

Note: The Tab Plate process is not set up for through hole plating. It is a surface plating process.
But when used on top of immersion Ni/Au, it is possible to plate hard-Gold in holes.

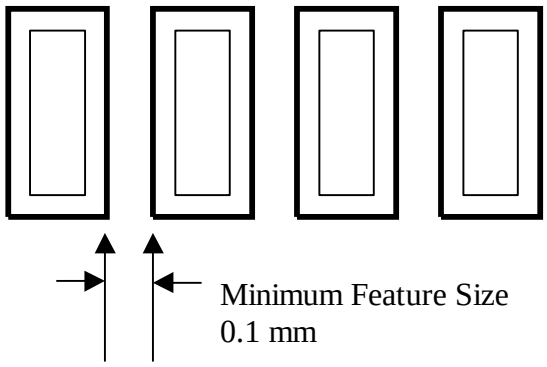
Selective Plating

It is possible to plate areas separately, with extra copper.
Typically it is used for selective via plating and raised SMD pads.
Contact Printca for further advise.

5. SOLDERMASK

Wetfilm 20µ, dryfilm 50µ, 75µ or 100µ, two-pack epoxy 100µ.
Openings in the soldermask should be designed acc. to isolation on outer layers.

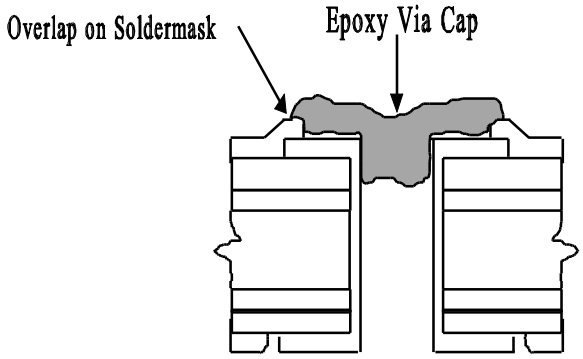
Ex: for a PCB with 6 mils isolation on outer layers, the soldermask opening should be designed as; pad size + 6 mils.
Minimum soldermask-string-width; allowed between SMD is 0.2mm with open vias and 0.1mm when vias are covered with soldermask..



Via Capping with Screened Resist

Hole capping is available through the Via Cap process. On boards coated with liquid photo-imaginable mask, the vias can be screened with soldermask creating an epoxy cap.

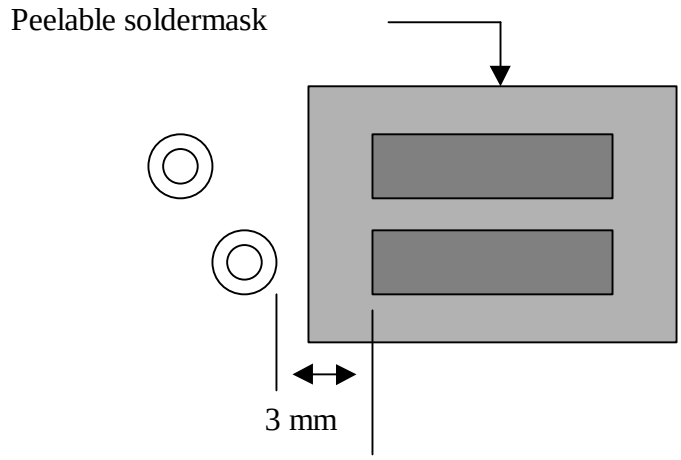
The maximum finished hole size for via capping is 0.5mm diameter
Generally, the non-test vias are capped on the bottom side of the board. Via capping on both sides results in raised or broken caps. Therefore, it is not permissible.
Via caps will have a raised surface of about 50µ above the outer layer copper pad.



Peelable Soldermask

Peelable soldermask (PSM) is a temporary soldermask which is selectively applied to a circuit board. Its purpose is to protect surfaces from being soldered.

Colour: Green or blue (two different types)
Nomenclature over Solder (HAL) will have poor adherence.
Due to registration, we recommend min.
1.5mm distance/overlap with peelable mask.

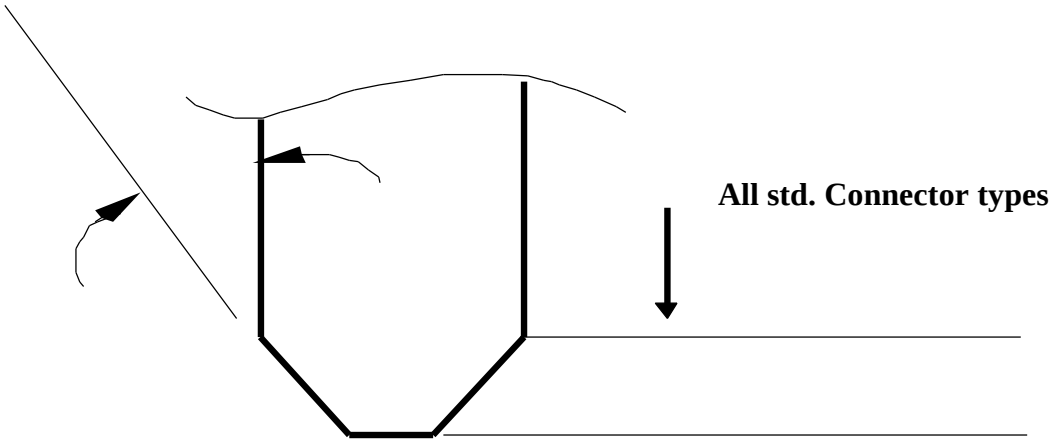


6. ROUTING

Std. router is 2.4mm, except for polyimide laminate, here 1.4mm is std..
Minimum router is 0.8mm.
Routing tolerance ±0.10mm

Please design a gerber-layer that represent the board contour, where the centre of the track is the edge of the board. It would be preferred if gerber circle commands as G74 and G75 is supported when corners are rounded.

Bevelling of edge connectors

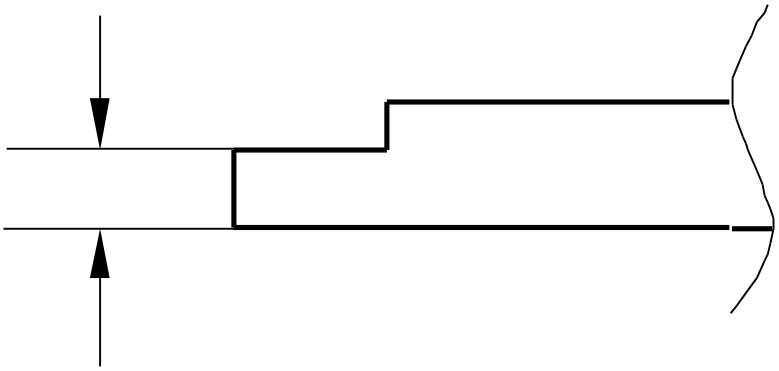


Scoring

V-cut or scoring is available
0.4mm scoring, 0.8mm to nearest copper from scoring centre line.

Depth controlled routing

It is possible to get the board edge thinner, due to rack mounting.



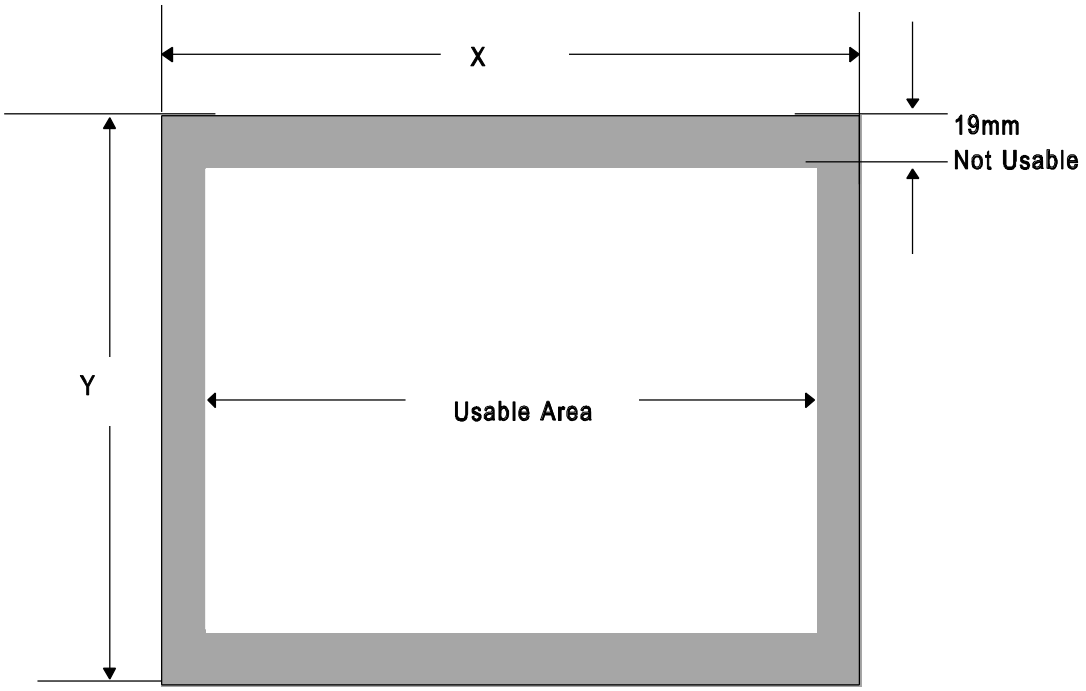
7. PANEL UTILISATION

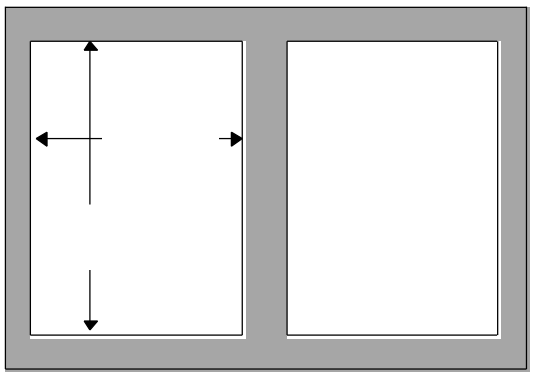
Panel sizes MLB; 12x18, 16x18, 12x21, 12x24, 16x21, 18x24 inches.
Panel sizes R/F; 12x18, 12x24, 18x24 inches

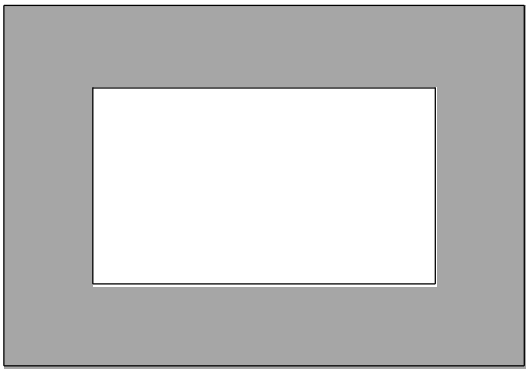
The most effective material utilisation will be achieved with boards or arrays of boards having their finished outline fit as efficiently as possible within the usable area of the panel . Test coupons must be within the usable area.
If the entire panel is shipped to the customer, the customer may negotiate to have locating holes and/or break-away tabs for insertion or surface mount equipment located outside the sable area. Material utilisation may be increased by utilising the scoring process.

Multilayer Usable Area Diagrams

For multilayer circuit boards, a border of 19mm around the panel can not be used for any part of the finished circuit board.







Excellent Panel Utilisation (84%)

Poor Panel Utilisation (33%)

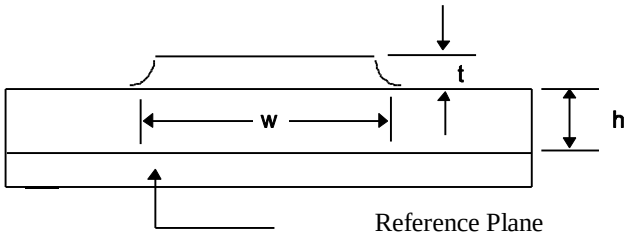
8. CONTROLLED IMPEDANCE

Characteristic Impedance

The characteristic impedance of a transmission line is dependent on the relationship of the conductor width, conductor thickness, dielectric thickness between conductor and ground-power reference planes, and the dielectric constant of the dielectric medium.
It is recommended that the designer contacts Printca to discuss impedance needs during the initial design phase. This will enable mutual understanding of requirements and impact of material characteristics, such as specific Dk-s and manufacturing processes, on needed impedance targets and tolerances.
The actual impedance may have to be tested via a small prototype build. This is often necessary when tight impedance tolerances are required, or in the case of small line widths and dielectric thicknesses, which are more sensitive to variations. A tolerance swing due to etching variations will be more significant for a 0.127 mm line width than for a 0.254 mm line, for example.

The recommended impedance tolerance is +/- 10 %. A lesser tolerance is often achievable, especially with fully embedded Microstrip and Stripline structures.

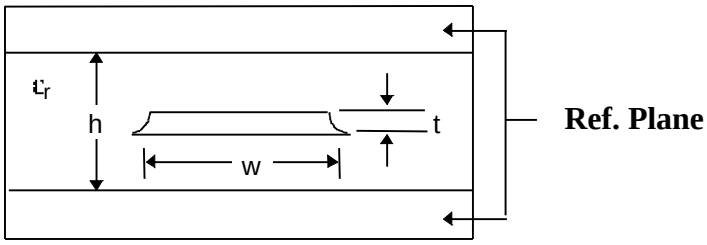
Surface Microstrip



The microstrip line is a popular transmission line structure for high speed digital circuits. The Surface Microstrip location on the external layer is subject to potentially greater impedance variables. This is due to the additional copper electro-plating it receives, resulting in increased line thickness and line width tolerances.

For critical applications, the Microstrip line can be embedded in dielectric material. The impedance can be calculated from the Surface Microstrip formula. Then for each 0.001 inch below the surface, subtract
1% of the impedance calculated. This derating factor provides good results for embedding up to approximately 0.381 mm. A thicker embedding has little additional effect.

Triplate stripline



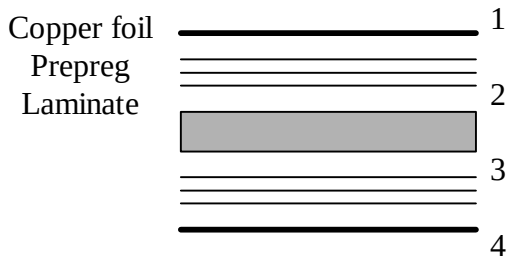
The stripline is embedded in dielectric material and is sandwiched between two reference planes. This configuration significantly reduces cross talk effect. This structure is most suitable for improving impedance tolerances.

Impedance Test Pattern

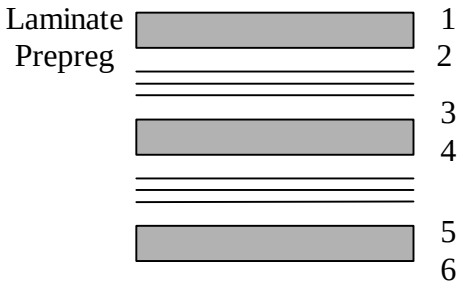
Actual Impedance will be measured via the TDR (Time Domain Reflectometry) method. Test coupon will be generated by Printca.

9. MULTILAYER CONSTRUCTION

Foil Lamination is the method of choice assigned by Printca. It is the most cost effective manufacturing process and minimises potential for bow and twist.
For SPACE applications laminate constructions are used due to surface quality.



Copper-foil MLB

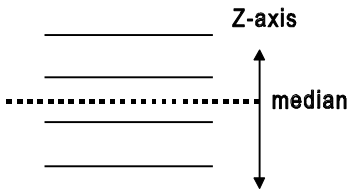


Laminate MLB

If specifying dielectric thickness, as may be required for impedance reasons for example, the dimensions should be selected from core or prepreg thicknesses that are available from Printca.

Dielectric thicknesses made up of prepreg depend on the type or the combination of different types of these materials. Printca will advise you of what combination of prepreg is suitable and of achievable dimensions and tolerances.
It is beneficial to discuss special dielectric requirements with Printca during the design stage if possible. This will allow time for material procurement if necessary. Also, manufacturing concerns can be addressed while an opportunity still exists to make changes.
Thickness is not the only indicator of material cost. Other factors, such as type, thickness tolerance, or the demand for this material may influence cost. If no specific dielectric thicknesses are required, it is best to allow Printca to make the material selection. Materials that will be utilised will meet industry standards, be of lowest cost, and allow the most effective manufacturing methods.
Maintaining a balanced lay-up in relation to the Z-axis median of the board will assure minimum bow and twist. This balance includes the following:

- Dielectric thickness of layer
- Copper thickness of layers and its distribution
- Location of circuit and plane layers
- Glass-styles used in laminates and prepregs



A higher number of layers normally means an increase number of plane layers. Planes need to be balanced around the Z-axis median line of the lay-up, and ideally located internal to the board.

If accepted Multilayer design rules are adhered to, boards will meet a maximum allowable bow and twist specification of 1% or better.
Printca would use thick laminate cores, min. 2 sheet prepregs between layers, only dimensional stable laminates. When using laminate constructions, the outer laminate is used for layer 1-0, to avoid shifted layers.

Recommended materials

Printca recommend to use 5, 8, 14, 22, 28 and 36 mils laminates for MLBs.

Prepreg thickness mils: Resin type

Glass-style	GF	BT	GI	GIJ
1080	0.0026	0.003	0.0031	0.0033
2113			0.0043	
2125	0.004			
2116		0.0046		0.0046
7628	0.007			

Outer Layer Circuitry

Circuit area and distribution between the front and back of the board should be balanced as closely as possible.
Plating thieving of low pattern density and cross hatching of external plane area should be considered.

Thickness Calculation and Tolerance

As the overall thickness of a multilayer board increases, the thickness tolerance should also increase. A good rule is to specify a tolerance of +/- 10% of the overall thickness.
Always indicate where the thickness measurement is to be taken. Examples might be: glass to glass at rail guides, over gold contacts, over solder mask, etc.

When calculating the potential board thickness, consideration needs to be given to certain design characteristics. An isolated .006 inch line may totally embed itself into the prepreg and make no contribution to the thickness of the board.

Pressed thickness is calculated as:
laminates (ML laminates is measured without copper foil)
+ prepreg pressed thickness

+ Copper thickness on planes
+ Outer layer copper foil

Filling of planes with resin

When having 70µ copper planes or thicker, it should be taken into account that there is resin to fill the openings in the plane, and when combined with polyimide resin system, GIL should be changed to GIJ when filling properties is needed.

Fabrication Drawing

The designer needs to specify the critical features of the design, i.e., finished board thickness, minimum dielectric spacing, number of layers and any electrical performance characteristic critical to the manufacture of the board, i.e., impedance requirements on the fabrication drawing. The fabricator should be left with the maximum amount of latitude the design will allow.

STANDARD MULTILAYER BUILD-UP-S

Cu.	Base mat.	Layer	Plane
4-layers			
17µ	Foil	1	
	2x7628 Prepreg		
35µ		2	
	0.036" Laminate		
35µ		3	
	2x7628 Prepreg		
17µ	Foil	4	

Pressed thickness 1.64mm

4-layers with 2 plane layers			
17µ	Foil	1	
	1x7628 Prepreg		
	1x2112 Prepreg		
35µ		2	X
	0.036" Laminate		
35µ		3	X
	1x2112 Prepreg		

1x7628 Prepreg
17µ Foil 4

Pressed thickness 1.55mm

6-layers

17µ Foil 1
3x2112 Prepreg
35µ 2
0.014" Laminate
35µ 3 X
2x2112 Prepreg
35µ 4 X
0.014" Laminate
35µ 5
3x2112 Prepreg
17µ Foil 6

Pressed thickness 1.55mm

8-layers

17µ Foil 1
3x2112 Prepreg
35µ 2
0.008" Laminate
35µ 3
2x2112 Prepreg
35µ 4 X
0.008" Laminate
35µ 5 X
2x2112 Prepreg
35µ 6
0.008" Laminate
35µ 7
3x2112 Prepreg
17µ Foil 8

Pressed thickness 1.60mm

10-layers

17µ Foil 1
2x2112 Prepreg
35µ 2

	0.005" Laminate		
35µ		3	
	2x2112 Prepreg		
35µ		4	
	0.005" Laminate		
35µ		5	X
	2x2112 Prepreg		
35µ		6	X
	0.005" Laminate		
35µ		7	
	2x2112 Prepreg		
35µ		8	
	0.005" Laminate		
35µ		9	
	2x2112 Prepreg		
17µ	Foil	10	

Pressed thickness 1.53mm

12-layers

17µ	Foil	1	
	2x1080 Prepreg		
35µ		2	
	0.005" Laminate		
35µ		3	
	2x2112 Prepreg		
35µ		4	
	0.005" Laminate		
35µ		5	
	2x1080 Prepreg		
35µ		6	X
	0.005" Laminate		
35µ		7	X
	2x1080 Prepreg		
35µ		8	
	0.005" Laminate		
35µ		9	
	2x2112 Prepreg		
35µ		10	
	0.005" Laminate		
35µ		11	
	2x1080 Prepreg		
17µ	Foil	12	

Pressed thickness 1.67mm