DDR3 SDRAM Interface Termination and Layout Guidelines

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Introduction

This application note provides guidelines on how to improve the signal integrity of your system and layout guidelines to help you successfully implement a DDR3 SDRAM interface on your system.

Synchronous Dynamic Random Access Memory (SDRAM) has continually evolved over the years to keep up with ever-increasing computing needs. The latest addition to SDRAM technology is DDR3 SDRAM. DDR3 SDRAM is the third generation of the DDR SDRAM family, and offers improved power, higher data bandwidth, and enhanced signal quality with multiple on-die termination (ODT) selection and output driver impedance control while maintaining partial backward compatibility with the existing DDR2 SDRAM standard.

DDR3 SDRAM offers features designed to improve signal integrity of increased bus speed. While some of the features are already available in DDR2 SDRAM, these features are further enhanced in DDR3 SDRAM. For example, the ODT feature is available in both DDR2 and DDR3 SDRAM, but in DDR3 SDRAM, the values of the ODT are based on the value of an external resistor—the RZQ resistor. In addition to using this ZQ resistor for setting the ODT value, it is also used for calibrating the ODT value so that it maintains its resistance value to within a 10% tolerance. This application note describes the following updated and new features in DDR3 SDRAM:

- ODT values selection
- Output driver impedance selection
- ZQ calibration
- Dynamic ODT usage

To take advantage of these new features offered by DDR3 SDRAM, Altera's Stratix III and Stratix IV FPGAs have special features to ease and expedite your implementation of DDR3 SDRAM interfaces.

With Leveling or Without Leveling

Altera offers the DDR3 SDRAM PHY with or without leveling.

With Leveling

DDR3 SDRAM DIMMs, as specified by JEDEC, always use a fly-by topology for the address, command, and clock signals. This standard DDR3 SDRAM topology requires the use of the Altera DDR3 SDRAM ALTMEMPHY megafunction with read and write leveling.

For more information on the ALTMEMPHY megafunction, refer to the *External Memory PHY Interface Megafunction User Guide (ALTMEMPHY)*.

Altera recommends that for full DDR3 SDRAM compatibility when using discrete DDR3 SDRAM components, you should mimic the JEDEC DDR3 µDIMMs fly-by topology on your custom PCBs.

Arria II GX devices do not support DDR3 SDRAM with read or write leveling, so standard DDR3 SDRAM DIMMs or DDR3 SDRAM components using the standard DDR3 SDRAM fly-by address, command, and clock layout topology are not supported. Refer to "Termination for DDR3 SDRAM Components (Without Leveling)" on page 27, for more information on how to use DDR3 SDRAM components with Arria II GX devices.

Use of the standard JEDEC DDR3 fly-by topology with leveling offers the following advantages:

- Easier layout
- Lower SSN for the memory
- Higher data rates

Refer to "Read and Write Leveling" on page 3 for more detailed information on read and write leveling.

Without Leveling

Altera also supports DDR3 SDRAM components without leveling, using a nonstandard, synchronous DDR2-like balanced address, command, and clock layout topology. DDR3 SDRAM interfaces without leveling operate at lower maximum data rates compared to the standard fly-by topology. DDR3 SDRAM interfaces without leveling may be desirable for the following reasons:

- The Altera device family does not support read and write leveling, so DDR3 SDRAM DIMMs or topology is not supported, but the I/O electrical standard is supported
- DDR3 SDRAM PHYs without leveling typically have a slightly lower PHY latency when compared to the DDR3 SDRAM PHY with leveling
- The DDR3 SDRAM PHY without leveling typically requires less FPGA resources than an equivalent DDR3 SDRAM PHY with leveling
- You may only require DDR2-like interface performance but want to use the lower power, potential cost, and availability benefits of DDR3 SDRAM components

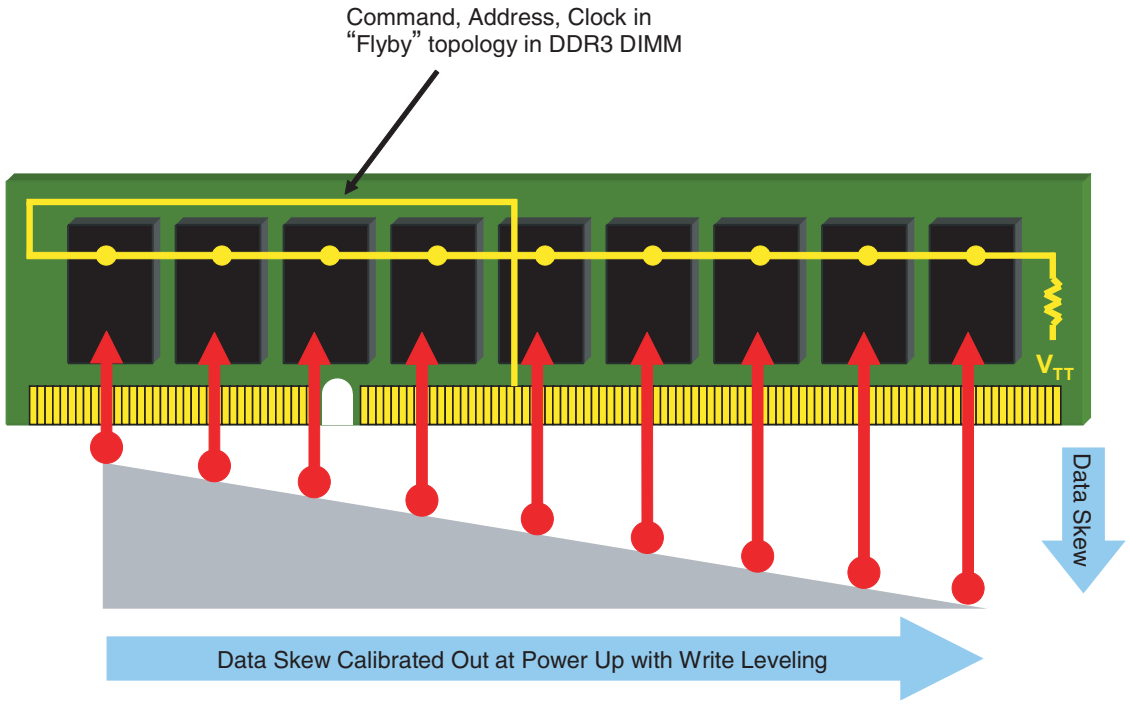
Comparing DDR3 and DDR2

The following sections review the differences between DDR2 and DDR3 SDRAM and the changes in the features that were made to DDR3 SDRAM. Understanding these differences makes the design process for your DDR3 SDRAM interface easier.

Read and Write Leveling

One major difference between DDR2 and DDR3 SDRAM is the use of leveling. To improve signal integrity and support higher frequency operations, the JEDEC committee defined a fly-by termination scheme used with the clocks and command and address bus signals. Fly-by topology reduces simultaneous switching noise (SSN) by deliberately causing flight-time skew between the data and strobes at every DRAM as the clock, address, and command signals traverse the DIMM (Figure 1).

Figure 1. DDR3 DIMM Fly-By Topology Requiring Write Leveling *(Note 1)*



Note to Figure 1:

(1) Source: *Consumer Electronics are Changing the Face of DRAMs*, By Jody Defazio, Chip Design Magazine, June 29, 2007.

The flight-time skew due to the fly-by topology led the JEDEC committee to introduce the write leveling feature on the DDR3 SDRAMs, thus requiring controllers to compensate for this skew by adjusting the timing per byte lane.

During a write, DQS groups are launched at separate times to coincide with a clock arriving at components on the DIMM, and must meet the timing parameter between the memory clock and DQS defined as t_{DQSS} of ± 0.25 t_{CK}.

During the read operation, the memory controller must compensate for the delays introduced by the fly-by topology. In Stratix® III and Stratix IV FPGAs, there are alignment and synchronization registers built in the input output element (IOE) to properly capture the data. Figure 2 shows two DQS groups returning from the DIMM for the same read command.

For information about the IOE block in Stratix III devices, refer to the *External Memory Interfaces in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*.

For information about the IOE block in Stratix IV devices, refer to the *External Memory Interfaces in Stratix IV Devices* chapter in volume 1 of the *Stratix IV Device Handbook*.

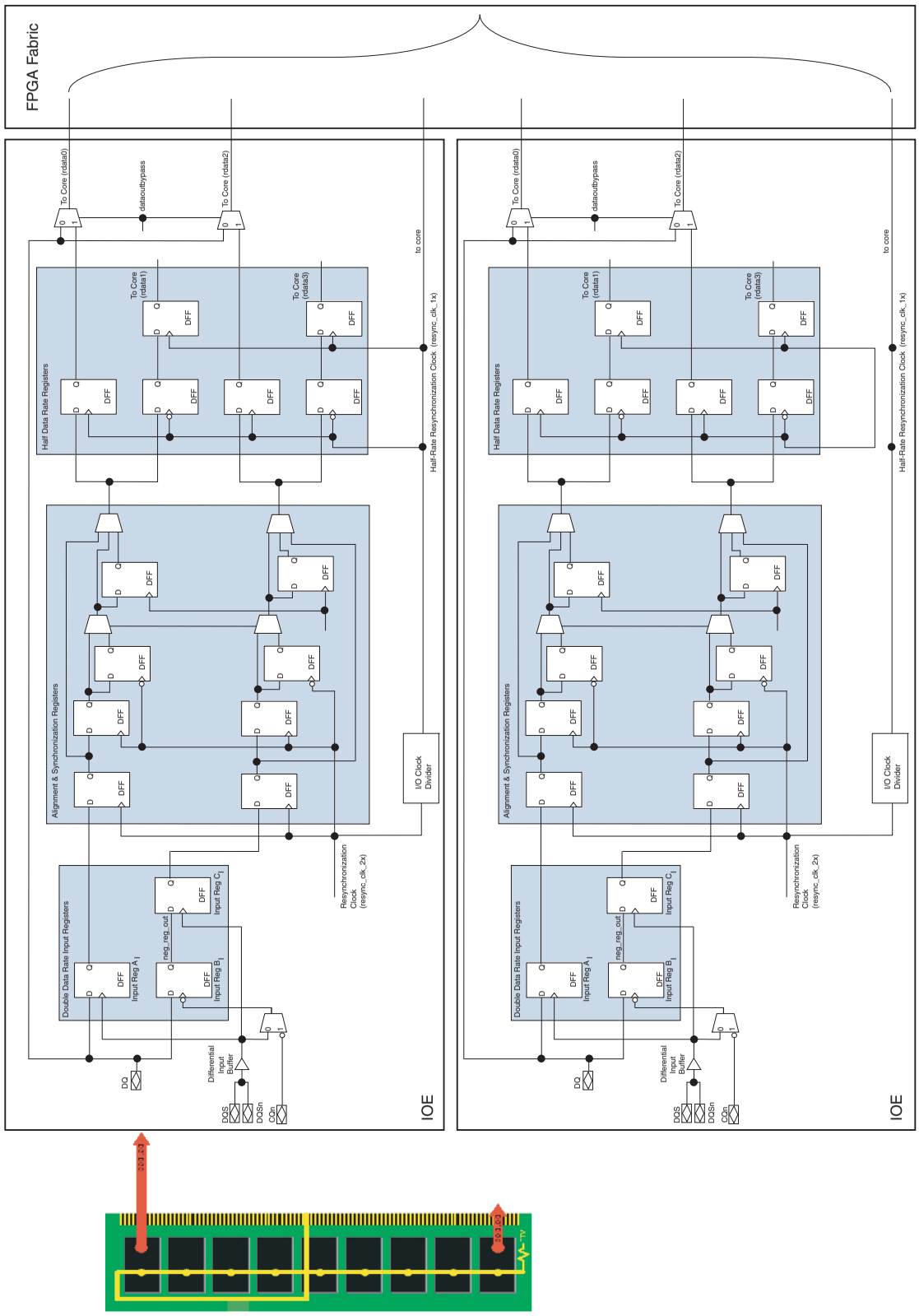


Figure 2. DDR3 DIMM Fly-By Topology Requiring Read Leveling

Calibrated Output Impedance and ODT

In DDR2 SDRAM, there are only two drive strength settings, full or reduced, which correspond to the output impedance of 18 Ω and 40 Ω, respectively. These output drive strength settings are static settings and are not calibrated; as a result, the output impedance varies as the voltage and temperature drifts. The DDR3 SDRAM uses a programmable impedance output buffer. Currently, there are two drive strength settings, 34 Ω and 40 Ω. The 40-Ω drive strength setting is currently a reserved specification defined by JEDEC, but available on the DDR3 SDRAM, as offered by some memory vendors. Refer to the datasheet of the respective memory vendors for more information about the output impedance setting. The drive strength setting is selected by programming the memory mode register setting defined by mode register 1 (MR1). To calibrate output driver impedance, an external precision resistor, RZQ, is connected between the ZQ pin and VSSQ. The value of this resistor must be 240 Ω ± 1%. If you are using a DDR3 SDRAM DIMM, RZQ is soldered on the DIMM so you do not need to layout your board to account for it. Output impedance is set during initialization. To calibrate output driver impedance after power-up, the DDR3 SDRAM needs a calibration command that is part of the initialization and reset procedure and is updated periodically when the controller issues a calibration command.

In addition to calibrated output impedance, the DDR3 SDRAM also supports calibrated parallel ODT via the same external precision resistor, RZQ, which is possible by using a merged output driver structure in the DDR3 SDRAM, which also helps to improve pin capacitance in the DQ and DQS pins. The ODT values supported in DDR3 SDRAM are 20 Ω, 30 Ω, 40 Ω, 60 Ω, and 120 Ω, assuming that RZQ is 240 Ω.

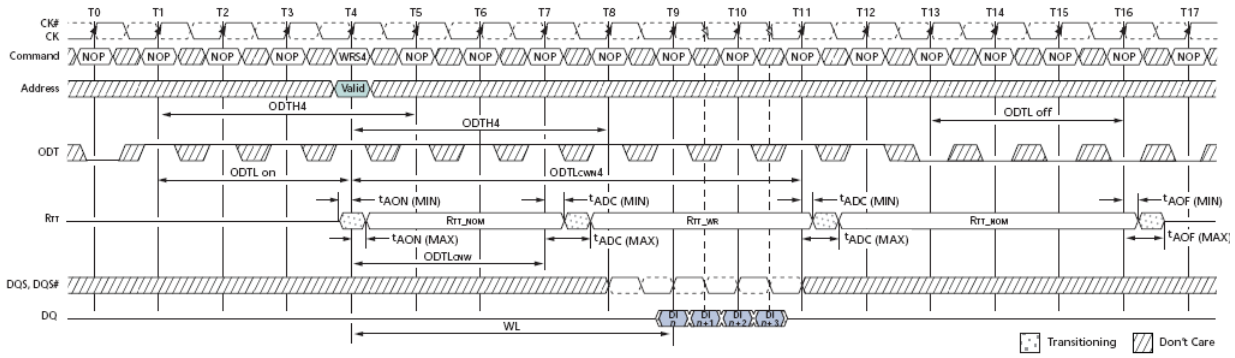
In DDR3 SDRAM, there are two commands related to the calibration of the output driver impedance and ODT. The first calibration command, ZQ CALIBRATION LONG (ZQCL), is often used at initial power-up or when the DDR3 SDRAM is in a reset condition. This command calibrates the output driver impedance and ODT to the initial temperature and voltage condition, and compensates for any process variation due to manufacturing. If the ZQCL command is issued at initialization or reset, it takes 512 memory clock cycles to complete; otherwise, it requires 256 memory clock cycles to complete. The second calibration command, ZQ CALIBRATION SHORT (ZQCS) is used during regular operation to track any variation in temperature or voltage. The ZQCS command takes 64 memory clock cycles to complete. Use the ZQCL command any time there is more impedance error than can be corrected with a ZQCS command.

For more information about using ZQ Calibration in DDR3 SDRAM, refer to the application note by Micron, *TN-41-02 DDR3 ZQ Calibration*.

Dynamic ODT

Dynamic ODT is a new feature in DDR3 SDRAM, and not available in DDR2 SDRAM. Dynamic ODT can change the ODT setting without issuing a mode register set (MRS) command. When you enable dynamic ODT, and there is no write operation, the DDR3 SDRAM is terminated to a termination setting of `RTT_NORM`; when there is a write operation, the DDR3 SDRAM is terminated to a setting of `RTT_WR`. The values of `RTT_NORM` and `RTT_WR` are preset by programming the mode registers, MR1 and MR2. Figure 3 shows the behavior of ODT when dynamic ODT is enabled.

Figure 3. Dynamic ODT: Behavior with ODT Asserted Before and After the Write *(Note 1)*



Note to Figure 3:

(1) Source: *TN-41-04 DDR3 Dynamic On-Die Termination*, Micron.

In the two-DIMM DDR3 SDRAM configuration, dynamic ODT helps reduce the jitter at the module being accessed, and minimizes reflections from any secondary modules.

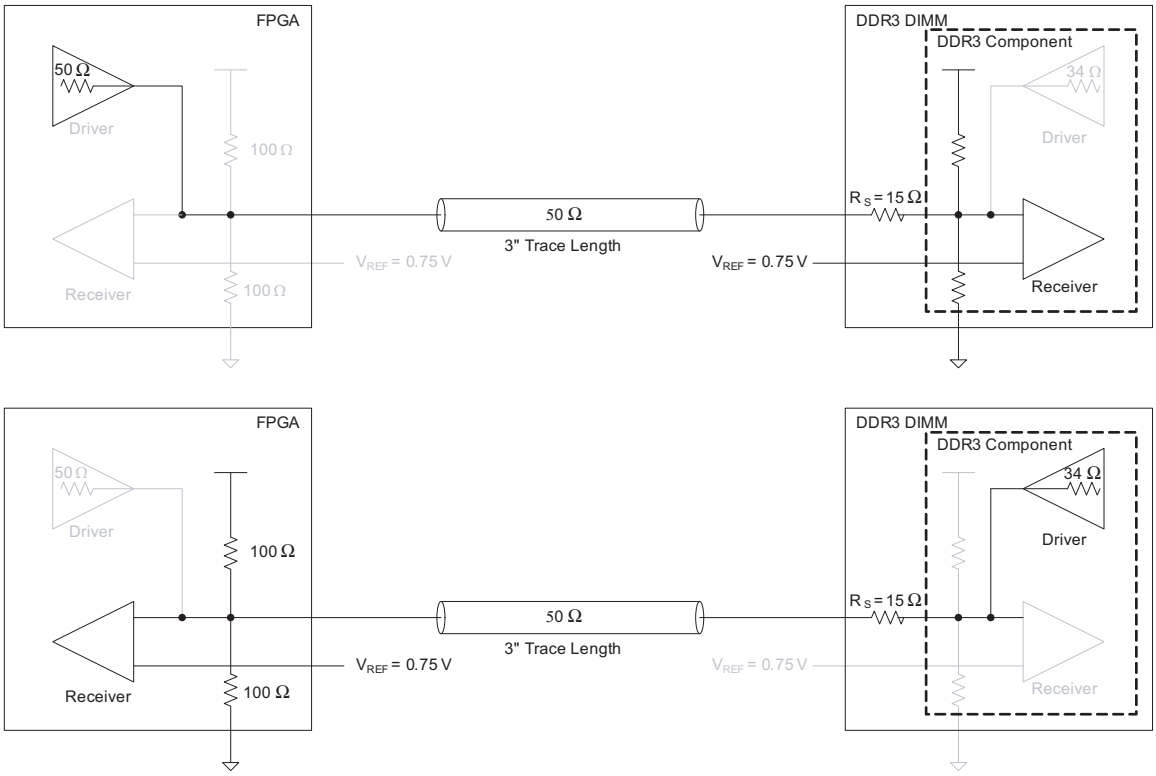
For more information about using the dynamic ODT on DDR3 SDRAM, refer to the application note by Micron, *TN-41-04 DDR3 Dynamic On-Die Termination*.

Dynamic OCT in Stratix III and Stratix IV Devices

Stratix III and Stratix IV devices support on-off dynamic series and parallel termination for a bi-directional I/O in all I/O banks. Dynamic OCT is a new feature in Stratix III and Stratix IV FPGA devices. Dynamic parallel termination is enabled only when the bi-directional I/O acts as a receiver and is disabled when it acts as a driver. Similarly, dynamic series termination is enabled only when the bi-directional I/O acts as a driver and is disabled when it acts as a receiver.

Additionally, the dynamic control operation of the OCT is separate to the output enable signal for the buffer. Hence, the Altera ALTMEMPHY megafunction can only enable parallel OCT during read cycles, saving power when the interface is idle.

Figure 4. Dynamic OCT between Stratix III and Stratix IV FPGA Devices



This feature is useful for terminating any high-performance bi-directional path because signal integrity is optimized depending on the direction of the data. In addition, dynamic OCT also eliminates the need for external termination resistors when used with memory devices that support ODT (such as DDR3 SDRAM), thus reducing cost and easing board layout.

However, dynamic OCT in Stratix III and Stratix IV FPGA devices is different from dynamic ODT in DDR3 SDRAM mentioned in previous sections and these features should not be assumed to be identical.

For detailed information about the dynamic OCT feature in the Stratix III FPGA, refer to the *Stratix III Device I/O Features* chapter in volume 1 of the *Stratix III Device Handbook*.

For detailed information about the dynamic OCT feature in the Stratix IV FPGA, refer to the *I/O Features in Stratix IV Devices* chapter in volume 1 of the *Stratix IV Device Handbook*.

Termination for DDR3 SDRAM Unbuffered DIMMs

The following sections describe the correct way to terminate a DDR3 SDRAM interface together with Altera® Stratix III and Stratix IV FPGA devices.

DDR3 SDRAM Unbuffered DIMM

The most common implementation of the DDR3 SDRAM interface is the unbuffered DIMM. Unbuffered DDR3 SDRAM DIMMs can be found in many applications, especially in personal computer (PC) applications. A DDR3 SDRAM unbuffered DIMM interface can be implemented in several permutations, such as single DIMM or multiple DIMMs, using either single-ranked or dual-ranked unbuffered DIMMs. In addition to the unbuffered DIMMs form factor, these termination recommendations are also valid for small-outline (SO) DIMMs and MicroDIMMs.

Table 1 outlines the different permutations of a two-slot DDR3 SDRAM interface and the recommended ODT settings on both the memory and controller when writing to memory.

Table 1. DDR3 SDRAM ODT Matrix for Writes *(Note 1)* and *(2)*

Slot 1	Slot 2	Write To	Controller OCT *(3)*	Slot 1		Slot 2	
				Rank 1	Rank 2	Rank 1	Rank 2
DR	DR	Slot 1	Series 50 Ω	120 Ω *(4)*	ODT off	ODT off	40 Ω *(4)*
		Slot 2	Series 50 Ω	ODT off	40 Ω *(4)*	120 Ω *(4)*	ODT off
SR	SR	Slot 1	Series 50 Ω	120 Ω *(4)*	Unpopulated	40 Ω *(4)*	Unpopulated
		Slot 2	Series 50 Ω	40 Ω *(4)*	Unpopulated	120 Ω *(4)*	Unpopulated
DR	Empty	Slot 1	Series 50 Ω	120 Ω	ODT off	Unpopulated	Unpopulated
Empty	DR	Slot 2	Series 50 Ω	Unpopulated	Unpopulated	120 Ω	ODT off
SR	Empty	Slot 1	Series 50 Ω	120 Ω	Unpopulated	Unpopulated	Unpopulated
Empty	SR	Slot 2	Series 50 Ω	Unpopulated	Unpopulated	120 Ω	Unpopulated

Notes to Table 1:

(1) SR: single-ranked DIMM; DR: dual-ranked DIMM.

(2) These recommendations are taken from the *DDR3 ODT and Dynamic ODT* session of the JEDEC DDR3 2007 Conference, Oct 3-4, San Jose, CA.

(3) The controller in this case is the FPGA.

(4) Dynamic ODT is required. For example, the ODT of Slot 2 is set to the lower ODT value of 40 Ω when the memory controller is writing to Slot 1, resulting in termination and thus minimizing any reflection from Slot 2. Without dynamic ODT, Slot 2 will not be terminated.

Table 2 outlines the different permutations of a two-slot DDR3 SDRAM interface and the recommended ODT settings on both the memory and controller when reading from memory.

Table 2. DDR3 SDRAM ODT Matrix for Reads *(Note 1)* and *(2)* (Part 1 of 2)

Slot 1	Slot 2	Read From	Controller OCT *(3)*	Slot 1		Slot 2	
				Rank 1	Rank 2	Rank 1	Rank 2
DR	DR	Slot 1	Parallel 50 Ω	ODT off	ODT off	ODT off	40 Ω
		Slot 2	Parallel 50 Ω	ODT off	40 Ω	ODT off	ODT off
SR	SR	Slot 1	Parallel 50 Ω	ODT off	Unpopulated	40 Ω	Unpopulated
		Slot 2	Parallel 50 Ω	40 Ω	Unpopulated	ODT off	Unpopulated
DR	Empty	Slot 1	Parallel 50 Ω	ODT off	ODT off	Unpopulated	Unpopulated
Empty	DR	Slot 2	Parallel 50 Ω	Unpopulated	Unpopulated	ODT off	ODT off
SR	Empty	Slot 1	Parallel 50 Ω	ODT off	Unpopulated	Unpopulated	Unpopulated

Table 2. DDR3 SDRAM ODT Matrix for Reads *(Note 1)* and *(2)* (Part 2 of 2)

Slot 1	Slot 2	Read From	Controller OCT *(3)*	Slot 1		Slot 2	
				Rank 1	Rank 2	Rank 1	Rank 2
Empty	SR	Slot 2	Parallel 50 Ω	Unpopulated	Unpopulated	ODT off	Unpopulated

Notes to Table 2:

(1) SR: single-ranked DIMM; DR: dual-ranked DIMM.

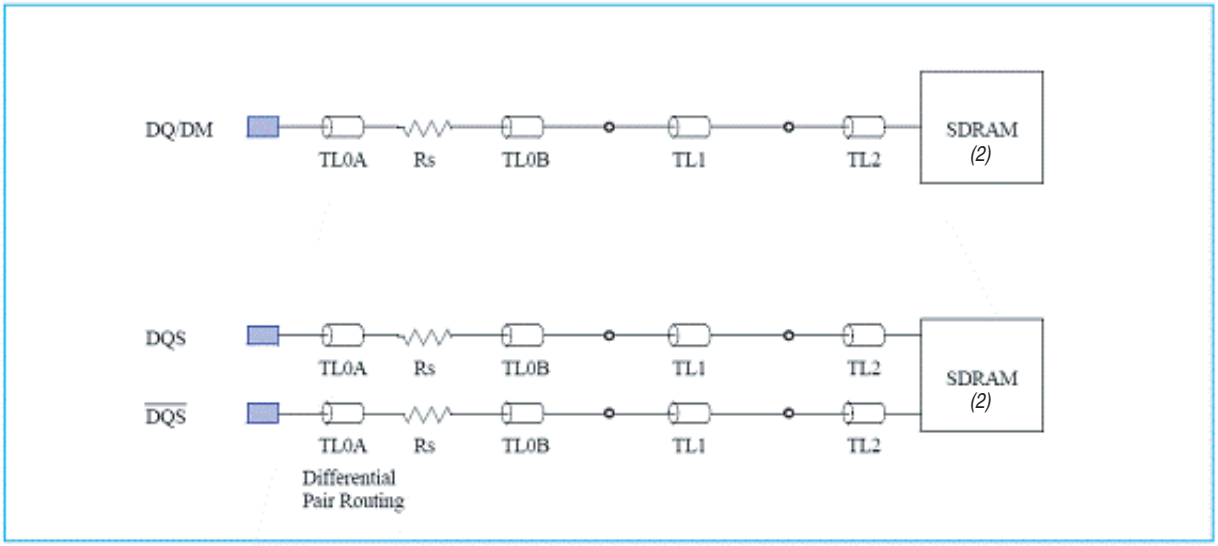
(2) These recommendations are taken from the *DDR3 ODT and Dynamic ODT* session of the JEDEC DDR3 2007 Conference, Oct 3-4, San Jose, CA.

(3) The controller in this case is the FPGA. JEDEC typically recommends 60 Ω, but this value assumes that the typical motherboard trace impedance is 60 Ω and that teh controller supports this termination. Altera recommends using a 50-Ω parallel OCT when reading from the memory.

DQS, DQ, and DM for DDR3 SDRAM Unbuffered DIMM

On a single-ranked DIMM, DQS, and DQ signals are point-to-point signals. Figure 5 shows the net structure for differential DQS and DQ signals. There is an external 15-Ω stub resistor, R_S, on each of the DQS and DQ signals soldered on the DIMM, which helps improve signal quality by dampening reflections from unused slots in a multi-DIMM configuration.

Figure 5. DQ and DQS Net Structure for 64-Bit DDR3 SDRAM Unbuffered DIMM *(Note 1)*



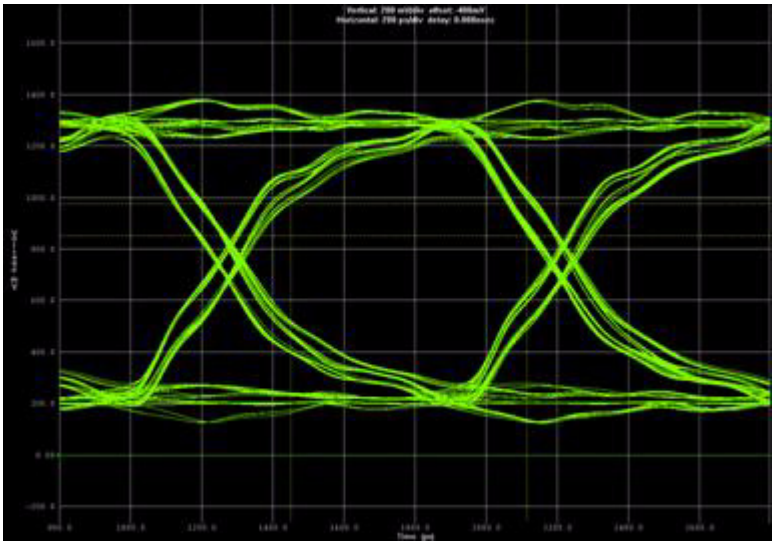
Notes to Figure 5:

(1) Source: *PC3-6400/PC3-8500/PC3-10600/PC3-12800 DDR3 SDRAM Unbuffered DIMM Design Specification*, July 2007, JEDEC Solid State Technology Association. For clarity of the signal connections in the illustration, the same SDRAM is drawn as two separate SDRAMs.

As mentioned in "Dynamic ODT" on page 6, DDR3 SDRAM supports calibrated ODT with different ODT value settings. If dynamic ODT is not enabled, there are three possible ODT settings available for `RTT_NORM`: 40 Ω, 60 Ω, and 120 Ω. When dynamic ODT is enabled, the number of possible ODT settings available for `RTT_NORM` increases from three to five with the addition of 20 Ω and 30 Ω. Table 1 shows that the recommended ODT setting on the DDR3 SDRAM is 120 Ω. Trace impedance on the DIMM is 60 Ω, and over-terminating the DDR3 SDRAM components on the DIMM with 120 Ω compensates for trace impedance variation on the DIMM due to manufacturing.

Figure 6 shows the write-eye diagram at the DQ0 of a DDR3 SDRAM DIMM using the 120-Ω ODT setting, driven by a Stratix III or Stratix IV FPGA using a calibrated series 50-Ω OCT setting.

Figure 6. ***Simulated Write-Eye Diagram of a DDR3 SDRAM DIMM Using a 120-Ω ODT Setting***



When over-terminating the receiver, the mismatch between load impedance and trace impedance causes ringing at the receiver (Figure 6). When the DDR3 SDRAM ODT setting is set to 60 Ω, there is less ringing at the receiver (Figure 7).

Figure 7. ***Simulated Write-Eye Diagram of a DDR3 SDRAM DIMM Using a 60-Ω ODT Setting***

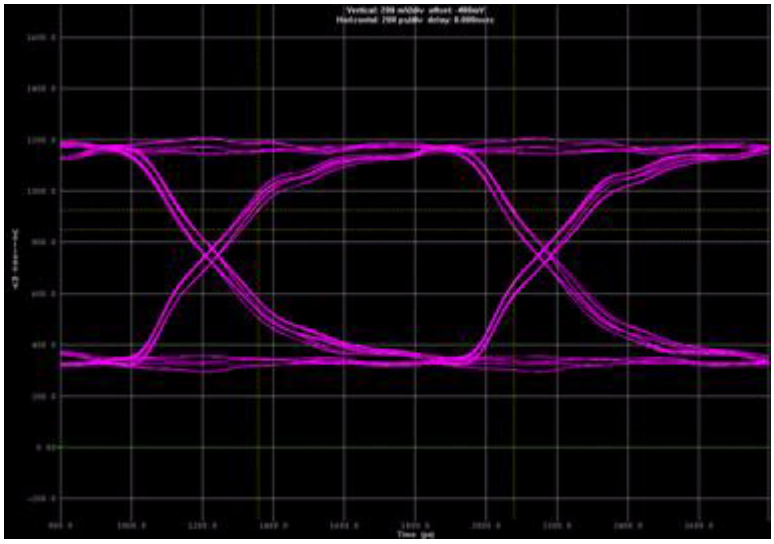


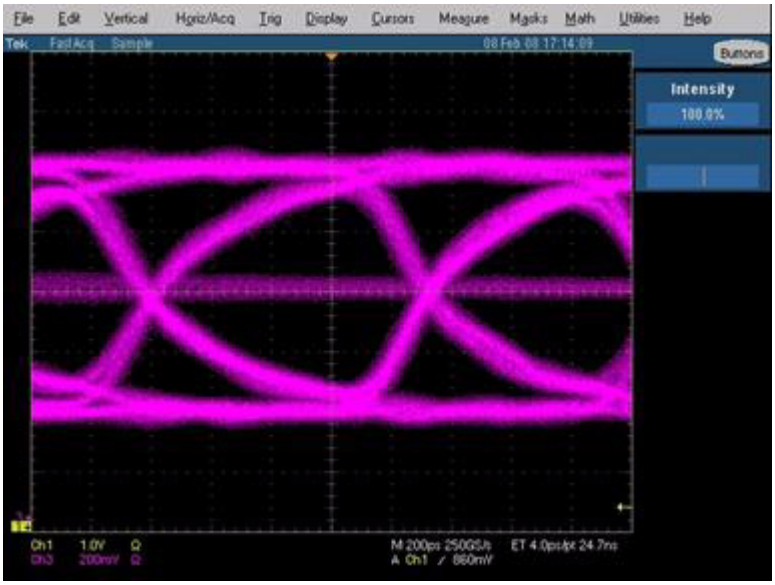
Table 3 compares the effects of the ODT setting on the eye diagram at the DDR3 SDRAM (receiver) when the Stratix III or Stratix IV FPGA is writing to memory.

Table 3. Write-Eye Diagram Using Different ODT Setting

ODT	Eye Height (V)	Eye Width (ps)	Overshoot (V)	Undershoot (V)
120-Ω ODT	0.84	713	—	—
60-Ω ODT	0.73	715	—	—

Although both 120-Ω and 60-Ω ODT settings result in excellent signal quality and acceptable eye opening, using 120 Ω results in a larger eye height because of over-termination, yet it has a minimal effect on eye width. Because the use of 60-Ω ODT results in less ringing, the 60-Ω ODT setting is used on the remaining DDR3 SDRAM DIMM testing featured in this document. Figure 8 shows the measured write-eye diagram using Altera's Stratix III and Stratix IV memory board.

Figure 8. ***Measured Write-Eye Diagram of a DDR3 SDRAM DIMM Using the 60-Ω ODT Setting***

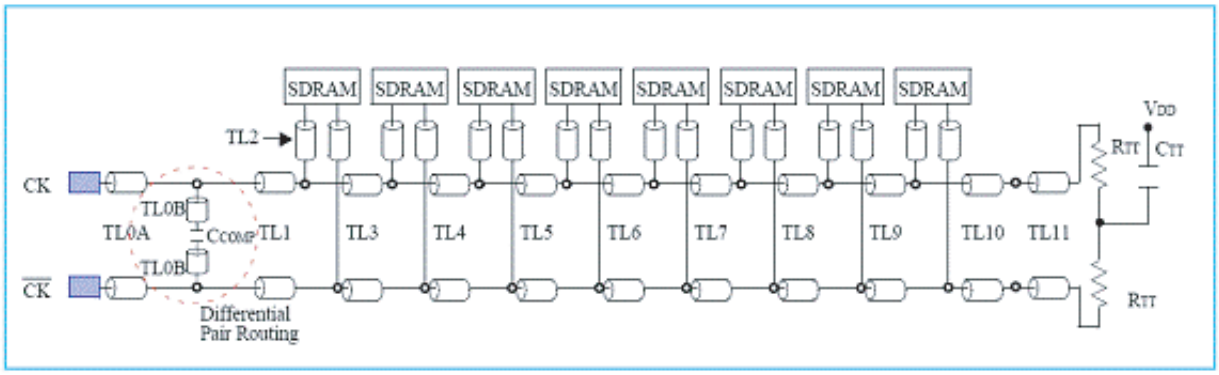


The measured eye diagram correlates well with the simulation. The faint line in the middle of the eye diagram is the effect of the refresh operation during a regular operation. Because these simulations and measurements are based on a narrow set of constraints, you must perform your own board-level simulation to ensure that the chosen ODT setting is right for your setup.

Memory Clocks for DDR3 SDRAM Unbuffered DIMM

For the DDR3 SDRAM unbuffered DIMM, memory clocks are already terminated on the DIMM, so you do not need to place any termination on your board. Figure 9 shows the net structure for the memory clocks and the location of the termination resistors, R_{TT}. The value of R_{TT} is 36 Ω, which results in an equivalent differential termination value of 72 Ω. On the DDR3 SDRAM DIMM, there is also a compensation capacitor, C_{COMP} of 2.2 pF, placed between the differential memory clocks to improve signal quality.

Figure 9. Clock Net Structure for a 64-Bit DDR3 SDRAM Unbuffered DIMM *(Note 1)*



Note to Figure 9:

(1) Source: *PC3-6400/PC3-8500/PC3-10600/PC3-12800 DDR3 SDRAM Unbuffered DIMM Design Specification*, July 2007, JEDEC Solid State Technology Association.

From Figure 9, you can see that the DDR3 SDRAM clocks are routed in a fly-by topology, as mentioned in "Read and Write Leveling" on page 3, resulting in the need for write-and-read leveling. Figure 10 shows the HyperLynx simulation of the differential clock seen at the first and last DDR3 SDRAM component on the unbuffered DIMM using the 50-Ω OCT setting on the output driver of the Stratix III and Stratix IV FPGA.

Figure 10. Differential Memory Clock of a DDR3 SDRAM DIMM at the First and Last Component on the DIMM

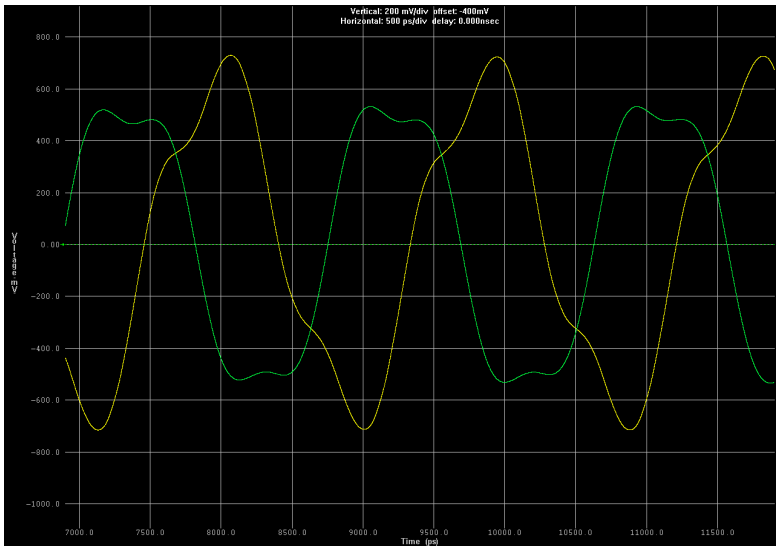
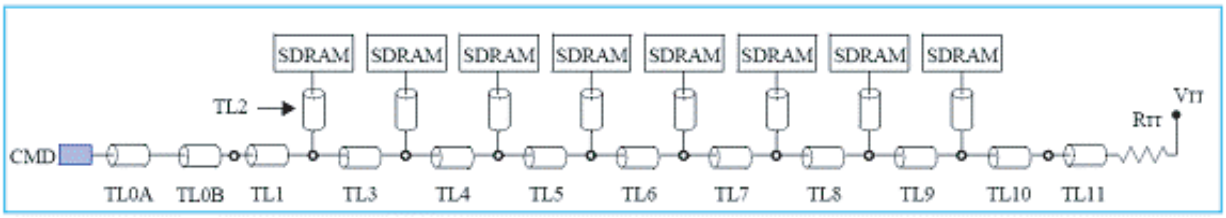


Figure 10 shows that the memory clock seen at the first DDR3 SDRAM component (the yellow signal) leads the memory clock seen at the last DDR3 SDRAM component (the green signal) by 1.3 ns, which is about 0.69 t_{CK} for a 533 MHz operation.

Commands and Addresses for DDR3 SDRAM Unbuffered DIMM

Similar to memory clock signals, the command and address signals are also terminated on the DIMM, so you do not need to place any termination on your board. Figure 11 shows the net structure for the command and address signals and the location of the termination resistor, R_{TT}, which has an R_{TT} value of 39 Ω.

Figure 11. Command and Address Net Structure for a 64-Bit DDR3 SDRAM Unbuffered DIMM *(Note 1)*



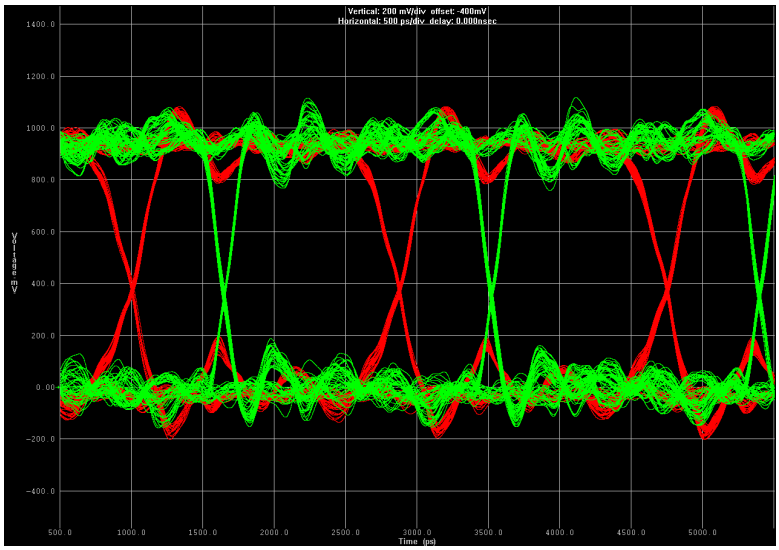
Note to Figure 11:

(1) Source: *PC3-6400/PC3-8500/PC3-10600/PC3-12800 DDR3 SDRAM Unbuffered DIMM Design Specification*, July 2007, JEDEC Solid State Technology Association.

In Figure 11, you can see that the DDR3 SDRAM command and address signals are routed in a fly-by topology, as mentioned in "Read and Write Leveling" on page 3, resulting in the need for write-and-read leveling.

Figure 12 shows the HyperLynx simulation of the command and address signal seen at the first and last DDR3 SDRAM component on the unbuffered DIMM, using a 25-Ω OCT setting on the output driver of the Stratix III and Stratix IV FPGA.

Figure 12. Command and Address Eye Diagram of a DDR3 SDRAM DIMM at the First and Last DDR3 SDRAM Component at 533 MHz *(Note 1)*



Note to Figure 12:

(1) The command/address simulation is performed using a bit period of 1.875 ns.

Figure 12 shows that the command and address signal seen at the first DDR3 SDRAM component (the green signal) leads the command and address signals seen at the last DDR3 SDRAM component (the red signal) by 1.2 ns, which is 0.64 t_{CK} for a 533-MHz operation.

Stratix III and Stratix IV FPGAs

The following sections review termination used on the single-ranked single DDR3 SDRAM DIMM interface side and investigate the use of different termination features available in Stratix III and Stratix IV FPGA devices to achieve optimum signal integrity for your DDR3 SDRAM interface.

DQS, DQ, and DM for Stratix III and Stratix IV FPGA

As mentioned in "Dynamic OCT in Stratix III and Stratix IV Devices" on page 7, Stratix III and Stratix IV FPGAs support the dynamic OCT feature, which switches from series termination to parallel termination depending on the mode of the I/O buffer. Because DQS and DQ are bi-directional signals, DQS and DQ can be both transmitters and receivers. "DQS, DQ, and DM for DDR3 SDRAM Unbuffered DIMM" on page 10 describes the signal quality of DQ, DQS, and DM when the Stratix III or Stratix IV FPGA device is the transmitter with the I/O buffer set to a 50-Ω series termination. This section details the condition when the Stratix III or Stratix IV device is the receiver, the Stratix III and Stratix IV I/O buffer is set to a 50-Ω parallel termination, and the memory is the transmitter. DM is a unidirectional signal, so the DDR3 SDRAM component is always the receiver. Refer to "DQS, DQ, and DM for DDR3 SDRAM Unbuffered DIMM" on page 10 for receiver termination recommendations and transmitter output drive strength settings.

Figure 13 illustrates the DDR3 SDRAM interface when the Stratix III and Stratix IV FPGA device is reading from the DDR3 SDRAM using a 50-Ω parallel OCT termination on the Stratix III and Stratix IV FPGA device, and the DDR3 SDRAM driver output impedance is set to 34 Ω.

Figure 13. DDR3 SDRAM Component Driving the Stratix III and Stratix IV FPGA Device with Parallel 50-Ω OCT Turned On

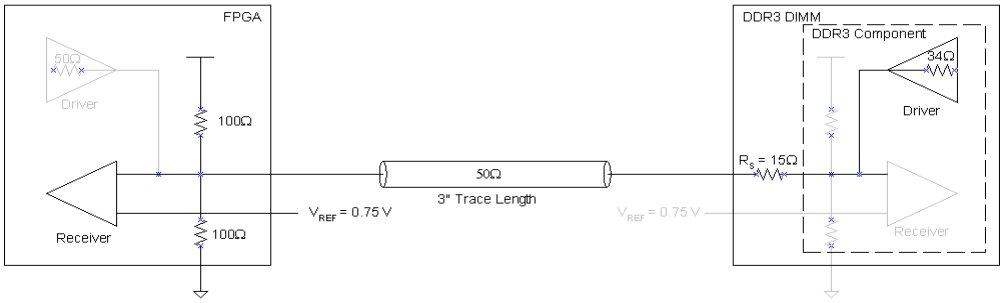
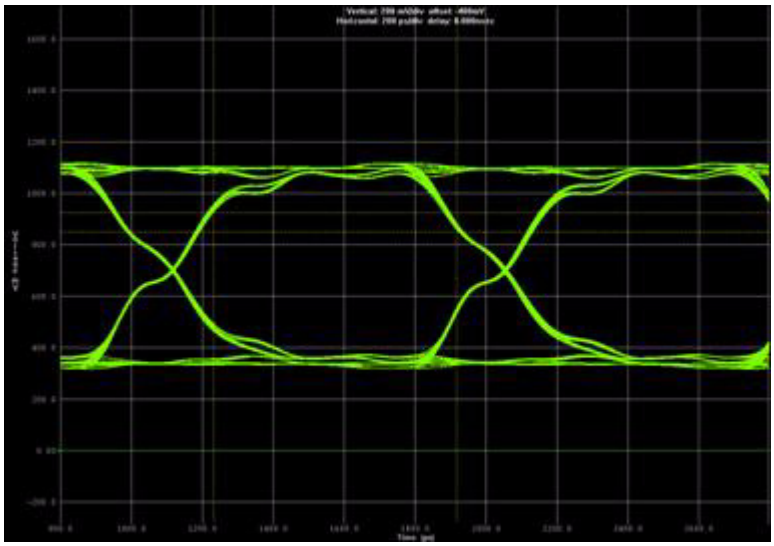


Figure 14 shows the simulation of a read from the DDR3 SDRAM DIMM with a 50-Ω parallel OCT setting on the Stratix III and Stratix IV FPGA device.

Figure 14. Read-Eye Diagram of a DDR3 SDRAM DIMM at the Stratix III and Stratix IV FPGA Using a Parallel 50-Ω OCT Setting



Use of the Stratix III and Stratix IV parallel 50-Ω OCT feature matches receiver impedance with the transmission line characteristic impedance. This eliminates any reflection that causes ringing, and results in a clean eye diagram at the Stratix III and Stratix IV FPGA.

Memory Clocks for Stratix III and Stratix IV FPGA

Memory clocks are unidirectional signals. Refer to "Memory Clocks for DDR3 SDRAM Unbuffered DIMM" on page 12 for receiver termination recommendations and transmitter output drive strength settings.

Commands and Addresses for Stratix III and Stratix IV FPGA

Commands and addresses are unidirectional signals. Refer to "Commands and Addresses for DDR3 SDRAM Unbuffered DIMM" on page 14 for receiver termination recommendations and transmitter output drive strength settings.

Summary

This section discusses terminations used for implementing the DDR3 SDRAM interface using the single-ranked, single unbuffered DIMM. Terminations for unidirectional signals, such as memory clocks and addresses and commands, are placed on the DIMM, thus eliminating the need to place terminations on the board. In addition, using the ODT feature on the DDR3 SDRAM and the Dynamic OCT feature of Stratix III and Stratix IV FPGA devices completely eliminates any external termination resistors, thus simplifying the layout for the DDR3 SDRAM interface when compared to that of the DDR2 SDRAM interface.

Termination for DDR3 SDRAM Components (With Leveling)

In addition to using DDR3 SDRAM DIMM to implement your DDR3 SDRAM interface, you can also use DDR3 SDRAM components. However, for applications that have limited board real estate, using DDR3 SDRAM components reduces the need for a DIMM connector and places components closer, resulting in denser layouts.

DDR3 SDRAM Components

The DDR3 SDRAM unbuffered DIMM is laid out to the JEDEC specification. The JEDEC specification is available from either the JEDEC Organization website (www.JEDEC.org) or from the memory vendors. However, when you are designing the DDR3 SDRAM interface using discrete SDRAM components, you may desire a layout scheme that is different than the DIMM specification. You have the following two options:

- Mimic the standard DDR3 SDRAM DIMM, using a fly-by topology for the memory clocks, address, and command signals. This options needs read and write leveling, so you must use the ALTMEMPHY megafunction with leveling.

  For more information on this fly-by configuration, continue reading this chapter.

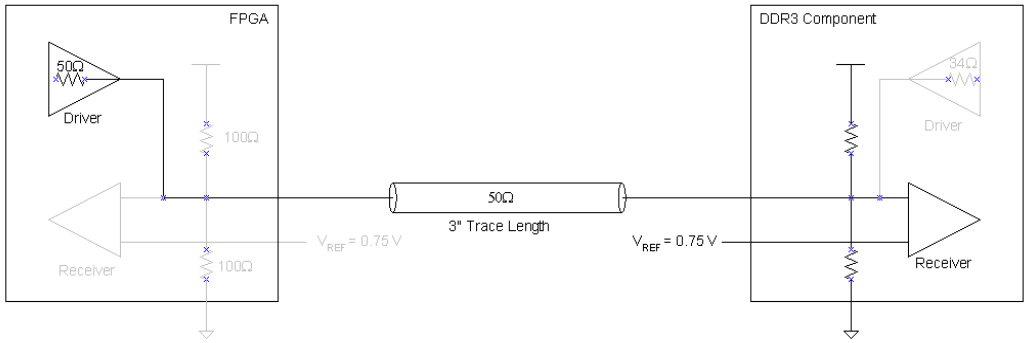
- Mimic a standard DDR2 SDRAM DIMM, using a balanced (symmetrical) tree-type topology for the memory clocks, address, and command signal. Using this topology results in unwanted stubs on the command, address, and clock, which degrades signal integrity and limits the performance of the DDR3 SDRAM interface.

  For more information on using this non-standard symmetrical configuration, refer to "Termination for DDR3 SDRAM Components (Without Leveling)" on page 27.

DQS, DQ, and DM for DDR3 SDRAM Components

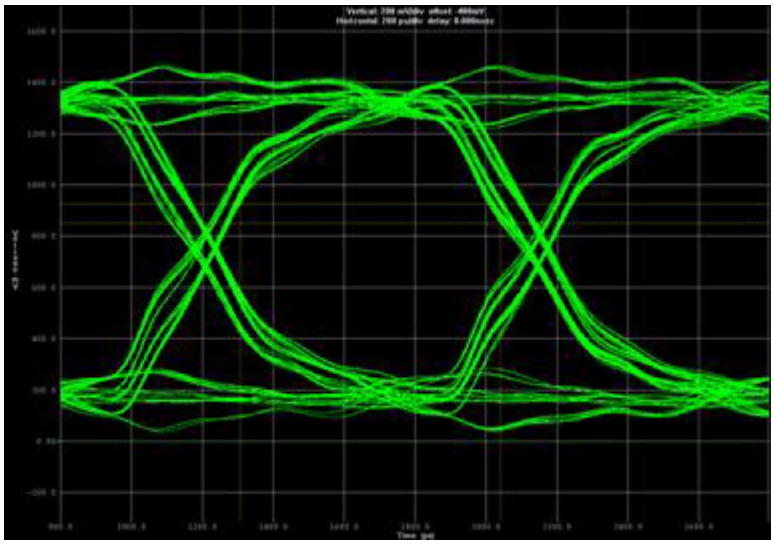
When you are laying out the DDR3 SDRAM interface using Stratix III or Stratix IV devices, you do not need to include the 15-Ω stub series resistor that is on every DQS, DQ, and DM signal, because DQS, DQ, and DM are point-to-point connections. Therefore, the recommended DQS, DQ, and DM topology appears (Figure 15) when the Stratix III or Stratix IV FPGA is writing to the DDR3 SDRAM.

Figure 15. Stratix III and Stratix IV FPGA Writing to a DDR3 SDRAM Components



When you are using DDR3 SDRAM components, there are no DIMM connectors. This minimizes any impedance discontinuity, resulting in better signal integrity. Figure 16 shows the simulated write-eye diagram at the DQ0 of a DDR3 SDRAM component using the 120-Ω ODT setting, and driven by a Stratix III or Stratix IV FPGA using a calibrated series 50-Ω OCT setting.

Figure 16. Write-Eye Diagram of a DDR3 SDRAM Component Using a 120-Ω ODT Setting



Similarly, Figure 17 shows the simulated write-eye diagram at the DQ0 of a DDR3 SDRAM component using the 60-Ω ODT setting, and driven by a Stratix III or Stratix IV FPGA using a calibrated series 50-Ω OCT setting.

Figure 17. Write-Eye Diagram of a DDR3 SDRAM Component Using a 60-Ω ODT Setting

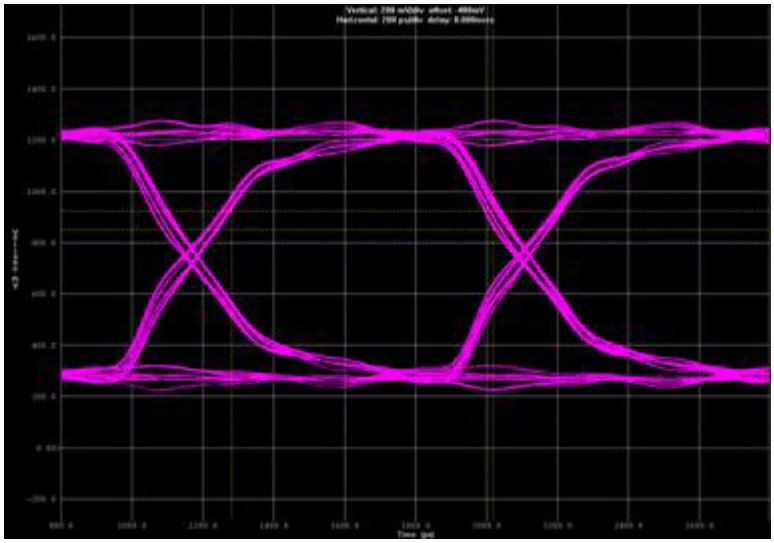


Table 4 compares the effects of the series stub resistor on the eye diagram at the DDR3 SDRAM (receiver) when the Stratix III or Stratix IV FPGA is writing to memory.

Table 4. Simulated Write-Eye Diagram with and without R_S and Using Different ODT Settings

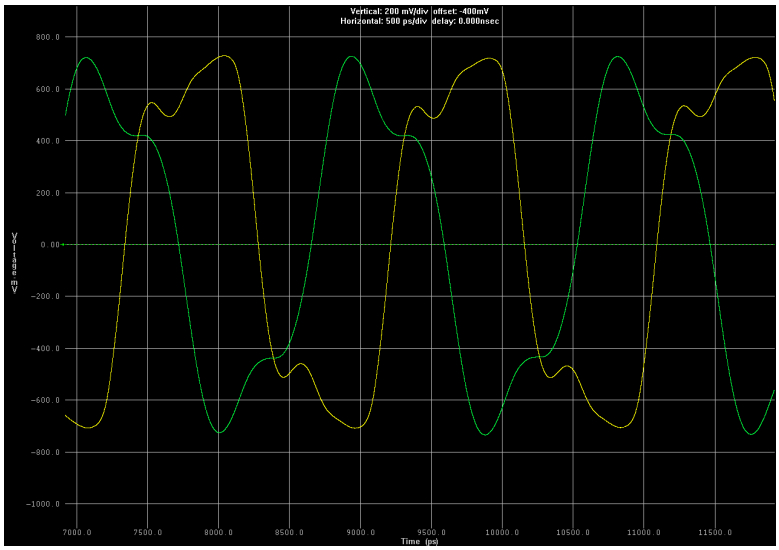
ODT	Eye Height (V)	Eye Width (ps)	Overshoot (V)	Undershoot (V)
120-Ω ODT with R_S	0.84	713	—	—
60-Ω ODT with R_S	0.73	715	—	—
120-Ω ODT without R_S	0.95	734	—	—
60-Ω ODT without R_S	0.83	737	—	—

Without the 15-Ω stub series resistor to dampen the signal arriving at the receiver of the DDR3 SDRAM component, the signal at the receiver of that component is larger than the signal at the receiver of a DIMM (Figure 6 and Figure 7).

Memory Clocks for DDR3 SDRAM Components

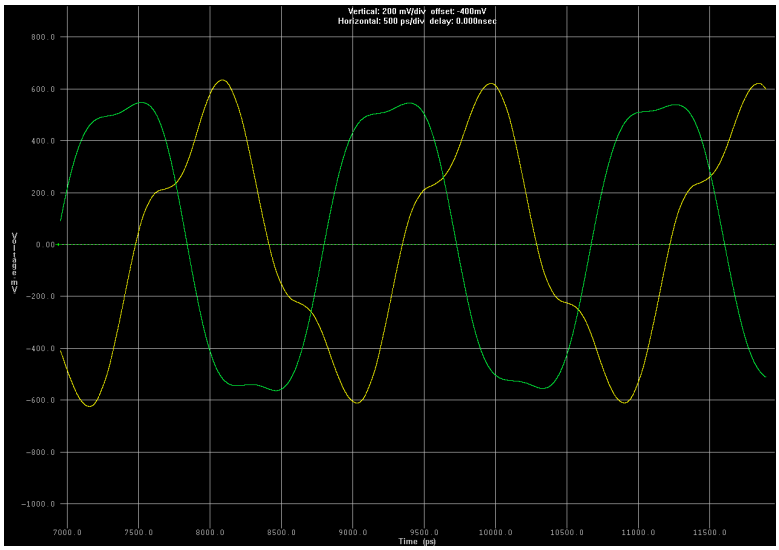
When you use DDR3 SDRAM components, you must account for the compensation capacitor and differential termination resistor between the differential memory clocks of the DIMM. Figure 18 shows the HyperLynx simulation of the differential clock seen at the first and last DDR3 SDRAM component using a flyby topology on a board, without the 2.2 pF compensation capacitor using the 50-Ω OCT setting on the output driver of the Stratix III and Stratix IV FPGA.

Figure 18. Differential Memory Clock of a DDR3 SDRAM Component without the Compensation Capacitor at the First and Last Component Using a Fly-by Topology on a Board



Without the compensation capacitor, the memory clocks (the yellow signal) at the first component have significant ringing, whereas, with the compensation capacitor the ringing is dampened. Similarly, the differential termination resistor needs to be included in the design. Depending on your board stackup and layout requirements, you choose your differential termination resistor value. Figure 19 shows the HyperLynx simulation of the differential clock seen at the first and last DDR3 SDRAM component using a flyby topology on a board, and terminated with 100 Ω instead of the 72 Ω used in the DIMM.

Figure 19. Differential Memory Clock of a DDR3 SDRAM DIMM Terminated with 100 Ω at the First and Last Component Using a Flyby Topology on a Board



Terminating with 100 Ω instead of 72 Ω results in a slight reduction in peak-to-peak amplitude. To simplify your design, use the terminations outlined in the JEDEC specification for unbuffered DDR3 SDRAM DIMM as your guide and perform simulation to ensure that the unbuffered DDR3 SDRAM DIMM terminations provide you with optimum signal quality.

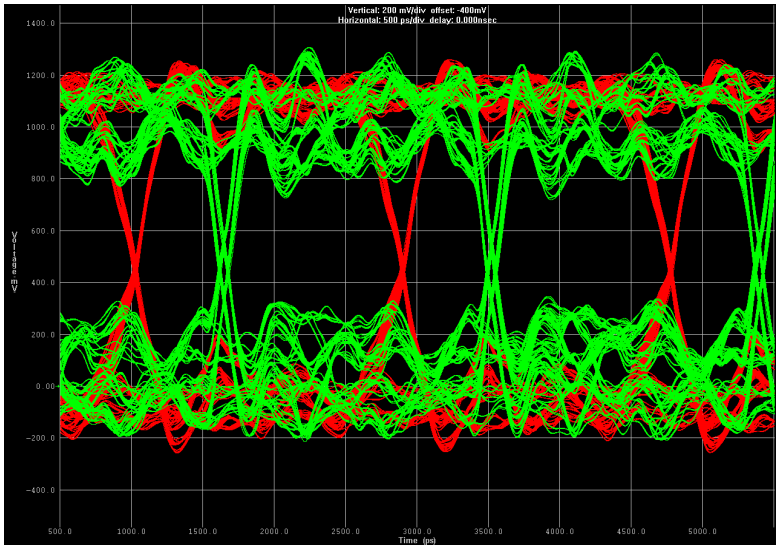
In addition to choosing the value of the differential termination, you must consider the trace length of the memory clocks. There is no specification on the flight-time skew between the first and last component when designing with DDR3 SDRAM components on your board. Altera's DDR3 ALTMEMPHY megafunction currently supports a flight-time skew of no more than 1 t_{CK}. If you use Altera's DDR3 ALTMEMPHY megafunction to create your DDR3 SDRAM interface, ensure that the flight-time skew of your memory clocks is not more than 1 t_{CK}.

☞ Refer to "Layout Considerations (with Leveling)" on page 24 for more information about layout guidelines for DDR3 SDRAM components.

Commands and Addresses for DDR3 SDRAM Components

As with memory clock signals, you must account for the termination resistor on the command and address signals when you use DDR3 SDRAM components. Choose your termination resistor value depending on your board stackup and layout requirements. Figure 20 shows the HyperLynx simulation of the command and address seen at the first and last DDR3 SDRAM component using a flyby topology on a board terminated with 60 Ω instead of the 39 Ω used in the DIMM.

Figure 20. Command and Address Eye Diagram of a DDR3 SDRAM Component Using Flyby Topology on a Board at the First and Last DDR3 SDRAM Component at 533 MHz, Terminated with 60 Ω



Terminating with 60 Ω instead of 39 Ω results in eye closure in the signal at the first component (the green signal), while there is no effect on the signal at the last component (the red signal). To simplify your design with discrete DDR3 SDRAM components, use the terminations outlined in the JEDEC specification for unbuffered DDR3 SDRAM DIMM as your guide, and perform simulation to ensure that the unbuffered DDR3 SDRAM DIMM terminations provide you with the optimum signal quality.

As with memory clocks, you must consider the trace length of the command and address signals so that they match the flight-time skew of the memory clocks.

Stratix III and Stratix IV FPGAs

The following sections describe termination used on the DDR3 SDRAM component interface side and investigate using the different termination features available in Stratix III and Stratix IV FPGA devices, so you can achieve optimum signal integrity for your DDR3 SDRAM interface.

DQS, DQ, and DM Termination for Stratix III and Stratix IV FPGA

Similar to the scenario highlighted in "DQS, DQ, and DM for Stratix III and Stratix IV FPGA" on page 15, the Stratix III and Stratix IV FPGA device is the receiver, the Stratix III and Stratix IV I/O buffer is set to a 50-Ω parallel termination, and the memory is the transmitter. The difference between the setup in "DQS, DQ, and DM for Stratix III and Stratix IV FPGA" on page 15 and the setup in this section is that there is no series stub resistor on the DQS, DQ, and DM signals. DM is a unidirectional signal, so the DDR3 SDRAM component is always the receiver. Refer to "DQS, DQ, and DM for DDR3 SDRAM Components" on page 17 for receiver termination recommendations and transmitter output drive strength settings.

Figure 21 illustrates the DDR3 SDRAM interface when the Stratix III and Stratix IV FPGA device is reading from the DDR3 SDRAM using a 50-Ω parallel OCT termination on the Stratix III and Stratix IV FPGA device and the DDR3 SDRAM driver output impedance is set to 34 Ω without the series stub resistor of 15 Ω.

Figure 21. DDR3 SDRAM Component Driving the Stratix III and Stratix IV FPGA Device with Parallel 50-W OCT Turned On

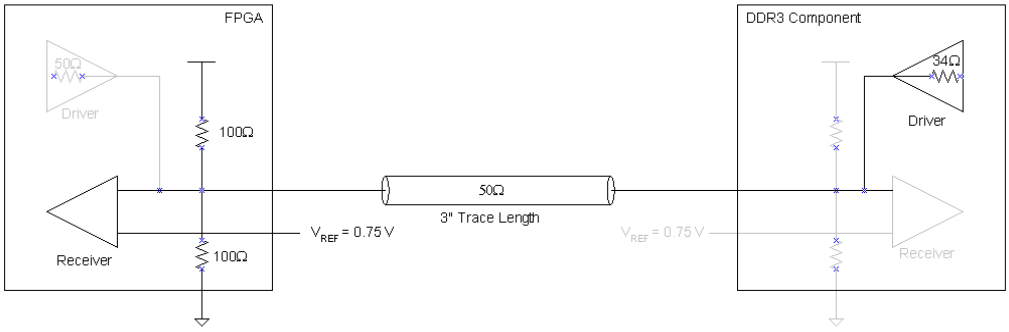


Figure 22 shows a simulation of a read from the DDR3 SDRAM DIMM with a 50-Ω parallel OCT setting on the Stratix III or Stratix IV FPGA device.

Figure 22. Read-Eye Diagram of a DDR3 SDRAM Component at the Stratix III and Stratix IV FPGA Using a Parallel 50-W OCT Setting

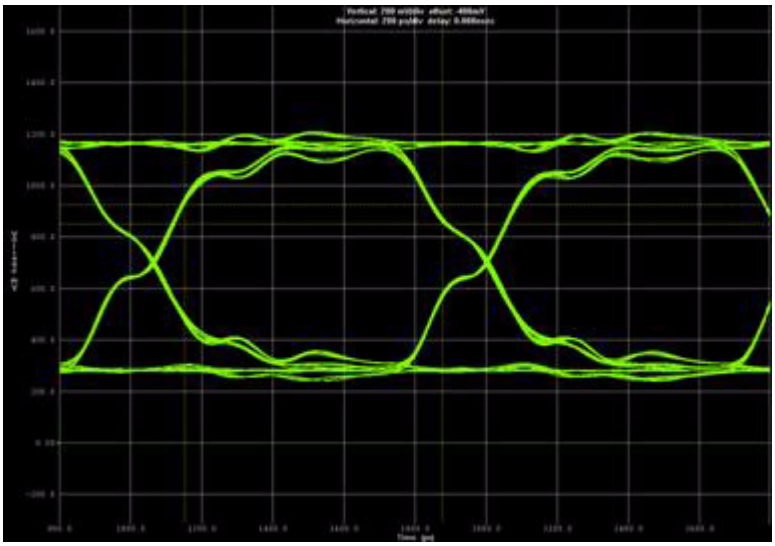


Table 5 compares the effects of the series stub resistor on the eye diagram at the Stratix III and Stratix IV FPGA (receiver) when the Stratix III or Stratix IV FPGA is reading from the memory.

Table 5. Read-Eye Diagram with and without RS Using 50-Ω Parallel OCT

ODT	Eye Height (V)	Eye Width (ps)	Overshoot (V)	Undershoot (V)
With R_S	0.70	685	—	—
Without R_S	0.73	724	—	—

Without the 15-Ω stub series resistor to dampen the signal, the signal at the receiver of the Stratix III and Stratix IV FPGA driven by the DDR3 SDRAM component is larger than the signal at the receiver of the Stratix III and Stratix IV FPGA driven by DDR3 SDRAM DIMM (Figure 13), and similar to the write-eye diagram in "DQS, DQ, and DM for DDR3 SDRAM Components" on page 17.

Memory Clocks Termination for Stratix III and Stratix IV FPGA

Memory clocks are unidirectional signals. Refer to "Memory Clocks for DDR3 SDRAM Components" on page 19 for receiver termination recommendations and transmitter output drive strength settings.

Command and Address Termination for Stratix III and Stratix IV FPGA

Commands and addresses are unidirectional signals. Refer to "Commands and Addresses for DDR3 SDRAM Components" on page 21 for receiver termination recommendations and transmitter output drive strength setting.

Summary

This section discusses terminations used to achieve optimum performance for designing the DDR3 SDRAM interface using discrete DDR3 SDRAM components. Though you must include termination for unidirectional signals, the overall layout for the DDR3 SDRAM interface using discrete DDR3 SDRAM components is easier compared to DDR2 SDRAM interfaces using discrete DDR2 SDRAM components, because of the fly-by daisy chain topology. To simplify your design processes, use the DDR3 SDRAM unbuffered DIMM specification provided by JEDEC as your guideline, because the trace length and termination values used in the DIMM configuration provide excellent signal quality.

Layout Considerations (with Leveling)

This section discusses general layout guidelines for designing your DDR3 SDRAM interface. These layout guidelines help you plan your board layout, but are not meant as strict rules that must be adhered to. Altera recommends that you perform your own board-level simulations to ensure that the layout you choose for your board allows you to achieve your desired performance.

Trace Impedance

The layout of single-ended signal traces are to be 50 Ω and the differential signal traces are to be 100 Ω with a ± 10% tolerance. Remove unused via pads as these cause unwanted capacitance.

Decoupling

To minimize inductance, use 0.1 µF in 0402 size or smaller capacitors. Keep V_{TT} voltage decoupling close to the DDR3 SDRAM components and pull-up resistors. Connect decoupling capacitors between V_{TT} and ground using a 0.1 µF capacitor for every other V_{TT} pin. For V_{DD} and V_{DDQ}, use 0.1 µF and 0.01 µF capacitors for every V_{DD} and V_{DDQ} pin.

Power

Route the ground, 1.5 V, and 0.75 V as planes. Route V_{CCIO} for memories in a single-split plane with at least a 20-mil (0.508 mm) gap of separation. Route V_{TT} as islands or 250-mil (6.35 mm) power traces. Route oscillators and PLL power as islands or 100-mil (2.54 mm) power traces.

General Routing Guidelines

Route using 45° angles and *not* 90° corners. Do not route critical signals across split planes. Route over appropriate V_{CC} and ground planes. Avoid routing memory signals closer than 25-mil (0.635 mm) to the memory clocks. Keep the signal routing layers close to ground and power planes.

Clock Routing Guidelines

Route clocks on inner layers with outer-layer run lengths held to under 500 mils (12.7 mm).

- 10-mil spacing for parallel runs < 0.5 inches (2× trace-to-plane distance)

- 15-mil spacing for parallel runs between 0.5 and 1.0 inches (3× trace-to-plane distance)
- 20-mil spacing for parallel runs between 1 and 6 inches (4× trace-to-plane distance)

Clocks must maintain length matching between clock pairs of ± 25 mils (0.635 mm). Differential clocks need to maintain length matching between positive and negative signals of ± 10 mils (0.254 mm), routed in parallel. The space between differential pairs must be at least 2× the trace width of the differential pair to minimize loss and maximize interconnect density. The maximum length from the first SDRAM to the last SDRAM must be no more than 6 inches (approximately 153 mm), which is the same maximum length for clocks specified by JEDEC for unbuffered DIMM. This maximum clock-length specification is only valid for unbuffered DIMM. For other DIMM configurations, check the necessary JEDEC specifications, as the maximum clock length may be different. For example, JEDEC specifies the maximum clock length for SODIMM to be 6.5 inches (approximately 166 mm).

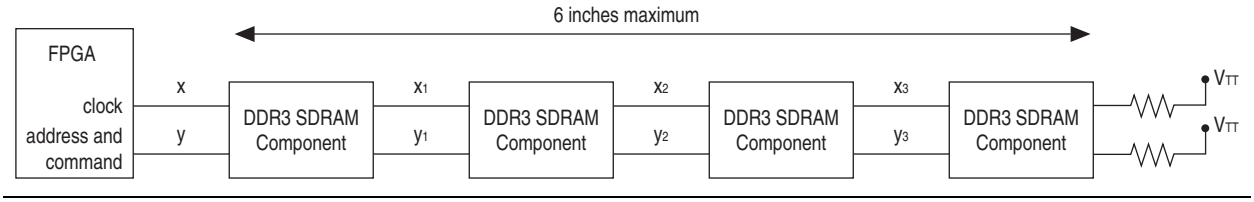
For example, differential clocks must be routed differentially (5 mil trace width, 10-15 mil space on centers, and equal in length to signals in the Address/Command Group). Take care with the via pattern used for clock traces. To avoid transmission-line-to-via mismatches, Altera recommends that your clock via pattern be a Ground-Signal-Signal-Ground (GSSG) topology (via topology: GND | CLKP | CLKN | GND).

Address and Command Routing Guidelines

Similar to the clock signals in DDR3 SDRAM, address and command signals are routed in a daisy chain topology from the first SDRAM to the last SDRAM. The maximum length from the first DRAM to the last SDRAM must be no more than 6 inches (approximately 153 mm), which is the same maximum length for clocks specified by JEDEC for unbuffered DIMMs. Ensure that each net maintains the same consecutive order. Unbuffered DIMMs are more susceptible to crosstalk and are generally noisier than buffered DIMMs. Route the address and command signals of unbuffered DIMMs on a different layer than DQ and DM, and with greater spacing. Do not route differential clock and clock enable signals close to address signals. Route all addresses and commands to match the clock signals to within ± 125 mil (± 3.175 mm) to each discrete memory component. Figure 23 shows the DDR3 SDRAM routing guidelines, where:

- $x = y \pm 125$ mil
- $x + x_1 = y + y_1 \pm 125$ mil
- $x + x_1 + x_2 = y + y_1 + y_2 \pm 125$ mil

Figure 23. DDR3 SDRAM Component Routing Guidelines



DQ, DQS, and DM Routing Guidelines

All signals within a given byte-lane group must be matched in length with a maximum deviation of ± 50 mils (± 1.27 mm). Keep the maximum byte-lane group-to-byte group matched length deviation to ± 150 ps or ± 0.8 inches (± 20 mm). To reduce SSN, Altera recommend that the consecutive SDRAM-to-SDRAM byte lane length is not increased in length equal to the respective address, command, or clock delay ± 25 ps (0.125 inch). Otherwise the DQ byte group matches the increase in length on the address and command group, then because of write leveling, all DQ group outputs switch at the same time at the FPGA during writes.

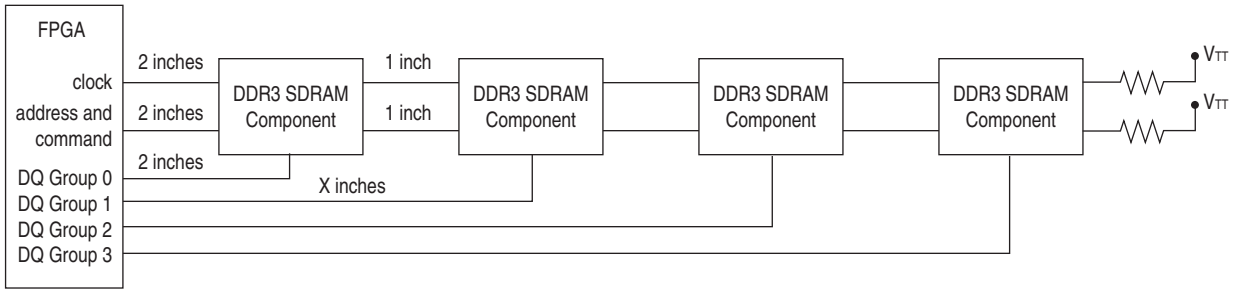
Maintain all other signals to a spacing that is based on its parallelism with other nets:

- 5 mils for parallel runs < 0.5 inches (approximately 1× spacing relative to plane distance)
- 10 mils for parallel runs between 0.5 and 1.0 inches (approximately 2× spacing relative to plane distance)
- 15 mils for parallel runs between 1.0 and 6.0 inches (approximately 3× spacing relative to plane distance)

Figure 24 shows the DDR3 SDRAM components DQ, DQS, and DM guidelines, where:

- X > 2 + 1+ 0.125 inches
- X < 2 + 1 – 0.125 inches
- So, 2.875 inches < X < 3.125 inches

Figure 24. DDR3 SDRAM Components DQ, DQS, DM Routing Guidelines



Termination

The previous sections use the combination of DDR3 SDRAM ODT and Stratix III and Stratix IV Dynamic OCT for DQS, DQS#, DQ, and DM. This practise reduces the need for external termination, and thus reduces both bill-of materials (BOM) cost and PCB size.

When using DIMMs, you have no concerns about terminations on memory clocks, addresses, and commands. If you are using components, use an external parallel termination of 40 Ω to V_{TT} at the end of the fly-by daisy chain topology on the addresses and commands. For memory clocks, use an external parallel termination of 75 Ω differential at the end of the fly-by daisy chain topology on the memory clocks. Using fly-by daisy chain topology helps reduce any stub reflection. Keep the length of the traces to the termination to within 0.5 inch (14 mm). Use resistors with tolerances of 1 to 2%.

Termination for DDR3 SDRAM Components (Without Leveling)

Altera support the use of DDR3 SDRAM components using a PHY without leveling.

To use the PHY without leveling, you should layout the DDR3 SDRAM components on your PCB in a DDR2-like topology. Operating DDR3 SDRAM components without leveling requires tighter layout rules and the use of more complex topologies. This section discusses these termination and layout requirements.

DDR3 SDRAM Components

This chapter describes how to implement the nonstandard DDR2-like balanced (symmetrical) topology for command, address, and clock signals. Using this alternative topology results in unwanted stubs on the address, command, and clock signals, which degrades signal integrity and limits the performance of any DDR3 SDRAM interface.

DQS, DQ, and DM for DDR3 SDRAM Components

The DDR3 SDRAM PHY without leveling uses the same topology and termination settings for the DQS, DQ and DM signals as the DDR3 SDRAM with leveling (refer to "DQS, DQ, and DM for DDR3 SDRAM Components" on page 17). However, while the topology and termination of these signals is identical, the layout rules differ, because of the balanced command, address, and clock signals. DDR3 SDRAM without leveling interfaces require much tighter DQ group to DQ group timing, refer to "Layout Considerations (without Leveling)" on page 31.

Memory Clocks for DDR3 SDRAM Components

Memory clocks in a DDR3 SDRAM interface without leveling should follow the same topology guidelines as a DDR2 SDRAM-type interface. However, SSTL15 type signaling is used instead of SSTL18.

For more information, refer to *AN 408: DDR2 Memory Interface Termination, Drive Strength, Loading, and Design Layout Guidelines*.

If your DDR3 SDRAM interface connects to a single component, you can use a simple point-to-point topology a 100 Ω differential terminator at the component end of the line.

Most interfaces use two, four, or eight DDR3 SDRAM components, so you should use a balanced T-type routing pattern, where all the trace segments are balanced for each path. The total trace length to the first DDR3 SDRAM component is identical to that of the last component, hence the trace delay for each component is the same, ensuring matched timing while helping to control any reflections.

Differentially terminate clocks at the component end of the line with a 100 Ω resistor. For more than one DDR3 SDRAM component, split the clock using a balanced T-topology. Place the 100 Ω termination resistor at the first split in the T (refer to Figure 25), or increase the resistor value and place a resistor at the end of each segment at the DDR3 SDRAM component (refer to Figure 26). Typically two segments require 200 Ω resistors; and four segments require 400 Ω resistors, but Altera recommend that you simulate your specific topology to be ascertain the correct value.

Figure 25. Placement of the Termination Resistor—at First Split

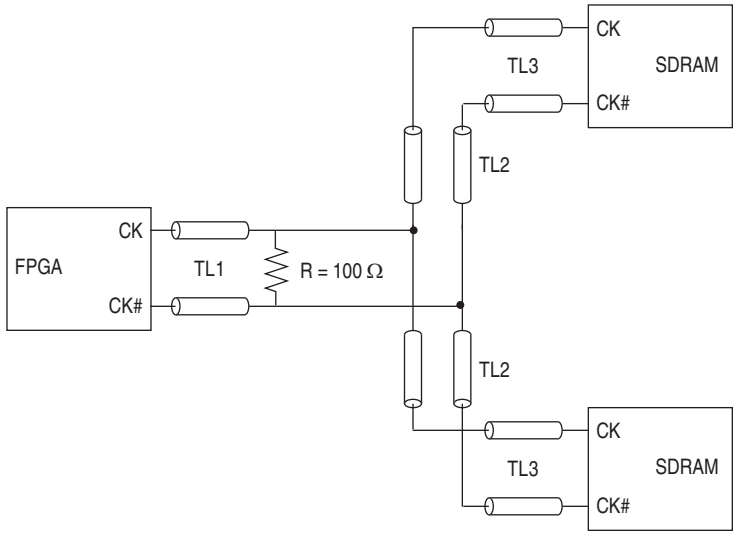
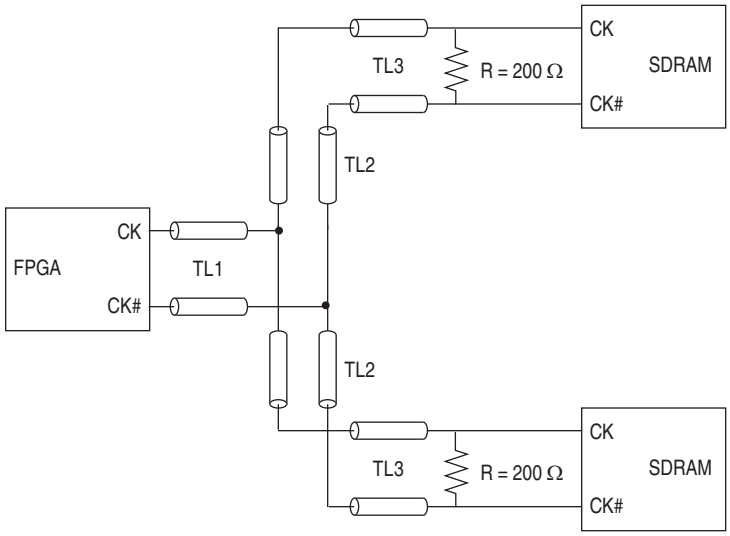


Figure 26. Placement of the Termination Resistor—End of Each Segment



Loading must not excessively degrade the slew rate of the memory clocks, so ideally a single differential clock pair does not drive more than four components. If a single clock pair drives eight or larger numbers of DDR3 SDRAM components, you must perform setup and hold deration, to allow accurate timing analysis. Altera recommend that you simulate any proposed topology before board completion, so you can perform deration and final timing analysis. DDR3 setup and hold deration may result in a lower than stated interface frequency to be achieved in any given device or speed grade combination.

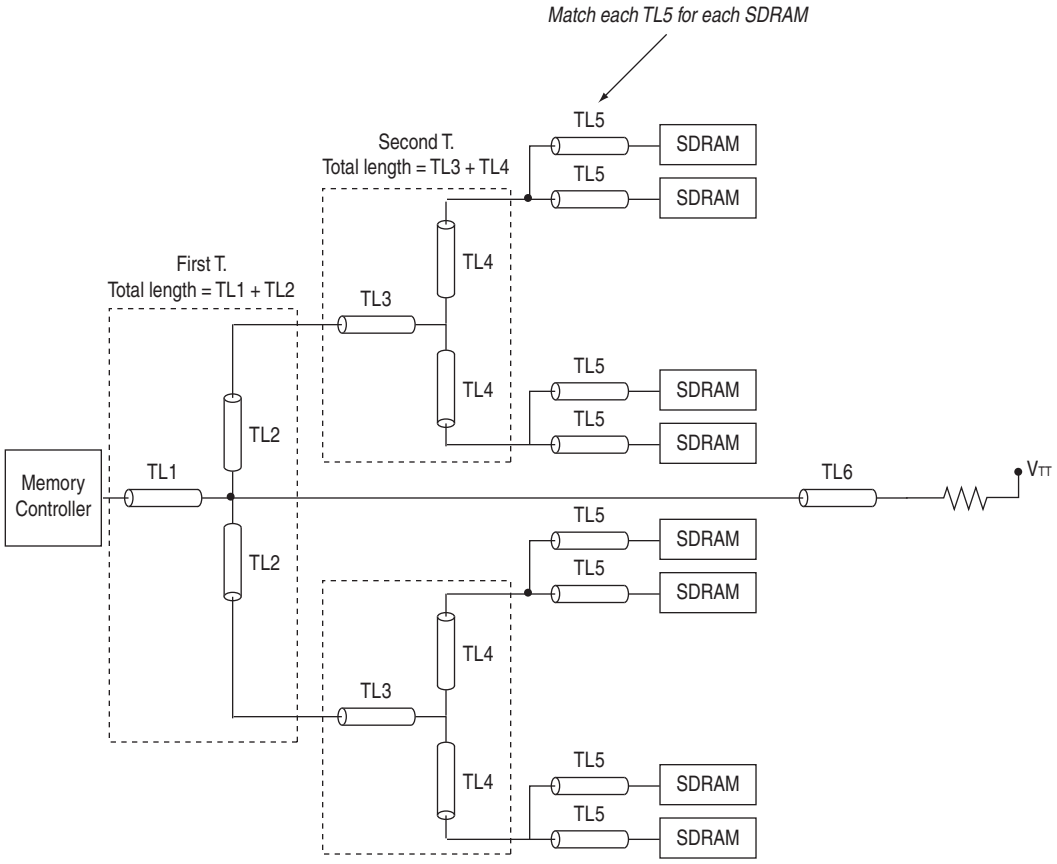
Command and Address for DDR3 SDRAM Components

Command and address signals are similar to memory clocks in topology, so you should use a balanced T-type routing pattern, where all the trace segments are balanced for each path. The loading on the address and command signals is typically larger with eight or sixteen loads not unusual. You should mimic the topologies that Jedec uses on DDR2 unbuffered DIMM raw cards A to C, as these topologies provide the best results.

Avoid topologies that Jedec uses on DDR2 unbuffered DIMM raw cards D, E, and F. Raw card D topologies typically suffer from loading resonances, which reduce timing margin. Additionally, raw cards E and F are not symmetrical balanced trees, as they use a planar solution, which again can reduce timing margin.

Command and address signals should always be terminated with a 50 Ω resistor to V_{TT}. Always place this single 50 Ω resistor at the first split in the T (Figure 27).

Figure 27. Placing the 50-Ω Resistor



Stratix III and Stratix IV FPGAs

The following sections describe the termination used on the DDR3 SDRAM components interface side and the different termination features available in the Stratix III and Stratix IV FPGAs when using a PHY without leveling, so that optimum signal integrity can be achieved for your DDR3 SDRAM interface.

DQS, DQ, and DM Termination for Stratix III Stratix IV FPGAs

It should be understood that the termination and topology for DQS, DQ, and DM signals is identical. The choice of leveling or without leveling DDR3 SDRAM PHY only affects the address, command, and clock termination schemes (refer to "DQS, DQ, and DM for Stratix III and Stratix IV FPGA" on page 15).

Because of the different timing requirements, the layout (trace matching) constraints for DQS, DQ, and DM do differ (refer to "Layout Considerations (without Leveling)" on page 31).

Memory Clocks Termination for Stratix III and Stratix IV FPGA

Memory clocks are unidirectional signals. When using DDR3 SDRAM components without leveling, mimic the termination and topology used for DDR2 SDRAM components, substituting differential SSTL18 class I with differential SSTL15 class I.

For more information, refer to *AN 408: DDR2 Memory Interface Termination, Drive Strength, Loading, and Design Layout Guidelines*.

Command and Address for Termination for Stratix III and Stratix IV FPGAs

Commands and addresses are unidirectional signals. When using DDR3 SDRAM components without leveling, mimic the termination and topology used for DDR2 SDRAM components, substituting SSTL18 class I with SSTL15 class I.

For more information, refer to *AN 408: DDR2 Memory Interface Termination, Drive Strength, Loading, and Design Layout Guidelines*.

Arria II GX FPGA

The following sections describe the termination used on the DDR3 SDRAM components interface side and the different termination features available in the Arria II GX devices when using a PHY without leveling, so that optimum signal integrity can be achieved for your DDR3 SDRAM interface without leveling.

DDR3 SDRAM component interfaces without leveling are routed identically to DDR2 SDRAM interfaces without leveling, hence DDR2 SDRAM interface recommendations apply.

DQS, DQ and DM Termination for Arria II GX FPGAs

The termination and topology and layout of DQS, DQ, and DM signals is identical if DDR2 (differential DQS mode) is compared to DDR3 SDRAM.

DDR3 SDRAM without leveling on Arria II GX devices should be considered identical to any DDR2 SDRAM components interface.

The memory end termination (Table 1 and Table 2) still applies. But you should use the FPGA end termination settings from *AN 408: DDR2 Memory Interface Termination, Drive Strength, Loading, and Design Layout Guidelines*.

As Arria II GX devices don't feature dynamic OCT, 50 Ω parallel discrete termination to V_{TT} should be used at the FPGA end of the line.

For more information, refer to "Layout Considerations (without Leveling)" on page 31.

Memory Clocks Termination for Arria II GX FPGAs

Memory clocks are unidirectional signals. When using DDR3 SDRAM components without leveling, mimic the termination and topology used for DDR2 SDRAM components, substituting Differential SSTL18 Class I with Differential SSTL15 Class I.

For more information about component termination and FPGA drive strength settings, refer to "Memory Clocks for DDR3 SDRAM Components" on page 19 and *AN 408: DDR2 Memory Interface Termination, Drive Strength, Loading, and Design Layout Guidelines*.

Command and Address for Termination for Arria II GX FPGAs

Commands and addresses are unidirectional signals. When using DDR3 SDRAM components without leveling, mimic the termination and topology used for DDR2 SDRAM components, substituting Differential SSTL18 Class I with Differential SSTL15 Class I.

For more information about component termination and FPGA drive strength settings, refer to "Commands and Addresses for DDR3 SDRAM Components" on page 21 and *AN 408: DDR2 Memory Interface Termination, Drive Strength, Loading, and Design Layout Guidelines*.

Summary

This section discusses the I/O standards, drive strength, termination and topologies to use so that you achieve optimum performance when designing with DDR3 SDRAM components without leveling. The topology is more challenging for command, address, and clock signals, but it is no harder than the previous generation DDR2 SDRAM interface, as the same requirements are used.

Layout Considerations (without Leveling)

This section discusses general layout guidelines for designing your DDR3 SDRAM component without leveling interface. These guidelines help you plan your board layout, but are not meant as strict rules that must be adhered to. Altera recommends that you perform your own board-level simulations to ensure that your implemented topology allows you to achieve your desired performance.

For more information, refer to *AN 408: DDR2 Memory Interface Termination, Drive Strength, Loading, and Design Layout Guidelines*.

When mimicking DDR2 unbuffered DIMM JEDEC topologies, Altera recommends that you use only raw cards A to C, as these are balanced symmetrical topologies and result in the optimum performance. Raw cards D to F are not symmetrical and are planar solutions, so should be avoided where possible.

When following DDR2 SDRAM component guidelines, the I/O standard for DDR3 is SSTL15 and not SSTL18. DDR3 SDRAM components have enhanced ODT and output drive strength features that you can use to improve the SI performance of a DDR3 SDRAM component without leveling solution, above that of a standard DDR2 implementation.

Altera's timing analysis assumes single-ranked DDR3 SDRAM designs only. Dual or quad ranked designs require timing deration. For more information on multirank topologies and layout guidelines, refer to *AN 444: Dual DIMM DDR2 SDRAM Interface Design Guidelines*.

Conclusion

By using the new features of DDR3 SDRAM and the Stratix III and Stratix IV FPGAs, you simplify your design process for DDR3 SDRAM. Using the fly-by daisy chain topology increases the complexity of the datapath and controller design to achieve leveling, but also greatly improves performance and eases board layout for DDR3 SDRAM.

DDR3 SDRAM components without leveling can also be used in an design when this may result in a more optimal solution or for use with devices that support the required electrical interface standard, but do not support the required read and write leveling functionality.

By using Altera FPGAs and the DDR3 SDRAM ALTMEMPHY megafunction, you simplify the datapath design and can take advantage of either the higher DDR3 SDRAM performance and straightforward board design in a design with leveling, or the lower power and cost performance advantages of DDR3 SDRAM components in a design without leveling.

References

This application note references the following documents:

- *JEDEC Standard Publication JESD79-3A, DDR3 SDRAM Specification, JEDEC Solid State Technology Association*
- *AN 408: DDR2 Memory Interface Termination, Drive Strength, Loading, and Design Layout Guidelines*
- *AN 436: Design Guidelines for Implementing DDR3 SDRAM Interfaces in Stratix III Devices*
- *AN 444: Dual DIMM DDR2 SDRAM Interface Design Guidelines*
- *External Memory Interfaces in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*
- *Stratix III Device I/O Features* chapter in volume 1 of the *Stratix III Device Handbook*
- *External Memory Interfaces in Stratix IV Devices* chapter in volume 1 of the *Stratix IV Device Handbook*
- *I/O Features in Stratix IV Devices* chapter in volume 1 of the *Stratix IV Device Handbook*
- *Micron Technical Note TN41-04: DDR3 Dynamic On-Die Termination Introduction*
- *Micron Technical Note TN41-08: DDR3-1066 Memory Design Guide for Two-Dimm Unbuffered Systems*
- *TN-41-02 DDR3 ZQ Calibration*, Micron
- *TN-41-04 DDR3 Dynamic On-Die Termination*, Micron

- *TN47-06: Updated JEDEC DDR2 Specifications*, Micron
- *TN47-17: DDR2 SODIMM Optimized Address/Command Nets*, Micron
- *TN47-19: DDR2 (Point-to-Point) Features and Functionality*, Micron
- *TN47-20: Point-to-Point Package Sizes and Layout Basics*, Micron
- *Consumer Electronics are Changing the Face of DRAMs*, Jody Defazio, Chip Design Magazine, June 29, 2007
- *DDR3 ODT and Dynamic ODT*, JEDEC DDR3 2007 Conference, Oct 3-4, San Jose, CA.
- *PC3-6400/PC3-8500/PC3-10600/PC3-12800 DDR3 SDRAM Unbuffered DIMM Design Specification*, July 2007, JEDEC Solid State Technology Association

Document Revision History

Table 6 shows the revision history for this application note.

Table 6. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
May 2009, v1.1	■ Support for DDR3 SDRAM components without leveling.	—
June 2008, v1.0	Initial release.	—

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