AN 18.15

PCB Design Guidelines for QFN and DQFN Packages

1 Introduction

This application note provides information on general printed circuit board layout considerations for the SMSC products using QFN and DQFN packages.

1.1 Audience

This application note is written for a reader that is familiar with PCB design, including signal integrity and thermal management implementation concepts.

1.2 Objective

The goal of this document is to provide implementation information that is specific to designing PCBs using QFN and DQFN packages. SMSC suggests that all implementations be confirmed with the user's PCB fabricator and PCBA assembler.

1.3 Overview

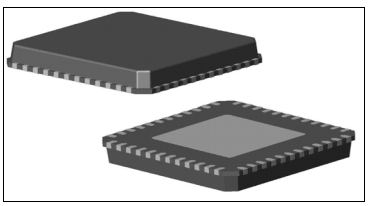
Successful implementation of QFN and DQFN packages requires special consideration for printed circuit board (PCB) layout and solderpaste stencil production. This application note describes the important items to consider.

2 PCB Layout Guidelines

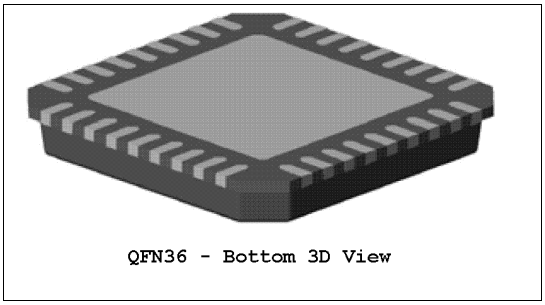
The guidelines presented are applicable to SMSC QFN and DQFN packaged devices and supersede earlier notes.

The following recommendations for optimizing the use of QFN and DQFN packages are suggestions based on SMSC's experience and knowledge and may be accepted or rejected. SMSC does not guarantee any design. Each company is finally responsible for determining the suitability of its own design.

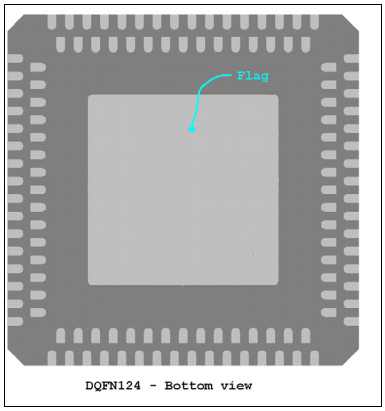
2.1 QFN/DQFN Designs



QFN packages are physically robust, thermally efficient, and occupy much less PCB space than equivalent QFP packages. They generally have superior lead inductance characteristics. They also present some particular design constraints.



QFN36 - Bottom 3D View



DQFN124 - Bottom view

QFN packages generally have a row (QFN) or two (DQFN) of perimeter pads (“pads”) around a larger central pad (“flag” or “Epad”) encapsulated in a plastic body. These packages are surface-mounted to the target system PCB by a solder reflow process. All of the SMSC QFN and DQFN packages are like this.

The perimeter pads are typically used for signal assignment, while the flag use is two-fold; as the primary thermal conduction path to remove package heat, and for device ground.

Many of the SMSC QFN devices use this flag as the primary – or ONLY – connection to ground (VSS), as well as a thermal conduction path.

During soldering the QFN device will float too high if too much solder paste is deposited under the device. This may not allow the perimeter pads to reach the PCB, causing “opens”. Also, the QFN will sink too low if too little solder paste is under the flag. This can cause the pads to “squeeze-out” solder, causing “shorts” between adjacent pads.

To address these issues, constraints are imposed for the use of these packages:

2.1.1 Flag Vias

Use as many vias as can practically fit within the flag. For example, this number should be at least eight vias for 36-pin devices and at least 16 vias for 6x6 mm flags. Use vias with a finished hole size (FHS) of 0.28 mm to 0.5 mm for best results.

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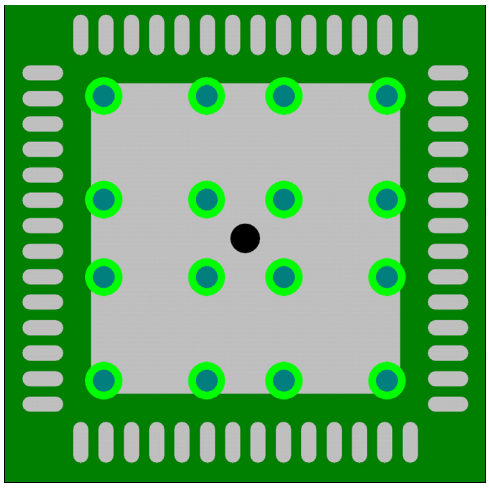

2.1.1.1 Thermal Performance

The more vias placed within the flag, the better thermal conduction to the internal ground planes, if any, and to thermal radiation and conduction floods or features on the opposite side of the PCB.

2.1.1.2 Signal Loop Area

The more vias placed within the flag and near its edges, the shorter the loop area to the internal device circuitry. This will reduce the signal return lengths.

2.1.2 Solder Stencil Considerations

Use a solderpaste stencil pattern for the flag composed of several small solder paste openings in the stencil (paste) data for the flag rather than a single, large opening. These four to nine openings should cover 70% - 80% of the flag dimension area. This will better meter paste deposition and improve the solder-ability of the flag.

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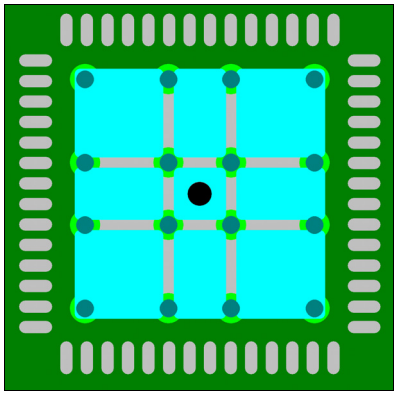

Consider the size, quantity, position, and type (tented, plugged, open, etc.) of vias used within the flag to determine their effect on the amount of solderpaste the may be wicked from the pad by the vias during soldering and make appropriate adjustments to the stencil openings and via positions.

2.1.3 Routing Hazards

2.1.3.1 QFN Packages

Avoid routing between the flag and the pads of a QFN device.

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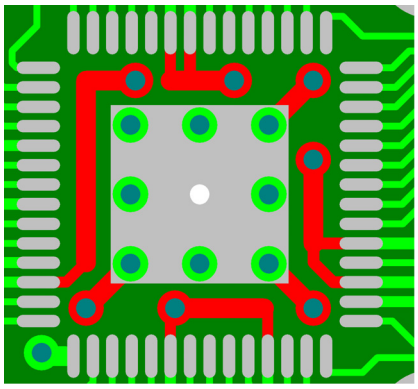

Routing and vias between the flag and the pads can easily be shorted to either the flag or to the pads because of the physical dynamics of the solder under the device. Shorts can occur to traces and, especially, to vias even if they are covered by soldermask. This is because the trace edges (crowns), via pad edges, and especially via hole edges can be exposed – particularly after thermal cycling during soldering processes.

Via tenting (capping) and via plugging can reduce the occurrences of these effects, but it is less expensive and more certain just to avoid putting traces or vias under the device in the first place.

2.1.3.2 DQFN Packages

Take special care when routing between the flag and the pads of a DQFN device.

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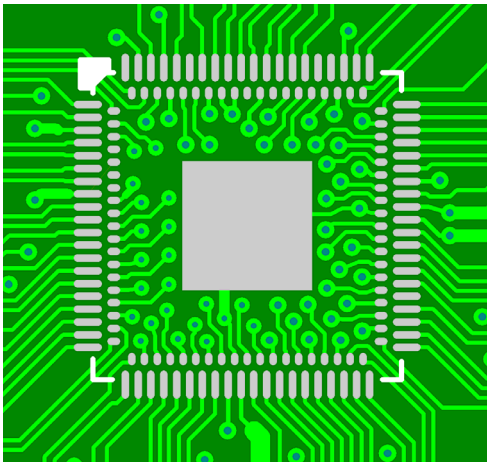

It is usually desirable to breakout the inner pads of a DQFN to the inside and drop vias to escape the part. Per the discussion above, this can cause shorts under the device, but the DQFN devices have a larger gap between the pads and the flag, making this problem less likely.

Via tenting (capping) and via plugging can reduce the likelihood of shorts.

Place any vias in the region between the flag and the pads carefully to allow proper ground (VSS) connection paths to the flag vias. Theses ground (VSS) paths must support the device needs and signal return path needs.

Make sure to carefully control the solderpaste stencil as well.

3 Application Note Revision History

Table 3.1 Customer Revision History

REVISION LEVEL & DATE	SECTION/FIGURE/ENTRY	CORRECTION
Rev. 1.1 (11-06-12)	Microchip logo added; company disclaimer modified	
Rev. 1.1 (12-10-10)	Section 2.1.1: Flag Vias	Changed “3.5-5.0mm” to “0.28 mm to 0.5 mm” in the last sentence.
Rev. 1.0 (02-09-09)	Initial document	